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Self-starting optical-electrical-optical homodyne clock-recovery for phase modulated signals

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We propose a novel self-homodyne optical-electrical-optical clock recovery technique for binary phase-shift keying signals using commercial optical and electrical components. We present the principle of operation as well as a proof-of-concept experiment for a 10.7 Gb/s NRZ BPSK signal clock-recovery transmitted over a dispersion compensated link of 20 km of SMF. Suppression of pattern related frequency noise at the output of the recovered clock is shown. The timing jitter of the recovered clock at 10.7 GHz was measured to be ~450 fs (integration range: 100 Hz -10 MHz). © 2017 Optical Society of America.

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Clock recovery (CR) is one of the first steps in today's digital coherent receivers [1, 2] for primary functions such as synchronization, data regeneration, and logic operation. Meanwhile, digital signal processing (DSP) has paved the way towards using advanced modulation formats with higher bit per symbol rates at the transmitter and compensation of transmission impairments at the receiver. Recovering the clock from the incoming optical signal is also required for synchronization of optical superchannels or reconstruction of coherent multi-wavelength sources at intermediate points such as optical add drop multiplexers in metro networks. In scenarios where full functionality of the receiver is not required and dispersion does not dominate the degradation of the signal, a circuit with simple hardware implementation (optical and/or electrical), enabling flexible data rate and analog CR is desirable. For phase modulation formats with weak or no clock components in their intensity spectra, all optical CR using nonlinear techniques such as four-wave mixing (FWM) and optical injection have been demonstrated. All optical CR for BPSK and/or DPSK modulation formats using Fabry-Pérot filters [3], mode-locked semiconductor optical amplifiers (SOAs) [4], self pulsating DBR lasers [5], and FWM in SOAs have been demonstrated [6, 7]. Recently, CR from NRZ QPSK modulation with a pre-processing stage (cross gain modulation with a CW pump in SOA followed by wavelength selective switch) to enhance the clock component and optical injection to a dual-mode amplified feedback DFB laser has been demonstrated [8]. All optical CR approaches could be implemented in an integrated platform using SOAs or mode-locked lasers. However, the recovered clock may incur excessive noise in the case of FWM based techniques, requiring narrowband electrical filters, post processing or frequency down conversion [6]. Optical injection based CR techniques [4-5, 8], shown to be effective in absorbing phase noise of the incoming signal, are usually limited to a very narrow locking range (typically ~1% of data rate) around the free running pulsation frequency of injected laser. This limits their interest for practical applications where a flexible optical transmitter is implemented with flexible baud rate [9]. As an alternative to all optical techniques, CR can be implemented after the BPSK demodulator and optical/electrical conversion using commercial modules based on electrical phase-locked-loops (PLLs) [10, 11]. These CR modules usually have a limited data rate for successful locking operation. It is also desirable for a CR scheme to be suitable for photonic integration, if it is to become part of a deployable optical receiver.

Previously, we demonstrated a self homodyne optical-electrical-optical (OEO) carrier recovery technique for BPSK signals in [11-13]. The carrier recovery scheme works by re-modulating the optical BPSK signal with the same or inverted data pattern which is regenerated at the electrical section of the OEO circuit. In this letter, for the first time, we demonstrate a self-homodyne optical-electrical-optical (OEO) self-starting CR technique for BPSK signals with standard, off-the-shelf optical and electrical components. We demonstrate that by modifying the logic operation of electrical section at OEO circuit and adding an optical-electrical feedback circuit, continuous phase switch between "0" and "π" occurs after re-modulating the optical BPSK signal. For a Mach-Zehnder modulator (MZM) biased at null, enabling phase-modulation, such

a continuous switching of the optical phase between 0 and π generates symmetric spaced side-bands separated at clock frequency, from which CR is enabled. An experimental proof–of-concept is demonstrated for a 10.7 Gb/s BPSK signal over a dispersion compensated 20 km link of SMF-28. The clock is independently generated from the incoming BPSK signal which can be used as standalone clock recovery module and/or as a clock distribution subsystem for an OEO carrier recovery circuit [11]. Unlike all optical CR schemes, additional CW pumps or pulsed sources are not required.

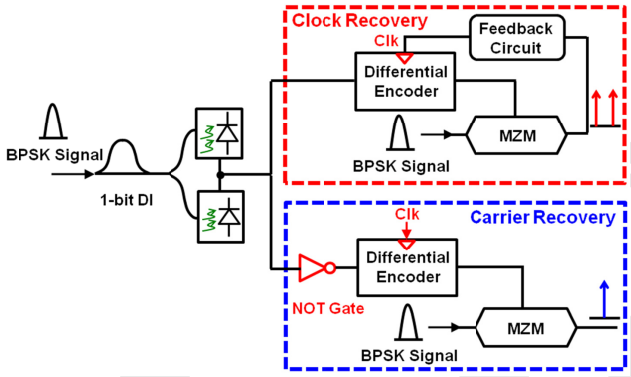


Fig. 1: Diagram of OEO self homodyne clock and carrier recovery from BPSK signal. DI: Delay Interferometer.

The diagram of the concept is shown in Fig. 1. The incoming BPSK optical signal is demodulated with assistance of a 1-bit delay interferometer (DI) and a balanced photodetector. After demodulation, the electrical signal is processed by a differential encoder which in turn re-modulates the optical signal to recover carrier (bottom diagram) or clock (top diagram). Note that one could use a variable free-spectral range DI to enable data rate flexibility in the scheme. If a *NOT* gate (Fig. 1 bottom diagram) is used before the differential encoder, the output will be the same or inverse of the data pattern at the transmitter. When a BPSK signal is re-modulated with the same or inverted data pattern, as described in Eq. (1), the phase modulation is removed from the optical signal (carrier recovery [12]). For CR, (top diagram) the *NOT* gate is removed at the input of the differential encoder, generating a different output pattern. Re-modulating the optical signal with this new pattern creates continuous phase switch between "0" or "π", at every bit sequence. In the optical spectrum, this generates carrier suppressed symmetric spaced side-bands at the frequency spacing equal to the data rate, recovering the clock (Fig. 1 top diagram). Here, we define φ_{Out} as the phase of the signal after re-modulation. For BPSK signal, re-modulating each bit with the same or inverted data results in all bits having the same phase information (all "0" or all "π"):

$$\begin{cases} \varphi_{Out} = \varphi_s + \overline{\varphi_s} = \pi \\ \varphi_{Out} = \varphi_s + \varphi_s = 0, 2\pi \end{cases}. \quad \textbf{(1)}$$

We show that by removing the *NOT* operation before the differential encoder, as shown in Fig. 1 top diagram, two optical side bands are generated at the output of the circuit, with the carrier component suppressed. The frequency spacing of these side bands is the same as the original clock, enabling a clock recovery operation. The MZM at CR circuit operates as a phase modulator (biased at null) the same as the MZM at the carrier recovery circuit. It should be noted that this CR scheme is different from a conventional clock data recovery using edge detectors and phase-locked loops [14]. While our CR scheme uses XOR functions (DI, differential encoder, second MZM) it is based on two concepts: the nonlinear characteristic of differential encoder when its input pattern is inverted; and transfer characteristics of MZM for phase switching between "0" and "π".

We consider an arbitrary data pattern comprising bits b_1 , b_2 , b_3 , ... , b_n each one being either a "0" or a "1", and with a phase information of "0" or "π". At the OEO module before the receiver, the differential encoder starts from a reference bit (0 or 1) and sequentially performs XOR operations to the incoming bit (b_i) with the result from the previous step (y_{i-1}) as follows:

$$y_i = b_i \oplus y_{i-1}\,, \quad \textbf{(2)}$$

where $\oplus$ is the XOR operator and y_i is the output. We prove, by mathematical induction, that when the bit sequence of a differential encoder is inverted, the output sequence is inverted or remains unchanged depending on the bit-index being an even or odd integer. We present the proof for reference bit of "1", but this will also hold for "0" reference bit at the differential encoder. We consider two base cases (initial steps) for first odd and even integer numbers, 1 and 2. For $n = 1$, the differential encoder output bit with the incoming bit, b_1, reads:

$$y_1 = b_1 \oplus 1 = 1 * \overline{b_1} + 0 * b_1 = \overline{b_1}\,. \quad \textbf{(3)}$$

Now, if the input bit is inverted ($\overline{b_1}$) the corresponding output (defined as $y_{\overline{1}}$) will be:

$$y_{\overline{1}} = \overline{b_1} \oplus 1 = 1 * b_1 + 0 * \overline{b_1} = b_1\,. \quad \textbf{(4)}$$

Therefore, for single (odd) bit the output will be inverted by inversion of the input pattern. For $n = 2$, the input bits are b_1, b_2 and the output of the differential encoder for the second bit, b_2 reads (using Eq. (3)):

$$y_2 = b_2 \oplus y_1 = b_2 \oplus \overline{b_1} = \overline{b_1} * \overline{b_2} + b_1 * b_2\,. \quad \textbf{(5)}$$

Now if the bit sequence is inverted, $\overline{b_1}$, $\overline{b_2}$ the differential encoder output ($y_{\overline{2}}$) for the second incoming bit, $\overline{b_2}$, reads:

$$y_{\overline{2}} = \overline{b_2} \oplus y_{\overline{1}} = \overline{b_2} \oplus b_1 = \overline{b_1} * \overline{b_2} + b_1 * b_2\,. \quad \textbf{(6)}$$

From Eqs. (5) and (6) we see that the second bit (even index) does not change by inversion of the input pattern. Taking the inductive step, we show that if n is even and assuming $y_{\overline{n}} = y_n$, then:

$$y_{\overline{n+1}} = \overline{y_{n+1}}\,, \quad \textbf{(7)}$$

and

$$y_{\overline{n+2}} = y_{n+2}\,, \quad \textbf{(8)}$$

For y_{n+1} incoming bit, the differential encoder output reads:

$$y_{n+1} = b_{n+1} \oplus y_n\,, \quad \textbf{(9a)}$$

and for $y_{\overline{n+1}}$ (inverted data pattern):

$$y_{\overline{n+1}} = \overline{b_{n+1}} \oplus y_{\overline{n}} = \overline{b_{n+1}} \oplus y_n\,, \quad \textbf{(9b)}$$

It can be shown that for an XOR operator:

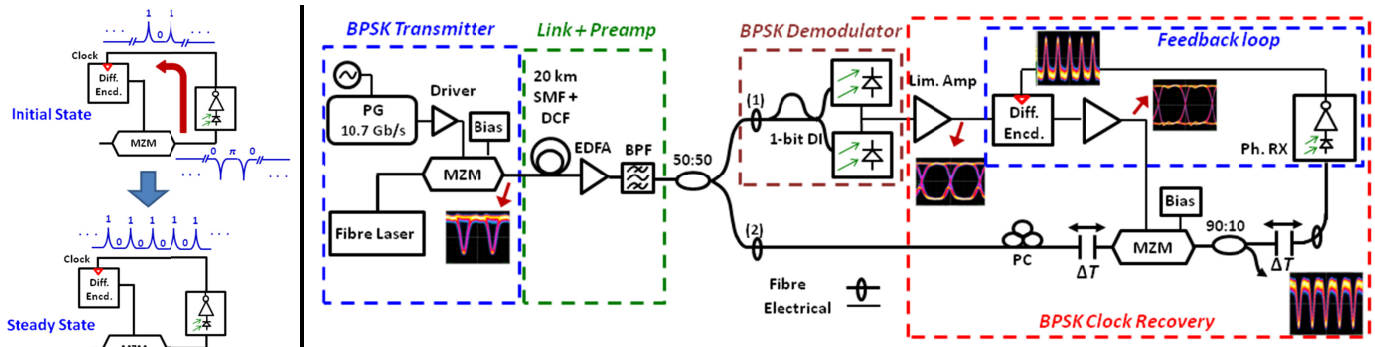
$$\overline{x \oplus y} = \overline{x} \oplus y = x \oplus \overline{y}\,, \quad \textbf{(10a)}$$

and

$$x \oplus y = \overline{x} \oplus \overline{y}\,. \quad \textbf{(10b)}$$

Using Eq. (10a), and comparing Eq. (9a) and (9b), we conclude $y_{\overline{n+1}} = \overline{y_{n+1}}$, which shows that Eq. (7) is correct for any odd index bit. In a similar way, using Eq. (10b) it can be seen that:

$$\begin{aligned} y_{\overline{n+2}} &= \overline{b_{n+2}} \oplus y_{\overline{n+1}} = \overline{b_{n+2}} \oplus \overline{y_{n+1}} \\ &= b_{n+2} \oplus y_{n+1}\,. \end{aligned} \quad \textbf{(11)}$$



Acronyms: DI: Delay Interferometer, Diff. Encd.: Differential Encoder, Lim. Amp.: Limiter Amplifier, MZM: Mach-Zehnder Modulator, Ph. RX.: Photo Receiver.

Fig. 2 (a). Self starting operation. (b). Experimental diagram of proof of concept experiment for BPSK signal.

This confirms that $y_{\overline{n+2}} = y_{n+2}$, which means that Eq. (8) holds for any even index bit. As a consequence, when the input pattern of a differential encoder is inverted, the output is only inverted for odd bits and remains unchanged for even bits. For the reference bit of "0", the proof remains the same except that the bits with even indices are inverted and the bits with odd indices do not change. In order to remove the phase modulation so that all output bit-sequence has the same value (carrier recovery), the demodulated signal should be inverted before the differential encoder. This can also be shown with similar analytical arrangement as above. Removing the *NOT* operator at the input of the differential encoder can be regarded as an "inversion" with respect to the carrier recovery circuit where the *NOT* operator is used (Fig. 1 bottom diagram). Then, the output phase is dependent on the indices of the bits as shown in Eqs. 7, and 8: For the bits with odd indices we have inversion at the output of differential encoder:

$$\varphi_{out}|Odd\ bits = \varphi_s + \overline{\varphi_s} = \pi\,, \qquad \textbf{(12)}$$

whereas for the bits with even indices (no change at the output of differential encoder) the output phase reads:

$$\varphi_{out}|Even\ bits = \varphi_s + \varphi_s = 0\,. \qquad \textbf{(13)}$$

As a result, we see a consecutive occurrence of "0" to "π" phase switch in the output phase of the optical signal when the *NOT* operator is not used. For a Mach-Zehnder modulator (MZM) biased at null, enabling phase-modulation, continuous switching of the optical phase between 0 and π generates symmetric spaced side-bands at the frequency spacing equal to the switch rate (bit rate of the original modulation) with the original carrier is suppressed.

A key part of the carrier or clock recovery schemes (Fig. 1) is a timing signal required to trigger the differential encoder. A practical implementation requires that the trigger signal to be generated within the clock recovery circuit. To address this, we implemented a feedback circuit to provide the timing signal required for the differential encoder. The feedback circuit uses a tap of the optical signal after re-modulation (recovered clock), optically delayed and detected with a 40 Gb/s photoreceiver (U2t XPRV1020), which converts it to an electrical signal with inverted bit sequence. The delay adjustment is required to synchronize the differential encoder's timing in order to provide the synchronized and correct logic pattern for re-modulation. The physical explanation (shown in Fig. 2(a)) for the self-starting process is as follows: in the first stage, when there is no recovered clock, the differential encoder's output does not affect the output of re-modulated signal (MZM output). Null transitions at the MZM output due to phase change between "0" and "π" generate pulses in the feedback circuit. These pulses trigger the differential encoder to produce the right bit value for the next incoming bit. Given Eqs. (12-13), only two consecutive pulses are required to generate phase switching between 0 and π at the output of MZM, stably starting the CR process. We expect the lock-up time required for formation of the clock to be equal to the appearance of first two consecutive transitions between 0 and 1 in the bit pattern plus the time delay of the feedback loop which is in the order of ~50 ns.

The experimental validation as a proof-of-concept is depicted in Fig. 2(b). The BPSK signal is generated by a narrow linewidth CW laser (NP Photonics, Rock Source), modulated by a MZM (biased at null) driven by NRZ data (PRBS 2^{31}-1) at 10.7 Gb/s. The signal is transmitted over a 20 km single-mode fibre, with dispersion compensation, amplification and filtering sections as shown in Fig. 2(b). At the receiver, the incoming optical signal is split into two paths. In path (1), the optical signal is de-modulated using a 1-bit DI, and both outputs are detected with a balanced detector. The electrical signal is then amplified before the differential encoder. The optical signal in path (2) is re-modulated with the electrical signal generated by the circuit in path (1). The feedback circuit included a fine tunable optical delay element followed by a high speed photo-receiver (U2T XPRV 1020). The fine delay element needs to be adjusted to form the CR with optimum delay range about 10% of the bit rate (~ 9.3 ps for 10.7 Gb/s).

Fig. 3 shows the optical spectra for the original BPSK signal (dashed black), the recovered clock (solid red) and the recovered carrier (solid blue, commercial CR module used for carrier recovery [11]). The inset in Fig. 3 shows the eye diagram of MZM output (inverted clock pulse) with no horizontal line at "0", confirming consecutive switching of the phase of the optical signal between 0 and π. In order to analyse the recovered signals in details, the RF spectrum of the recovered clock (solid-red) and recovered carrier (solid-blue) are taken and depicted in Fig. 4. The RF spectra of the signals have components at clock frequency and harmonics as well as side-bands corresponding to PRBS length. Note that in Fig. 4 the PRBS length was reduced (set to 7) in order to enable observation of spur tones at ~84.25 MHz in the wide frequency span. The recovered carrier signal has a weak clock component coming from null transitions of MZM, as expected. These intensity fluctuations can be fully suppressed using optical injection-locking [13].

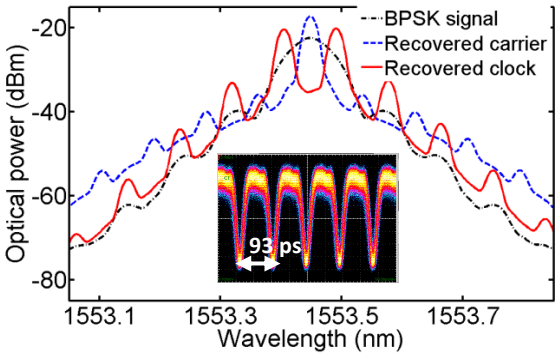


Fig. 3: Optical spectra of the BPSK signal (dashed-black), recovered clock (red), and the recovered carrier (blue). Inset: eye diagram of the MZM output, inverted clock pulse.

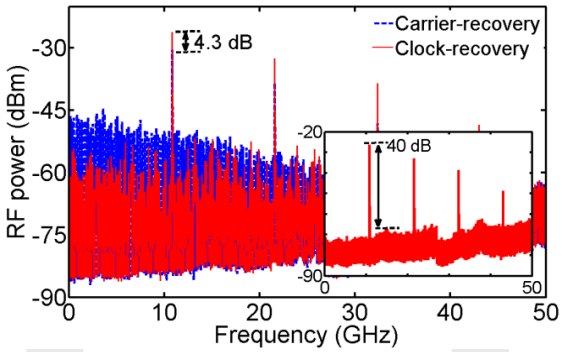


Fig. 4: RF spectra of the recovered clock (red) and carrier (blue) with resolution bandwidth (RBW) 300 kHz. PRBS: 2^7-1. Inset: RF spectrum of recovered clock, PRBS 2^{31}-1.

In the RF spectrum of the recovered clock, two features can be observed. Firstly, the power of the clock component (10.7 GHz) in CR case is larger by ~4 dB, compared with that of the recovered carrier. Secondly, the power of spur tones related to pattern length was significantly suppressed around the clock frequency down to the low frequency range. We expect suppression of these tones for any PRBS length from the clock recovery scheme. This could be attributed to the larger side bands generated in the optical spectrum of the clock recovery signal due to the phase switch at MZM output in every clock cycle. When converted to the electrical signal, this spectrum generates larger power for the component at clock frequency and weaker power at PRBS related spur tones. This is beneficial for practical application of the clock as it relaxes the filter requirements for suppressing the pattern dependent spur tones. The RF spectrum of recovered clock for PRBS length of 2^{31}-1 (inset of Fig. 4) is shown with RF SNR to be ≈40 dB for resolution bandwidth of 300 kHz. The timing jitter of the clock component in the RF spectrum (10.7 GHz) was calculated by integrating the normalized single side band measured phase noise spectrum (integration range: 100 Hz-10 MHz) to be ≈ 0.03 rad (~450 fs) indicating an excellent phase noise performance. This value is more than 50% better than all optical FWM in SOA technique [6-7] measured to be ~1 ps for a 21.4 GHz clock. Compared to all filtering techniques ([3]), values of ~710 fs were reported for a 10 GHz recovered clock, measured from the scope with precision time-base. The maximum available optical power in the feedback loop was around -1.6 dBm (692 μW) at the input of photoreceiver, with total gain conversion of 50 V/W, the amplitude of electrical signal at the clock input of differential encoder is estimated to be ~ 34 mV. We expect some residual jitter due to the low level of signal at the clock input of the differential encoder which should be improved by using a larger signal. With the availability of the components such as an extra MZM and differential encoder, one can implement simultaneous and independent carrier and clock recovery for BPSK signals using this scheme. The recovered clock can be distributed to synchronise the differential encoder for the carrier recovery circuit as well. This scheme uses standard electronic and optical components, make it an ideal option for photonic integration with practical deployment. We also note that despite some dispersion tolerance of BPSK modulation and demodulator [15], this scheme still requires reasonable pulses and therefore, dispersion compensation is required if the scheme is to be used for long haul transmission.

In conclusion, we demonstrated a novel clock recovery scheme for BPSK signals using an optical-electrical-optical self-homodyne technique. The self-starting clock recovery is based on generation of side bands for an MZM biased at null, giving a continuous phase switching between "0" and "π". A proof of concept experiment was implemented for a 10.7 Gb/s BPSK with 20 km transmission and dispersion compensation showing suppression of pattern related spur tones at the RF spectrum of recovered clock as well as excellent phase noise performance.

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