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Bridge to Digital Converters for Environmental Monitoring in Edge IoT Devices

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Doctor of Philosophy

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I, Annamaria Fordymacka, certify that this thesis is my own work and I have not obtained a degree in this university or elsewhere on the basis of the work submitted in this thesis.

Annamaria Fordymacka

Abstract

Continuous air monitoring is crucial for maintaining safe and comfortable home and work environments, particularly in industries that handle flammable or toxic gases, which pose serious health risks. Consequently, there is an increasing focus on developing wearable gas sensors to protect workers in manufacturing and other sectors requiring constant exposure monitoring. This thesis explores interfaces for resistive gas sensors and discusses the distinct challenges in designing environmental monitoring edge IoT devices. The Wheatstone bridge (WhB), which is the conventional architecture for interfacing with resistive-based sensors, typically produces a mV-level differential signal that needs to be detected in a higher common-mode voltage. This presents particular challenges for ADCs digitising WhB outputs, commonly referred to as Bridge-to-Digital Converters (BDCs), which need to have high input impedance and gain, be linear, and have offset and noise levels similar to those of the WhB.

This work proposes three bridge-to-digital conversion solutions to address challenges in resistive sensor-based monitoring systems. First, it introduces a successive approximation register (SAR) based bridge-to-digital converter (BDC) that utilizes an error-feedback modulator DAC, providing a low-area alternative to the traditional binary weighted approach. The BDC occupies 0.01 mm^2 area, and consumes 7.4 μW with a 45 ms conversion time. It achieves 9.1 ENOB for a DC input and a Walden FoM of 0.65 nJ/conv-step. Secondly, a ramp-based BDC is detailed, employing the same DAC with non-uniform sampling to enhance both resolution and sampling frequency. The BDC occupies an area of 0.014 mm^2. It achieves an SNR of 49.97 dB and 65.6 dB, for dynamic and static inputs, respectively. The BDC consumes 30 μW with a 0.41 ms conversion time, resulting in a Walden FoM of 0.048 nJ/Conv-step. Finally, a threshold detection-based BDC is presented, aimed at reducing power consumption by decreasing the volume of generated output data. This design occupies 0.012 mm^2 with 10 bits resolution, consuming 4.8 μW of power while operating at a clock frequency of 20 MHz. All BDCs are designed using a 65-nm CMOS technology and offer a wide input range of 830 mV.

Despite the unique design constraints associated with gas sensors, the methodologies discussed in this thesis have broader applications in the IoT field, where most devices must operate for prolonged periods without requiring battery replacement, while managing vast amounts of continuously collected data.

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Glossary

ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
BDC	Bridge-to-Digital Converter
CCIA	Capacitively-Coupled Instrumentation Amplifier
CFIA	Current Feedback Instrumentation Amplifier
CMRR	Common-Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
EFM	Error Feedback Modulator
ENOB	Effective Number Of Bits
EOC	End Of Conversion
FFT	Fast Fourier Transform
FOM	Figure of Merit
IA	Instrumentation Amplifier
INL	Integral Non-Linearity
IoT	Internet of Things
LSB	Least Significant Bit
MEMS	Microelectromechanical Systems
MOX	Metal Oxide
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NEF	Noise Efficiency Factor
NOC	Non-Overlapping Clocks
OSR	Oversampling Ratio
PCB	Printed Circuit Board

PEF	Power Efficiency Factor
RTL	Register Transfer Level
SAR	Successive Approximation Register
SCR	Switched-Capacitor Resistor
SNR	Signal-to-Noise Ratio
TD	Threshold Detection
VCO	Voltage Controlled Oscillator
WhB	Wheatstone Bridge
$\Delta\Sigma$	Delta-Sigma

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Chapter 1

Introduction

Advances in electronics enable a spectrum of new applications and concepts, such as the Internet of Things (IoT). An ability to connect billions of devices embedded with sensors to the internet allows us to create sophisticated networks of devices that collect and share data, thus monitoring and analysing our environment autonomously with the capability of informing us about any detected anomalies. The number of emerging IoT applications demonstrate its unlimited potential, where many applications concern not only our convenience but, above all, aim to improve our health and safety. Therefore, more and more such devices are found in our homes, factories, offices and cars. As the number of IoT devices is growing exponentially, the International Data Corporation (IDC) predicts that more than 41 billion connected devices are expected to be in use by 2025 [1]. Furthermore, since the IoT is able to leverage from other emerging technologies, such as an artificial intelligence (AI) and 5G, its relevance is expected to continue, leading to further market growth.

While IoT devices offer endless possibilities, they also present a number of challenges for integrated circuit designers. This thesis focuses on interfaces to resistive sensors used in hazardous gas detection and air quality monitoring. According to the World Health Organization (WHO) there are approximately 7 million deaths each year associated with air pollution [2], justifying the increasing number of sensors being embedded in intelligent buildings to monitor a range of parameters from heating to air quality [3].

There is thus a drive to develop wearable gas sensors for the personal safety of employees in manufacturing and other sectors where exposure must be monitored [4]. Although these sensors offer some distinct design constraints, as will be mentioned throughout this thesis, the methodology described here may also find IoT applications such as wearable devices for detecting vibration thresholds in machinery for predictive maintenance, proximity detection in hazardous areas, or monitoring hydration and fatigue levels of workers in extreme environments.

1.1 Gas Monitoring Systems

Continuous air monitoring is critical to provide a safe and comfortable work and home environment. The Health and Safety Authorities (HSAs) in many countries have issued guidelines and recommendations in relation to acceptable exposure limits, especially for industries handling flammable or toxic gases, which can lead to death. Figure 1.1 illustrates an example of CO (carbon monoxide) exposure limits which should be satisfied in the workplace.

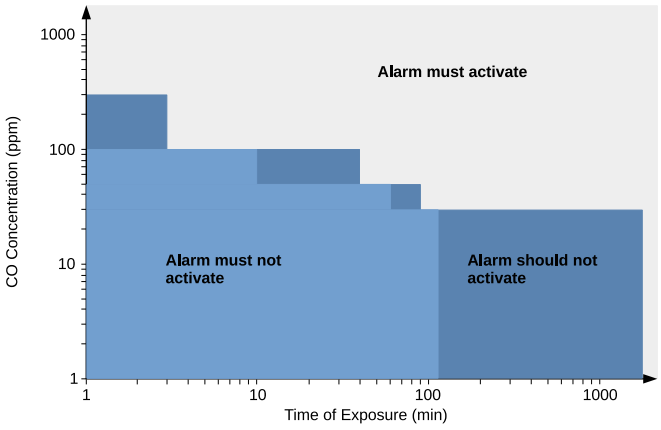


Figure 1.1: Example of carbon monoxide (CO) concentration levels [5].

It is important to notice that, while there is a maximum exposure value, which immediately triggers an alarm to evacuate, there are also time limits associated with lower exposure levels. This means that, if the worker is not restricted to one location during the work shift, it may not be sufficient to observe the gas concentration in the building alone but also a handheld device to measure personal exposure limit (PEL) may be required. According to [5], it is also crucial to customise the alarm trigger points for

the target gas, the environment and the types of detectors used. This can avoid false alarm triggers, which are both disruptive and costly. Furthermore, these levels may need to be revised regularly in response to a changing regulation and environment, which requires a flexible monitoring system. While the exposure limits are regulated in industry, it is equally important to monitor the gas levels in our homes, as many people rely on gas or solid fuels for appliances and space heating.

1.2 Harmful Gases

The non-exhaustive list here includes some of the most prevalent gases and explains their properties, justifying the need for continuous detection systems:

- Carbon monoxide (CO) is a poisonous, colourless, odourless and tasteless gas caused by incomplete burning of fuels. It is produced in dangerous levels by faulty or blocked fuel-burning appliances. It can be detected not only in homes and industry but also in mobile homes, boats and other locations. Due to its properties it is difficult to detect without designated devices. When CO is breathed in, it combines with haemoglobin, reducing the oxygen delivered to vital organs. While the poisoning can be easily prevented by proper ventilation if detected early, often the person's health deteriorates without their awareness, especially during someone's sleep, and this can be fatal. This is why CO is often referred to as the "silent killer". According to [6], 6 people in Ireland die from CO poisoning every year. Also, while exposure to high levels of CO can be lethal in a matter of minutes, low level exposure can result in long-term health complications. Another reason why it is important to keep track of the ambient CO concentration level is the possibility of explosion during leakage as it is an extremely flammable gas.
- Carbon dioxide (CO_2) is one of the components of the atmosphere and, at low concentration levels, it is harmless to humans. Because CO_2 is expelled during exhalation, it is present in confined, badly ventilated spaces that are occupied by people. As its concentration increases, it becomes toxic and, over prolonged inhalation, it can cause mild effects such as headaches, anxiety or dizziness. It is also associated with declining concentration, drowsiness and lethargy leading to

decreased productivity, which is why it is important to track CO_2 levels in places such as schools and offices. At very high concentrations it generates a sharp and acidic odour in the air and long exposure can lead to airway obstruction or even cardiac arrest [7].

- Smoke arises as a result of an incomplete combustion of materials. It can be decomposed into particulates consisting of soot and non-particulates consisting of organic compounds, which are very volatile [8]. While the soot can be very damaging to electronics and other exposed materials, inhaling fine particles of the smoke is harmful as it affects the eyes and the respiratory system, causing breathing difficulties and degrading overall health. Since smoke can be used as an early sign of fire, fire detection systems often rely on smoke detectors, which are also low-cost, meaning they can be easily acquired [9]. Based on the Centre of Fire statistics [10], 84% of fire deaths and 70% of fire injuries amongst the participating countries occur in residential buildings. This justifies the need for fire detection systems, not only in industry, but also in households.

As can be concluded from the above list, the greatest risk of gas poisoning stems from the odourless nature of many hazardous gases and the non-obvious early symptoms. Despite the fact that with early intervention many health implications can be avoided, once the symptoms are recognised, it may be too late. This justifies the need for technological assistance.

1.3 Gas sensors

The operation of gas sensors can be based on different material properties, such as optical, acoustical or calorimetric [11]. This thesis will focus on sensors which translate gas concentration to electrical variations and that can be easily incorporated within integrated circuits. There are several metrics that need to be considered when choosing a gas sensor for a target application; some of the most important ones are sensitivity, selectivity and response time. In addition to these, low energy consumption, reliability and size are also crucial, especially when sensors are battery operated, have to work for many years and when regular control is expensive, as is the case for many IoT monitors.

Some of the most commonly used gas sensors in IoT, due to their overall performance and low fabrication cost, are fabricated in Metal Oxide (MOX) Semiconductor [12] technology. In this type of sensor, the gas concentration is related to the electrical conductivity of the heated metal oxide material. The equivalent circuit of this sensor is represented in Figure 1.2. Here, R_H is a heating resistance, V_H is a heating voltage, R_s is the sensor's resistance and V_{CC} is a supply voltage.

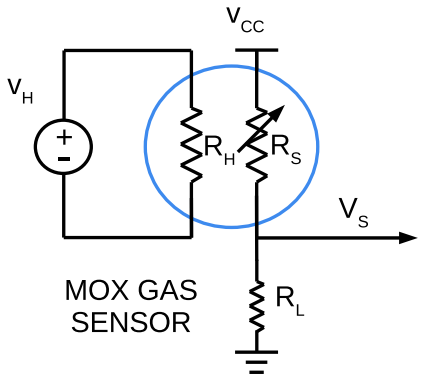


Figure 1.2: An equivalent circuit diagram of a MOX sensor.

With the load resistor, R_L, added externally, the output voltage, V_S, can be calculated as:

$$V_S = \frac{V_{CC} R_L}{R_S + R_L}. \tag{1.1}$$

There are three types of heating components that can be used in MOX sensors: ceramic tube, planar ceramic substrate and microelectromechanical systems (MEMS). MEMS technology allows for greater miniaturisation and power efficiency, making it a more enticing solution for portable electronics, compared to the ceramic tube and planar ceramic substrates [13]. MEMS gas sensors can offer a wide measurement range [14], resulting typically in a 20 kΩ to 2 MΩ change in internal resistance. Generally, the MOX gas sensor requires high operating temperatures of 100 °C to 450 °C [15]. Running the sensor in continuous mode would be inefficient for this type of application, where air concentration changes slowly over time and so, to extend the battery life, duty cycling is often implemented. The minimum time for which the sensor needs to be enabled to acquire an accurate reading is specified by the manufacturer and is usually several

seconds. The off time can be estimated from the expected rate of change of the gas concentration and can vary depending on the air ventilation facilities.

1.4 Conditioning circuits

The diagram in Figure 1.3 represents the architecture of a sample gas readout system. The system consists of a power unit, a sensor with front-end electronics and a low power micro-controller with a transceiver. The sensor output changes based on the gas concentration in the air. To interpret the data from the sensor, the signal needs to pass through the conditioning unit and the driver before it can be digitised by an ADC. The signal biasing, level-shifting and amplification ensure that the signal is within the ADC input range. It is common to use a third to fifth-order anti-aliasing filter to prevent signals that are outside of the sampling frequency band from being digitised and compromising the results. Finally, the data processing unit is required to process the data, communicate with the other nodes on the network and trigger an alarm if the harmful gas concentration exceeds the normal range. In conventional systems, data processing is usually performed by a micro-controller.

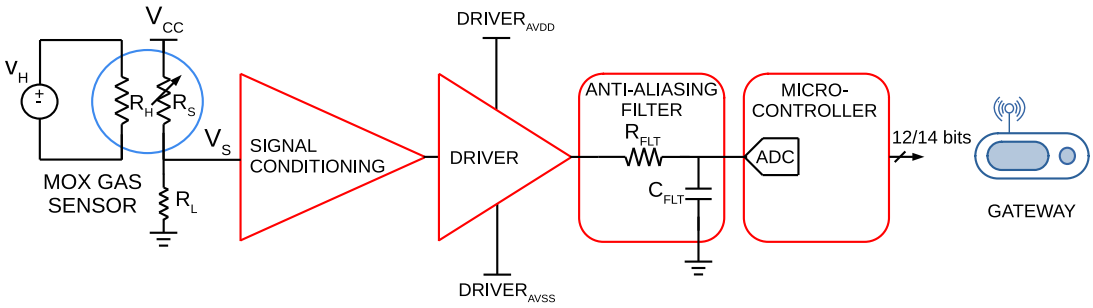


Figure 1.3: System diagram of a gas readout system.

1.5 Scientific Contribution

A number of challenges are present when designing gas monitoring systems. The retrofitting of buildings with wired gas detectors is often cost-prohibitive, leading to the growth of battery-powered wireless IoT based sensors. Often there are a large number of sensors, and they must operate for years without battery replacement, as this could otherwise result in high overhead expenses. This is especially difficult, as

most gas sensing materials must be heated to temperatures between 100 °C and 450 °C. Another big challenge is the volume of data being collected. When the device is in active mode it needs to sense the surrounding air at a rate that ensures early detection in case of a leak or general air quality deterioration. This means that there is data being collected continuously and only a small fraction of it is informative, as the gas concentration usually stays within well defined bounds. This can be even more prevalent when the sensor arrays are used to detect multiple gases at the same time. While it is possible to analyse data locally, often it is sent wirelessly from the device to the processing unit and stored in the cloud. When designing sensors, not only must the device be extremely energy efficient, but its form factor is limited as it needs to fit in a portable device [12, 16].

Conventional ADCs follow the Nyquist theorem which states that to achieve full signal reconstruction the sampling rate should be twice the maximum input signal frequency [17] for a baseband signal. More recently, many ADCs have adopted sub-sampling [18] to digitize RF signals, while maintaining a sample rate twice the signal bandwidth, to ensure that the transmitted signal can be fully reconstructed. However, in air quality monitoring and environmental alarm monitoring applications, the critical information is whether the environment is safe or not, so full reconstruction of the input signal may not be required. For example, once the concentration of CO is below a certain level, its absolute value is not particularly important. Hence, a threshold detection approach is applicable, where the observed CO level is simply compared against a variable predetermined reference level to determine if further action is required.

This thesis proposes three bridge-to-digital conversion solutions that address challenges in monitoring systems based on resistive sensors. A successive approximation register (SAR) based bridge-to-digital converter (BDC) with an error-feedback modulator DAC, which offers a low-area alternative to the popular binary weighted approach, is presented. A ramp-based BDC that uses the same DAC, while leveraging non-uniform sampling to improve resolution and sampling frequency, is also presented. Both solutions provide a wide input range. The thesis also proposes a threshold detection based BDC. A threshold detection approach aims to decrease the power consumption of the

whole monitoring system, where instead of generating a continuous stream of output data, it monitors the sensor levels and produces a flag when a pre-programmed, safe threshold is crossed.

1.6 Thesis Organisation

The organisation of the thesis is now presented. Chapter 2 introduces the reader to the data converters. It highlights the popular architectures and explains important metrics. Chapter 3 describes in detail the implementation of a SAR-Based Bridge-to-Digital Converter. It presents the results achieved and compares them against the state-of-the-art. Chapter 4 presents the threshold detection based converter, which uses the same architecture as in chapter 3, but a different algorithm targeting wireless monitoring systems. Chapter 5 presents the ramp-based BDC which targets issues seen in chapter 3. The measured results are presented and discussed. Finally, all the work is summarised and future work is proposed in chapter 6.

The research described in this thesis has led to the following publications:

- A. Fordymacka and I. O'Connell, "A 0.01-mm^2 0.83-V Input Range SAR-Based Bridge-to-Digital Converter", IEEE Solid-State Circuits Letters, vol. 3, pp. 330-333, 2020, doi: 10.1109/LSSC.2020.3018427.
- A. Fordymacka and I. O'Connell, "A 0.01-mm^2 0.83-V Input Range SAR-Based Bridge-to-Digital Converter", Technical Paper, IEEE 47th European Solid-State Circuits Conference (ESSCIRC), Grenoble, France, 2021. (Virtual)
- A. Fordymacka and I. O'Connell, "Threshold Detection ADC For Continuous Monitoring Applications," 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Lansing, MI, USA, 2021, pp. 571-574, doi: 10.1109/MWSCAS47672.2021.9531751.
- A. Fordymacka, G. Salgado and I. O'Connell, "A Counting Based Bridge to Digital Converter Achieving a Walden FoM of 0.048 nJ/conv-step", 31st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Nancy, France, 2024.

Chapter 2

Data Converters

This chapter is divided into three main parts. The first section serves as an introduction to the basics of data converters and explains the most important terms that are used throughout this thesis. The second part discusses the most popular architectures, highlighting the latest research on bridge to digital converters, which are the main focus of this thesis. Finally, the SAR ADC and its building blocks are explained in more detail, as this architecture forms the basis for the proposed BDCs discussed in chapters 3 to 5.

2.1 ADC theory

The role of analog to digital converters (ADC) is to connect the physical world with digital computing, thus taking advantage of digital signal processing. Benefiting from technology scaling, digital electronics allows sophisticated computation and storage of an abundant amount of data at low cost. Moreover, data in digital form has inherent noise immunity, which results in high reliability. The aforementioned qualities are especially important in monitoring applications, where sensing the physical phenomena and computing changes continuously in real time puts high demands on the systems. Figure 2.1 represents the main steps of the conversion process in a traditional analog to digital converter which takes a continuous-time analog input signal and converts it to a discrete time form represented by binary numbers. The different stages are explained

in the subsections below.

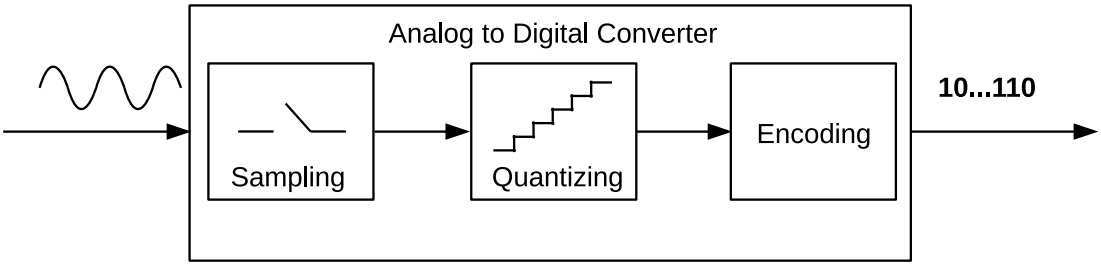


Figure 2.1: Analog to digital conversion.

2.1.1 Sampling

Sampling is the step by which a continuous-time signal is converted into a discrete-time signal. While there can be exceptions, typically the conversion is performed at regularly spaced intervals defined by a sampling clock, as illustrated in Figure 2.2.

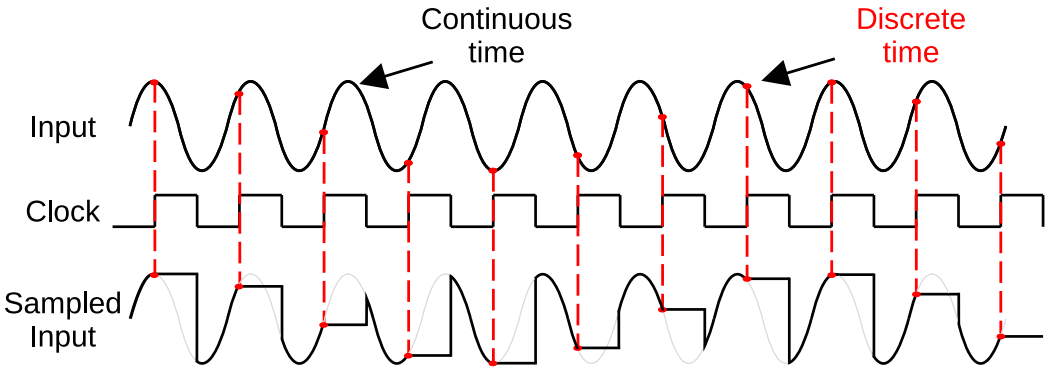


Figure 2.2: Sampling of an input signal. The voltage signal is first tracked during the sampling phase and then held at a constant amplitude for the duration of the conversion.

According to the Nyquist-Shannon sampling theorem [17], to be able to correctly reconstruct the input signal afterwards, the sampling rate must be at least twice the rate of its highest frequency component for a low pass signal. Let's look at the sampled input signal which is represented by red dots in Figure 2.3. If the sampling clock, f_s, has a lower frequency than the signal of interest, f_x, during reconstruction the input can be indistinguishable from other signals that fall outside the expected frequency range, $nf_s \pm f_x$, where n is an integer.

This unwanted signal phenomenon is called aliasing. To eliminate aliasing, the frequency of the input signal must be bounded. This can be achieved by passing the

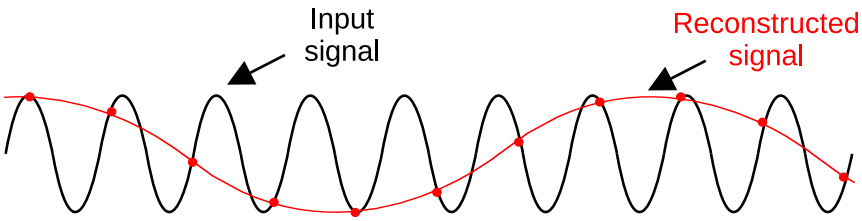


Figure 2.3: The aliasing effect, where the reconstructed signal (red) appears to be a sine wave of a lower frequency than the input signal (black).

input signal through a band-limiting filter before it is sampled by an ADC. This removes any undesirable frequencies that could enter the spectrum of interest. However, in practice, the filter is not able to either completely remove the aliasing or can distort the waveform when the signal is close to the Nyquist limit. Therefore, the sampling of the input is often carried out at a higher frequency than required theoretically, i.e. it is oversampled.

2.1.2 Quantisation

Once the input signal is sampled, the quantiser converts its continuous amplitude into a digital representation, in the format of binary numbers. The digital output word, B, is given by:

$$B = b_{N-1}2^{N-1} + ... + b_2 2^2 + b_1 2^1 + b_0 2^0 \tag{2.1}$$

where N is the number of output bits, often referred to as the resolution of the ADC, b_0 is the least significant bit (LSB) and b_{N-1} is the most significant bit (MSB).

While there are a variety of quantiser architectures available in the literature, some of which will be described later, the concept can be visualised as comparing the signal to a range of known references which represent an equivalent binary code. Due to the fact that the maximum voltage range (V_{FS}, full scale range) which can be converted by an ADC is divided into a finite number of levels, there is an inherent conversion error introduced. This error is called the quantisation error and its value is $\pm(1/2)LSB$, where the LSB is defined as:

$$LSB = \frac{V_{FS}}{2^N}. \tag{2.2}$$

The LSB is the smallest increment of the output signal that the converter can represent, as illustrated in Figure 2.4.

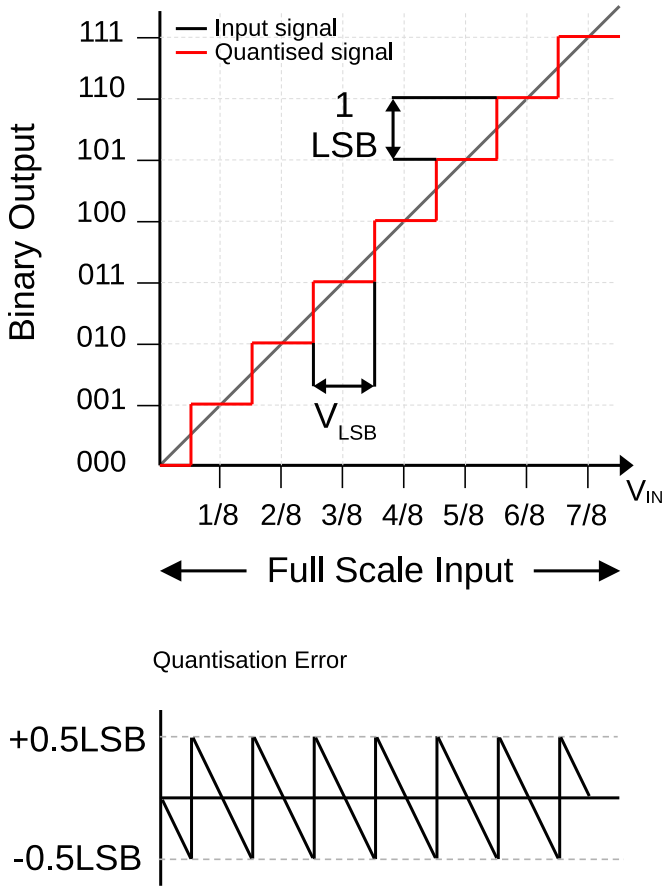


Figure 2.4: ADC transfer characteristics. LSB definition and quantisation error (for 3-bit ADC).

The error that can be tolerated depends on the target application. However, it is important to note that while the quantisation error decreases with an increase in the resolution of the ADC, it does not always grant a proportional improvement in the accuracy of the ADC. The accuracy of the converter is further limited by implementation imperfections, which will be discussed in more detail in subsequent sections.

2.1.3 Encoding

Finally, depending on the quantiser architecture, its output may need to be further encoded to generate a meaningful binary representation to be used by the chosen processing unit.

2.1.4 Linearity

As already known from subsection 2.1.2, in the ideal ADC, the accuracy is limited only by the quantisation error. However, due to circuit non-idealities, linearity errors appear, meaning that the ADC's input-output response is non-uniform across the input range. The sources of those errors can depend on design choices. The most important measurements for linearity are:

- Integral Non-Linearity (INL), represented in Figure 2.5, is a deviation in LSB from an ideal analog to digital transfer curve:

$$INL(i) = \frac{V_{in}(i) - iV_{LSB}}{V_{LSB}}, \forall_i = 0...(2^N - 1). \tag{2.3}$$

- Differential Non-Linearity (DNL), represented in Figure 2.6, is a deviation of each step size from the ideal step size:

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{V_{LSB}} - 1, \forall_i = 0...(2^N - 2). \tag{2.4}$$

- Offset, represented in Figure 2.7, is a deviation between the first ideal step and the first actual step.

- Gain error, represented in Figure 2.8, is a deviation between the slope of the ideal transfer curve and the slope of the actual transfer curve, after the offset error is removed.

The gain and offset errors typically can be easily compensated for; however, while the literature proposes a number of DNL and INL error calibration methods [19, 20], these are often non-trivial.

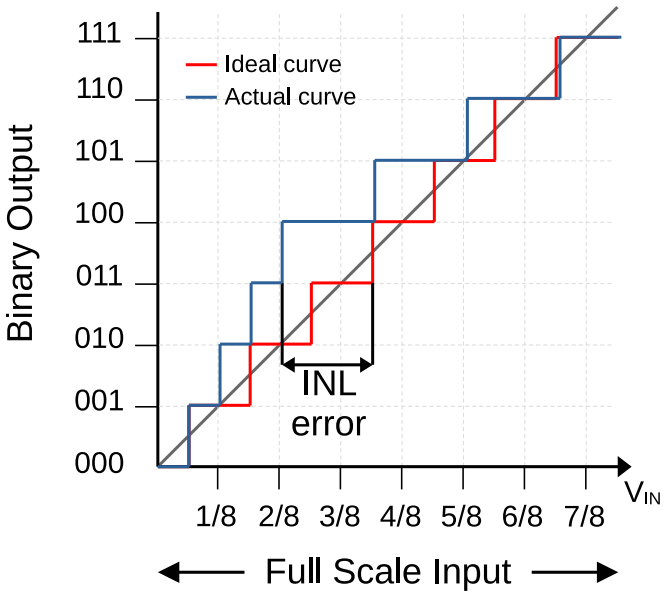


Figure 2.5: Representation of the integral non-linearity, showing the deviation from a straight line.

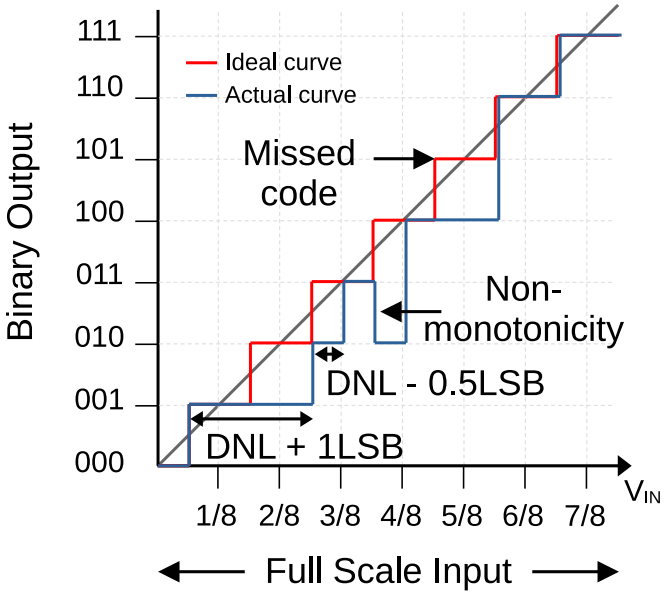


Figure 2.6: Representation of the differential linearity, illustrating disparities between ideal and actual curves.

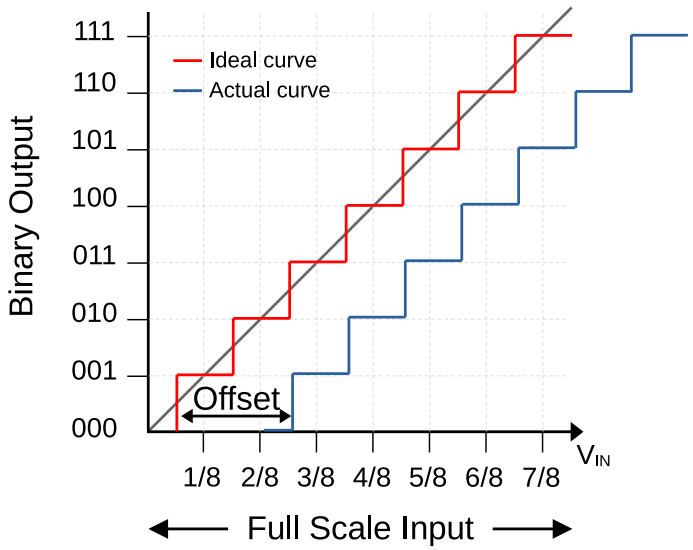


Figure 2.7: Representation of the offset error, shown as the distance from the ideal transfer function.

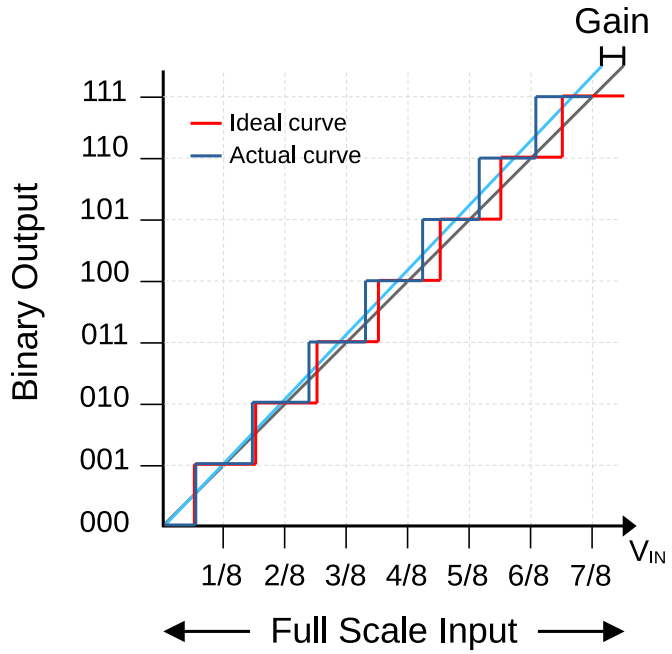


Figure 2.8: Representation of the gain error, showing the deviation from the ideal transfer function.

2.1.5 Sampling non-idealities

The sampling circuit can be represented by a capacitor with a switch, such as in Figure 2.9. Initially, the switch is closed and the capacitor is charged to the input signal. After a predefined time, the switch is opened and the amplitude, V_{out}, can be quantised by the next stage of the ADC. In the ideal circuit the capacitor should hold the exact value of the input voltage; however, there are a number of sources of error introduced during sampling which can degrade the performance of the ADC. The non-idealities which are most relevant for this thesis are explained below.

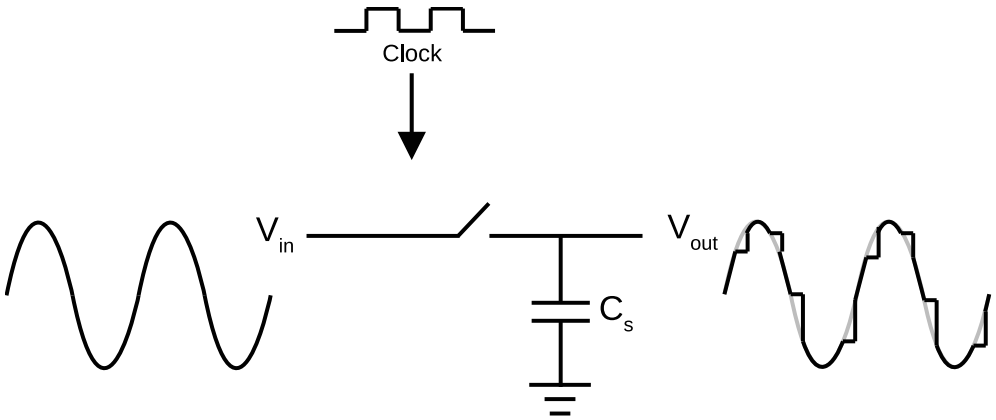


Figure 2.9: Simplified diagram of a sampling circuit.

2.1.5.1 Settling Error

As already discussed, the sampling block consists of a switch and a capacitor, where the switch is implemented by a Metal Oxide Semiconductor (MOS) transistor, as in Figure 2.10. This can be modelled as a simple RC circuit, where R_{on} is the on-resistance of the MOS device and C_s is the total sampling capacitance, which is illustrated in Figure 2.11. From the RC approximation equations, the settling time required for an ADC to achieve a target precision can be derived as a multiple number of the time constant [21]. Here, the precision can be determined as a fraction of LSB.

It can be established from the RC charging time, that for a sampled input voltage V_{in}, after time $t_{sampling}$ the output voltage V_{out} will be (assuming the capacitor is discharged at the start of the sampling time):

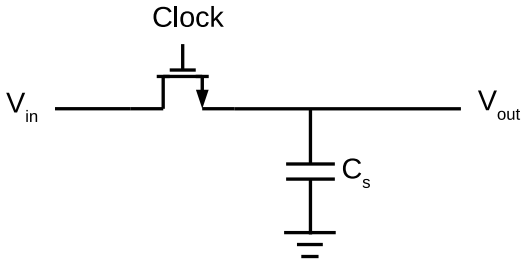


Figure 2.10: Sampling switch implemented with MOS.

$$V_{out} = V_{in}(1 - e^{-\frac{t_{sampling}}{\tau}}) \tag{2.5}$$

where,

$$\tau = R_{on}C_s \tag{2.6}$$

Equation 2.5 can be further rearranged to express $t_{sampling}$ in terms of a multiple of the time τ.

$$t_{sampling} = -\tau \ln(1 - \frac{V_{out}}{V_{in}}) \tag{2.7}$$

Assuming a full-scale input signal, $V_{in} = V_{FS}$, and a maximum of $(1/2)LSB$ settling error, V_{out} can be calculated as:

$$V_{out\,\frac{1}{2}LSB} = V_{FS}(1 - \frac{1}{2 * 2^N}) \tag{2.8}$$

By substituting (2.8) into (2.7), the minimum time required for the full-scale input signal to settle to $(1/2)LSB$ can be obtained as:

$$t_{sampling} = -\tau \ln(\frac{1}{2 * 2^N}) = \tau \ln(2 * 2^N) \tag{2.9}$$

Since the settling time is directly related to the resolution of the ADC, the number of required time constants will increase with N. For example, a minimum of 7.62 time constants will be sufficient for 10-bit ADCs, while 10.4 time constants are needed for

14-bit accuracy.

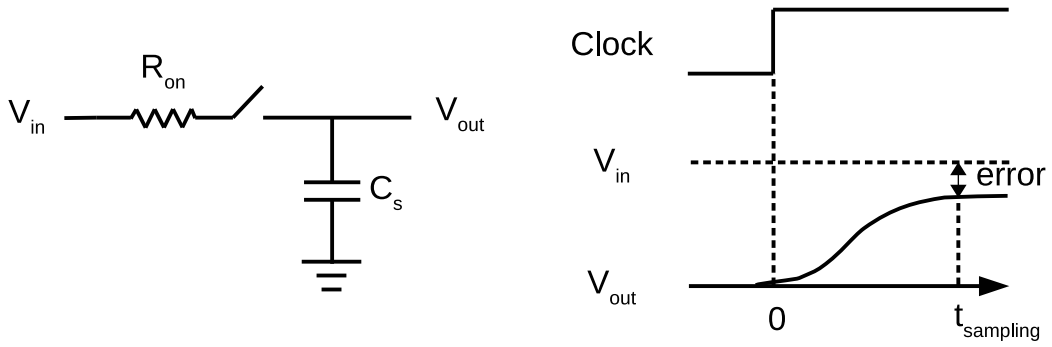


Figure 2.11: Sampling error due to RC charging time.

It is also important to mention that a complementary switch (CMOS), consisting of both NMOS and PMOS devices connected in parallel, may be preferred when implementing a sampling circuit. Firstly, it can support rail-to-rail inputs, given that the supply level significantly exceeds the voltage threshold values of the MOS devices [22]. Secondly, a CMOS switch helps to mitigate the on-resistance dependency of the NMOS and PMOS devices. R_{on} varies with the drain/source voltage levels, which could otherwise adversely impact high-resolution and high-speed ADCs, by causing significant distortions and limiting the bandwidth ($R_{on} * C_s$). Finally, the PMOS and NMOS devices in the transmission gates can be sized such that, when the switch is opened, opposite charges that would be injected from the channel of each device cancel each other out [23], reducing any unwanted voltage error at the output.

2.1.5.2 Thermal Noise

The settling time is not the only concern resulting from the non-ideal components. The internal resistance R, which is the on resistance of the MOS switch summed with all the resistive elements, contributes a thermal noise equal to [24]:

$$e_{noise} = \sqrt{4kTRBW} \tag{2.10}$$

where, k is the Boltzmann's constant, T is the temperature in Kelvin and BW is the bandwidth in Hertz.

However, since the sampling circuit is in fact a low-pass filter, to attain the noise that

Table 2.1: Thermal noise of capacitors at 300K

C_s (F)	$v_{\sqrt{(kT/C_s)}}$ (Vrms)
1f	2m
10f	643μ
1p	64μ
10p	20μ

is visible at the output, the spectral density of equation (2.10) needs to be integrated over the noise bandwidth f:

$$v^2_{C_s,noise} = \int_0^\infty \frac{4kTRdf}{1+(2\pi f)^2R^2C_s^2}, \tag{2.11}$$

which evaluates to:

$$v^2_{C_s,noise} = \frac{kT}{C_s}. \tag{2.12}$$

Inferring from the above equation, the sampling noise is inversely proportional to the size of the sampling capacitor, as tabulated in Table 2.1.

Therefore, the size of the sampling capacitor not only affects the settling time but also plays a critical role in defining the accuracy of the ADC system. Since, in this case, a large capacitor may be preferred to filter out the noise, selecting the size of the capacitor introduces an important design trade-off. Here, the improved accuracy of the sampled signal is offset by increased area, power consumption and decreased sampling rate.

2.1.5.3 Jitter

In the ideal ADC system, the sampling clock should be perfectly periodic; however, in the presence of noise the timing of the clock edges may fluctuate. This effect is called jitter and may cause the input signal of the ADC to be sampled at non-equally spaced time instances, thereby leading to amplitude errors. This is illustrated in Figure 2.12.

Mathematically, the amplitude error of a sampled sine wave input:

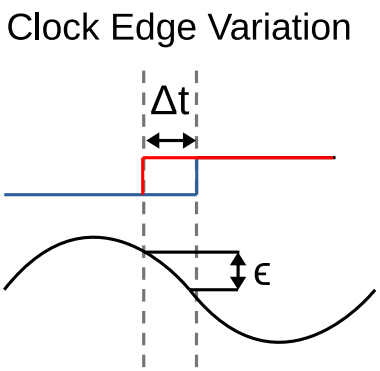


Figure 2.12: Sampling errors due to clock jitter.

$$V_{in}(t) = A\sin(2\pi f_{in}t), \tag{2.13}$$

can be modelled by the time derivative of the signal function [25]:

$$\frac{dV_{in}(t)}{dt} = 2\pi A f_{in}\cos(2\pi f_{in}t) \tag{2.14}$$

where the maximum error will occur when the cosine function equals 1, at time $t = 0$:

$$\frac{dV_{in}(t)}{dt}|_{t=0} = 2\pi A f_{in}. \tag{2.15}$$

Finally, the maximum error ϵ, in the sampled voltage, due to the jitter Δt, can be represented as:

$$\epsilon = 2\pi A f_{in}\Delta t \tag{2.16}$$

2.1.5.4 Leakage

Another source of sampling error which can particularly manifest itself in ADCs with high resolution and low sampling rates is switch leakage. When the switch is opened, the capacitor should hold a fixed voltage output until the quantisation is complete. However, due to the structure of the MOS devices, there is a junction leakage current

present which, depending on the leakage current direction, can either increase or decrease the sampled output voltage. Furthermore, the leakage can increase by orders of magnitude when the devices operate at high temperatures. According to [26], for a target resolution and sampling rate f_s the size of the sampling capacitor should be selected such that it upholds the leakage current limit in equation (2.17). This is to ensure that the capacitor does not charge or discharge by more than $(1/2)LSB$ during quantising.

$$I_{leakage} < \frac{V_{FS}}{2^N} f_s C_s. \tag{2.17}$$

2.1.6 Signal-to-Noise Ratio

The resolution of an ADC is defined by the number of discrete digital levels, LSBs, that an ADC can produce for a full-scale analog input. However, it is important to note that the resolution isn't necessarily interchangeable with the accuracy of the ADC, which can be affected by linearity and dynamic errors. To understand how well a signal can be digitised, the Signal-to-Noise Ratio (SNR) is characterised, from which an Effective Number Of Bits (ENOB) can be determined.

SNR is the ratio of the RMS full-scale sinusoidal input signal power to the RMS value of the noise [27]. This is typically expressed in dB as:

$$SNR = 20\log\frac{V_{in,RMS}}{V_{noise,RMS}} \tag{2.18}$$

For a full-scale signal, the RMS value of the sinusoidal input signal, $V_{in,RMS}$, is:

$$V_{in,RMS} = \frac{V_{FS}}{2\sqrt{2}} = \frac{2^N(V_{LSB})}{2\sqrt{2}} \tag{2.19}$$

From subsection 2.1.2, in the ideal ADC, the noise is equivalent to the quantisation noise (Q_e) due to the rounding errors, i.e. all values between $\pm(1/2)LSB$ are considered equiprobable:

$$Q_{e,RMS} = \sqrt{\frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{0.5V_{LSB}} (V_{LSB})^2 \, dV_{LSB}} = \frac{V_{LSB}}{\sqrt{12}}. \tag{2.20}$$

By substituting equation (2.19) and (2.20) into (2.18) we get:

$$SNR = 20\log \frac{\frac{2^N (V_{LSB})}{2\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}}, \tag{2.21}$$

which is commonly represented in terms of N:

$$SNR = 6.02N + 1.76 \tag{2.22}$$

Finally, by rearranging equation (2.22), ENOB can be calculated for the measured SNR from:

$$ENOB = \frac{SNR - 1.76}{6.02}, \tag{2.23}$$

where ENOB $\leq N$.

2.2 ADC Types

As ADCs are one of the key components of electronic systems, extensive research and development has been carried out in this field, resulting in multiple architectures targeting all kinds of applications. In order to facilitate the choice of the design for the selected application, ADCs can be distinguished based on their sampling rate, as represented in Figure 2.13. ADCs are considered Nyquist converters when their sampling rate is just above Nyquist, i.e. $f_s > 2f_{max}$, which was discussed in Section 2.1.1. Oversampled ADCs, where $f_s >> 2f_{max}$, are slower but offer superior quantisation noise reduction compared to Nyquist architectures. Under-sampling, also referred to as sub-sampling converters, where $f_s < 2f_{max}$, are used in narrow bandwidth applications to fold the signal back to lower frequencies. ADCs can be also categorised based on the quantisation domain. While so far this thesis has mainly focused on quantis-

ing the input in the voltage domain, alternative reference domains such as current or time/frequency signals can be also utilized. For instance, frequency-based quantization can be applied using a Voltage-Controlled Oscillator (VCO), where the input signal modulates the oscillation frequency. These are further explored in Section 2.2.4.

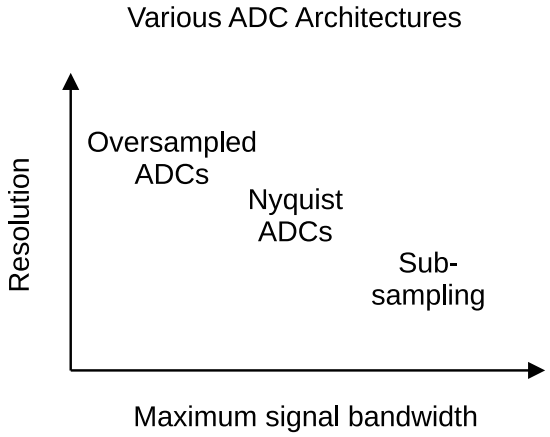


Figure 2.13: A representation of the resolution vs maximum signal bandwidth of three different types of ADCs.

2.2.1 Nyquist

There are many architectures that can be distinguished in this category, with the two main ones being SAR and flash. Their designs and performance differ significantly, but both are popular in their own range of applications. Successive approximation register (SAR) ADCs target low power applications where mid-range accuracy and speeds are required, whereas flash ADCs can achieve high conversion rates but their resolution is limited by the area and power consumed.

2.2.1.1 Flash ADC

The flash ADC is illustrated in Figure 2.14. This architecture consists of a reference level generator block which generates $2^N - 1$ levels for N bit resolution, $2^N - 1$ comparators and a logic block.

The input is compared against each reference level and all the comparators make their decisions in parallel, outputting either 1 if $V_{in} > V_{DAC}$ or 0 if $V_{in} < V_{DAC}$. The

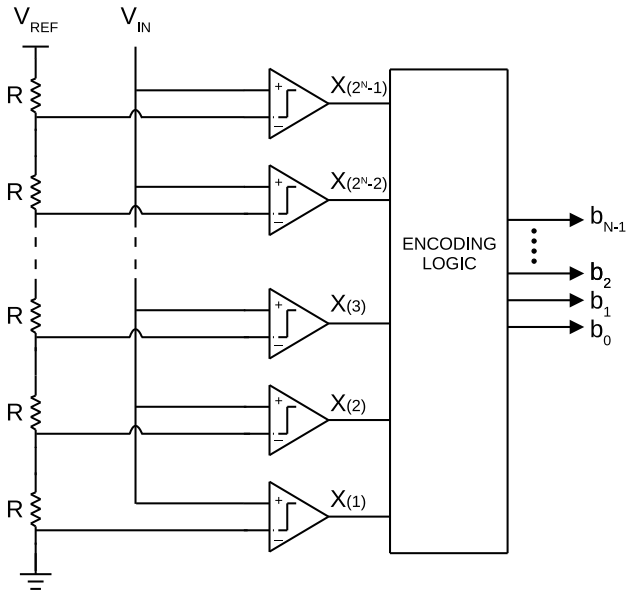


Figure 2.14: Simplified block diagram of a Flash ADC.

decisions of the comparators form a thermometric code [1] that is then converted into a binary equivalent. This whole procedure can be completed during one clock cycle, where half of the clock cycle is used to make the comparisons and the second half is used for the encoding, achieving very fast conversion rates. Nonetheless, this ADC is rarely implemented for applications with resolution over eight bits due to the high design complexity caused by the required number of comparators, resulting in large area and power consumption.

2.2.1.2 SAR ADC

As illustrated in Figure 2.15, a SAR ADC is designed with 4 major blocks: track and hold, DAC, comparator and logic. As opposed to the flash ADC, the conversion is performed in sequence using a single comparator, which is more power efficient. While this ADC cannot compete with the flash architecture in terms of conversion rate, it uses a binary search algorithm which can approximate an unknown signal with a resolution of N bits in N clock cycles (N+1 including the sampling period).

The operation is as follows: when the sampling switch is closed, the ADC tracks the input signal, as already explained in Section 2.1.5. Upon opening the sampling switch

[1] Thermometric code is a unary numeral system where, in this application, the output code is represented by a sequence of consecutive '1's (e.g., '111' for 3).

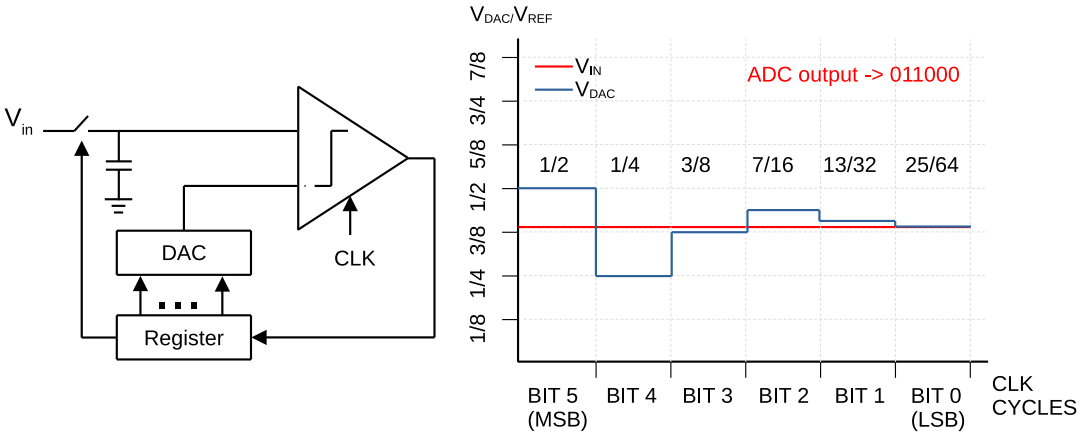


Figure 2.15: Simplified block diagram of a single-ended SAR ADC and sample approximation of 6-bit ADC.

the binary search algorithm commences. First, the N-bit register sets its MSB to 1 while keeping all other bits 0, which forces the DAC output to midscale, that is $V_{REF}/2$. When settled, the comparator is enabled and the input signal V_{IN} is compared to V_{DAC}. Based on the comparator's decision, the MSB of the register is either kept at 1 (for $V_{IN} > V_{DAC}$) or flipped to 0 (for $V_{IN} < V_{DAC}$). The register then continues with the bit trial by setting the consecutive bit (MSB-1) to 1, forcing the V_{DAC} to either increase or decrease by $V_{REF}/4$:

- $V_{DAC} = 3V_{REF}/4$ for $V_{IN} > V_{DAC}$, or
- $V_{DAC} = V_{REF}/4$ for $V_{IN} < V_{DAC}$

The approximation continues in this binary search fashion: with each bit decision, the voltage step is halved ($V_{REF}/8$, $V_{REF}/16$, etc.), effectively narrowing the voltage search range by a factor of two until the register holds an N-bit number representing the ADC's output.

Owing to recent advancements, the SAR can be considered one of the most versatile and most commonly used ADCs for data-acquisition applications [28]. The highly digital architecture benefits from process scaling, thus occupying a small area. It can achieve high accuracy (12-14-bits) and, while its speed is inversely proportional to resolution, it can still operate in the tens-of-MHz range. In the common implementation, SAR ADCs consume only dynamic power, making them power efficient. Furthermore, this

structure can operate at a low supply of $V_{DD} < 0.3V$ and, with advanced energy schemes, in [29, 30] it was shown to achieve an efficiency of 0.44-fJ/Conversion-Step. Due to a broad range of benefits, there is an ever increasing interest in this architecture, with many hybrid architectures also proposed in the literature [31], some of which will be mentioned in the later sections.

2.2.2 Oversampled ADC

One of the techniques to achieve high resolution is oversampling. Oversampling requires that the sampling rate of the ADC must be much greater than the maximum frequency of the input signal. The oversampling ratio is described mathematically in terms of the Nyquist rate sampling criteria, $f_{s,ny}$, and the maximum bandwidth f_b as:

$$OSR = \frac{f_s}{f_{s,ny}} = \frac{f_s}{2 * f_b} \tag{2.24}$$

The intent of oversampling is to distribute the quantisation noise across a broader frequency range resulting in noise reduction within the band of interest, as illustrated in figure 2.16. Using this technique, doubling the sampling ratio can yield a 3 dB improvement in SNR.

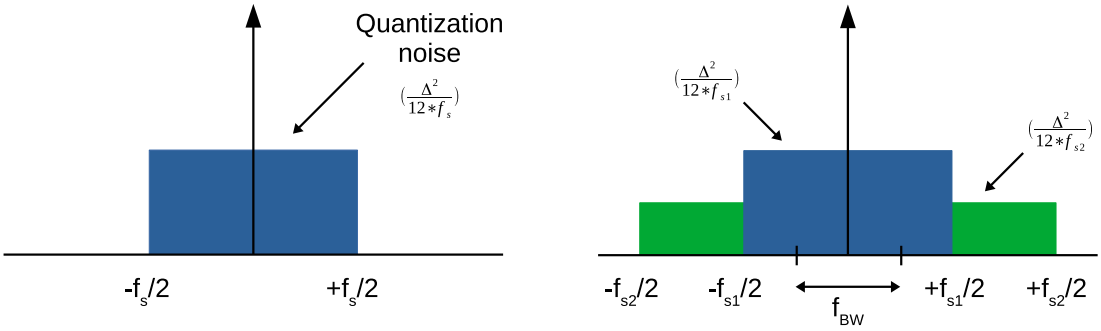


Figure 2.16: Quantisation noise inside and outside the band of interest.

Noise shaping is another concept related to oversampling, where the quantisation noise is now pushed towards the outside of the band of interest, as illustrated in Figure 2.17. This provides additional improvement to the SNR, as the high frequency noise can be processed in the digital domain. While doubling the sampling ratio can already yield a 3 dB improvement in SNR, first-order noise shaping can bring this improvement up

to 9 dB for each doubling of the sampling ratio [32].

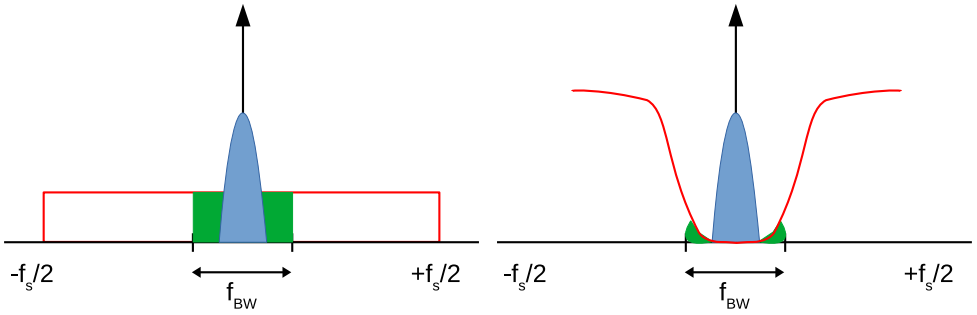


Figure 2.17: Noise shaping of the quantisation noise.

Oversampling and noise shaping are both exploited in Delta-Sigma ADC architecture, commonly also represented with Greek letters as $\Delta\Sigma$. The $\Delta\Sigma$ ADC is one of the most ubiquitous choices for applications where a high effective resolution [33], above 12-bits, is required at medium-to-low speeds. A simplified block diagram is represented by Figure 2.18. The basic blocks of the $\Delta\Sigma$ ADC are a 1-bit quantizer (comparator), a 1-bit DAC and an integrator. The DAC translates the output to the analog domain and feeds it back to the input stage. This arrangement forms a closed loop system. While multi-bit DACs can also be used, these require additional circuitry to remove the non-linearity that results from a more complex design.

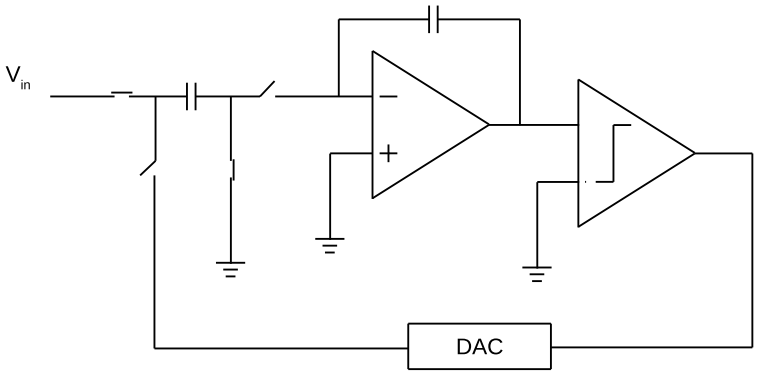


Figure 2.18: Simplified block diagram of a noise-shaping ADC.

The feedback-loop shapes the noise by pushing it to higher frequency, after which the digital low-pass filter is used to remove the quantisation noise falling outside the signal bandwidth and a down sampler reduces the output sampling rate. This results in a high resolution A/D conversion process which can be achieved with a low-bit quantizer. It is also important to note that oversampling relaxes the requirements on the anti-

aliasing filter; furthermore the requirement can be completely eliminated when using a continuous-time ΔΣ ADC [34]. Due to the benefits that come with noise-shaping techniques, these are also employed in traditionally non-oversampled architectures such as SAR ADCs, which have demonstrated >100 dB SNDR[2] [35, 36].

2.2.2.1 ΔΣ modulator

A ΔΣ modulator [32, 33] is the main component of the oversampled ΔΣ ADC. It is a form of pulse-density modulator which converts a continuous time analog input into a 1-bit data stream. The modulator is composed of a loop filter H (an integrator) followed by a 1-bit quantizer (a comparator) whose output is fed back and subtracted from the input signal, as represented using a linear model in Figure 2.19.

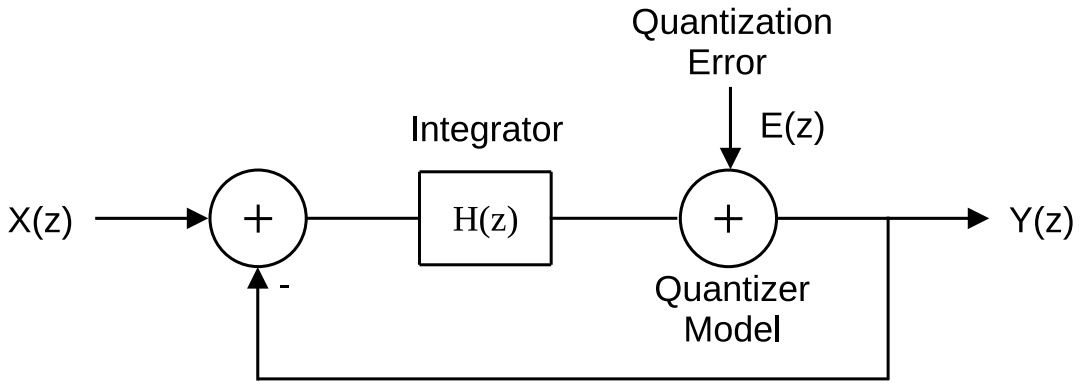


Figure 2.19: Linear model of a 1st-order ΔΣ modulator.

From the linear model the system can be represented by transfer functions in equation (2.25). Here, the first part of the equation is the signal transfer function (STF) and the second part is the noise transfer function (NTF).

$$Y(z) = (\frac{H(z)}{1+H(z)}) * X(z) + (\frac{1}{1+H(z)}) * E(z). \tag{2.25}$$

Using $H(z) = 1/(z-1)$ in equation (2.25) leads to equation (2.26). It can be seen that the input signal is being delayed by one sample but remains otherwise unaltered. However, the quantisation noise is undergoing a $(1-z^{-1})$ transfer function, and is being pushed up to high frequencies.

[2]SNDR, or Signal-to-Noise-and-Distortion Ratio, quantifies the ratio of the power of the desired signal to the combined power of noise and distortion introduced by the converter.

$$Y(z) = z^{-1} * X(z) + (1 - z^{-1}) * E(z) \tag{2.26}$$

By adding another integrator to the noise shaping loop, a 2nd-order modulator can be obtained. This further shapes the quantizer's noise by essentially replacing it with another $\Delta\Sigma$ modulator, as in Figure 2.20. The modulator now yields a noise shaping function of $(1 - z^{-1})^2$:

$$Y(z) = z^{-1} * X(z) + (1 - z^{-1})^2 * E(z). \tag{2.27}$$

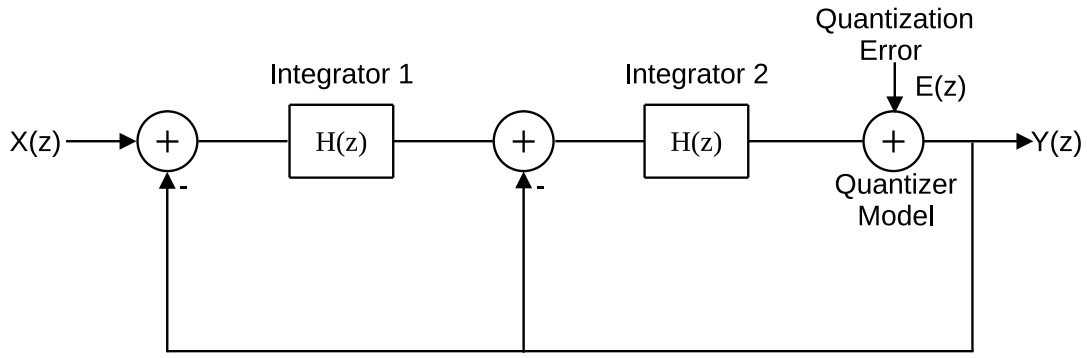


Figure 2.20: Linear model of a 2nd-order $\Delta\Sigma$ modulator.

It can be deduced that the noise shaping capability of the $\Delta\Sigma$ modulator is determined by its order. A 1st-order modulator can achieve 20 dB/decade noise shaping while the 3rd-order can improve it to 60 dB/decade. The order is determined by the number of integrators in the loop filter. There is, thus, an apparent motivation to keep increasing the order but, because this is a closed loop system, stability issues become a concern. Addressing those issues and the increased number of integrators add a high level of complexity and an increase in power consumption and area.

2.2.2.2 Error feedback modulator

Another type of the $\Delta\Sigma$ modulator is an error feedback modulator (EFM) [37, 38, 39] which, among other applications, can be utilised in oversampled digital-to-analog converters. As depicted by the linear model represented in Figure 2.21, the modulator is composed of a quantiser modelled by a gain element $1/M$ and its noise signal $E(z)$,

a scaling element M and a loop filter H_e which, this time, is located in the feedback path. Thus, in this structure, rather than feeding back the output of the modulator, the system filters and feeds back the quantisation error.

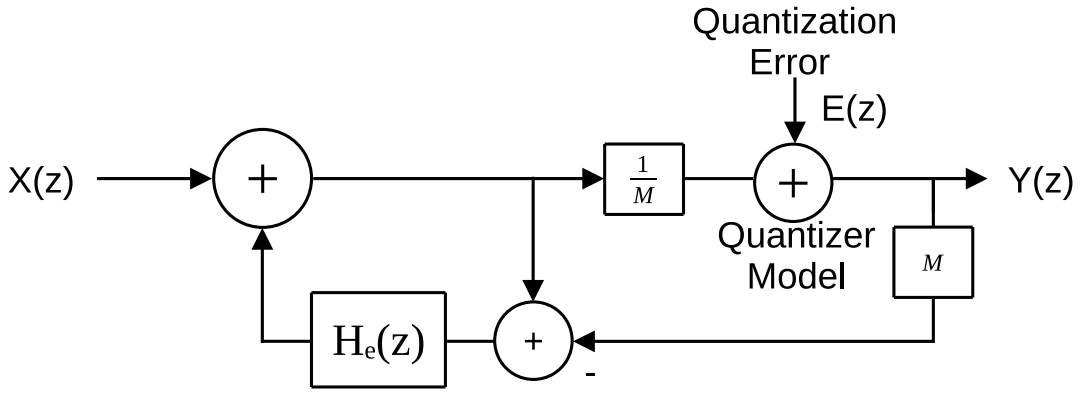


Figure 2.21: Linear model of a 1st-order error feedback modulator.

From the linear model, the z-transform function in equation (2.28) can be derived. This indicates that the input is scaled by the modulator, while the quantisation noise is high-pass filtered.

$$Y(z) = (\frac{1}{M}) * X(z) + (1 - z^{-1}) * E(z). \tag{2.28}$$

The error feedback structure can be readily implemented using a digital accumulator composed of a full adder and a register. The output of the modulator corresponds to a one-bit "carry out" output of the full adder while the n-bit "sum" is fed back to the loop. Owing to its digital nature, with advances in technology, this topology can achieve high area, power and speed efficiency.

2.2.3 Sub-sampling and event-driven ADCs

Whereas the Nyquist and oversampled ADCs are often designed with sinusoidal input signals in mind, in many sensor readout applications the signals that require conversion do not have the same constraints. Sensors, such as those in environmental monitoring or healthcare, often produce non-periodic outputs with extended intervals of inactivity. Thus, contrary to the traditional sampling approach in Figure 2.22(a), compressed sensing (CS) algorithms [40, 41, 42] can be applied to take advantage of the sparsity

and the pre-existing knowledge of the input signal. Fundamentally, instead of sampling the data periodically, a non-uniform sampling strategy can be utilised to only extract the relevant information, such as the amplitude and position of the pulses of interest, thereby highly reducing the amount of captured data and relaxing the sampling rate requirement on the ADC. A high-level diagram of analog-to-information conversion is represented in Figure 2.22(b). One of the recent examples of applications that have adopted sub-sampling is that of digitising RF signals [18].

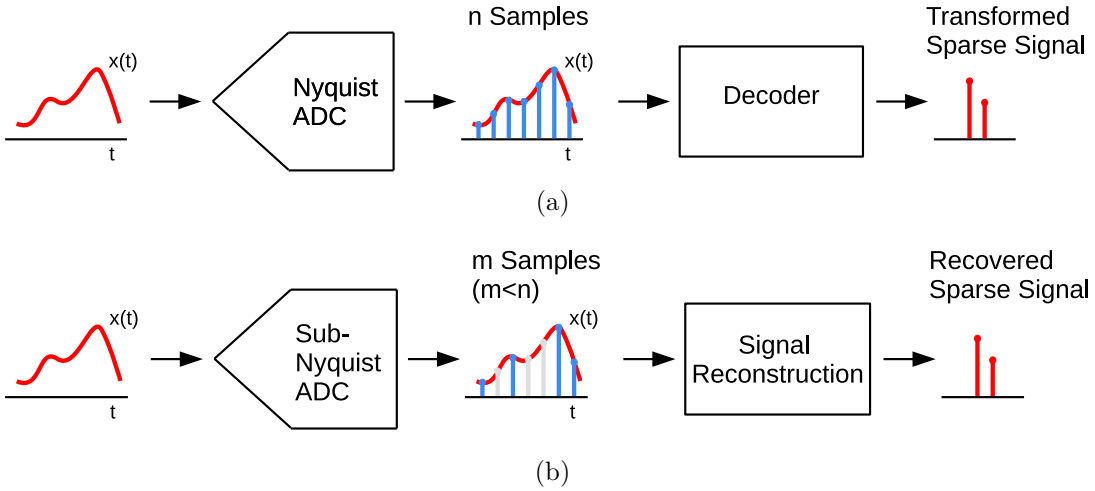


Figure 2.22: A high-level diagram of Nyquist sampling (a) and analog-to-information conversion (b) [43].

However, while CS can relax some aspects of the design it also adds some complexity to the system, especially when feature enhancing filters [44, 45] are required. Another approach that can be applied to achieve event-based sampling is level-crossing sampling [46, 47], where the observed input signal is simply compared against evenly spaced reference levels. Thus, instead of sampling the input signal periodically, the ADC tracks the input continuously and generates an output when a change in the input, such as a pulse, is detected. This can be implemented with the Level-Crossing ADC (LC-ADC) architecture represented in Figure 2.23. The ADC uses two comparators to track the input signal, within upper and lower bounds of the 1 LSB wide window, generated by the DAC. When the input signal crosses either of the bounds, the thresholds are updated by 1 LSB in the direction of the crossing and two outputs are generated, namely the code and the time-stamp for the applications that require signal reconstruction.

Note that, since this system does not sample the input with a clock, it is alias free and its in-band quantization error is reduced, resulting in a higher SNDR than in the conventional ADC with the same number of bits [48]. However, this architecture is susceptible to slope overload, where the ADC can be unable to update the thresholds quickly enough to track a fast changing signal over its full scale. Furthermore, the traditional implementation uses power-inefficient continuous-time circuits. These issues were addressed in [49, 50, 51].

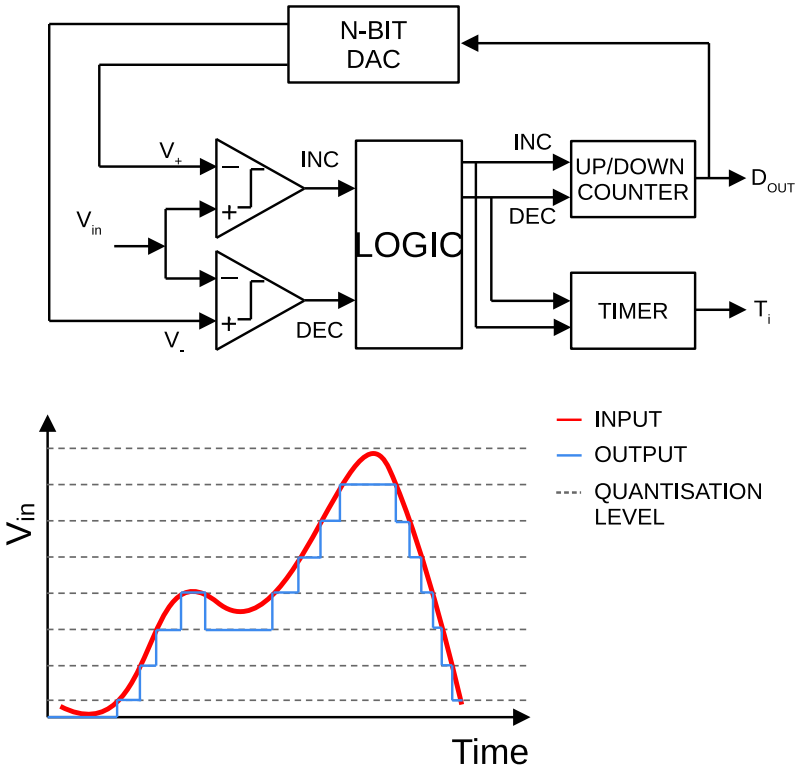


Figure 2.23: Diagram of Level crossing ADC with conversion levels.

2.2.4 Time-based ADCs

While technology scaling is necessary to keep up with the growing demand for processing power, its benefits favour high-speed digital over an analog design [52]. This makes it increasingly difficult to achieve a high accuracy analog to digital conversion in the voltage domain due to a reduction of the supply voltage (VDD), which further results in a lower signal swing, and hence a decreasing SNR [53]. To take advantage of smaller gate lengths, many researchers working with smaller transistor geometries are looking for a solution by quantising the input signal in the time domain [54]. Moreover,

since the time-mode circuits are inherently digital, moving signal processing from the voltage to the time domain can result in a more robust design, as these offer more immunity to interference such as cross talk or substrate coupling [55]. Consequently, the time-based ADCs have gained traction in recent years. One of the older architectures that is prevalent in portable instrument applications, such as digital multi-meters, are integrating ADCs [56]. The integrating ADC, sometimes referred to as a charging or ramp ADC, can achieve high resolution, >12-bits, but is limited by conversion rate. However, the slow speed isn't a big drawback in many sensing applications, such as air quality monitoring. Another type of time-based quantizer is a voltage controlled oscillator (VCO). The main appeal of this converter is its highly digital topology, with reduced area and increased conversion rates, allowing it to achieve conversion rates of Gsamples/s [57, 58]. Additionally, VCO-based ADCs have the appealing property of first-order noise shaping of their quantisation error [59]. However, due to non-idealities such as jitter or non-linearity, to achieve good performance, an increase in power consumption is warranted.

2.2.4.1 Integrating ADCs

A single slope ADC, as illustrated in Figure 2.24, is the most basic type of integrating ADC. This architecture uses an integrator to generate a ramp that can be used to compare against the input. As the reference voltage V_{REF}, resistor R, and capacitor C are fixed parameters, the integrator's output voltage, V_{RAMP}, is directly proportional to time, as described with the following expression:

$$V_{RAMP} = \frac{1}{RC}\int_0^T (V_{REF})\,dt \; = \frac{TV_{REF}}{RC}, \tag{2.29}$$

The integrator's parameters are chosen so that the voltage step of the ramp during each clock cycle is equivalent to one LSB. As the V_{RAMP} is increasing, the counter records the number of clock cycles (each of duration T) it takes for the V_{RAMP} to exceed the input voltage, which is indicated by a comparator's decision. When the comparator's output toggles, the counter's output is latched, representing the ADC's binary output code. Finally, the control logic clears the counter and resets the ramp

generator before the next conversion can start. The resolution of the integrating ADC is directly proportional to the conversion time, which is 2^N clock cycles for a full-scale input. However, there are some solutions proposed, such as code-prediction methods used in [60], to overcome the resolution and speed issues.

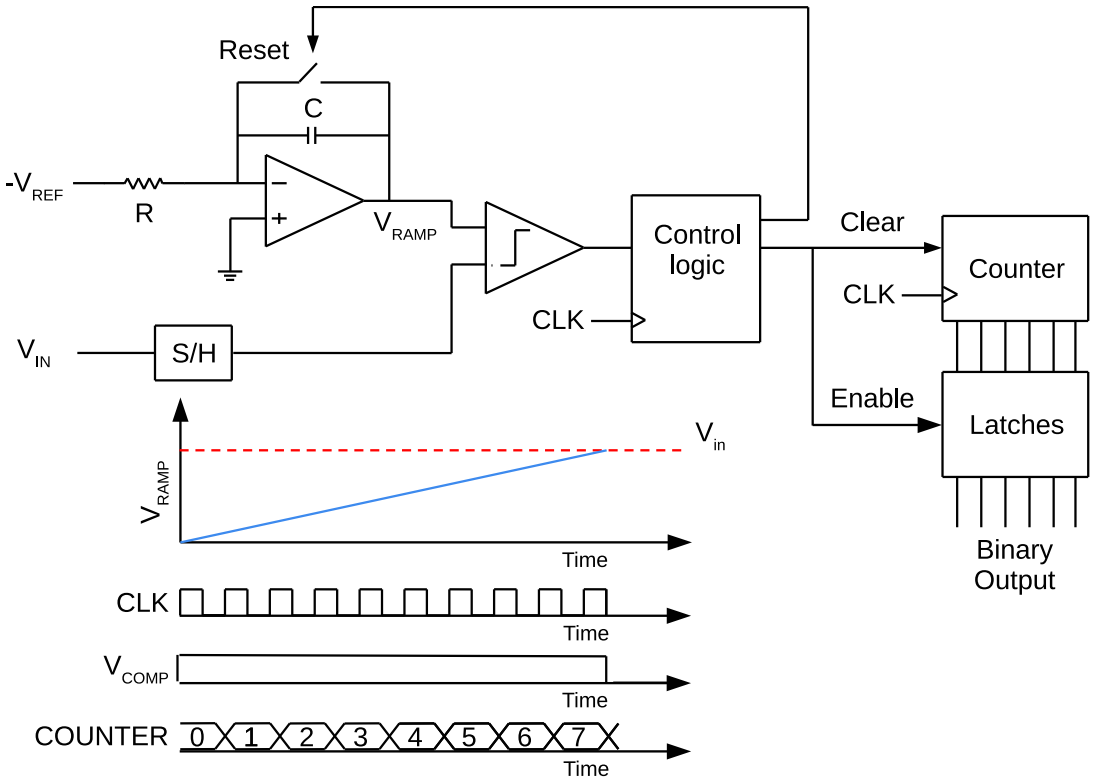


Figure 2.24: Simplified diagram of a conventional single-slope-based ADC with a timing diagram.

Considering that the output accuracy of a single-slope ADC depends on the accuracy of the integrator and its RC components, dual-slope ADCs [61] are often implemented to mitigate most linear error sources, including temperature and ageing effects. In this case, as represented in Figure 2.25, instead of connecting the sampled input V_{IN} directly to the comparator, first the sampled V_{IN} is integrated for a fixed time period T_1, after which the V_{REF}, with an opposite polarity to the input, is applied to the integrator for time T_2. Thus, the input voltage can be obtained from the ratio of T_1 to T_2 and the reference voltage:

$$\frac{V_{IN}}{V_{REF}} = \frac{T_2}{T_1}. \tag{2.30}$$

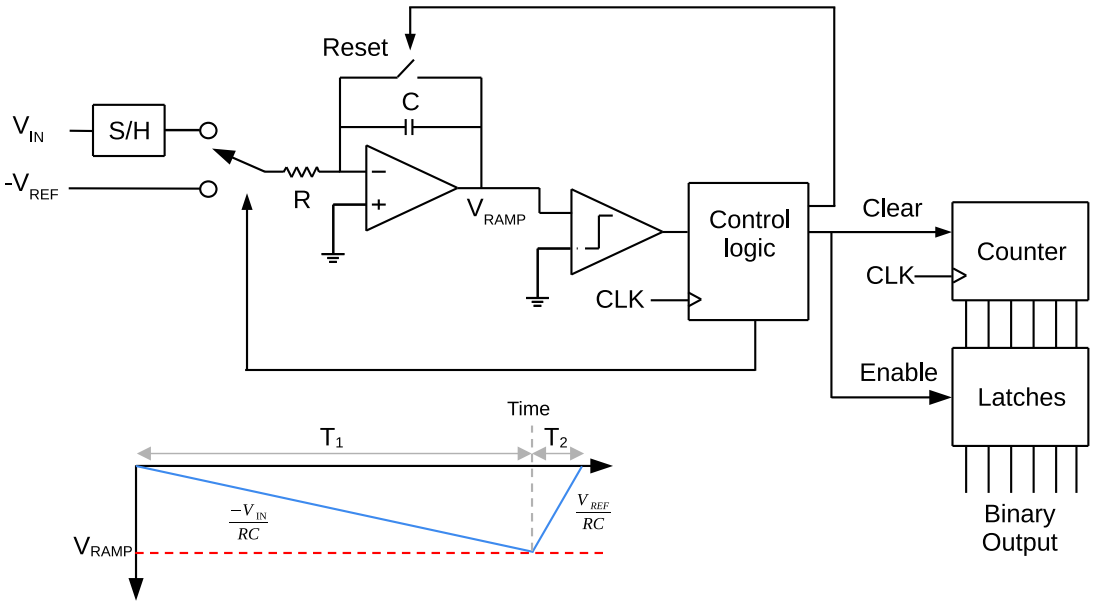


Figure 2.25: Simplified diagram of a conventional dual slope-based ADC with a timing diagram.

As can be expected, the improved accuracy of dual-slope ADCs comes at the cost of a further speed penalty, where the conversion time is now twice as long as that of the single-slope ADC. Note that, while the actual conversion times of the slope ADCs scale with the magnitude of the input voltage, the conversion rate is often calculated based on the worst case scenario, to keep a fixed output data rate and simplify data processing.

2.2.4.2 Digital ramp ADC

A digital-ramp ADC, also called a counter ADC, has a very similar operation to the slope ADC, as can be seen by comparing Figures 2.24 and 2.26. The main architecture difference is in how the ramp signal is generated. A counter ADC uses a static DAC whose output is increased by one LSB every clock cycle until it exceeds the input amplitude. Thus, instead of a continuous output, a staircase like ramp is generated. Since this DAC can be implemented with resistor strings, it may be considered an easier and cost-effective alternative to an integrated circuit. The main advantages of resistor string DACs is the inherent monotonicity [62] and digital like architecture. It is, however, impractical for resolutions above 10-bits due to having a large area and a long settling time. While the conversion time of the traditional implementation of

this ADC is the same as of a single-slope ADC, variations such as multiple-ramp [63], two-step [64] and asynchronous [65] were proposed, showing increased potential for this architecture.

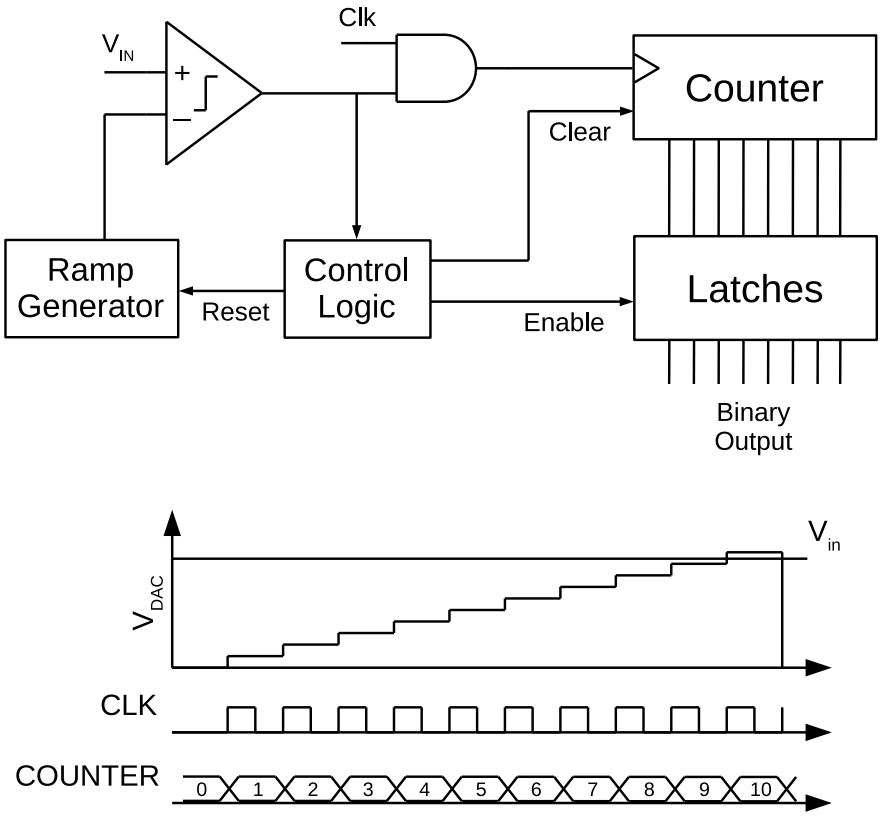


Figure 2.26: Block diagram of a counter ADC with a timing diagram

2.2.4.3 VCO-based ADC

A voltage-controlled oscillator (VCO), as the name suggests, is an oscillator whose frequency depends on the applied input voltage. In the VCO-based ADC (as illustrated in Figure 2.27), the input voltage is converted into a continuous series of pulses whose frequency is proportional to the input. The pulses are counted during the sampling phase and the count is translated into its binary equivalent. The quantiser can be implemented using a highly digital architecture, for example utilising a ring oscillator [66], achieving high speeds limited only by the logic gate delay. The resolution of this ADC depends on the range of frequencies that the VCO can produce. Multi-phase VCOs can be used to increase the resolution and speed. As the VCO produces a continuous phase output, the quantisation error of the previous sample is not lost but is

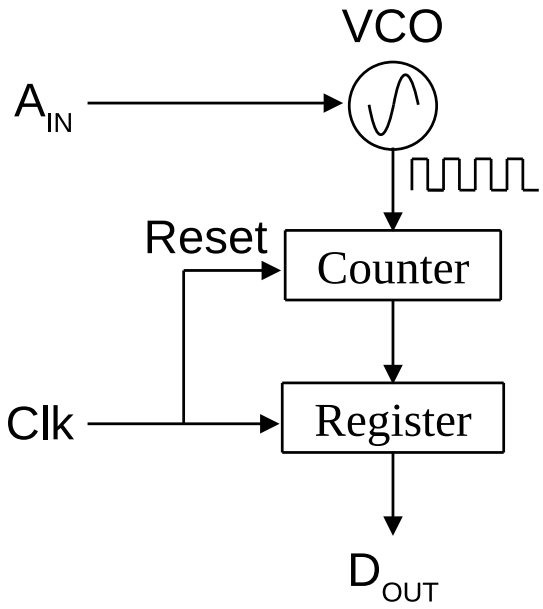


Figure 2.27: VCO-based quantizer.

accounted for in the following measurement, resulting in an inherent first-order quantisation noise-shaping property, similar to that of a $\Delta\Sigma$ ADC. While these features can make this architecture very appealing, it is susceptible to non-linearity and process, voltage-supply, and temperature (PVT) variations [54, 57]. A digital calibration method can be implemented to improve some of the issues with VCO-based quantisers. To further reduce its non-linearity while taking advantage of its highly digital hybrid architecture, structures with the VCO embedded in a $\Delta\Sigma$ modulator were proposed [67].

2.3 SAR ADC

While the top level operation of the SAR ADC has already been introduced in Section 2.2.1.2, the detailed description of the conventional single-ended architecture, represented in Figure 2.28, is intended to provide background to the design discussed in Chapters 3 - 5.

2.3.1 DAC

The DAC's function is to generate a reference voltage for the comparator. It can be designed using various architectures, such as a resistor string [68], switched-capacitors

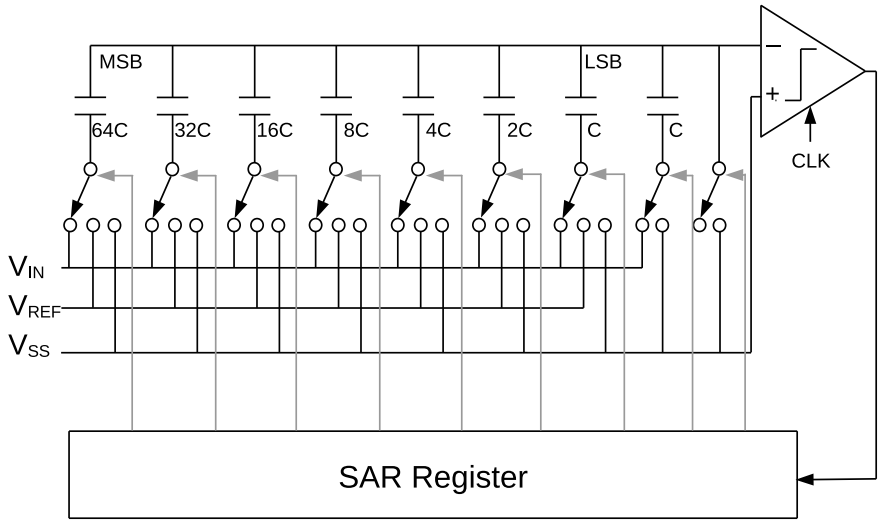


Figure 2.28: Conventional implementation of DAC in single-ended ADCs.

[69], or a mix of both. While there are some recent SAR ADCs utilising a resistive string DAC [70, 71], the capacitive DAC is the more popular choice [28], as it can also form part of the sample and hold circuit.

2.3.1.1 Binary weighted capacitor DAC

An example of a single-ended SAR ADC with a switched-capacitor DAC is represented in Figure 2.28. As depicted, the DAC is formed by an array of binary-weighted capacitors. The operation is now described. At the beginning of the conversion, all the capacitors are connected to V_{IN} to sample the signal; this way the sample and hold circuit functionality is implemented utilising the same capacitors. Next, the binary search starts by sequentially switching the bottom plates of the capacitors to either V_{REF} or V_{SS}, depending on the comparator's decisions, while the top plate floats, enabling the charge distribution. The two main advantages of a capacitor DAC are power efficiency, because there is no static power dissipation, and linearity, because this is a function of the ratio of the capacitors, which results in good matching. The linearity can also be further improved with digital calibration techniques [72]. One of the disadvantages of the capacitive DAC is the large number of elements required.

2.3.1.2 Split-capacitor DAC

To decrease the number of elements in a switched-capacitors DAC, an attenuator capacitor (also called bridge capacitor) can be added to split the array into two sub-arrays, as in Figure 2.29. According to Ahuja [69], a 10-bit 5-5 split capacitor DAC requires only 63 unit elements, as opposed to 1023 units in the binary-weighted architecture. However, the split-capacitor DAC is more sensitive to unit-capacitor mismatch and parasitic capacitances, which negatively affect the linearity and can lead to a larger consumed area.

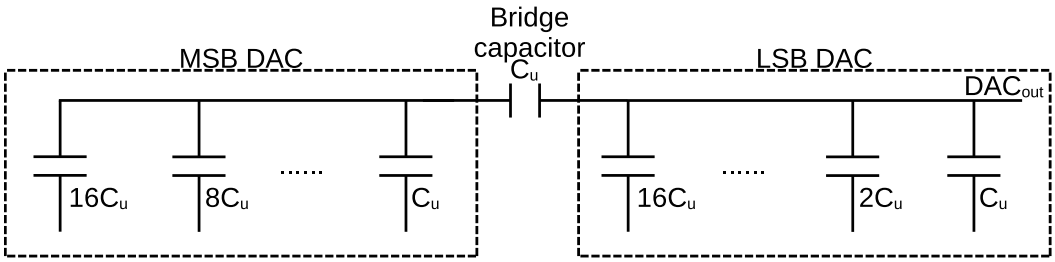


Figure 2.29: Diagram of a 5-5 split-capacitor DAC.

2.3.1.3 Redundancy

Redundancy [73, 74] is a digital error correction method for static non-linearities which helps minimise the sampling capacitors, saving power and area. It is also beneficial in a high sampling rate SAR ADC as it relaxes DAC settling requirements which, in turn, allow an increase in sampling frequency. Instead of a traditional binary network, the method utilises a sub-radix-2 redundant DAC architecture, where the DAC capacitors are scaled using a smaller factor. Figure 2.30 illustrates a sample split-capacitor DAC array with redundancy which was proposed in [75].

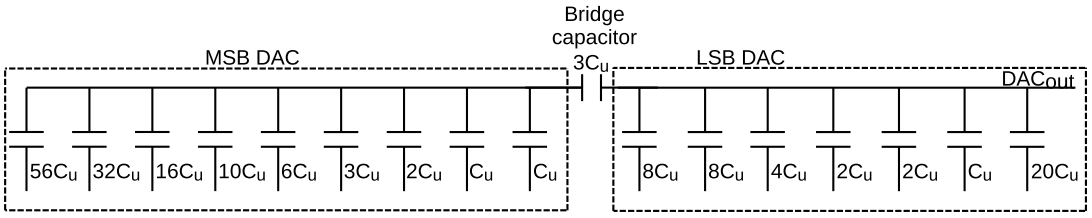


Figure 2.30: Schematic of a split-capacitor DAC array with redundancy [75].

This gives the SAR ADC a possibility to recover from a bad comparator decision by representing every input voltage by more than one digital code, as demonstrated in

Figure 2.31. However, the extra decision steps increase the complexity of the DAC and logic, as the output code needs to be converted to a binary code.

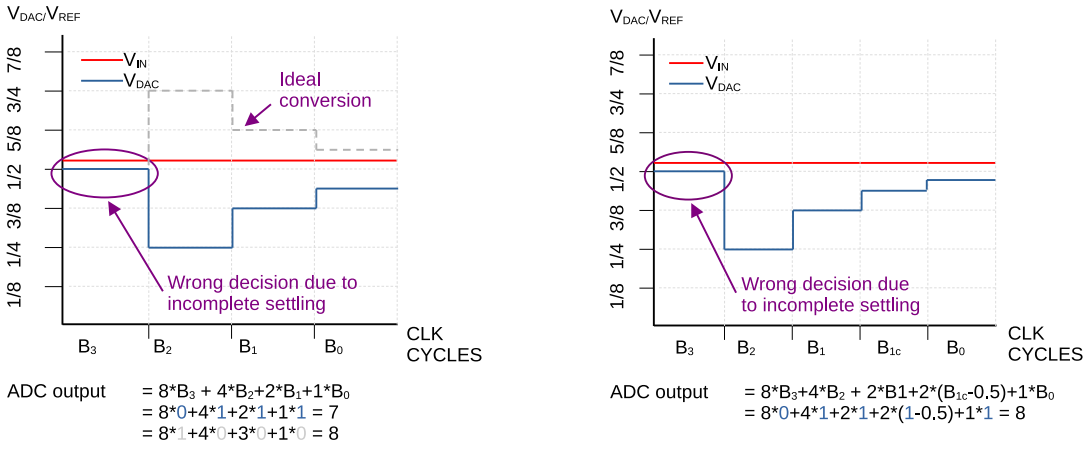


Figure 2.31: Diagram of a successive approximation search without compensation (a) and with the redundancy (b).

Some other methods to increase the efficiency of the SAR ADC can include the LSB-first successive approximation (SA) [76], where power is saved by checking the signal activity before running the full binary search, or the Semi-Resting DAC [77] where the 11-bit SAR ADC is split into two 10-bit ADCs, each responsible for conversion of half of the input range. After the sampling phase, the signal polarity is detected looking at the MSB and one of the 10-bit ADCs is disabled. This enables a potential reduction of power.

2.3.2 Comparator

The comparator is another crucial element in the design of an ADC and, in particular, a SAR ADC. As the name suggests, its main function is to compare the input signal against the reference. The output of this comparison then drives the successive approximation register. There are many comparator architectures to choose from, depending on the target application; however, dynamic comparators are preferable in SAR ADCs due to the power consumption. Most of such comparators consist of a preamplifier and a latch, as in Figure 2.32. The pre-amplification relaxes the noise requirements by amplifying the input to the latch, which reduces the noise of the latch when it's referred

to the input. This allows for a faster latch operation, saving power consumption. If the differential input is small, the latch may not have enough time to resolve, thereby entering metastable state and introducing errors to the ADC.

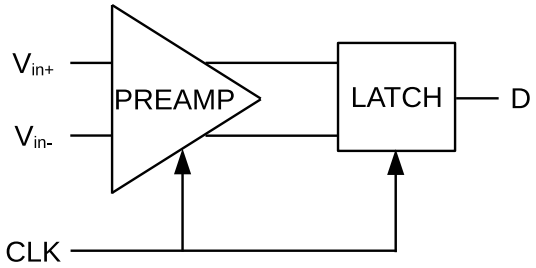


Figure 2.32: Main building blocks of a dynamic comparator, consisting of preamplifier and a latch.

A commonly utilised comparator architecture in SAR ADCs is the StrongARM latch [78], which is illustrated in Figure 2.33. The circuit is composed of a differential input pair, two cross-coupled pairs to realise the latch and four pre-charge switches. Initially, when the CLK is low, the differential input pair $(M_1 - M_2)$ is off and the V_{OUT} nodes are pre-charged to V_{DD}. Once the CLK transitions high, the PMOS switches turn off and M_1 and M_2 turn on, each starting to draw a current in proportion to the difference between V_{In1} and V_{In2}. Since, at this stage, the cross-coupled NMOS pair $(M_3 - M_4)$ would still be off, the current is flowing from nodes P and Q, causing the V_P and V_Q voltage difference to exceed that of the input node difference, resulting in amplification. Once the V_P and V_Q nodes fall to $V_{DD} - V_{THN}$, the NMOS cross-coupled pair is turned on thereby enabling further amplification by allowing the current to flow from the X and Y nodes. Finally, when the V_X and V_Y nodes discharge to $V_{DD} - V_{THP}$, the PMOS cross-coupled pair is turned on thereby discharging one output node to zero while charging the other to V_{DD}, producing a rail-to-rail output V_{OUT} resulting from the V_{IN} difference. The output of the StrongArm is then followed by a reset-set (RS) latch to ensure the correct output is read by the logic. The zero static current, rail-to-rail outputs, and the fact that the input-referred offset is controlled by one differential pair brought the StrongArm latch into popularity [79]. One of the downsides of this topology, however, is a kickback current drawn from the inputs and the supply.

In a high resolution SAR ADC (over 10 bits) the comparator can dominate the power

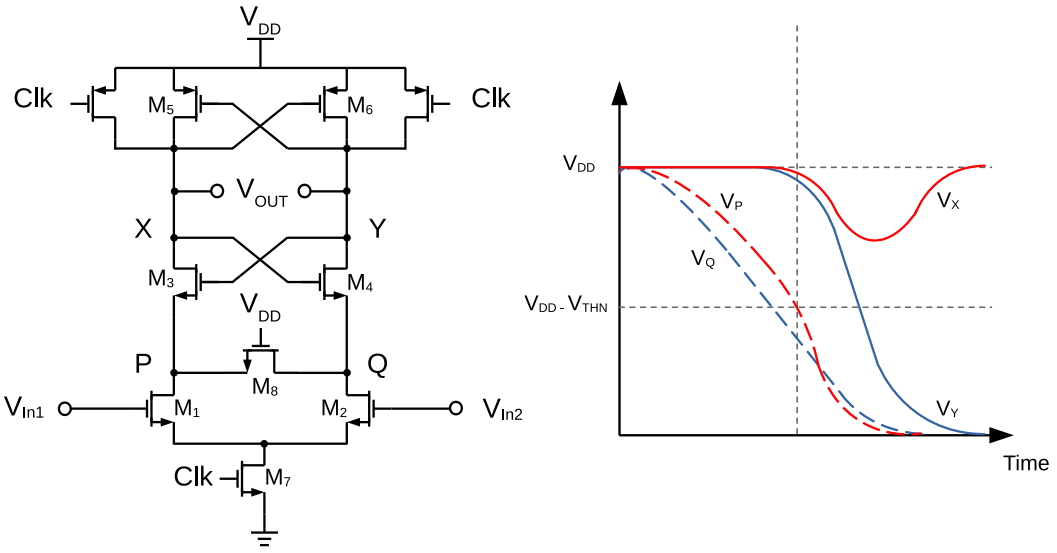


Figure 2.33: Transistor level diagram of a StrongArm latch comparator, with its associated voltage levels during amplification and regeneration stages.

consumption [31]. One of the proposed solutions available in the literature to decrease the power consumption of a comparator is a bidirectional topology [80] where amplification happens at both rising and falling clock edges. The capacitances at the V_{OUT} nodes are charged to only $\frac{1}{2}V_{DD}$, saving approximately half the energy consumed by a preamplifier, at the expense of introducing extra complexity to the level detector and clock controls. Another option could be adding a capacitor in series with the tail (such as M_7 in Figure 2.33), as was done in [81]. The purpose of this is to cease an amplification once the signal is ready to be latched. This method saves power, similar to the bidirectional architecture, with less design effort.

2.3.3 SAR Logic

The simplest SAR logic can be implemented with just a number of sequential flip flops, proportional to the resolution of the ADC, as in Figure 2.34. After the control block exits the reset state, the logic enables sampling for one or two clock cycles, depending on the design. Once the SAR algorithm commences, the DAC switches are controlled sequentially from MSB to LSB. After closing each switch, the logic waits on the comparator decision to either keep that switch closed or opened and latching the equivalent zero or one before proceeding to the next bit. Once the LSB switch is set, the latched binary code forms the SAR ADC's output.

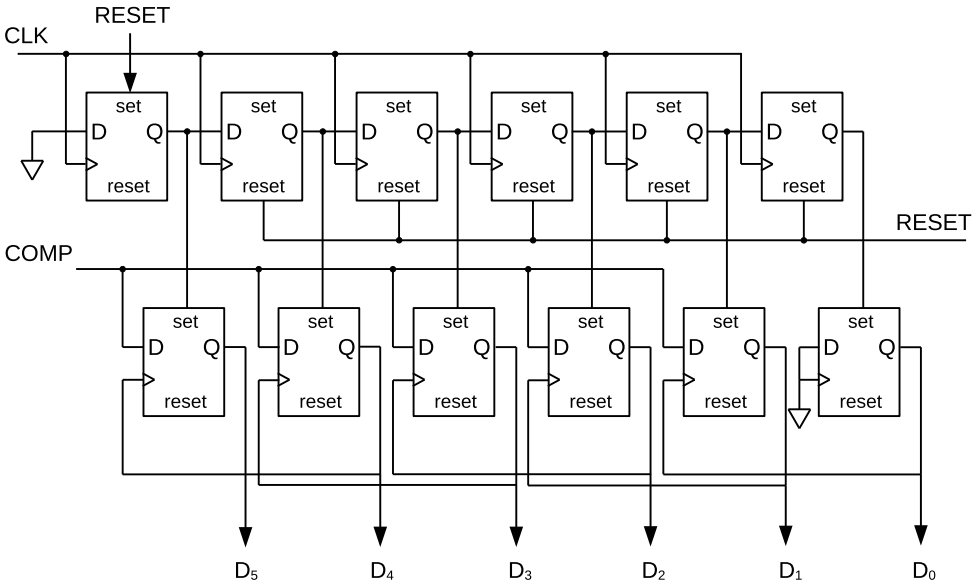


Figure 2.34: SAR logic for a 6-bit converter.

The example just described uses a master clock to control all the SAR ADC building blocks and to drive each stage of the binary search. The bottleneck of that is the clock period needs to provide enough time for the DAC to settle to the required accuracy and for the comparator to make its decision, which would be determined by the worse-case scenario. Additionally, in high-speed ADCs, the generation of this high-speed internal clock adds a significant overhead, substantially increasing the power consumption of the converter. Nowadays, asynchronous (or self-synchronized) logic has become an attractive alternative [82, 83, 84, 85]. Here, a much slower master clock running at the sample rate is used to achieve the uniform sampling, but the binary-search algorithm is executed asynchronously. Here, each stage of the conversion cycle is triggered by a ready signal issued by the comparator after it makes its decision. Additionally, mechanisms such as a complimentary CMOS NAND gate with an adjusted input threshold [82] are implemented in the comparator to force the ready signal and prevent issues in case of a slow comparator resolve time.

2.4 Bridge to Digital Conversion

The Wheatstone bridge (WhB) [86] is the conventional architecture for interfacing to resistive based sensors. The measuring circuit is obtained by placing the unknown

resistive sensor, R_s, in a diamond-shaped configuration with 3 other known resistors, as illustrated in Figure 2.35. To determine R_s, first the known resistors are adjusted until V_{OUT} has zero potential and then R_s can be simply computed from the ratios of the resistors, where R_s/R_3 equals R_2/R_4. This method gives a highly accurate result because it is independent of variations of the power supply, V_{REF}.

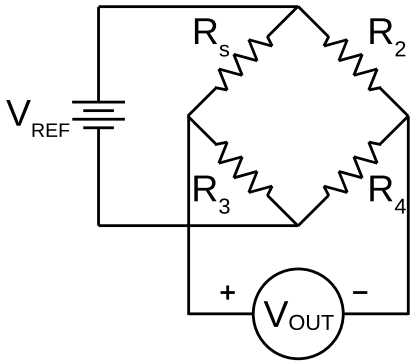


Figure 2.35: Typical Wheatstone Bridge configuration.

The unknown resistance R_s can also be computed directly by measuring V_{OUT} and substituting all the known resistor values into equation (2.31). Assuming that no current is drawn by the ADC measuring V_{OUT}.

$$\frac{V_{OUT}}{V_{REF}} = \frac{R_2R_3 - R_SR_4}{(R_S + R_3)(R_2 + R_4)} \tag{2.31}$$

Instead of varying the resistance of the WhB components, the majority of bridge interface circuits rely upon measurement of changes in V_{OUT}. The WhB output is typically a mV-level differential signal that needs to be detected on a greater common-mode voltage. As a consequence, so as not to impair the performance, the ADC needs to have a high input impedance and gain, be linear and have an offset and noise in the range of that of the WhB. Additionally, the ADC is required to have high power-supply and common-mode rejection ratios [87]. In sensor applications, high energy efficiency is also indispensable. All of this makes the design of the ADC challenging, even with relaxed sampling rate requirements in range of few kHz.

Conventionally, ADCs interfacing to a WhB, commonly called Bridge-to-Digital Converters (BDCs), require the differential output to be buffered and amplified, before be-

ing digitised. Recent advancements have seen the development of Direct BDCs where the output of the Wheatstone Bridge is connected directly to the converter. The two approaches are described below.

2.4.1 Conventional BDCs

The conventional bridge-to-digital converter is illustrated in Figure 2.36. As depicted, before the output from the bridge is digitised by an ADC, it is first preconditioned by an instrumentation amplifier (IA). The ability to share the ADC reference voltage with the BDC means distortions on the reference are cancelled out, resulting in a relaxed reference requirement.

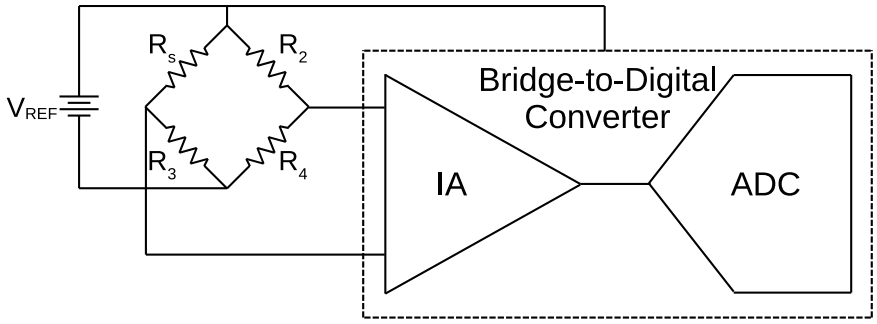


Figure 2.36: System diagram of a conventional Bridge-to-Digital Converter.

The IA has three important functions; first, to amplify the amplitude difference between the differential outputs from the bridge; second, to provide a high impedance to the bridge and a low impedance to the ADC input and, finally, to suppress unwanted common-mode signals [88]. Other requirements include low input-referred noise and low power consumption. The IA is a critical block in a conventional WhB converter because any noise it adds to the input signal is later sampled by the ADC. Therefore, there has been a lot of research done to improve the performance of this block [87]. Some of the IA architectures widely used in BDCs are the 3-Opamp IA, the Current Feedback IA (CFIA) and the Capacitively-Coupled IA (CCIA), all illustrated in Figure 2.37.

The three-opamp IA and CFIA have two noise-critical input stages, requiring two high-gain amplifiers [89]. While they both have high input impedance, they both have a low power efficiency [90]. With good design, the Common-Mode Rejection Ratio (CMRR)

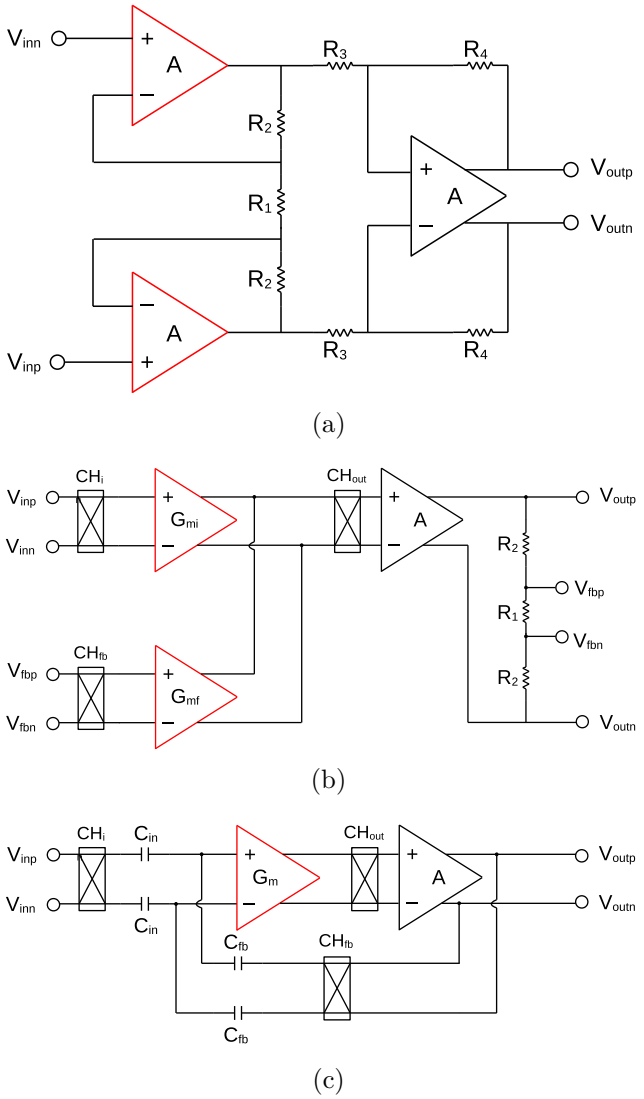


Figure 2.37: Standard architectures of three-opamp (a), CFIA (b) and CCIA (c) instrumentation amplifiers. CFIA and CCIA both employ chopping.

of a CFIA can reach above 120 dB, which is superior to the three-opamp IA. The gain accuracy of the CFIA is, however, limited due to the matching of the two input stages, G_{mi} and G_{mf}, but can be compensated with Dynamic Element Matching (DEM) and gain error-correction techniques [91]. The CCIA requires only one high-gain input stage, while achieving both high-power efficiency and gain accuracy, allowing it to became a popular choice [92, 93, 94, 95]. The common-mode voltage range of the CCIA is also superior as it exceeds the supply voltage, owing to the input capacitors. The CFIA and CCIA amplifiers have a wider input voltage swing than the three-opamp structure and, thus, are often preferred in high precision applications.

As denoted by CH in Figures 2.37(b) and 2.37(c), the CFIA and CCIA amplifiers often employ chopping, which is a dynamic offset compensation technique. Chopping can reduce the initial offset of an amplifier by a factor of 100 to 1000 and also helps to reduce offset drift over temperature or time [96]. Additionally, it suppresses in-band 1/f noise. However, it can limit the input impedance of the CCIA, where the impedance is inversely proportional to the chopping frequency. Chopping is also responsible for generating output spikes at twice its frequency; while, in theory, this could be easily mitigated by adequately timing the sampling of the ADC, this can introduce further issues, such as an increase in noise aliasing. Noise aliasing is also introduced if the alternative auto-zeroing technique is used instead of chopping. However, it can be shown [93] that implementing both techniques simultaneously can mitigate each others' shortcomings.

Preconditioning of the WhB output relaxes the ADC's requirements. Nonetheless, a high resolution converter is still required, making noise-shaping-based designs a popular choice, such as in [97, 98]. The benefits of these architectures were already discussed in Section 2.2.2. VCO-based ADCs, which were explained in Section 2.2.4.3, are also extensively researched in the area of WhB interfaces [99]. Finally, SAR ADCs, while traditionally targeting mid-range resolution applications, are also showing promising results [100, 101, 102].

2.4.2 Direct BDCs

The conventional BDC architectures may be preferable in demanding applications; however, the requirement for high-gain amplifiers makes it complex and an area inefficient solution. In order to reduce the design effort, an IA and an ADC were embedded into a single loop, as in Figure 2.38. This type of bridge converter is called a Direct BDC (D-BDC).

While in D-BDC the design effort can be focused entirely on a single loop, this unquestionably tightens even further the already stringent ADC requirements. Hence, continuous-time architectures are preferable, to eliminate aliasing and thermal noise [87]. The DEM technique and chopping are also often implemented [103] to increase

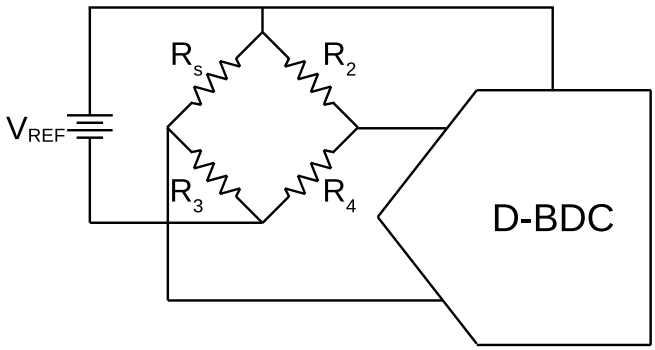


Figure 2.38: System diagram of a Direct Bridge-to-Digital Converter.

accuracy and stability. Two recognised architectures that can satisfy the challenging requirements are continuous-time $\Delta\Sigma$ modulators [104], and more recently, the voltage-controlled oscillator (VCO) [105]. Continuous-time $\Delta\Sigma$ modulators are more efficient and occupy significant area mainly due to the integrating capacitors. VCO-based designs can reduce the area but typically require more power.

2.5 ADC and BDC Metrics

As already mentioned in the previous section, depending on the target application, various ADC architectures can be employed. To compare their performance, two popular Figures of Merit (FoMs) are widely used.

- The Walden FoM [106] is preferred for ADCs whose performance is limited due to quantisation noise, which are typically ADCs with a resolution below 10 bits, and is given by:

$$FoM_w = \frac{P}{2^{ENOB} * f_s}. \tag{2.32}$$

  Here, P is the power consumed, $ENOB$ is the effective number of bits and f_s is the Nyquist sampling frequency of the ADC. The units of the Walden Figure of Merit are fJ/conversion-step and the lower the calculated FoM the better the efficiency that is achieved. When ENOB is increased by 1, FoM is halved, given the other parameters remain unchanged. The ADC performance trend based on the Walden FoM is represented in Figure 2.39(a).

- The Schreier FoM [107], in turn, is better suited for ADCs whose performance is limited by thermal noise and that achieve resolution higher than 10 bits and is given by:

$$FoM_s = SNDR_{dB} + 10\log(\frac{BW}{P}). \tag{2.33}$$

Here $SNDR$ is the signal to noise and distortion ratio in dB, BW is the Nyquist bandwidth of the ADC and P is the power consumed. The resulting unit of this FoM is dB and the higher number indicates a more efficient ADC. The original Schreier FOM was defined without accounting for distortion [108]. The ADC performance trend based on this FoM is represented in Figure 2.39(b).

BDCs can be compared using either the aforementioned FoMs or Noise Efficiency Factor (NEF) and Power Efficiency Factor (PEF). NEF and PEF are recognised as better ratings of the energy-efficiency of BDCs, which determines the performance of the IAs [87].

- NEF

$$NEF = V_n\sqrt{\frac{2I_{tot}}{\pi * V_t * 4kT * BW}}, \tag{2.34}$$

where, V_n is the input-referred noise voltage of the amplifier, I_{tot} is the total current from the supply, V_t is the thermal voltage kT/q and BW is the bandwidth.

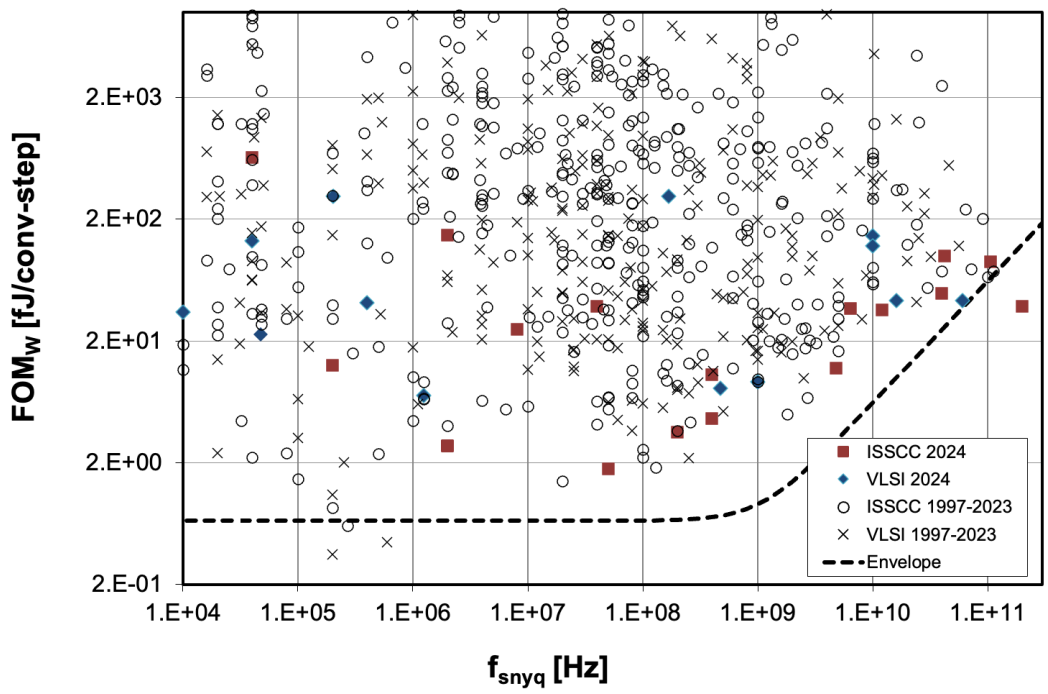
- PEF includes the supply voltage.

$$PEF = NEF^2 * VDD, \tag{2.35}$$

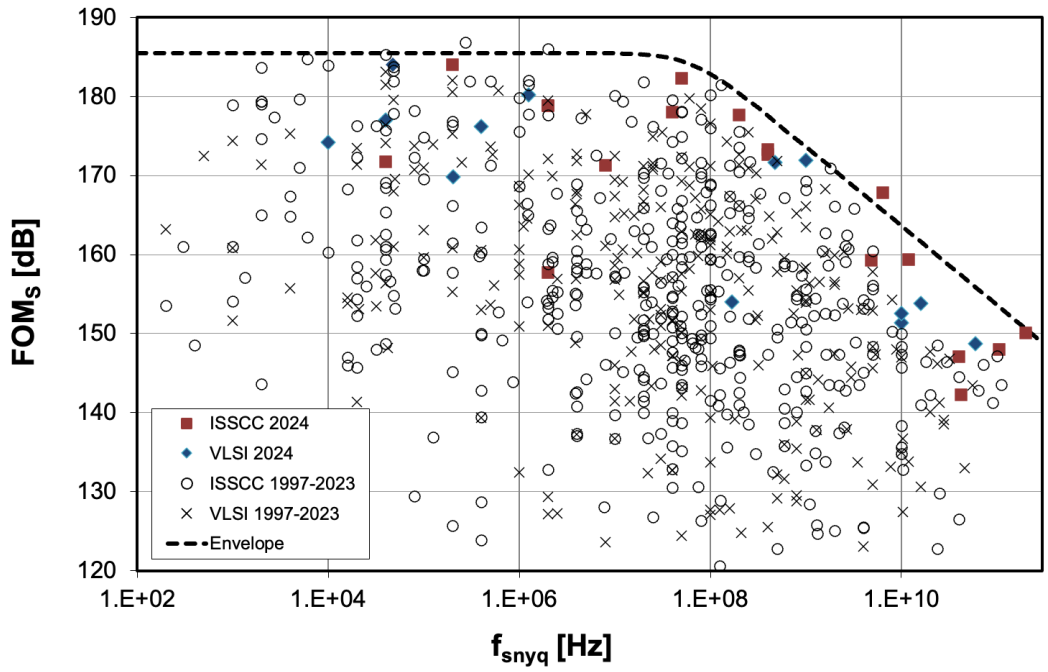
where, V_{DD} is the supply voltage.

2.6 Summary and Conclusions

This chapter introduced the background theory of analog-to-digital conversion. The conversion process of a continuous-time analog input signal to a discrete-time form



(a)



(b)

Figure 2.39: ADC figures of merits: Walden (a) and Schreier (b). [109]

was presented, and sampling non-idealities were highlighted. Subsequently, the most commonly used ADC architectures in a range of applications were outlined, justifying the choice of SAR architecture. The main building blocks of a conventional single-ended SAR ADC were also described in more detail. The chapter then followed on to a bridge-to-digital conversion, which is the traditional architecture for interfacing to resistive sensors, such as gas sensors, and forms the backbone of the next chapters. It discussed the requirements and challenges of digitising a Wheatstone Bridge output, which is typically a mV-level differential signal that needs to be detected on a greater common-mode voltage. Both traditional and direct BDCs were then introduced. Finally, the ADC and BDC metrics were defined, and the trends of Walden and Schreier's figures of merit were presented. Those figures of merit are used to provide a comprehensive evaluation framework highlighting the critical trade-offs between current consumption, resolution and frequency performance. The targeted design space for this research focuses on ADCs utilised in high-performance, low-power applications, such as IoT sensors.

Chapter 3

SAR-based Bridge-to-Digital Converter

This chapter describes the design and implementation of a SAR-based bridge to digital converter. A highly digital SAR-based topology was chosen as it achieves good efficiency and scales well with technology; however, there is a limit to how small the area of SAR-based ADCs can be made because of matching and layout constraints. To overcome the area limitations, the popular binary-weighted DAC was replaced by a Switched-Capacitor Resistor (SCR) approach driven by an Error-Feedback Modulator. This significantly reduces the area requirement because the capacitors used can be small, compared to an n-bit binary weighted capacitor DAC, while also relaxing the matching requirements between the individual bits. Furthermore, based on the assumption that environmental signals are slow in nature, the sample-and-hold circuit was eliminated, extensively simplifying the sensor front-end. Since the input is connected directly to the comparator, it is a high impedance node and, as such, there is no requirement for the sensor to provide any charge or current, eliminating the requirement for any input buffer in the signal path. Additionally, this eliminates the aliasing of out-of-band noise in-band, and removes the requirement for any anti-aliasing filters. As the output of the DAC is not sampled, its thermal noise constraints are relaxed significantly. These changes allow the Wheatstone bridge to be reduced to a simple

resistor divider, requiring fewer external components, providing a better power-to-area trade-off, a higher flexibility and a wide input range of 830 mV, suitable for gas sensor applications.

3.1 Modified Wheatstone Bridge

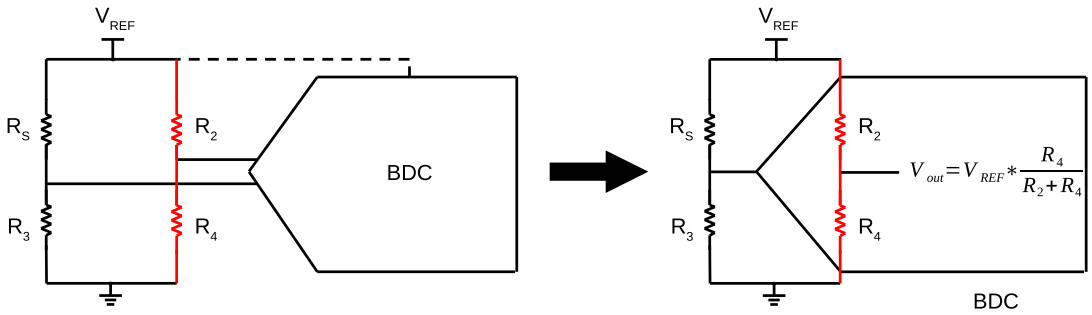


Figure 3.1: Block diagram of the modified Wheatstone Bridge.

As explained in Chapter 2, a traditional Wheatstone Bridge is built with a resistive sensor and three known resistors. To determine the resistance of the sensor, the user tunes the two known resistors until the bridge is balanced, i.e. until V_{OUT} has zero potential, allowing the unknown sensor resistance, R_s, to be deduced. If both adjustable resistors are on one side, the WhB can instead be considered as two simple voltage dividers, where the first divider is built by the sensor and a known resistor R_3 and the second divider can be integrated within the ADC and provides the reference for the comparator. Thus, it can be re-used as a DAC, which is presented in Figure 3.1. While the tunable resistors could be implemented with resistive DACs, these could impair the bridge's sensitivity and, thus, its temperature sensing resolution while also adding a high static power dissipation. To avoid these issues, Switched Capacitor Resistors (SCRs) were used instead, as illustrated in Figure 3.2. A switched capacitor can exhibit a resistor like property, following Ohm's law, when it is periodically switched between two voltage supplies, V_1 and V_2, in a break-before-make fashion. This is illustrated in Figure 3.3.

Assuming that $V_1 > V_2$, when switch S_1 closes the capacitor is connected to V_1 and the charge of CV_1 is transferred on to the capacitor. Subsequently, when S_1 is open and S_2 is closed, some of the charge, $C(V_1 - V_2)$, is transferred to V_2. As the switching

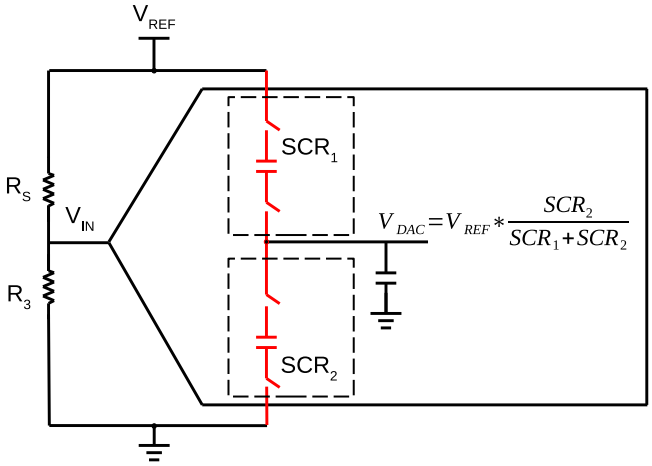


Figure 3.2: WhB with switched capacitor resistors.

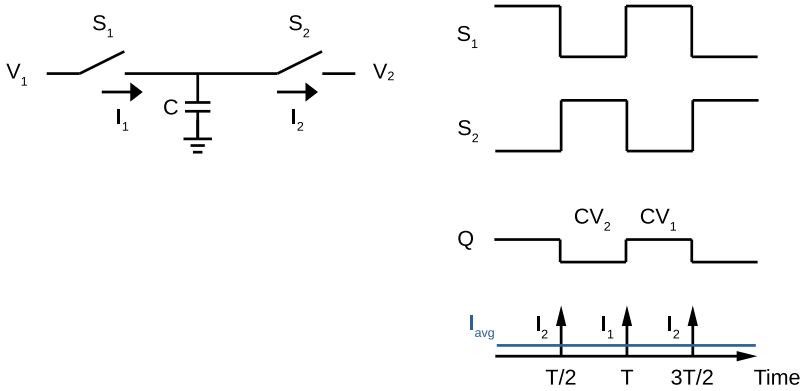


Figure 3.3: Switched capacitor resistor with timing diagram [110].

continues the average current from V_1 to V_2 can be found as:

$$I_{avg} = \frac{C(V_1 - V_2)}{T}, \tag{3.1}$$

which, after rewriting, resembles Ohm's law:

$$I_{avg} = \frac{(V_1 - V_2)}{T/C}, \tag{3.2}$$

with an equivalent resistance of:

$$R_{eq} = \frac{T}{C}. \tag{3.3}$$

The resistance will then depend on the capacitor size and the switching period, T. Thus, the switched-capacitor resistor provides a highly flexible and power efficient programmable resistor for the WhB.

3.2 Binary Search using SCR

The top level architecture of the proposed BDC is illustrated in Figure 3.4. It uses the successive approximation approach, as discussed in Section 2.2.1.2, whereby the output of the switched capacitor divider, V_{DAC}, is compared with the input voltage V_{IN}, using a comparator. The DAC is controlled by the logic such that its voltage, V_{DAC}, follows a standard binary search algorithm to infer the applied input voltage, V_{IN}. This is illustrated in Figure 3.5. The binary search is implemented with SCRs (SCR_1 and SCR_2) by scaling the values of resistance in a reciprocal manner. To set V_{DAC} to mid-range at the beginning of the conversion, both resistance values must be equal. Since the capacitance values of SCR_1 and SCR_2 are fixed, this is achieved by a ratio at which the charge is either transferred from the SCR_1 to the averaging capacitor (indicated in Figure 3.5 in red), C_{avg} at V_{DAC} output node, or from the C_{avg} to the SCR_2 (indicated in Figure 3.5 in blue). At this level of abstraction, if sixteen clock cycles are considered, to set V_{DAC} to mid-range the charge must be transferred eight times from SCR_2 to C_{avg} and eight times from C_{avg} to the SCR_2, making both resistance values equal. Following this procedure, to set V_{DAC} to the next level, for example of $0.75 * V_{REF}$, the ratio of charge transfer must be $12 : 4$, and so forth.

A mathematical model of the BDC has been simulated for a range of different inputs and the results showing the successive approximation procedure are plotted in Figure 3.6, further demonstrating the concept.

3.3 DAC Architecture

The adaptive rate of charge transfer between the internal and averaging capacitors, based on the comparator output, was realised by a 1^{st}-order Error Feedback Modulator, as illustrated in Figure 3.7. As explained in Section 2.2.2.2, the EFM block translates

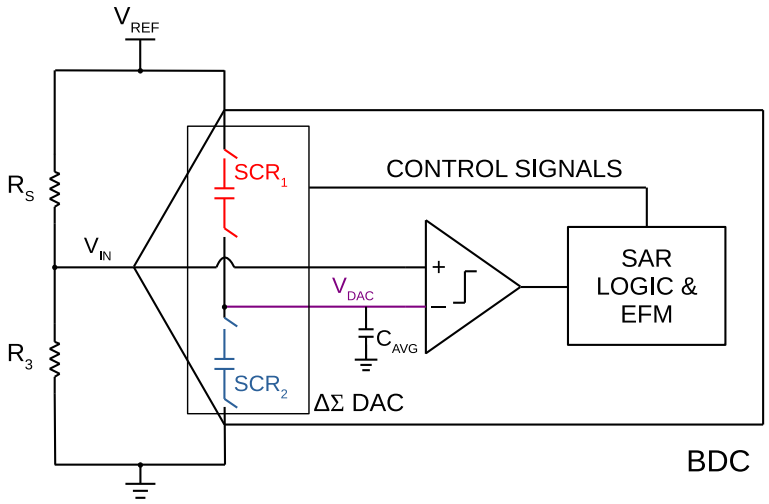


Figure 3.4: Top level block diagram of the SAR based BDC.

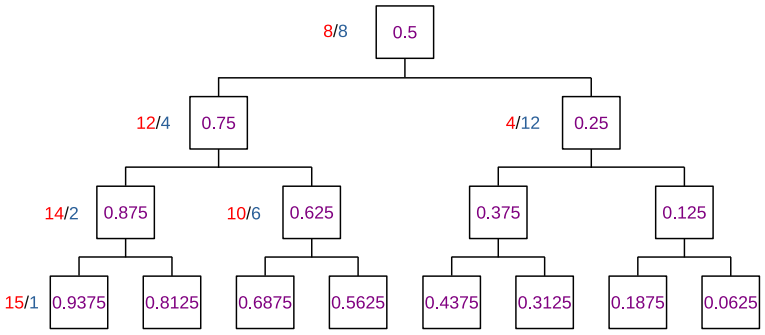


Figure 3.5: SAR approximation represented by resistance ratios.

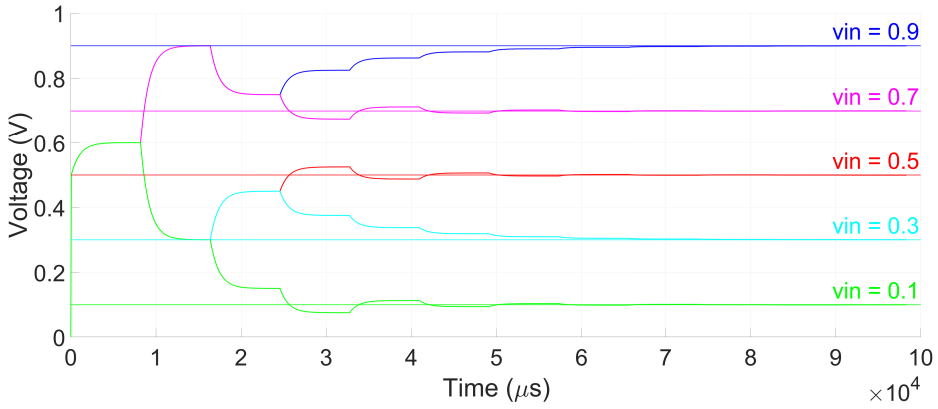


Figure 3.6: Matlab model of the BDC's successive approximation plotted across a range of inputs.

a multi-bit parallel signal into a 1-bit wide density stream.

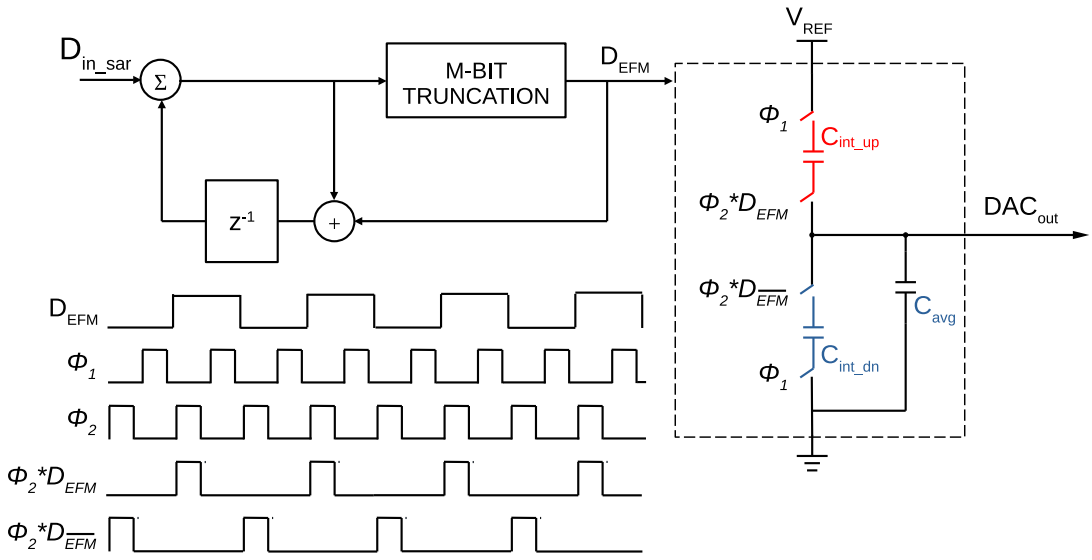


Figure 3.7: A block diagram of an error-feedback modulator driving switched capacitor resistors.

For example, in this case, to set V_{DAC} to mid-range, the SAR logic would generate an output code of $4'b1000$, as it would in a traditional 4-bit SAR. The EFM would then generate a digital pattern with alternating 1's and 0's of equal density. Similarly, other density patterns can be generated. The EFM output selects between C_{int_up} and C_{int_dn} to connect to C_{avg} during ϕ_2. If $D_{EFM} = 1$, C_{int_up} connects to C_{avg}, thereby charging up the C_{avg}. For $D_{EFM} = 0$, C_{int_dn} connects to C_{avg} discharging the C_{avg}. Finally, to facilitate repeated charge transfer, the internal capacitors must be reset to their respective reference voltages (V_{ref} or V_{ss}) during ϕ_1. The two required clock phases, each with a frequency twice that of the EFM, are generated by non-overlapping clocks ensuring that only one switch is on at any time and so eliminating the possibility of short circuits. The timing diagram in Figure 3.7 illustrates the main clock signals.

The output of this $\Sigma\Delta$ DAC, when C_{avg} is connected to C_{int_up}, can be mathematically represented by equation (3.4), while the new value when C_{avg} is connected to C_{int_dn} can be calculated from (3.5). Here, V_{ref} is the reference voltage used by the DAC and C_{int} ($C_{int_up} = C_{int_dn}$) is the DAC unit capacitor. As can be deduced from the equations, the number of EFM clock cycles needed to reach the desired output depends on the chosen capacitor sizes.

$$V_{out_up}(i) = \frac{C_{int}V_{ref}}{(C_{int} + C_{avg})} + \frac{C_{avg}V_{out}(i-1)}{(C_{int} + C_{avg})} \tag{3.4}$$

$$V_{out_dn}(i) = \frac{C_{avg}V_{out}(i-1)}{(C_{int} + C_{avg})} \tag{3.5}$$

Figure 3.8 shows the DAC output for a sample binary search. To ensure that the DAC fully settles before the next comparison takes place, multiple clock cycles are allocated to the DAC. The number of EFM clock cycles needed for the DAC to settle is referred to as the Oversampling Ratio (OSR).

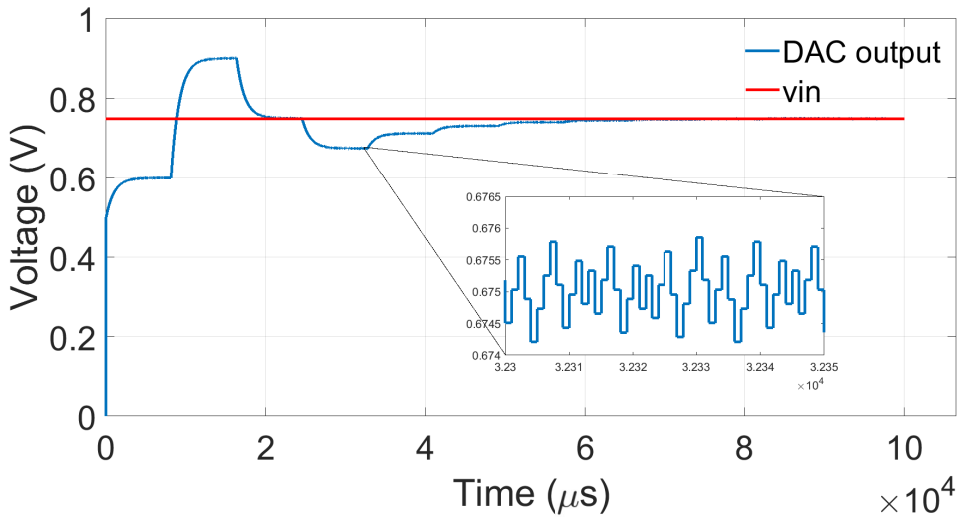


Figure 3.8: Simulated DAC settling and the concomitant ripple (inset).

As visible in the inset of Figure 3.8, there is a ripple due to the continuous charging and discharging of the C_{avg}. The size of this voltage ripple is given by:

$$V_{ripple} = V_{ref} * \frac{C_{int}}{C_{int} + C_{avg}} \tag{3.6}$$

Since, the ripple is not completely attenuated by C_{avg}, which behaves as a low-pass filter, it can ultimately limit the achievable resolution. To increase the resultant resolution, the ratio of C_{avg} to C_{int} must increase. This, however, extends the time for the DAC to reach its target value, reducing the ADC throughput. To expedite settling without aggravating the ripple, a second pair of SCRs were added in parallel to the

DAC, as in Figure 3.9. Those SCRs have been implemented with larger capacitors enabled only for the first 32 to 256 EFM clock cycles, depending on the user's selection, after each new input value provided to the DAC.

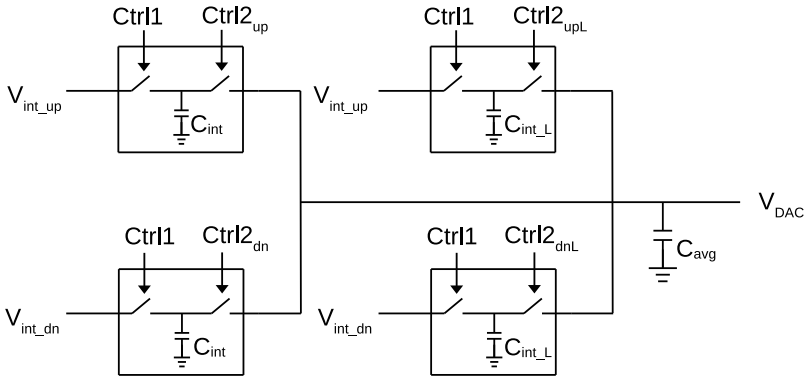


Figure 3.9: Schematic of a DAC showing implemented SCRs with their control signals.

3.3.1 Thermal noise

Thermal noise, which is considered to be a limiting factor in ADCs with a resolution above 12-bits, is inversely proportional to the size of the sampling capacitor, as described in Section 2.1.5.2. While in this proposed BDC the input signal isn't sampled, the differential comparator experiences sampled noise from the DAC input, which is contributed by the switched capacitor network. Therefore, the noise is equal to the noise of the equivalent resistor R_{eq} and is calculated from equation (3.7):

$$\bar{v}_n = \sqrt{4kTR_{eq}} = \sqrt{4kT\frac{1}{fC_{int}}} \tag{3.7}$$

Additionally, because C_{avg} is significantly larger than C_{int}, it acts as a low-pass filter resulting in a thermal noise contribution much less than one LSB, without limiting the size of C_{int}.

3.3.2 Mismatch

Since the thermal noise is not a limiting factor in the DAC and the ratio between the internal and averaging capacitors defined the maximum achievable resolution of the ADC, it may be tempting to make the C_{int} infinitesimally small. However, any

mismatch between the C_{int_up} and C_{int_dn} due to the fabrication process can lead to gain error. As illustrated in Figure 3.10, a 0.05 fF of capacitance difference can introduce a gain error of 740 μV which, in turn, can translate to 2.5 LSB for a reference voltage of 1.2 V. Fortunately, the gain error can be easily calibrated.

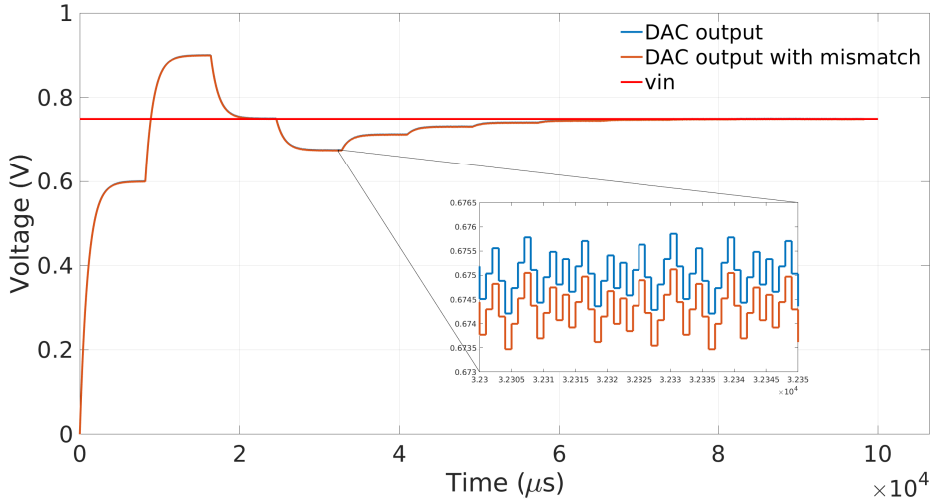


Figure 3.10: DAC output error for a 0.05 fF mismatch

3.4 Circuit Implementation

Figure 3.11 presents the detailed block diagram of the proposed BDC and internal clock generation. While this ADC was implemented for 12-bit resolution, due to the highly digital nature of the DAC it offers a high level of programmability allowing the trade-off between resolution, power and speed to be optimised for a given application. The OSR, the number of clock cycles allowed for the DAC to settle, is selectable with a minimum of 256 and a maximum of 32768 cycles. The activation duration of the larger capacitor is also adjustable. The SAR clock is generated based on the selected OSR. The comparator is given 64 EFM clock cycles of decision time after the DAC has settled. Figure 3.11b shows the top level timing diagram.

The BDC has been realised in TSMC 65 nm CMOS technology. While the most popular node for the sensor technology is 180 nm, moving to lower geometries offers a smaller form factor which is important for IoT applications. Figure 3.12 illustrates the top level layout. This design occupies only 0.01 mm^2. The detailed implementation of the

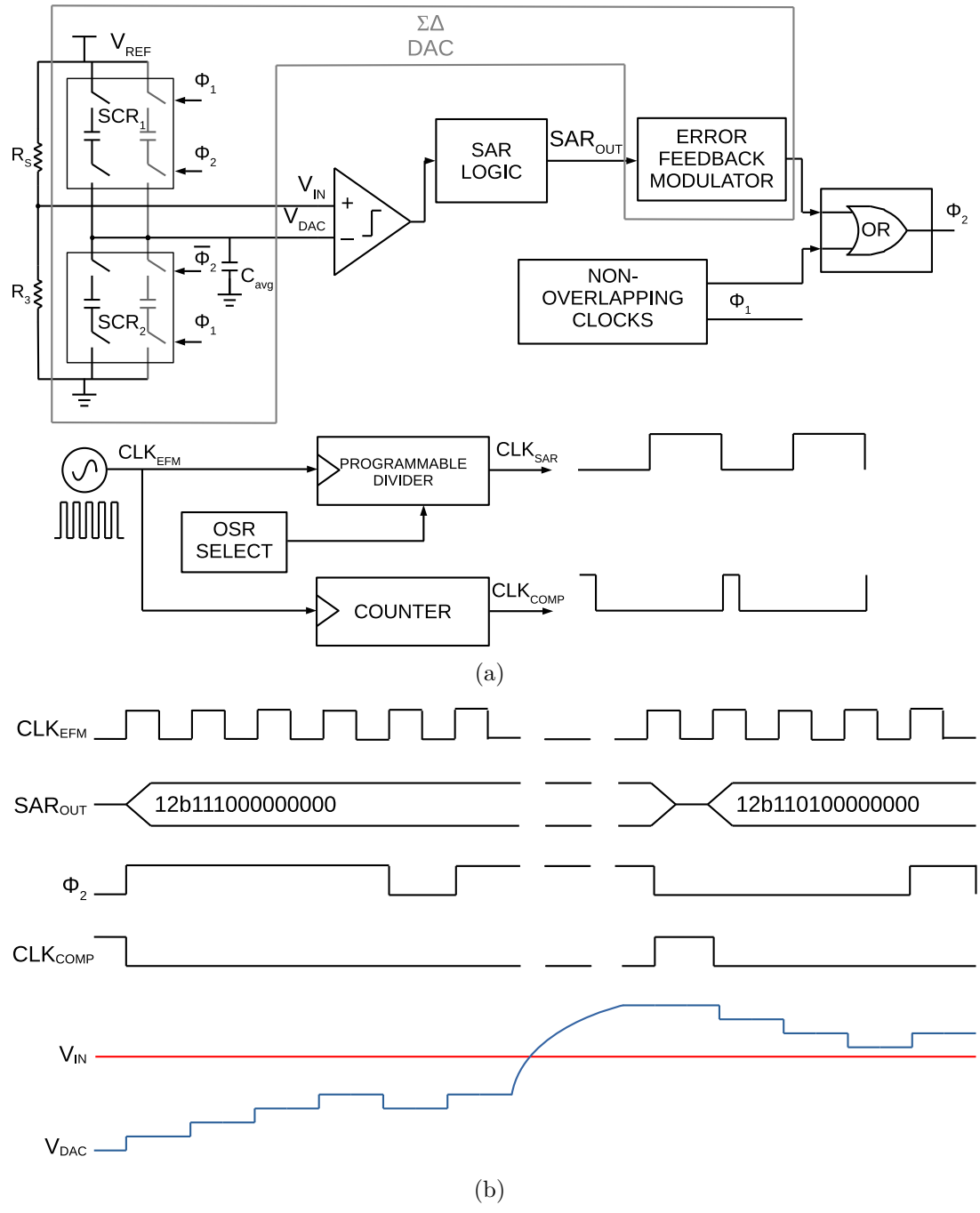


Figure 3.11: Detailed view of the proposed architecture including internal clock generation (a) and system timing diagram (b).

individual blocks is discussed next.

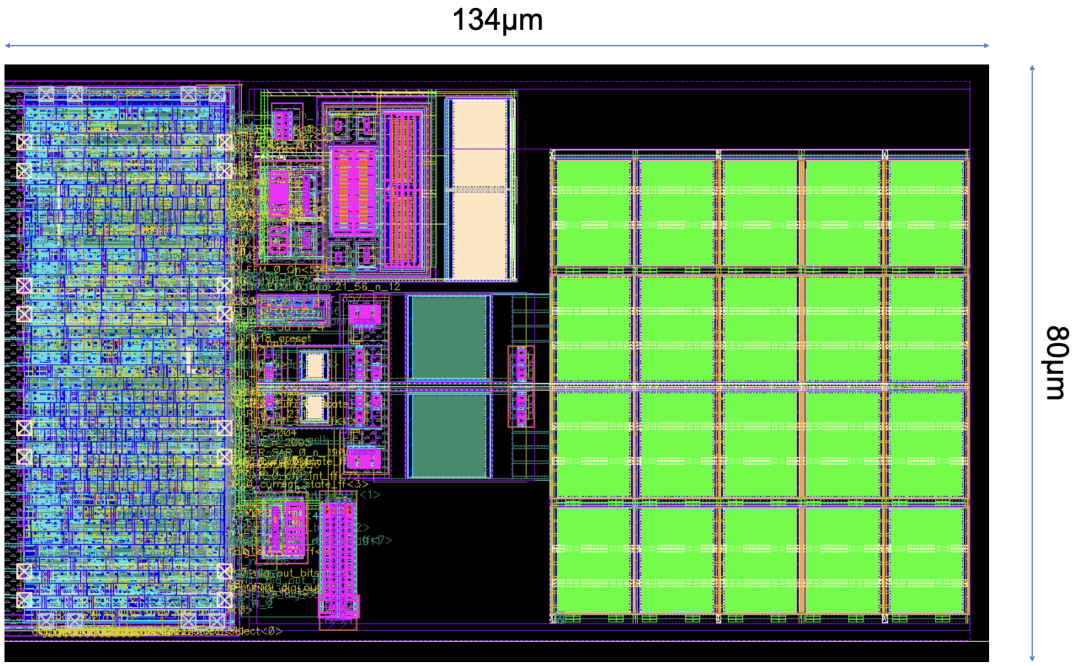


Figure 3.12: Top level layout of the BDC.

3.4.1 Delta-Sigma DAC

As described in earlier sections, the DAC has been realised with four switched capacitor resistor cells driven by an EFM, which takes the 12-bit code from the SAR logic and generates a bit stream to realise the target voltage. Two cells are made from unit capacitors and two have ≈8x unit capacitances to accelerate the settling time. The top level of the DAC, with combinational logic, is represented in Figure 3.13. The logic is required to enable the individual SCR cells. The non-overlapping clocks (NOC) are required to drive the SCR switches in addition to the EFM signal and to prevent shorting the circuits during transitions.

3.4.1.1 Switched capacitor resistor cell

Each switched capacitor resistor cell is implemented with two T-gate switches and a capacitor, as in Figure 3.14. T-gate switches are used to ensure full voltage swing at the DAC output and to reduce charge injection. The DAC was implemented with a unit capacitor size of 20 fF, which was limited by the mismatch, as analysed in section 3.3.2. The averaging capacitor of 10 pF was chosen to reduce the output ripple. The resistor

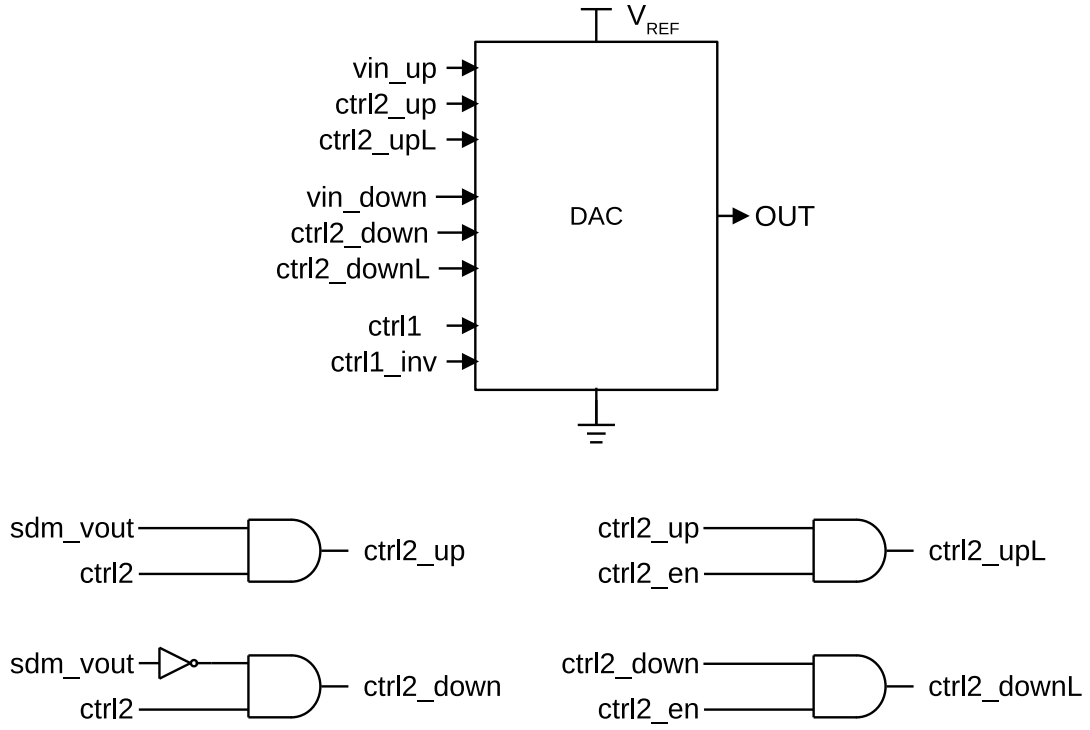


Figure 3.13: Top level schematic of Delta-Sigma DAC.

cells used for the initial settling boost were implemented with larger capacitors of 167 fF and, to minimise leakage, high threshold voltage (V_{th}) switches were used. Standard V_{th} switches with lower resistance are used elsewhere to decrease the RC constant. Equal sizes where chosen for both NMOS and PMOS transistors to minimise charge injection. The symmetrical structure of the DAC minimises any potential variations in the circuit.

Figure 3.15 shows the layout of the SRC cells. The smaller cell has a size of 100 μm^2 and the larger cell is 300 μm^2. As outlined, the averaging capacitor adds 4000 μm^2, resulting in a total area of 4800 μm^2.

3.4.1.2 1st-order Error Feedback Modulator

An Error Feedback Modulator, as discussed in Section 2.2.2.2, was chosen to drive the DAC switches due to its digital design, low area and high power efficiency. Because the DAC is not limited by quantisation noise owing to the large capacitor at the output, a 1st-order implementation was deemed sufficient. While RC delay is more critical, it is not affected by the modulator order.

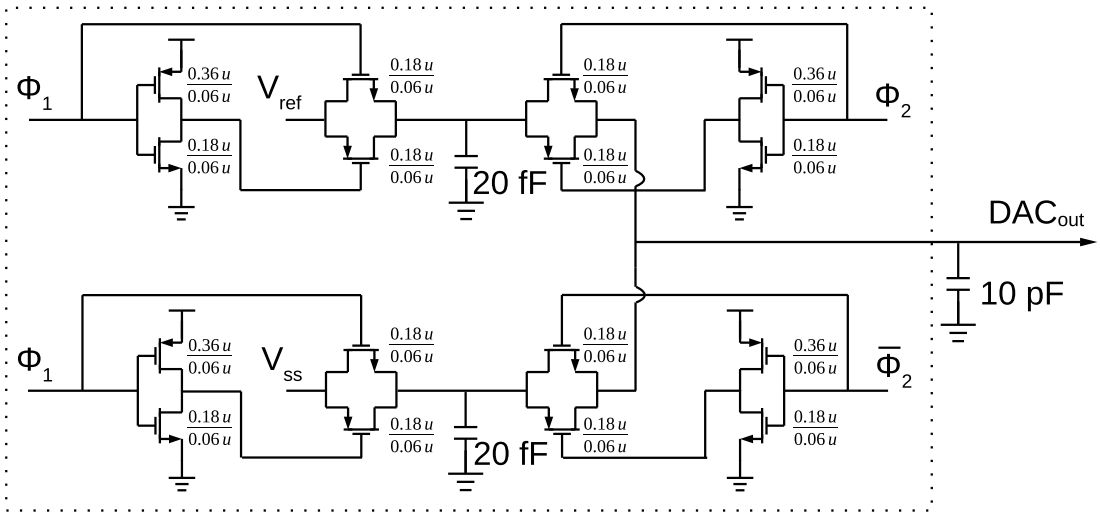


Figure 3.14: Transistor level diagram of the switched capacitor resistor cells with the unit capacitors.

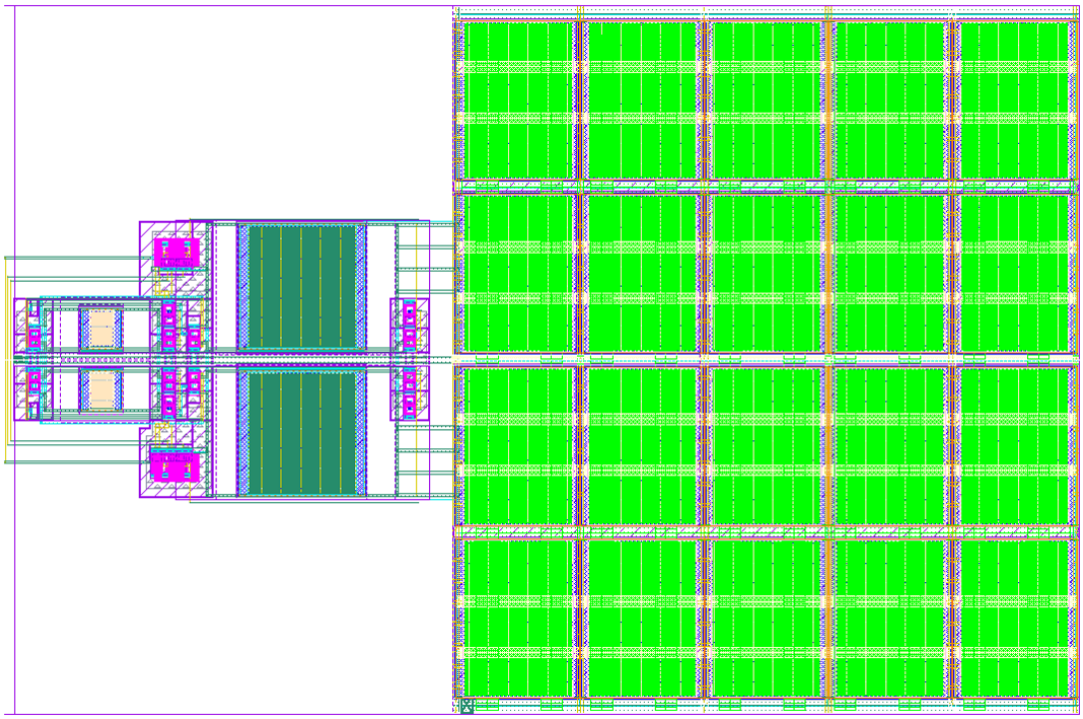


Figure 3.15: Layout of the switched capacitor resistor cells and the averaging capacitor.

The block diagram of the implemented modulator is represented in Figure 3.16. The truncator extracts a quantisation error ϵ_{LSB}, which is passed to a low-pass filter before being summed with the input D_{in_sar}. In this digital topology, instead of using an integrator, the filter is implemented with a simple delay block.

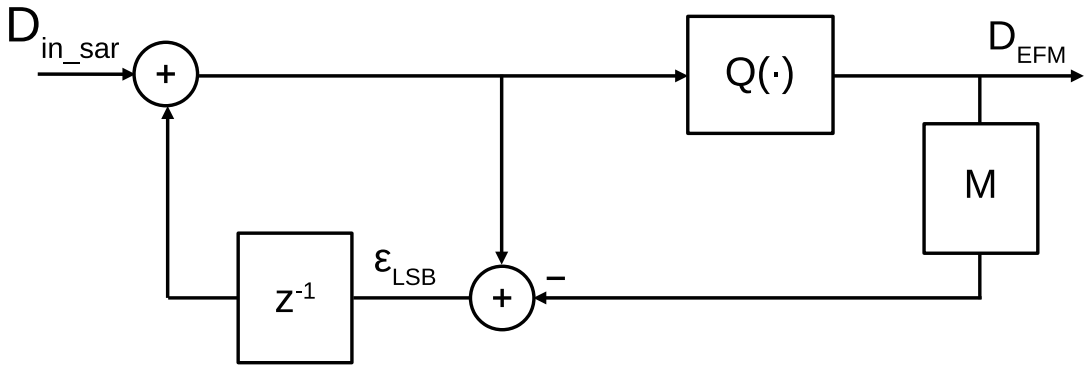


Figure 3.16: Block diagram of implemented 1st-order EFM.

The resulting output of the modulator is described mathematically by:

$$D_{EFM} = D_{in_sar} + (1 - z^{-1})\mathcal{E}_{LSB}. \tag{3.8}$$

The modulator was simulated and its output is plotted against the input voltage in Figure 3.17, where the output density of "ones" and "zeroes" was averaged and multiplied by the reference voltage. Since this is a fully digital modulator, it is designed in the Verilog language and it resides in the logic blocks, as will be discussed in Section 3.4.3.

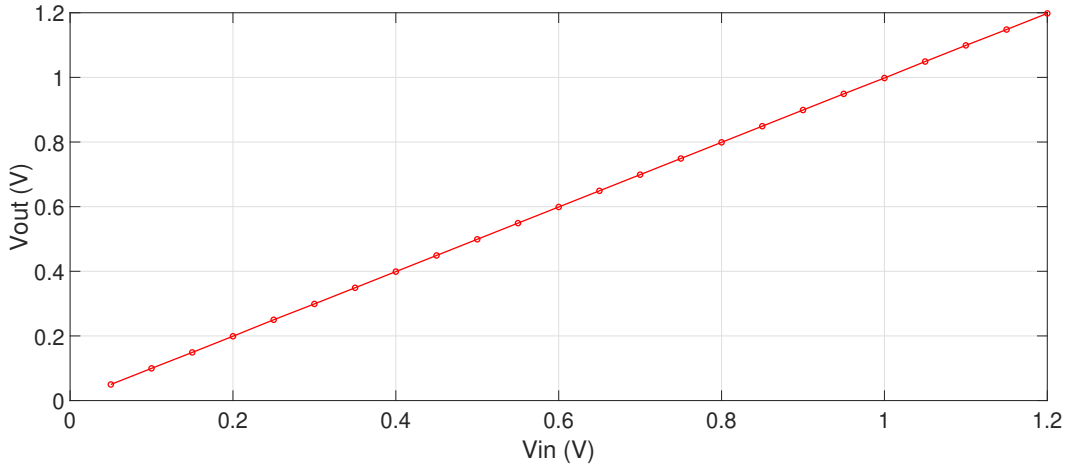


Figure 3.17: EFM output versus input.

3.4.1.3 Non-Overlapping Clock

As represented in Figure 3.18, the Non-Overlapping Clock (NOC) block was implemented using inverters and NAND gates. Since the circuitry needs to be stable over a range of temperatures, enough delay between the clocks had to be ensured. A chain of fourteen inverters gave the desired results. The chain is driven by a master clock. The NAND gate ensures that the chain is enabled only when the other edge goes low. Minimum size devices were employed except for the final inverter that needs a higher drive strength. Standard-Vt devices are selected to match the power and speed requirements.

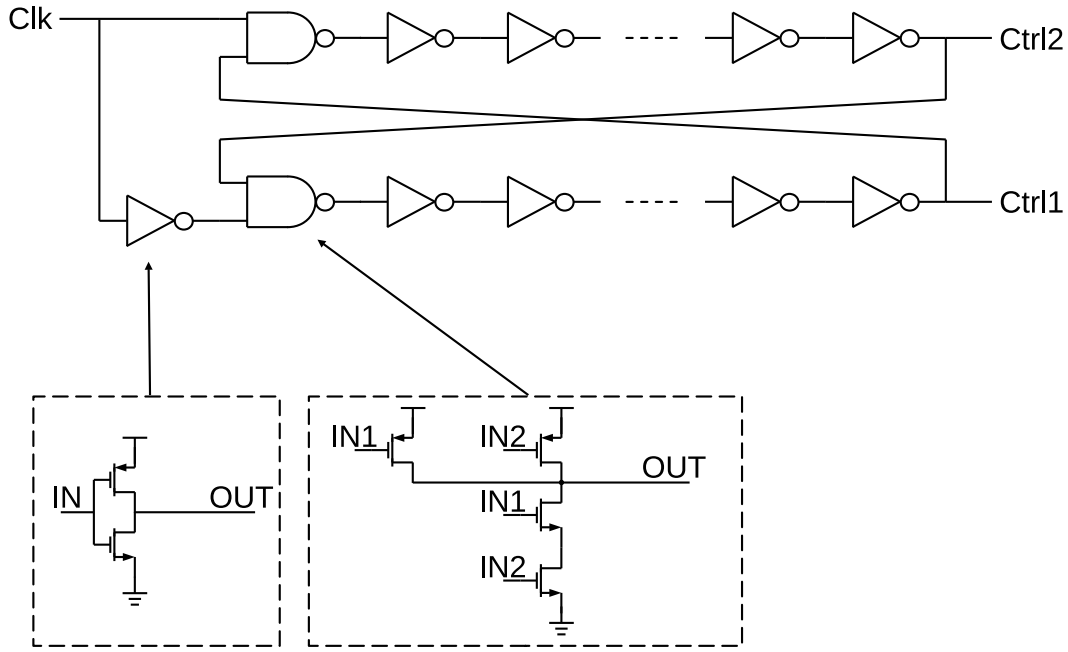


Figure 3.18: Schematic of the non-overlapping clock (NOC) generation circuit.

Figure 3.19 shows a layout of the implemented block with the locations of the different circuits highlighted. The block occupies 100 μm^2.

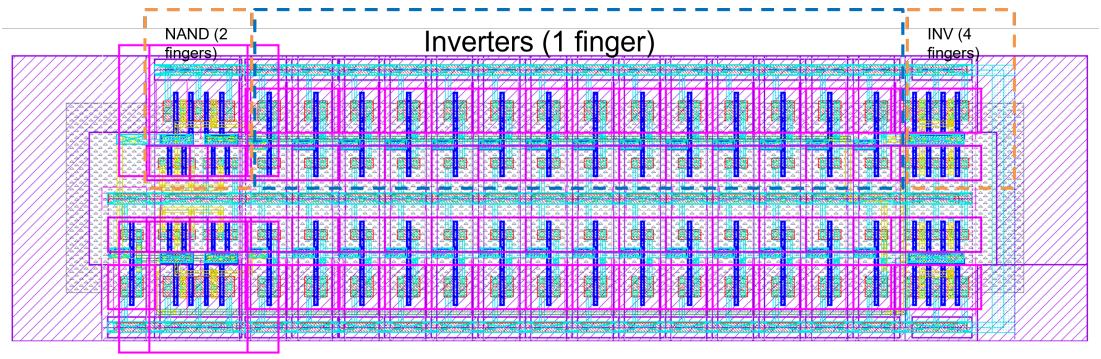


Figure 3.19: Layout of the non-overlapping clock (NOC) circuit.

Extracted (post layout) simulations were conducted to ensure the circuit meets the required timing constraints with the parasitic elements from the layout included. The results for the implemented NOC are shown in Figure 3.20. There is a visible delay of 300 ps between the high pulses of the outputs during which both of the output signals are low.

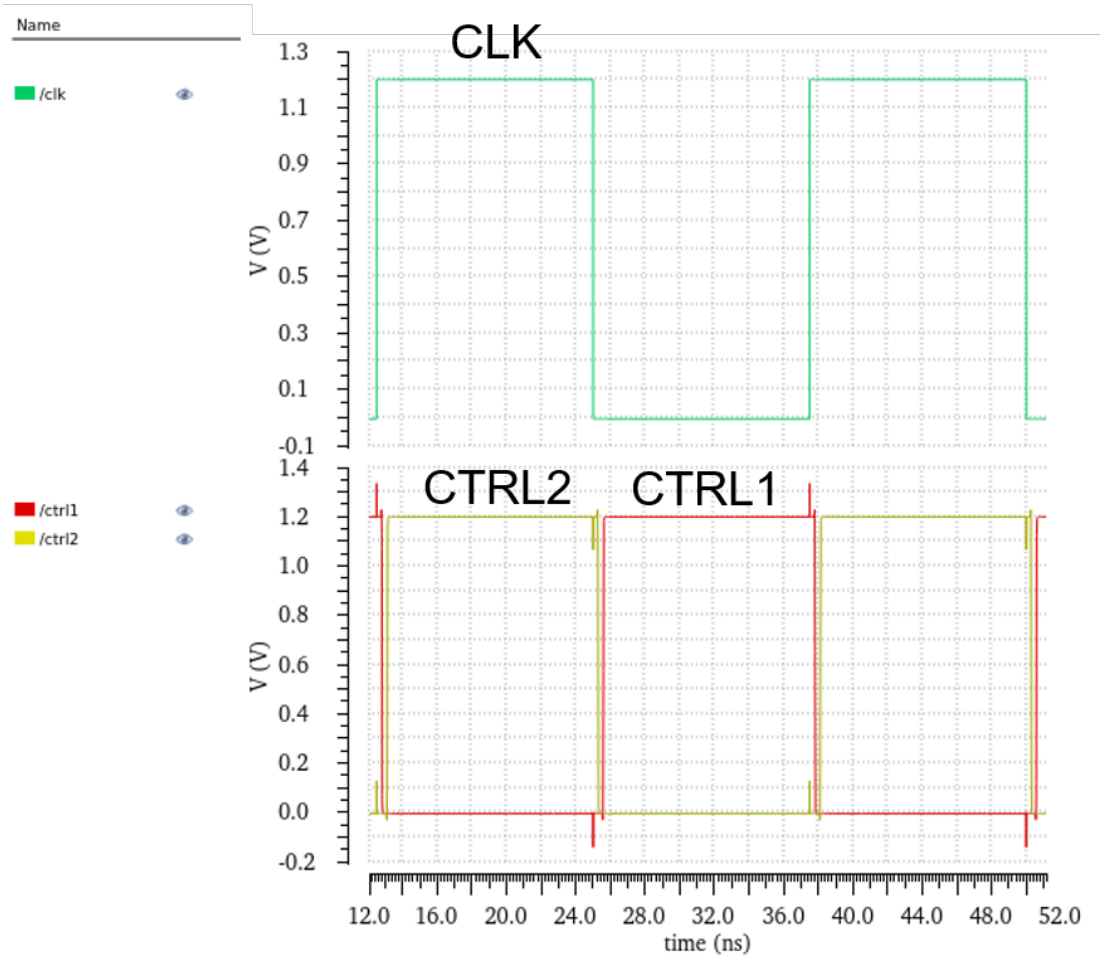


Figure 3.20: Extracted (post layout) simulation of non-overlapping clocks.

3.4.1.4 DAC simulation results

The simulated results in Figure 3.21 show the DAC output increasing from ground potential to the mid-scale, 600 mV. For the first 64 CLK_{EFM} cycles all 4 SCRs are enabled, resulting in the observable initial rapid increase in output voltage. Subsequently, the large capacitors are disconnected, causing the transition into a longer time constant RC curve and finally settling to the input signal. The inset shows a 1.25 mV zoom-in on the peak-to-peak ripple which is present at the output. The ripple is a by-product of

charge transfer between the internal and averaging capacitors which continues beyond the settling point.

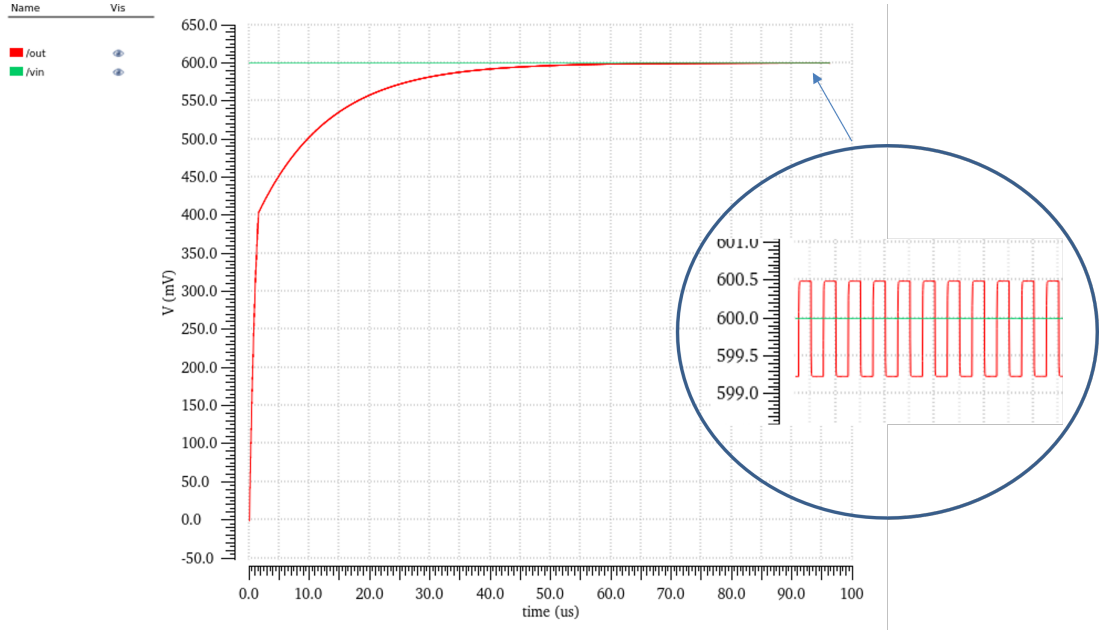


Figure 3.21: Simulated DAC output.

In this example, a duty cycle of 50% for the mid-scale voltage is as expected, but it differs between target output values. This means that the variation in DAC output can introduce a quantisation error at the time of the comparator's decision. Additionally, the post layout extraction revealed a mismatch between the internal capacitors due to parasitic capacitance in the interconnects, which manifested as a gain error. The introduced error for an input of 900 mV is between 2.5 mV and 3.5 mV, as depicted in Figure 3.22. Nonetheless, the total error is repeatable and, while not trivial, could be readily corrected by using simple digital calibration. This, however, was outside the scope of this project; hence, all results presented here do not contain any digital calibration.

Finally, Figure 3.23 shows that the DAC is linear over the input range for a sample set of temperatures.

3.4.2 Comparator

The comparator [111], illustrated in Figure 3.24, is realised as a double-tail dynamic latch with PMOS input transistors. This architecture is commonly used in designs oper-

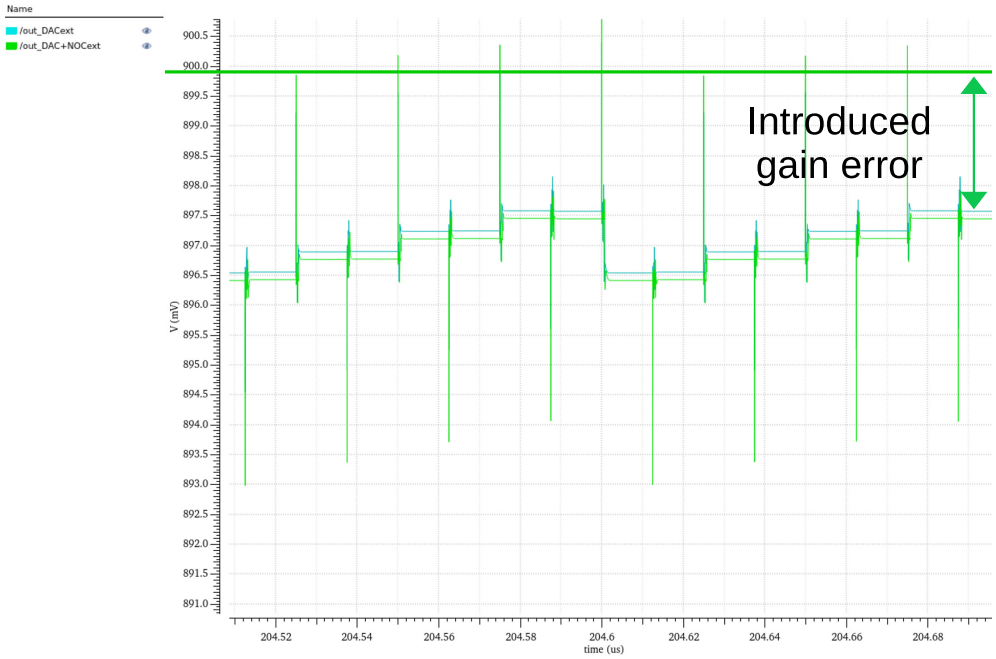


Figure 3.22: The extracted results showing introduced gain error that is due to layout related mismatch.

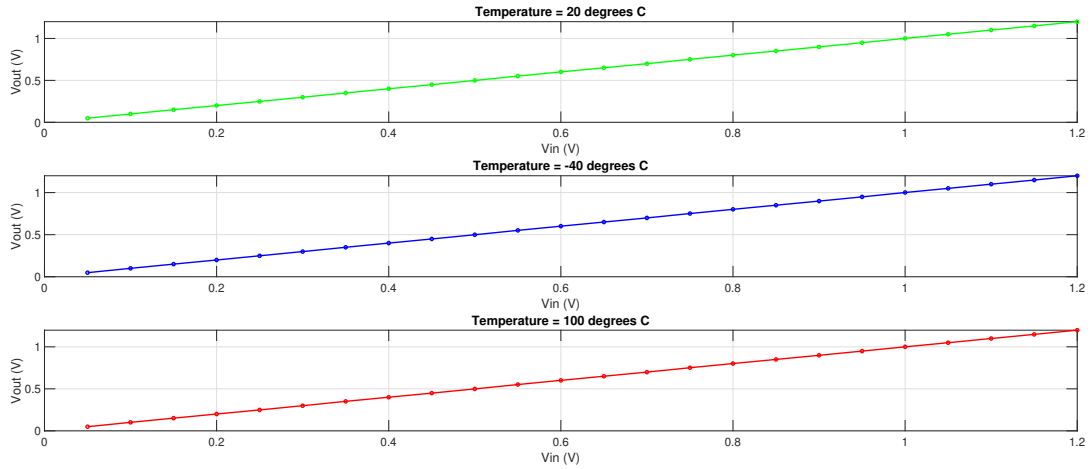


Figure 3.23: DAC linearity for temperature range.

ating from low supply rails due to its low voltage headroom requirements. Additionally, the double-tail dynamic latch has a relatively low offset across its full scale range and provides good shielding between input and output. Furthermore in this implementation, due to the large OSR required by the DAC, any comparator kickback, which is minimised by the presence of a pre-amp, will have thoroughly dissipated by the next comparator decision. Figure 3.25 presents the implemented layout of the comparator with its main blocks indicated. The comparator occupies 1000 μm^2.

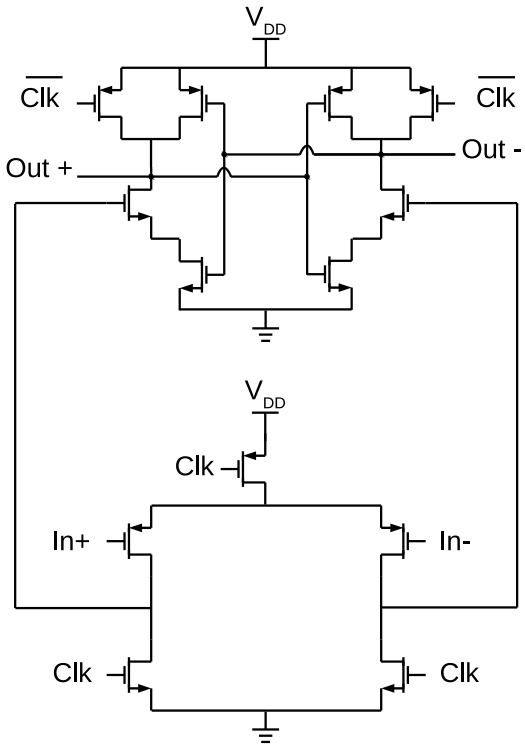


Figure 3.24: Schematic of double-tail dynamic latch comparator with preamplifier.

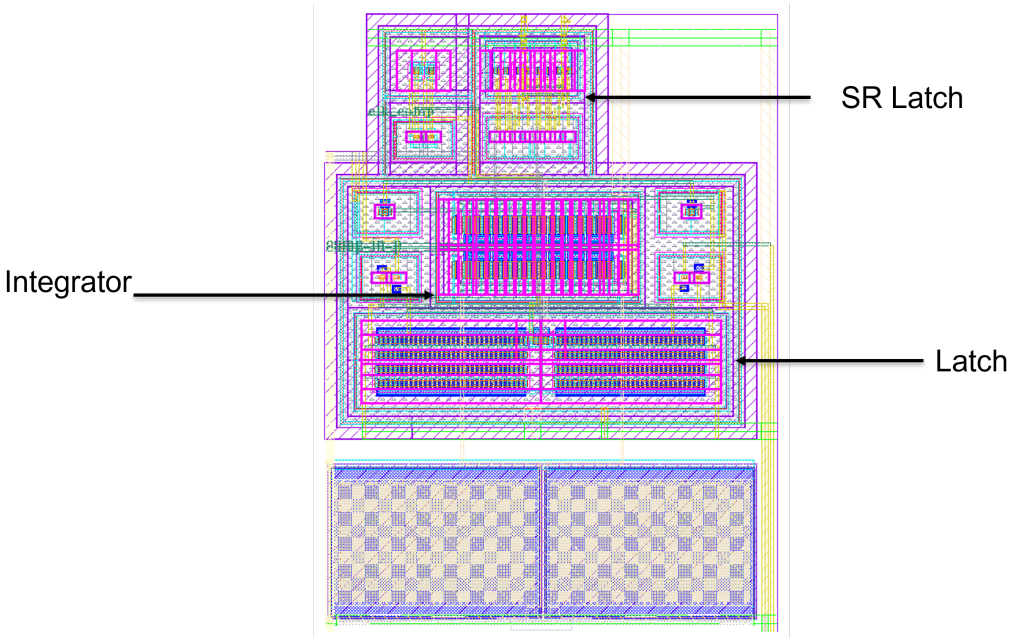


Figure 3.25: Comparator layout with main sub-blocks indicated.

Because the DAC requires a large OSR, in order to not further limit the operating speed of the SAR, the comparator is only enabled for a fixed 64 CLK_{EFM} cycles after the DAC has settled. This duration was selected to exceed the maximum expected comparator decision delay of 45 ns, as in Figure 3.26.

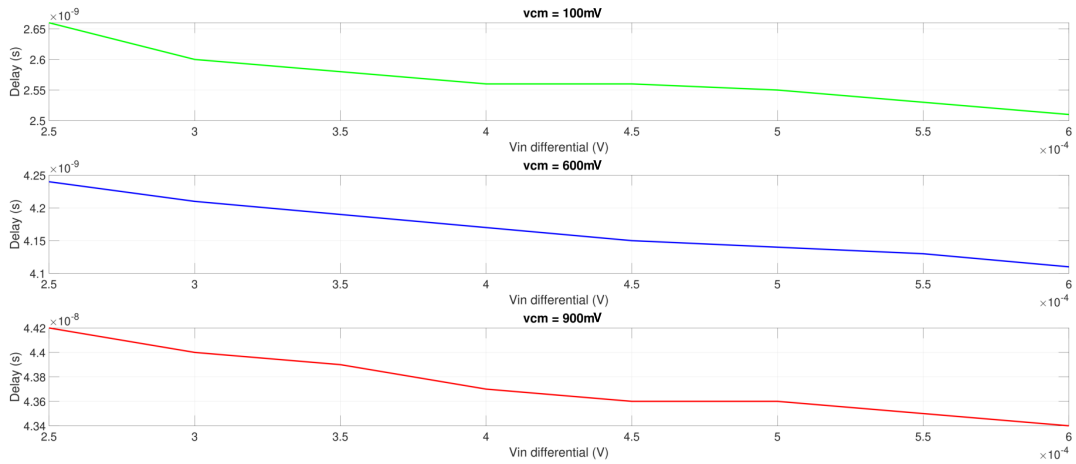


Figure 3.26: Extracted results showing a maximum comparator delay of 45 ns across the input common mode.

Also, because the DAC exhibits glitches at the output due to the charge injection, a 1.35 ns delay has been added to allow the DAC output to fully settle; this is illustrated in Figure 3.27.



Figure 3.27: Comparator being enabled after DAC settling.

The input range of this comparator is 830 mV with a 1.2 V supply, limited by the PMOS input transistors. The simulated post-layout noise is 60 $\mu Vrms$ and the offset presented in Figure 3.28 is 178 μV. Hence, the comparator's performance exceeds the

requirements of this BDC.

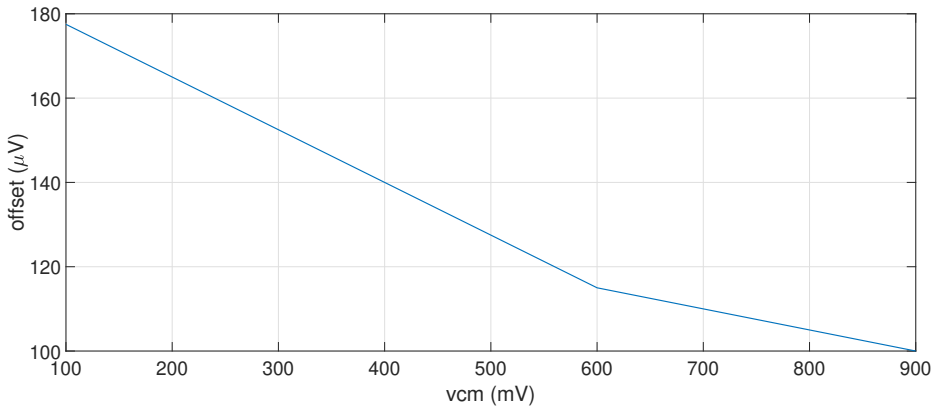


Figure 3.28: Extracted simulations showing a maximum offset of 178 μV across the input common mode.

3.4.3 Logic

This BDC offers a high level of flexibility mainly due to its highly-digital DAC structure. It can be easily pre-programmed to achieve the best trade-off between resolution, power and speed for a given application.

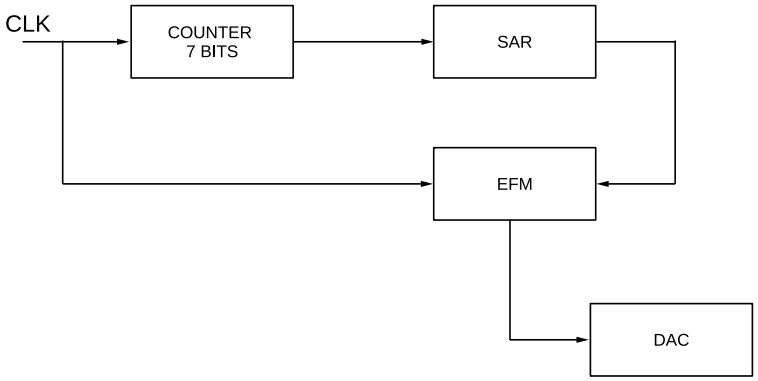


Figure 3.29: Representation of blocks implemented within the logic.

The top level diagram of an implemented logic block is shown in Fig. 3.29. The SAR algorithm is the core of the BDC and sets the DAC to the required level based on the comparator input and is similar to the standard SAR ADC. The output of the EFM drives the SCR switches, as discussed in Section 3.4.1.2. Finally, the 15-bit wide counter generates an internal clock for the SAR ADC. The programmable signals are:

- Oversampling ratio - the number of sigma-delta modulator clock cycles required for one bit trial.

- DAC 2 duration - duration for which a second pair of SCRs (with larger capacitors) are active to expedite settling time.
- Resolution - a control bit added to enable either twelve or fourteen SAR decision cycles.

Note that full redundancy [112], resulting in a sub radix-2 search, could be easily added; however, to simplify the implementation, it was limited to a standard binary search. A sample configuration of the BDC is exercised in Figure 3.30 showing 12 and 14-bit decision cycles.

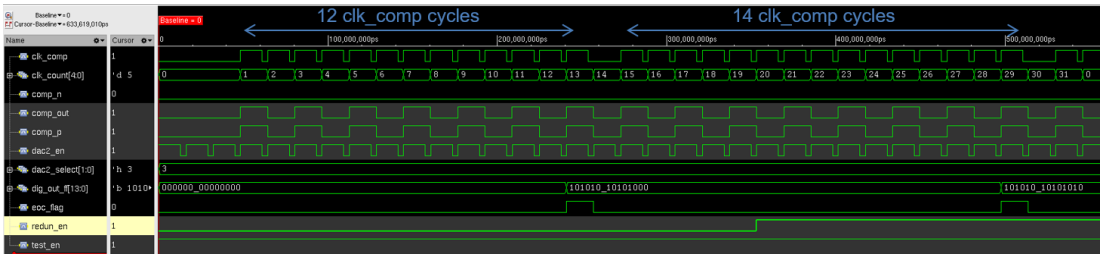


Figure 3.30: Simulated sample configuration of the BDC showing 12 and 14-bit decision cycles.

The logic was designed in Register Transfer Level (RTL) Verilog and implemented with the help of synthesis and place and route tools. The resulting layout, Figure 3.31, occupies 2200 μm^2 of area.

3.4.3.1 SAR BDC state machine

Figure 3.32 illustrates the flow chart of the SAR BDC state machine. Once the device exits the *Hard Reset* state, the ADC is correctly initialized and ready to start its first conversion upon entering the *Reset* state. During this state, the DAC is set to mid-scale, and all other registers are reset to their default values. States $S2a$ through $S2c$ represent the conversion process. Initially, the system waits for the comparator decision; based on this decision, the logic updates its internal registers. The number of conversion steps depends on the *redun_en* setting. After all decisions are made, the system transitions to the $EOCflag$ state, where the end of conversion flag is raised, signalling the completion of the conversion. From here, the system can initiate a new conversion cycle by transitioning back to the *Reset* state.

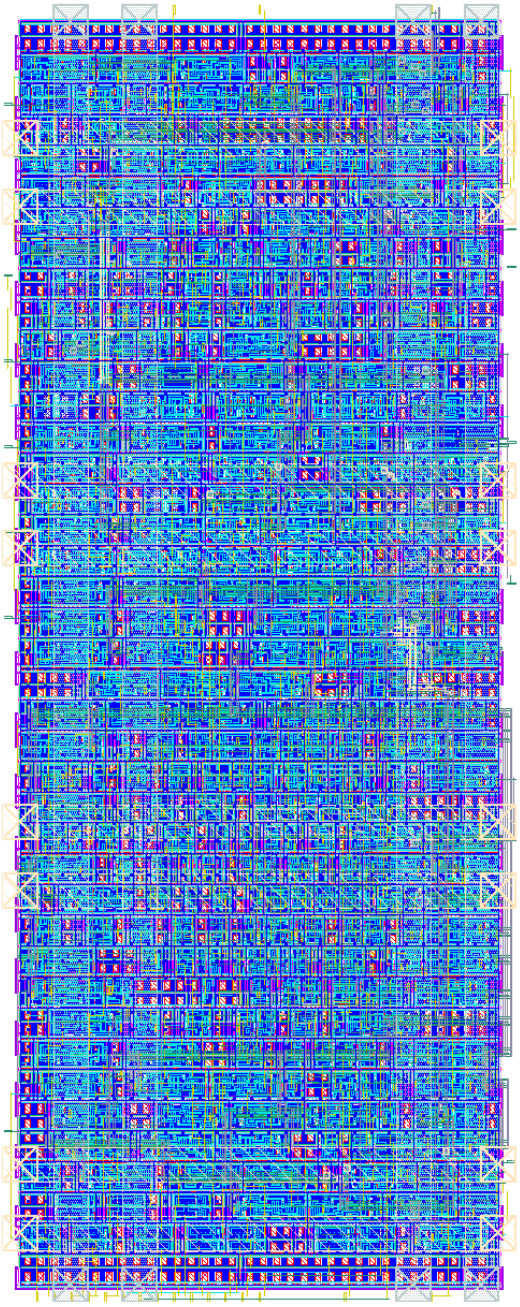


Figure 3.31: Logic layout post place and route.

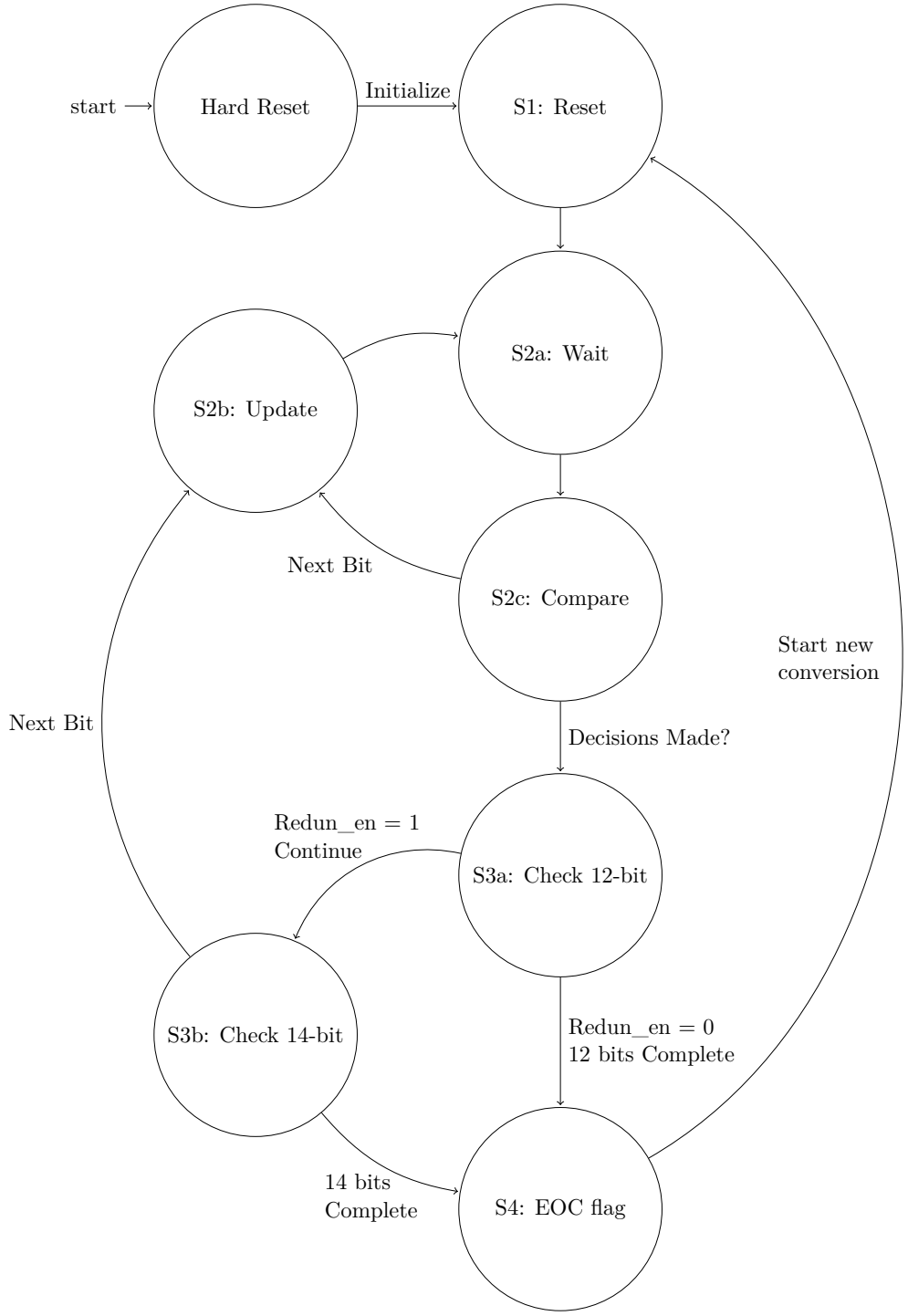


Figure 3.32: Representative diagram of the state machine of the operation of the BDC

3.4.3.2 Clocks generation

In this architecture the SAR block operates at a much slower rate than the DAC. To generate the SAR signal internally the main 40 MHz EFM clock is divided down, based on the required oversampling ratio. The divider is implemented with an 8:3 multiplexer and a 15-bit counter, as illustrated in Figure 3.33.

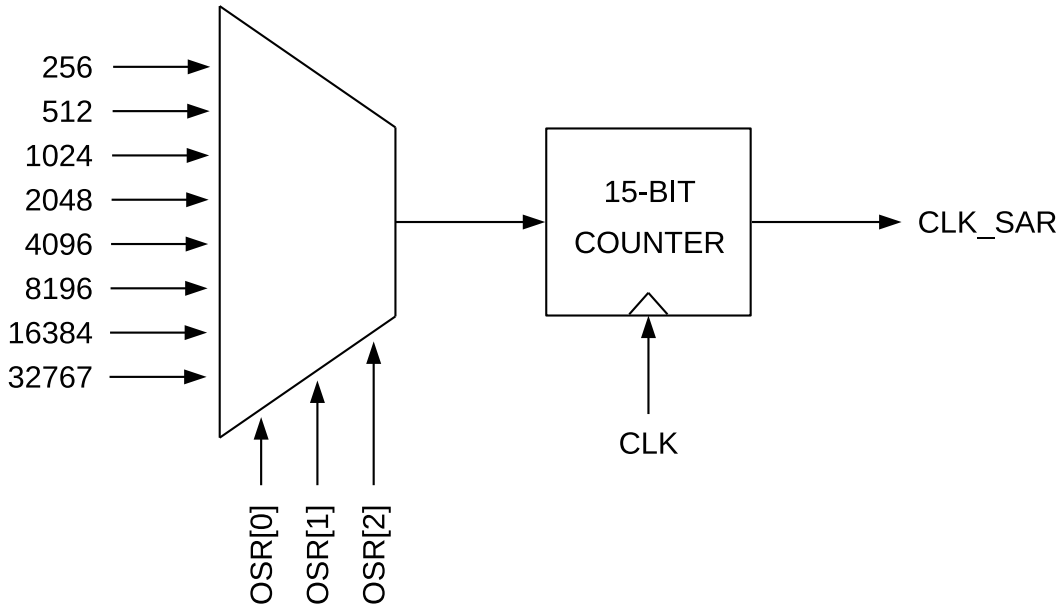


Figure 3.33: Clock Divider.

The 3-bit OSR register selects the divide ratio between 256 and 32767. Such a broad span was implemented to facilitate changes of the averaging capacitor. The CLK_SAR was simulated and is represented in Figure 3.34. The comparator operates on the shorter logic low period.

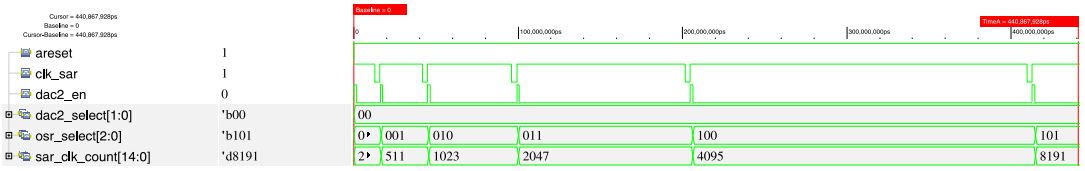
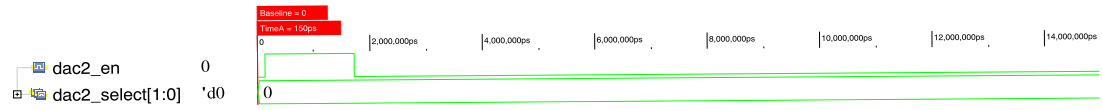
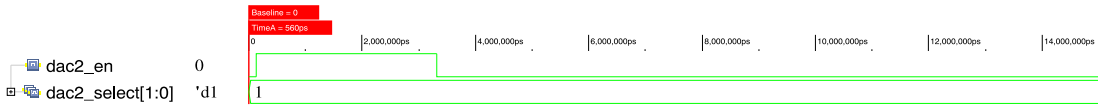


Figure 3.34: Operation of the 8:3 multiplexer.

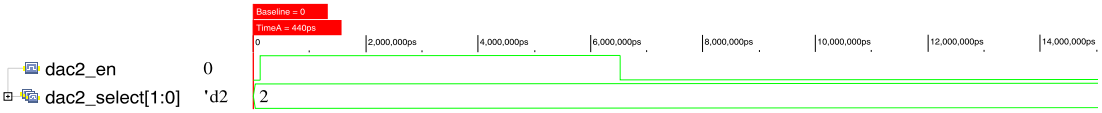
A smaller multiplexer is also implemented to generate a variable signal to enable DAC 2, whose functionality is represented in Figure 3.35.



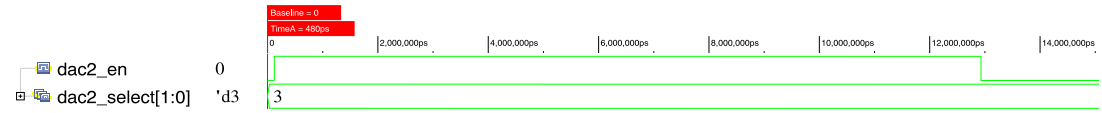
(a) Plot showing a dac2_en signal duration for dac2_select = d'0



(b) Plot showing a dac2_en signal duration for dac2_select = d'1



(c) Plot showing a dac2_en signal duration for dac2_select = d'2



(d) Plot showing a dac2_en signal duration for dac2_select = d'3

Figure 3.35: Plot showing the selectable DAC 2 duration.

3.5 Results

Figure 3.36 shows a die photo of the fabricated BDC. An input-output (I/O) ring and decoupling capacitors are clearly visible in the image. The main blocks of the BDC are illustrated in the zoomed view.

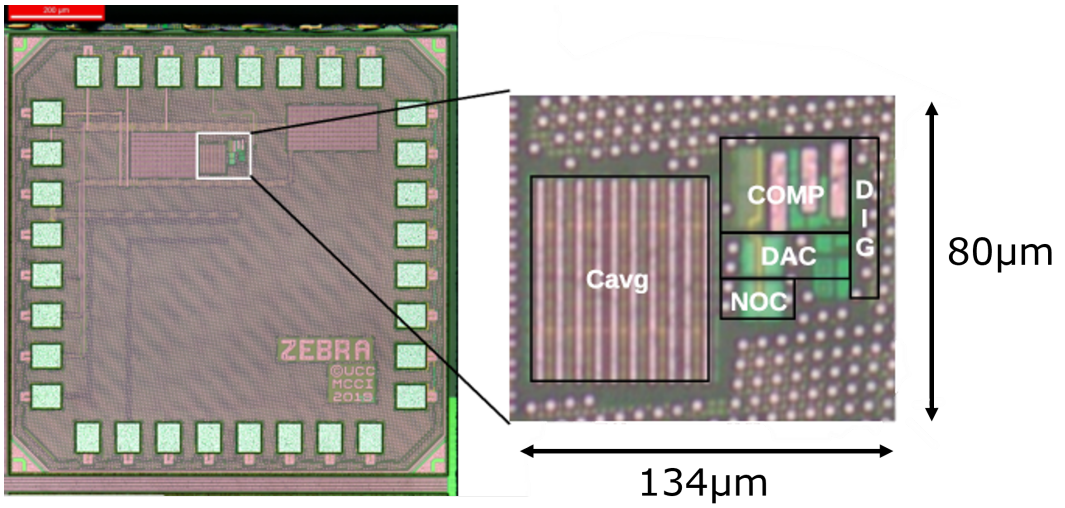


Figure 3.36: Die photograph with a zoomed view of a core BDC occupying 0.01mm^2.

The following sections describe how the data was collected and individual results are presented and discussed. Due to the small size of the die, the number of available I/O pads was limited. Considering all the blocks were fabricated for the first time, the available pads were used to maximise the visibility of the internal nets. This did not leave any pads for an additional interface, so the data must be collected "on the fly". Thus, instead of accessing the binary output string from the ADC's logic, the sequential comparator's output is captured instead. Table 3.1 provides a comprehensive list of I/O pads, along with their respective descriptions. Each entry outlines the pin name, the type (input/output) and its functionality.

Table 3.1: Description of Input and Output (I/O) Pads

Pin name	**Type**	**Description**
CLK	Input	Clock input
RESETB	Input	Reset signal (active low)
REDUN_EN	Input	14/12 SAR cycles select
OSR0	Input	DAC oversampling ratio select
OSR1	Input	DAC oversampling ratio select
OSR2	Input	DAC oversampling ratio select
DAC2_SEL0	Input	Secondary DAC activation duration select
DAC2_SEL1	Input	Secondary DAC activation duration select
COMP_IN_N	In/Out	Comparator input/DAC output
COMP_IN_P	Input	Comparator input
AVDD_COMP	Input	Comparator power supply
AVSS_COMP	Input	Comparator ground
AVDD_NO_CLOCKS	Input	Non-overlapping clocks power supply
AVSS_NO_CLOCKS	Input	Non-overlapping clocks ground
AVDD_REF	Input	DAC power supply
AVSS_REF	Input	DAC ground
AVDD_DIGITAL	Input	Digital power supply
AVSS_DIGITAL	Input	Digital ground
AVDD_TEMP_SENSOR*	Input	Temperature sensor power supply
AVSS_TEMP_SENSOR*	Input	Temperature sensor ground
DVDDIO1V2	Input	I/O ring digital power supply 1.2 V
DVDDIO2V5	Input	I/O ring digital power supply 2.5 V
AVDDIO2V5	Input	I/O ring analog power supply 2.5 V
VSSIO	Input	I/O ring ground
EOC_FLAG	Output	End of Conversion flag
COMP_OUT	Output	Comparator output
TEMP_SENSOR1_OUT*	Output	Temperature sensors output
TEMP_SENSOR2_OUT*	Output	Temperature sensors output

*Pins are not relevant for the work discussed in the thesis.

3.5.1 Laboratory Setup

The PCB used to test the fabricated design is shown in Figure 3.37. Apart from the power supplies and outputs, the board also has an input filter, with an input source select and a voltage regulator to produce a steady reference from the noisy power supply. Jumpers are used to manually reset and program the chip. The programmable pins are DAC_SEL, which selects the number of cycles the secondary DAC is activated for and an OSR setting for the oversampling ratio. When REDUN_EN is high, fourteen comparator decisions are taken during one approximation instead of twelve.

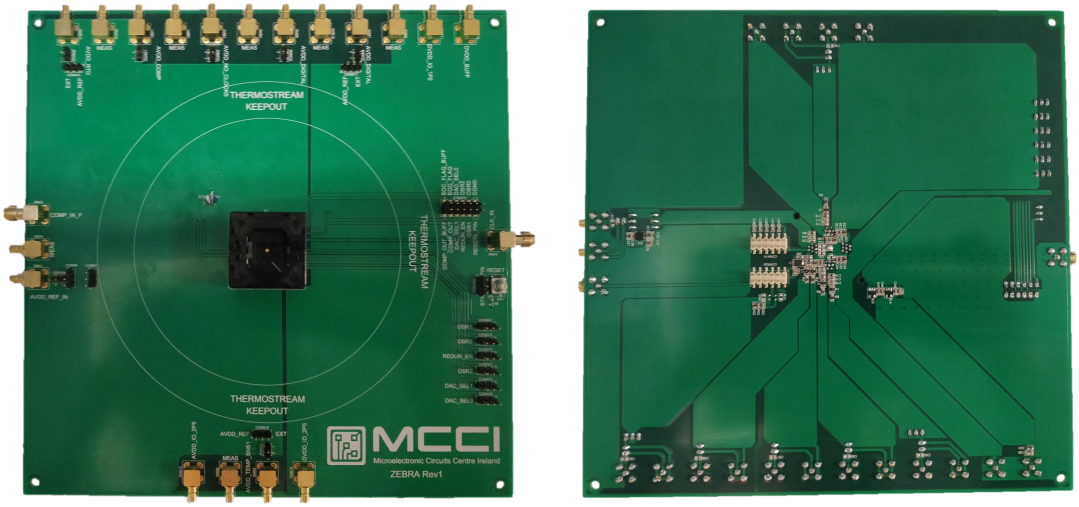


Figure 3.37: Designed PCB. Front (a) and back (b).

The laboratory setup is shown in Figure 3.38. As visible, the following equipment was used to collect data:

- The power was supplied by Rohde & Schwarz HMP4040 supplies.
- The clock was generated using a Keysight 33500B Series Waveform Generator Trueform and an Agilent Technologies 81150A (higher maximum frequency output).
- The DC/ramp/sinusoid inputs were generated using a Keysight 33500B Series Waveform Generator Trueform.
- Power measurements were captured using an R&S HM 8112-3 multimeter.

A Digilent Digital Discovery logic analyser was used to read and store the digital data locally from which the ADC outputs were reconstructed:

- CLK,
- EOC,
- COMP_OUT.

To ensure a high precision in capturing data an internal clock of 305.175781 Hz (10 MHz/32768) had to be generated in the analyser. This clock was triggered on digital incoming data that were probed at the same frequency; the generated clock was, in turn, used as a trigger to capture the EOC and comparator signals with the Digital Discovery logic analyser.

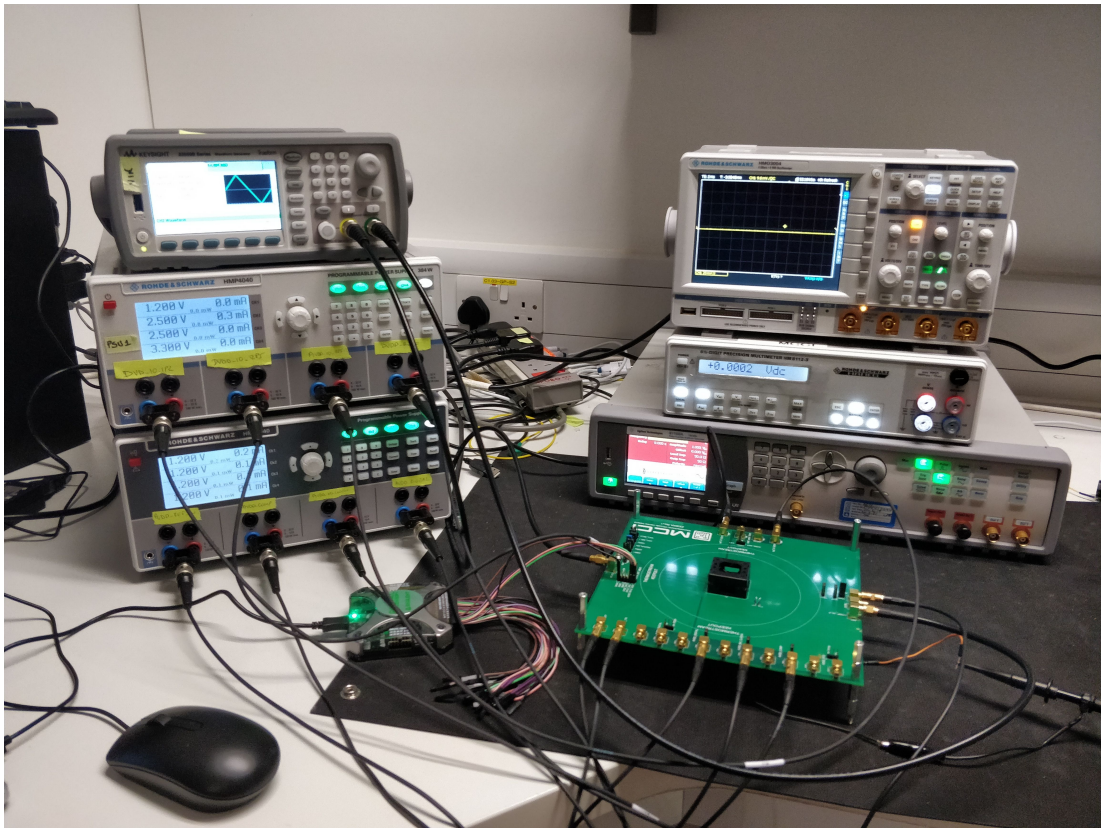


Figure 3.38: Photograph of laboratory setup.

3.5.2 Lab Results

Once the data was collected using the Digital Discovery logic analyser, a Python script extracted the comparator outputs from the Excel data files and converted them into

decimal codes for further processing in Matlab. For measurements such as an FFT, where the device had to operate over several hours, a clock drift could be observed. In such cases, the same comparator output was read twice giving fifteen instead of fourteen comparator outputs between two consecutive EOC signals and producing a measurement error. This error could be observed periodically. The Python script was used to detect and remove this anomaly.

3.5.2.1 SAR Approximation

Before the performance tests were conducted, the functionality of the BDC was verified visually. The following settings were used:

- Clk: 10 MHz (100 ns period),
- OSR set: 32768,
- DAC_SEL: 31,
- REDUN_EN: 0,

As indicated by the screenshots from the oscilloscope in Figures 3.39 and 3.40, this was done by setting a DC input signal (green line) and observing whether the DAC output (yellow line) converged correctly based on the comparator decisions (blue line). From this test, it can be concluded that the BDC is converting as expected.

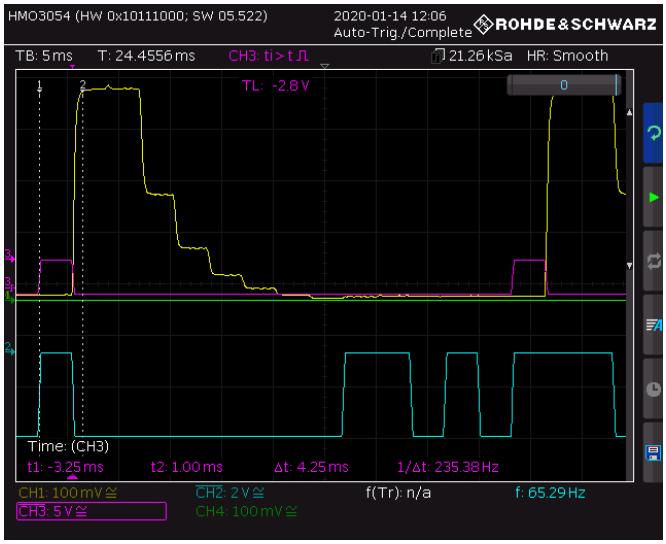


Figure 3.39: DAC convergence for 0V input.

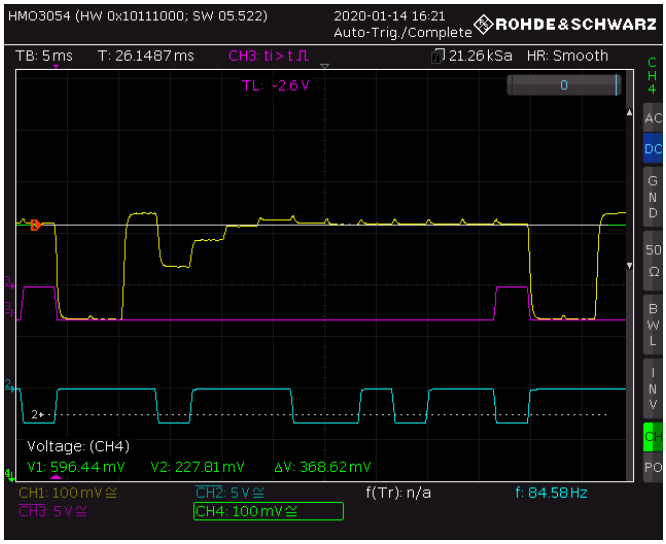


Figure 3.40: DAC convergence for 0.6 V input.

The period of the SAR clock was confirmed from the EOC period (purple line) allowing the BDC output to be attained. An offset could then be calculated by substituting the BDC output value for 0 V input into equation (3.9):

$$V_{offset} = \frac{D_{out}}{2^N - 1} * V_{REF}, \tag{3.9}$$

From Figure 3.39, the output code is 12'b000000110101, or decimal 53. The voltage reference is 1.2 V giving an offset of:

$$V_{offset} = \frac{53}{4095} * 1.2 = 0.0155\ V. \tag{3.10}$$

The test was repeated for eight values across the input range at 0.1 V intervals. The results are summarised and plotted in Figure 3.41. The BDC appears linear for this small set of values. The detailed results are presented in the next section.

3.5.2.2 Linearity

A histogram test was carried out to measure differential non-linearity (DNL) and integral non-linearity (INL). The test is performed by applying a full-scale ramp input signal, whose rate of change is smaller than the smallest input step that can be resolved by the BDC in that time. Furthermore, to ensure a high accuracy for the test, the ap-

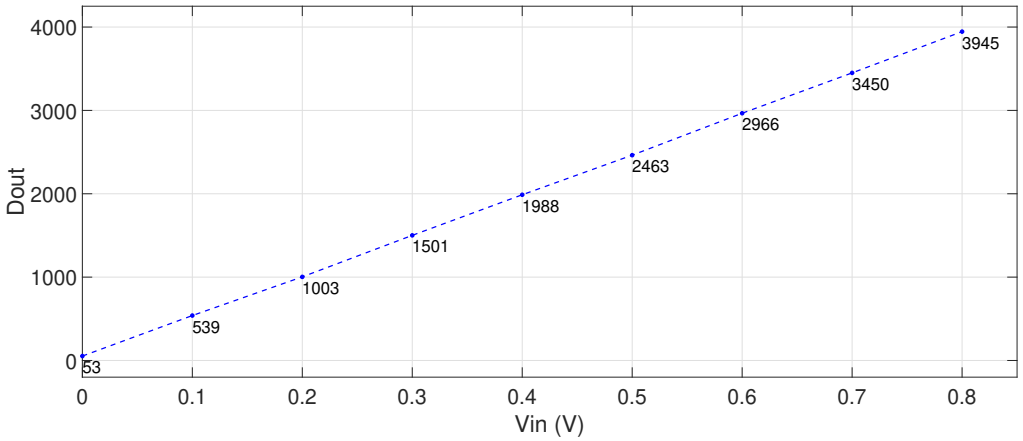


Figure 3.41: Plot of an output code vs the input voltage.

plied ramp must have allowed multiple samples for each LSB step to be taken. Once the data was collected, the digital output code could be plotted against the analog input. The DNL and INL values were then derived by calculating the deviations of each point on the acquired transfer function, after offset and gain corrections, from the ideal transfer function.

Due to the long BDC conversion time, an input ramp with a frequency of 110 μHz and 300 mVpp range with 185.0 mV offset was selected for this measurement. The collected output data was processed, extracted and plotted using Matlab software. As shown in Figure 3.42, the maximum DNL and INL measured were +2/-1 LSB and +3.13/-3 LSB, respectively, for a 12-bit output code. As can be observed from the plot, there is no visible INL step between the LSB and MSB transition, as would typically appear in a binary weighted DAC.

3.5.2.3 Repeatability

Another measure taken to characterise the static performance of the BDC was a repeatability test. This simple test is performed by collecting a large number of samples (32,768 samples were taken here) for a DC input signal. The variations in the output code correspond to the amount of noise (quantisation, thermal and flicker) present in the ADC. A mid-scale input was chosen and the output is illustrated in Figure 3.43. The results show a peak to peak variation of 1.5 mV.

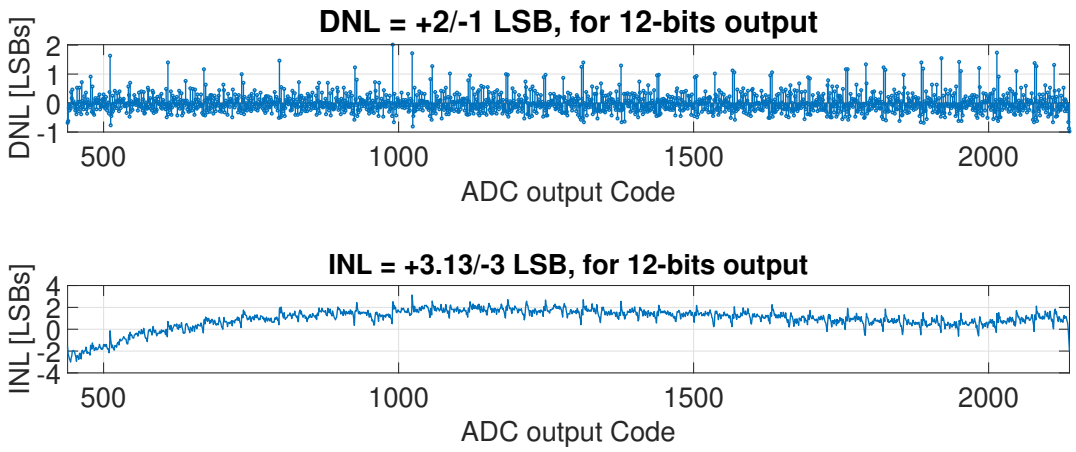


Figure 3.42: Measured DNL and INL for ramp input.

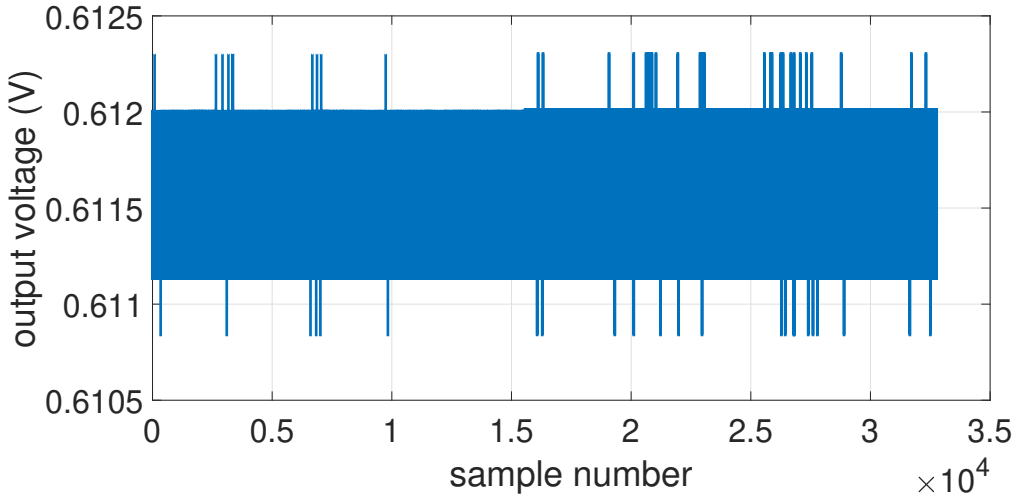


Figure 3.43: Repeatability test for a 600 mV input signal.

3.5.2.4 Spectral analysis

While the primary application of this implemented data converter is not expected to be used with sinusoidal input signals, the spectral test has been performed as it is widely used to benchmark the performance of standard ADCs. Because the input signal isn't sampled, any large variation of the signal during the conversion results in an error; however, this shouldn't be a concern during normal operation, due to the slow-moving nature of the input signal. Nevertheless, this can be minimised by implementing a redundancy technique.

The spectral test reveals how much white noise is present in the ADC's band of interest

and was carried out by applying a sinusoidal waveform and performing a Fast Fourier transform (FFT) on the collected output data, to check for any unwanted tones. To perform an FFT, N samples spaced by $T_s = 1/f_s$ seconds had to be obtained. The FFT was performed for a low frequency input signal of 0.0017 Hz with an amplitude of 600 mVpp. Figure 3.44 shows the spectrum of the reconstructed sinusoidal output. The ADC achieves a peak SNDR of 50.6 dB and SNR of 56 dB. The high noise floor close to DC is caused by the DC leakage, which introduces unwanted low-frequency noise during measurement.

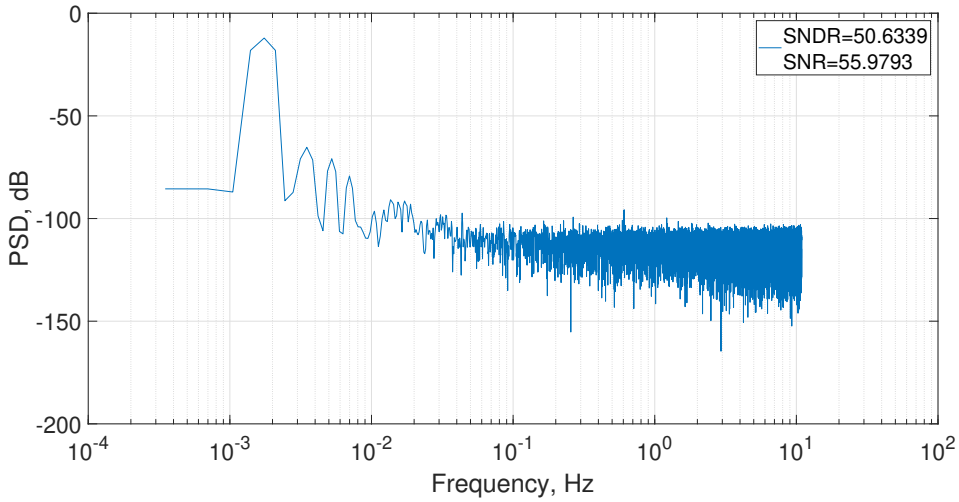


Figure 3.44: Measured output spectrum (65 536 points).

3.5.2.5 Power

Current consumption was measured for OSRs of 32768 and 8192, respectively, and the results are visualised in a pie chart in Figure 3.45. For the higher OSR setting, this BDC draws an average of 6.2 μA from the 1.2 V supply, of which 3.44 μA is consumed by the digital logic (including non-overlapping clocks), when clocked with a 10 MHz clock, resulting in a conversion time of 45 ms. The reference current is measured to be 1.3 μA with the clock applied. The remaining 1.46 μA is consumed by the comparator. There is only 0.21 μA current saving when using the lower accuracy setting. In summary, the power consumption is dominated by the digital logic and it's directly related to the operational frequency.

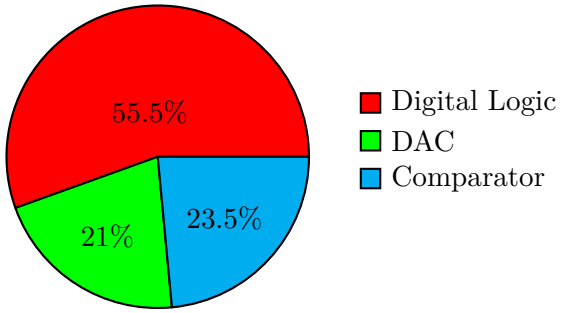


Figure 3.45: Power consumption breakdown of the BDC operating at a 10 MHz clock frequency and 32768 OSR.

3.6 Summary and Conclusion

This chapter presented a design and implementation of a SAR-based bridge-to-digital converter. Both simulated and measured results were shown and discussed. For observability, the DAC output was brought off-chip, adding parasitic capacitance to the node. The noise contributed by the PCB could be limiting the performance of the BDC. The other reason for degradation was flicker noise which was not compensated for in this design. The noise associated with the unit capacitors is not visible due to the large OSR of 32768 and the fact that the sampled thermal noise is not integrated.

The results of the proposed architecture are summarised in Table 3.2 and can compete with state-of-the-art solutions. The input range of 830 mV is over six times greater than in [101] and more than three times greater than in [113]. The BDC also consumes significantly less power than [113] and [114], with a competitive FOM_W of 0.65 nJ/conv. While [101] is more efficient, SAR ADCs usually require low-noise power-hungry input buffers and anti-aliasing filters in the front-end, which are not needed here.

The complete BDC also occupies the lowest area, excluding [113], where such information wasn't provided. The main results from this chapter were presented at the IEEE European Solid-State Circuits Conference on 17^{th} of September 2021.

In addition to the quantitative advantages, the DAC structure allows the ADC to be easily programmed, enabling the optimal balance between required resolution and speed for specific applications. This also allows the BDC to respond to input changes in real-time. This high flexibility makes this ADC particularly superior for physical-to-digital

Table 3.2: Performance Summary and Comparison With Other Bridge-To-Digital Converters

	This BDC	**CICC 2021 [115]**	**ISSCC 2018 [101]**	**VLSI 2017 [113]**	**JSSCC 2015 [114]**
Readout Type	SAR	VCO	SAR	$\Sigma\Delta$	VCO
Technology [nm]	65	180	180	180	180
Area [mm^2]	0.01	0.05	1.7	–	0.36
Supply Voltage (V)	1.2	1.8	1.2	1.8	5/1.8
Input range	830mV	4mV	±68mV	±16mV to ±128mV	±4uA
Power Consumption (μW)	7.4	20	2	19[a]	340
Conversion Time (ms)	45	1	4	62.5	400
SNR (dB)	56	31	54.2	66.4	73
FoM$_W$ [nJ/conv]	0.65	0.69	0.019	0.7	37.25

[a]including bias, ADC clocks, and digital decimation

applications. Chapter 4 further explores this topic by introducing a threshold detection-based ADC. Instead of using a successive approximation, the DAC generates threshold levels that track the input signal, similar to a level-crossing architecture. The input is then periodically compared to these threshold levels, but the output is generated only when a threshold is crossed, providing critical information to the system.

While Bridge-to-Digital converters are expected to be used in applications with signal frequencies below 50 kHz, their slow conversion time poses a bottleneck for this architecture. In this revision, the DAC is given the same number of clock cycles for each approximation. However, it is observed that the voltage step is halved with each consecutive approximation, indicating potential time savings. Despite this, the DAC still requires approximately 16k clock cycles for conversion. Chapter 5 presents a highly-digital slope-based BDC that utilises the switched capacitor DAC more efficiently. Additionally, the DAC has been redesigned to minimize mismatch effects.

Chapter 4

Threshold Detection based ADC

As discussed throughout this thesis, the present work targets sparse and slowly varying signals produced by resistive sensors in environmental monitoring and similar applications. While the architecture proposed in Chapter 3 meets many of the requirements, this chapter expands on the previous design to enable a true physical-to-information sensor system. In such a system, the BDC provides actionable data where, instead of providing a periodic set of readings, it only sends an interrupt to the system when an alarm is triggered. This indicates to the system that an action is required. This maximises the time that the micro-controller can spend in low power, sleep states. The proposed Threshold Detection (TD) based ADC reused the blocks from the previous design but its logic block was modified. Instead of the popular successive approximation, it periodically compares the input signal to an internally generated threshold. This approach offers a number of key advantages: firstly, the critical information is contained in a single bit, i.e. is the input signal above or below the threshold value, thus minimising the data that needs to be transmitted. Secondly, the comparator is only required to make a single decision. Finally, due to the robust digital nature of this architecture, the user can easily program a number of thresholds, their values, and set a required delay between successive samples, to accommodate a variety of gas and other sensing applications.

Due to the fact that both the DAC and comparator blocks were already described in

detail in Chapter 3, this chapter will only focus on the top-level implementation and the improvements to the design presented in Chapter 3.

4.1 Threshold Detection

Figure 4.1 illustrates a probable gas sensor output scenario, similar to the carbon monoxide concentration in Figure 1.3. In the plot, the signal (in blue) remains below 9 ppm (harmless) for a few hours, before starting to increase past 50 ppm, which could induce detrimental health symptoms. Subsequently, the signal oscillates between 9 ppm and 50 ppm before ramping back down to harmless concentration levels. Depending on the sampling frequency, there could be thousands of samples of data generated that would have to be read and potentially processed by a receiver. In the IoT device, the data may have to be sent to the cloud. The proposed threshold detection concept moves the first decision process of whether the sensor output level exceeds an undesirable threshold from the micro-controller to the ADC. The TD-ADC follows the input signal and compares it periodically to the pre-programmed 9 ppm reference level, only generating an output when the level is crossed and, subsequently, updating a DAC to the next threshold level and starting a timer. The micro-controller is woken up from sleep only if either the signal exceeds the higher threshold level or the concentration exposure timer is activated. In both cases, the TD-ADC generates less output data compared to traditional ADCs, offering significant power savings.

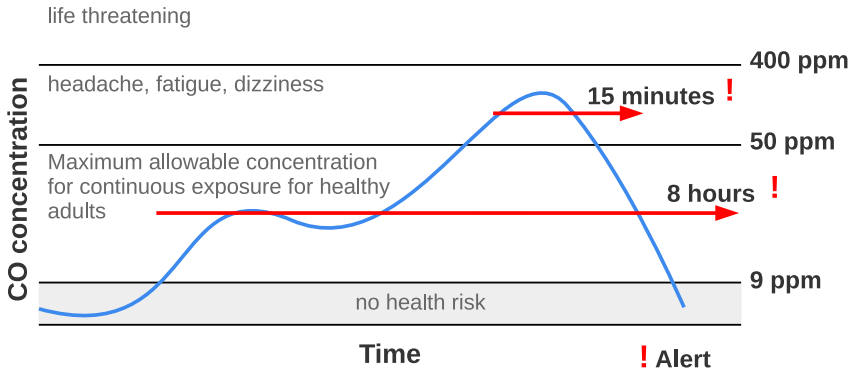


Figure 4.1: Example of carbon monoxide concentration levels and their impact on an individual's health.

4.2 Top Level Design

The top level diagram of the designed TD-ADC is illustrated in Figure 4.2. As can be seen, the architecture design is equivalent to a SAR BDC from Chapter 3, with the SAR logic replaced with a threshold detection algorithm.

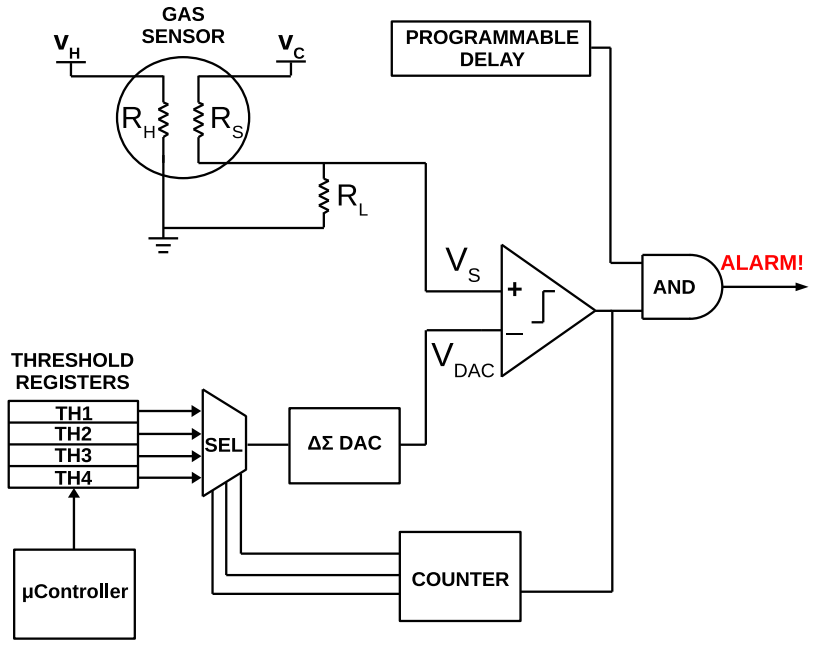


Figure 4.2: Block diagram representing the proposed threshold detection based ADC concept, whereby the input generated by the resistor divider is compared against the 4 different levels.

The operation of the ADC is now outlined. During the initialisation stage the microcontroller programs the threshold and delay registers to the desired exposure values and time limits, respectively. Upon completion, the DAC is enabled and allowed to fully settle to the first desired threshold level, TH1. Once settled, the comparator is enabled and the input signal generated by a resistor divider formed by the resistive gas sensor and a known resistor, V_s, is compared periodically against the aforementioned reference. Assuming V_s remains below the TH1 threshold, no alarm is triggered and the logic waits until the level is crossed. At the instant when V_s exceeds TH1, the comparator output goes high and the DAC is updated to the next level, TH2. A delay counter is also started.

The subsequent state is triggered based upon one of the two possible events, as shown in Figure 4.3. If V_s crosses TH2 the DAC is again updated to the next upper level,

TH3, and the comparisons become more frequent. The logic then follows this algorithm, raising the reference until an alarm is triggered. Otherwise, the alarm would be triggered if V_s remains below TH3 (or TH4) long enough for the counter to reach the pre-set delay.

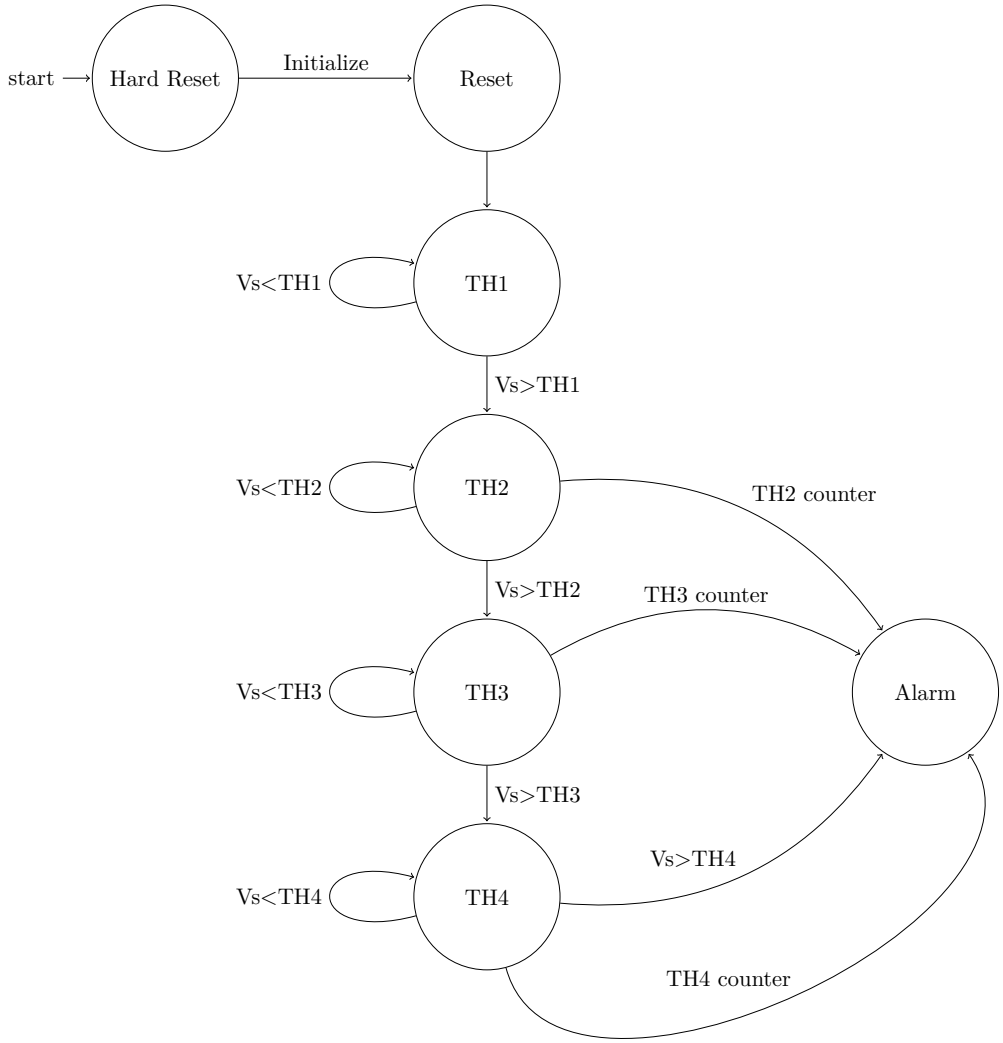


Figure 4.3: State diagram of the implemented logic

4.3 Implementation

Figure 4.4 shows a schematic of the designed ADC. Similar to the previous design, the desired threshold voltage is realised with a $\Delta\Sigma$ DAC. Note that while an N-bit switched-capacitor DAC could be used to generate a desired threshold level, the $\Delta\Sigma$

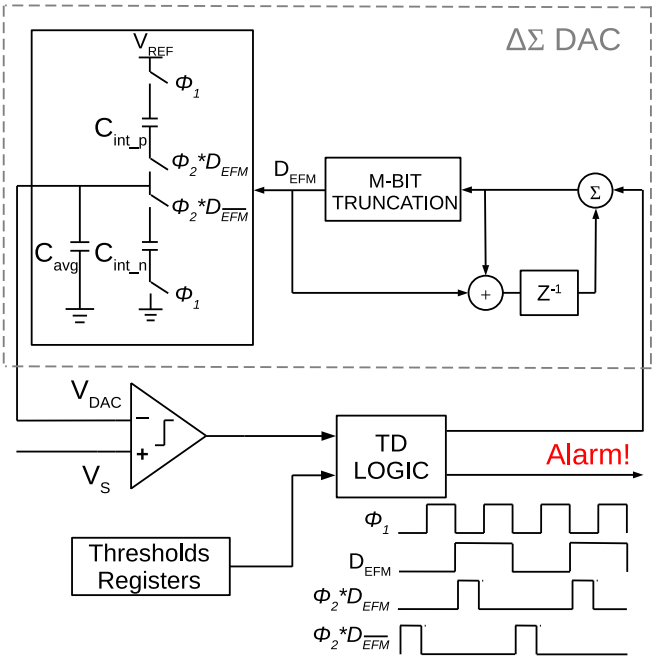


Figure 4.4: Schematic of the proposed Threshold Detection based ADC with a timing diagram.

DAC approach has already been established as a viable low-power and low-area alternative. Additionally, as the DAC needs to settle only once per threshold level, once the desired voltage is reached it can achieve a high resolution comparison at high speed. Also the DAC is not required to charge and discharge as frequently; this makes the architecture more efficient.

The input signal is not sampled but is connected directly to a double-tail dynamic latch comparator with PMOS input transistors. Since the comparator is only required to make one decision per ADC output, the power consumption is dominated by the leakage current, as opposed to the dynamic power. This provides significant power savings in systems that operate at low frequencies.

The logic and comparator operate from the same clock, which is a divided-down version of the master clock. The DAC operates at the master clock frequency but, once settled, it can be refreshed at much lower rates.

The layout of the proposed TD-ADC is illustrated in Figure 4.5. The ADC has been designed in TSMC 65 nm CMOS technology, and it occupies only 0.012 mm^2. Both the averaging capacitor and logic consume the largest area. The layout of the logic

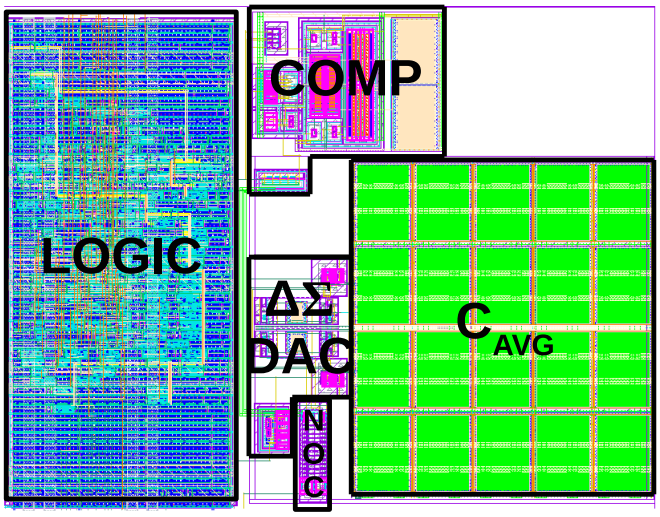


Figure 4.5: Layout of the Threshold Detection ADC occupying 0.012 mm^2 in 65 nm CMOS.

consumes 0.0042 mm^2. The size of the logic, which could be further optimised, is dependent on the number of internal registers that are used to store the thresholds and delay times.

4.4 Results

In this design, four non-uniformly distributed threshold levels were used. Simulations show that it takes 2792 clock cycles for the DAC to ramp from 0 V to 300 mV, while only 404 more clock cycles are needed to ramp from 0 V to 600 mV. Here, a clock with a 50 ns period was applied to the system, which resulted in a settling time of 140 μs. For densely spaced thresholds this number will be significantly lower. The operation of the ADC is presented in Figure 4.6. In the first case (a), the input is increasing gradually. When individual thresholds are passed each time the comparator output goes high, the DAC is updated consecutively to the next threshold. The alarm is triggered when the input crosses threshold 4 and the maximum level is reached. In the second case (b), the input crosses the first two thresholds and stays between thresholds 2 and 3. The alarm is triggered after the maximum delay is reached, indicating excessive exposure to a moderate gas concentration.

During the above operation the simulated power consumption was 4.7 μW. The biggest contributors were the logic and non-overlapping clocks drawing 3 μW and 1.5 μW

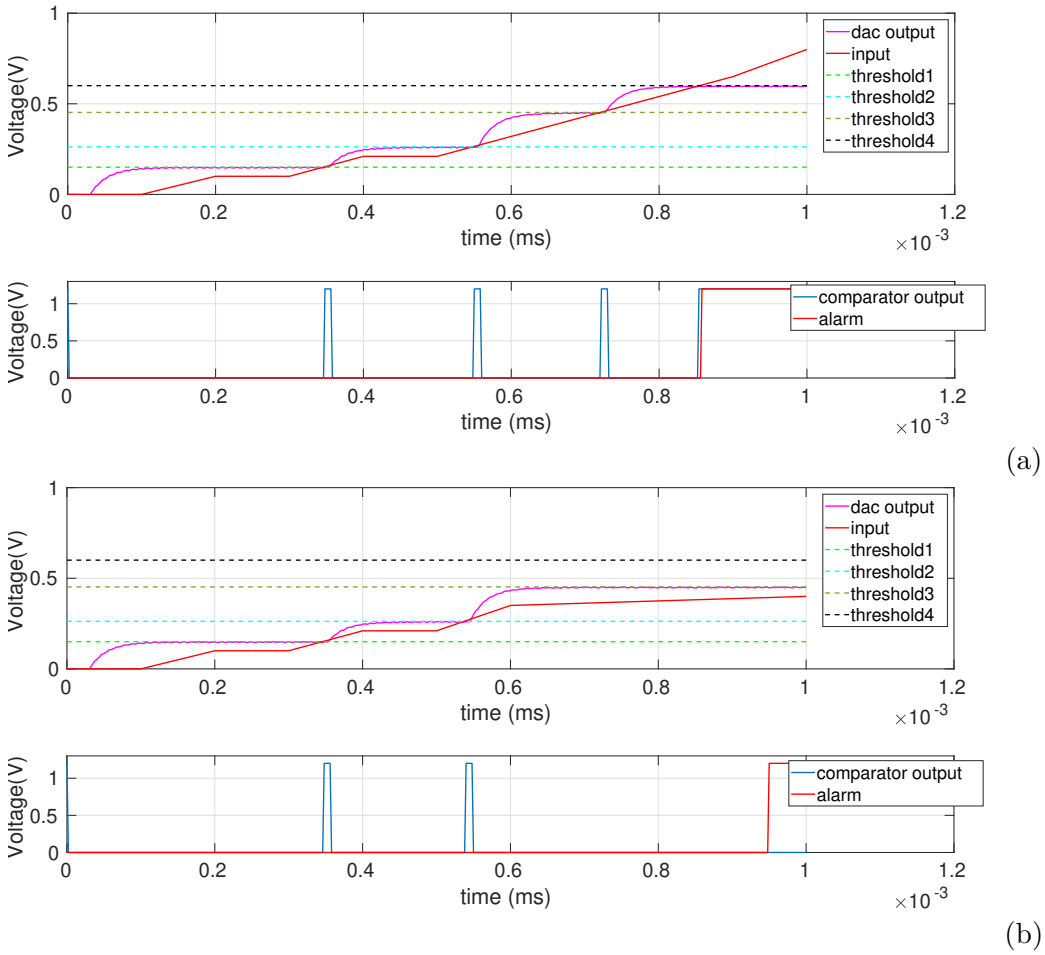


Figure 4.6: The post-layout simulation results of the Threshold Detection ADC operation for (a) threshold triggered alarm and (b) delay triggered alarm scenario.

respectively. The DAC consumes 194 nW and the comparator which is operating at much lower frequency consumes 113 nW.

4.5 Summary and Conclusion

This chapter presented a design and implementation of a threshold detection based ADC, which is an alternation to the design presented in chapter 3. Both schematic and extracted simulation results were discussed. The results are also summarised in Table 4.1 and compared against the state of the art and the design from chapter 3. This work significantly reduces the power consumption compared to the previous work. Also it compares favourably to [12, 116, 117].

Based on the results presented, the threshold detection based ADC is shown to be

Table 4.1: Performance Summary and Comparison With Other Bridge-To-Digital Converters

	This work	**Chapter 3**	**Sensors 2019 [12]**	**MWSCAS 2019 [116]**	**JSSC 2017 [117]**
Readout Type	TD-ADC	SAR	Oscillator-based	SAR	Time Domain
Technology [nm]	65	65	130	180	40
Area [mm^2]	0.012	0.01	0.125	0.045	0.015
Supply Voltage (V)	1.2	1.2	1.5	1.2/1.8	0.6
Power Consumption (μW)	4.8	7.4	450	2070	3.3
SNDR (dB)	50.6[a]	50.6	48	45.16	–

[a]based on results in chapter 3

an unconventional but a viable solution for monitoring resistive environmental sensors including gas sensors. The input signal can be closely tracked by using a higher density of threshold levels. The proposed ADC could also be easily expanded to include a second DAC and comparator enabling the input signal to be bounded by two threshold levels, similar to a level-crossing ADC. However, for the majority of home and office based air quality monitoring applications, this was not deemed necessary.

This type of ADC is very flexible due to its highly digital nature, as the threshold values, the number of output bits and the time delays can be modified in situ. Compared to the SAR algorithm presented earlier, each conversion requires only one clock cycle per decision, independent of the requisite resolution, assuming that the $\Delta\Sigma$ DAC has already settled.

Furthermore, results indicate that the ADC can greatly reduce the amount of generated output data, minimising the amount of data that needs to be wirelessly transmitted, significantly reducing the power consumption and thereby extending the battery life of the edge IoT device. The main results from this chapter were presented at the IEEE International Midwest Symposium on Circuits and Systems on 10$^{\text{th}}$ of August 2021.

Chapter 5 goes back to the more traditional ADC implementation focusing on improving the ADC from Chapter 3. The chosen architecture is modelled on a ramp ADC

architecture but reusing, however, an improved DAC design from already presented designs. The goals for Chapter 5 are to improve the conversion rate and minimise the gain error.

Chapter 5

Counting-Based Bridge-to-Digital Converter

This chapter introduces a counting-based Bridge-to-Digital Converter that can be used either with a single-element resistive sensor or in a Wheatstone-bridge (WhB) configuration. The modified topology attempts to tackle some of the drawbacks of the SAR-based BDC already discussed in Chapter 3. Unlike the changes introduced in Chapter 4, the BDC tracks the signal and generates a periodic output like a traditional ADC. A slope-based topology isn't as commonly used as it achieves low conversion speeds and targets narrow bandwidths; however, this isn't a problem for environmental monitoring based IoT applications. The concept of using it as a resistance-to-digital converter was already introduced in [118, 119], where the authors used a dual-slope approach, showing benefits such as high precision and noise immunity. Additionally, dual-slope ADCs can mitigate inaccuracies resulting from component value variations. This thesis attempts to simplify the slope-based design by replacing the ramp generator with a compact and power-efficient switched-capacitor DAC, making it a highly digital architecture and adding programmability. Furthermore, it uses only one internal capacitor and one integrating capacitor which eliminates mismatching requirements. Any mismatch between those two capacitors results in a minor gain error which can be easily calibrated out. However, unlike the traditional ramp generator, the proposed DAC

does not realise uniform steps. In fact, the use of a ramp-generator with non-uniform steps offers many advantages.

To take advantage of the smaller voltage steps, two modes of operation (single-slope and dual-slope) are proposed. Note that while the dual-slope operation was simulated and visualised, errors introduced by the coarse and fine registers observed in the silicon measurements prevented further analysis of its performance relative to the single-slope operation.

This chapter focuses on the implemented architecture. Much emphasis will also be placed on highlighting the differences between this design and the design from Chapter 3. Like the previous design, this BDC is fabricated in 65 nm CMOS and occupies an area of 0.014 mm^2. It has a wide input range of 780 mV and achieves an SNR of 49.97 dB. It consumes 30 μW at a 0.41 ms conversion time, resulting in a Walden FoM of 0.048 nJ/Conv-step.

5.1 Counting-Based BDC

As already explained in Chapter 2, a conventional ramp ADC operates as follows: a synchronous comparator compares the input signal, V_{IN}, against an internally generated, uniformly increasing ramp signal, V_{RAMP}. A counter continues to increment while $V_{RAMP} < V_{IN}$. When the ramp crosses the input, the comparator output toggles, and the counter's output is latched, representing the ADC's binary output. Before the ADC can continue to the next conversion, the control logic clears the counter and resets the ramp generator. The ramp generator is typically realised using active elements or a unary DAC. Traditionally, the voltage step at each clock cycle is equivalent to one LSB and the counter records the number of clock cycles it takes for the ramp to reach the applied input signal level.

A detailed diagram of the implemented ADC is illustrated in Figure 5.1. It is similar to the aforementioned counter ADC where the ramp voltage, V_{RAMP}, is monotonically increasing at each clock cycle and compared against the input voltage, V_{IN}, until V_{RAMP} is equal to, or greater than, V_{IN}. However, unlike the traditional ramp or counter-based

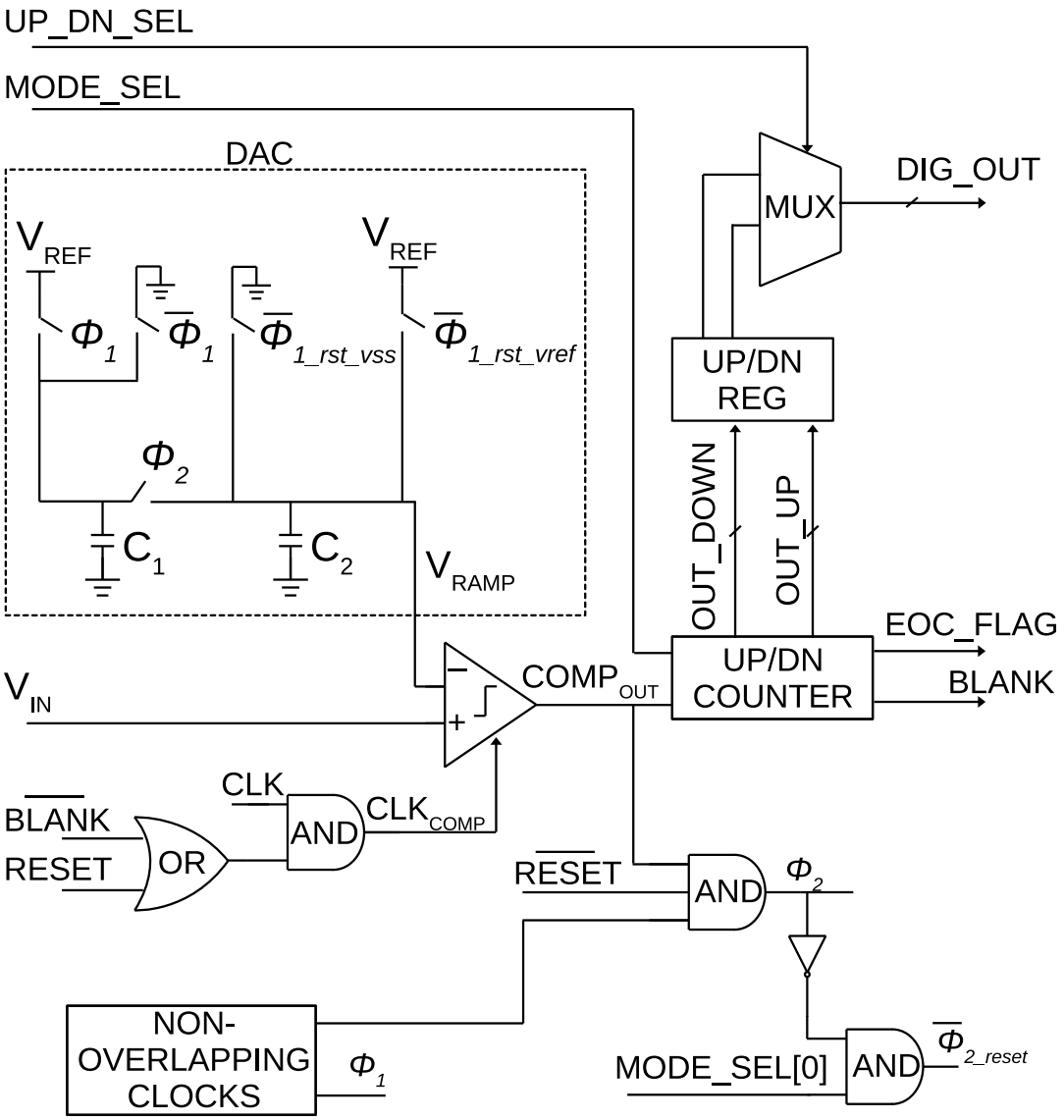


Figure 5.1: Block diagram of the digital ramp ADC.

ADC, the ramp generator is replaced with a simple switched capacitor circuit similar to that implemented and tested in Chapter 3. Here, only one internal capacitor is utilised to eliminate the layout mismatch which led to the gain error in the earlier design. However, unlike the traditional ramp, the new ramp circuit does not realise uniform steps.

5.1.1 Updated SCR DAC

The updated DAC has been implemented using a feedback capacitor, C_1, and an integrating capacitor C_2, and five switches, as shown in Figure 5.2.

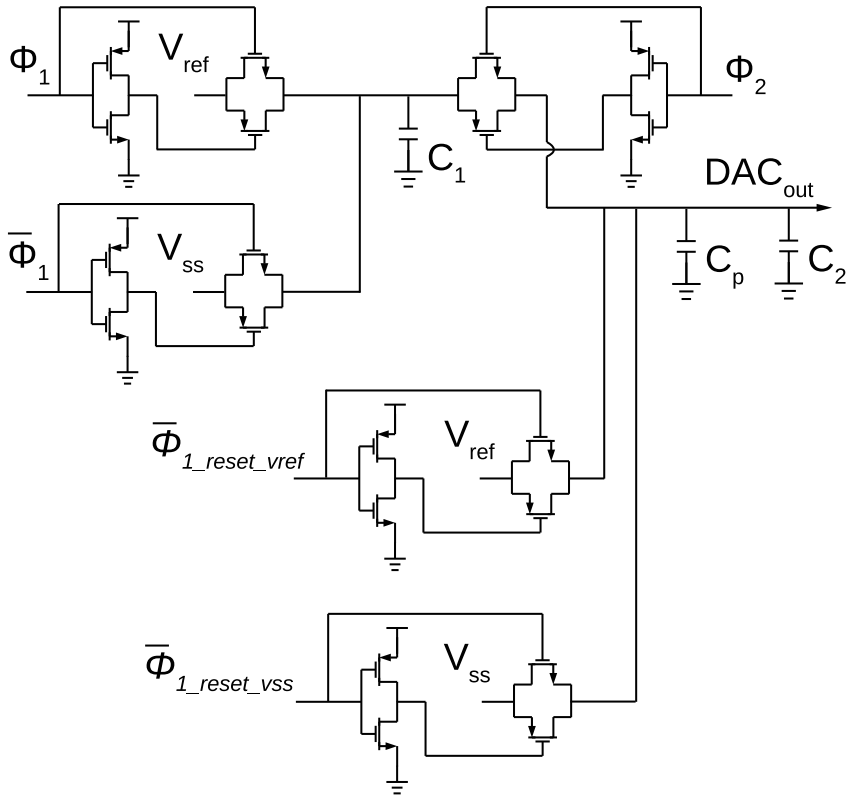


Figure 5.2: Transistor level implementation of the DAC including parasitic capacitor Cp and illustrating both ramp up and ramp down capability.

Its operation is similar to the prior design, where the charge transfer between C_1 and C_2 is triggered on two phases of a non-overlapping clock. Initially, during reset, C_2 is discharged to ground. Subsequently, during ϕ_1, C_1 is charged to V_{REF}, when ramping up. Then, during ϕ_2, C_1 is connected to C_2, transferring the sampled charge from C_1 to C_2. However, as the voltage on C_2 increases, less charge is transferred to C_2 on each subsequent clock cycle as the residual voltage on C_2 increases. Therefore, the amount of charge that is transferred between C_1 and C_2 depends on the previous output, V_{RAMP}(i-1), as described by equations:

$$V_{RAMP_up}(i) = \frac{C_1 V_{ref}}{(C_1 + C_2)} + \frac{C_2 V_{out}(i-1)}{(C_1 + C_2)}, \tag{5.1}$$

$$V_{RAMP_dn}(i) = \frac{C_2 V_{out}(i-1)}{(C_1 + C_2)}. \tag{5.2}$$

This results in the output waveform of V_{out} following an RC settling curve. To im-

prove robustness, the proposed DAC also has the capability to ramp down from V_{REF}. Depending on whether the DAC is ramping up or ramping down it will create either coarse or granular step sizes near the rails. It takes just over 1000 clock steps to ramp up from 0V to 0.8V. Although, in the absence of an active element such as an integrator, the DAC isn't able to produce uniform step sizes as in popular architectures, this architecture can produce smaller repeatable steps than that of the capacitor ratio (C_1/C_2) without consuming any active power.

Because the amount of charge transferred between C_1 and C_2 depends on the previous output, V_{RAMP}(i-1), as described by the equations (5.1) and (5.2), the output curve is exponential, as in Figure 5.3.

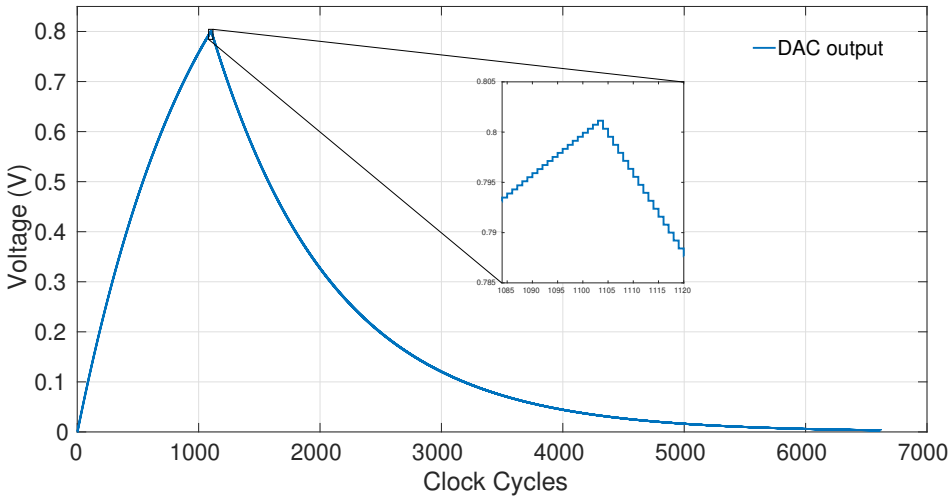


Figure 5.3: DAC sweep.

5.1.2 Modes of Operation

Since the switched-capacitor DAC isn't able to produce uniform steps that would directly correspond to the LSB as in traditional ADCs, to take advantage of the smaller voltage steps, two modes of operation are proposed, as illustrated in Figure 5.4.

The ramp up only mode may be selected when a higher speed is preferred over accuracy or when the input is closer to the ground rail. For a higher accuracy, a slower dual-slope approach is proposed. Here, V_{RAMP} first ramps up from ground, followed by a ramp down from V_{DD}. The two times are then recorded to give a calibrated output. A

dual-slope approach [118] is also widely used to mitigate any temperature and ageing effects.

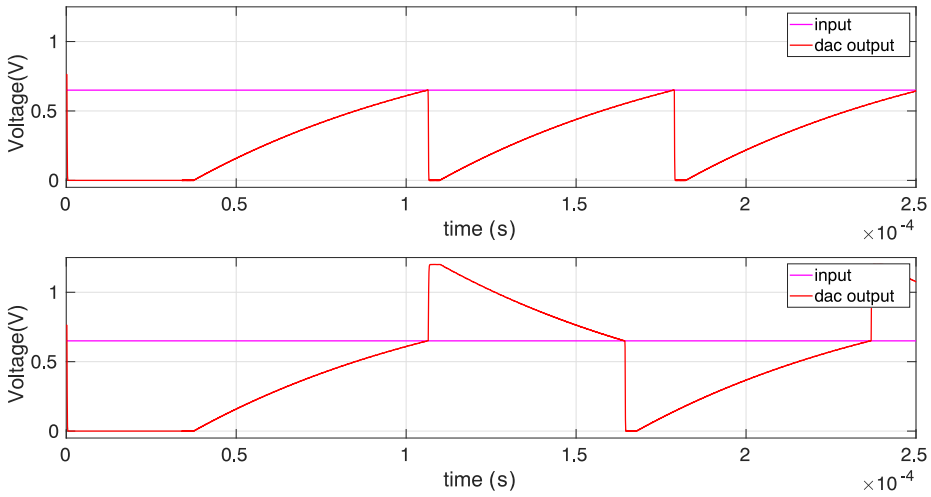


Figure 5.4: Modes of operation illustrated. Ramping up only (top) and Ramping up then ramping down (bottom).

The BDC can run in a continuous mode or it can be synchronised using a Start of Conversion (SOC) signal. The latter can provide a periodic output at the slower rate. The speed of the SOC can be either adapted to the expected input voltage range or taking into account the maximum time it takes to ramp up or ramp down across the full scale. While running the BDC in continuous mode may be preferable in higher speed input tracking applications, whereby the output is generated as soon as the comparator makes its decision, note that only one comparator decision is necessary for an output code to be generated.

A blank signal, which has a programmable duration, was introduced to prevent the comparator making decisions prematurely, which would reset the counter and send the BDC into an infinite loop. This is especially important when ramping down, after the DAC is reset to a V_{REF} which is above the comparator's input range.

5.2 Implementation

The proposed BDC was fabricated in TSMC 65 nm CMOS technology. Its layout, as seen in Figure 5.5, occupies only 0.014 mm^2. The double-tail dynamic latch comparator

and non-overlapping clock blocks were utilised from the prior design. The DAC has been implemented with one internal 20 fF capacitor, C_1. This capacitance was chosen to minimise the area and the reference current. The area is dominated by digital logic which occupies 0.007 mm^2. While the logic is predominantly implemented with a counter and a set of registers, it also includes an I2C interface. This interface was chosen due to the limited number of pads available, allowing mitigation of some of the issues from the first tape out and simplifying the process of programming and reading registers.

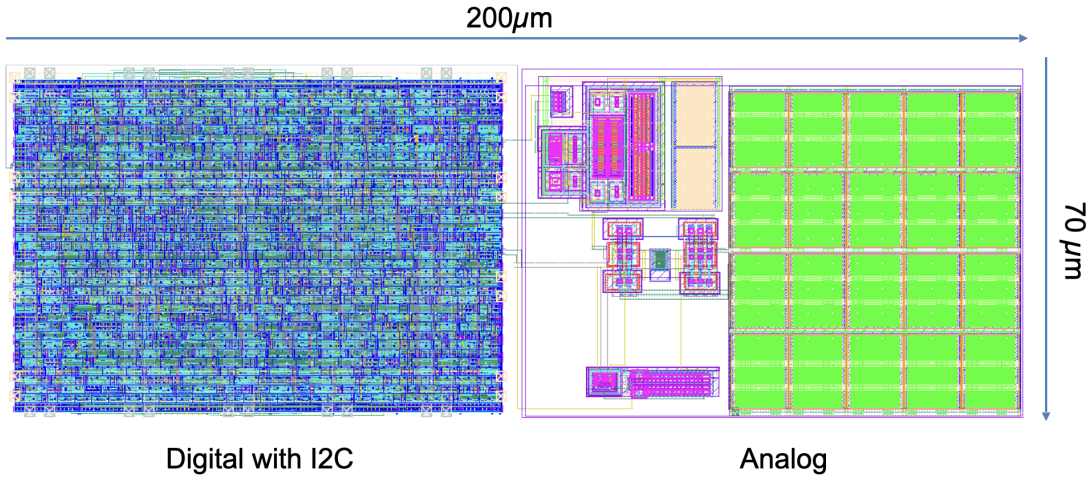


Figure 5.5: Layout of the implemented counting BDC.

The post-layout design with the IO ring has been simulated, and the results are presented in Figure 5.6. The results show the ADC conversion of a DC input during ramp-up mode.

5.3 Measured Results

The die micrograph of the fabricated counting BDC is shown in Figure 5.7. For this tape-out, a flip-Chip interconnection method was chosen, in which the solder bumps were deposited on the chip pads, as visible from the image. Flip-chip in Package (FCiP) technology provides improved thermal and electrical performance compared to more conventional wire-bond packaging [120].

An interposer was designed to facilitate the connection of FCiP onto the PCB board in Figure 5.8. The PCB board was made smaller to shorten the conductive traces and

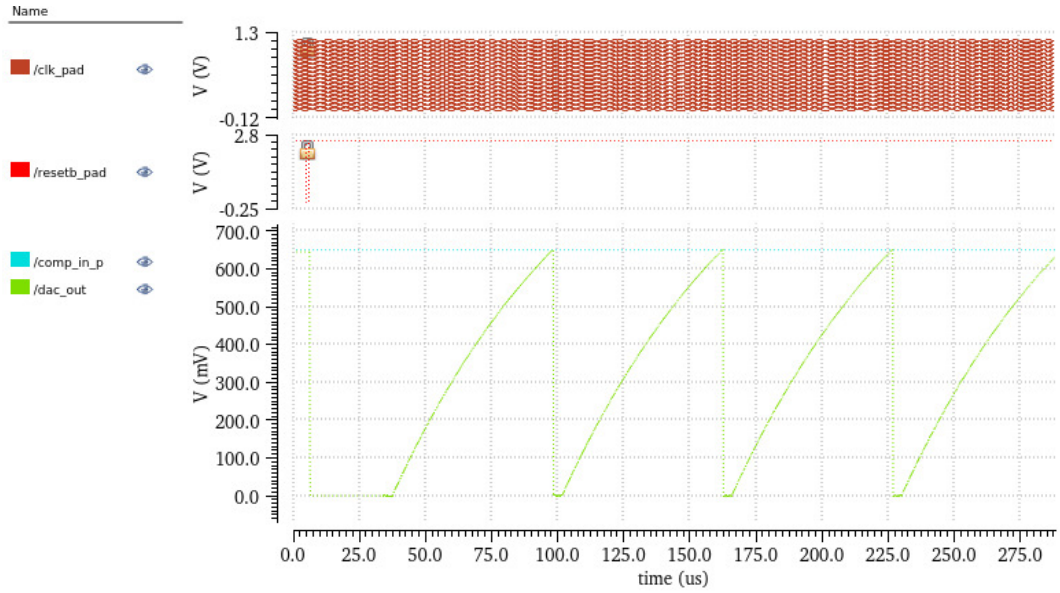


Figure 5.6: Simulation of post-layout extracted BDC with IO ring showing ramp-up mode.

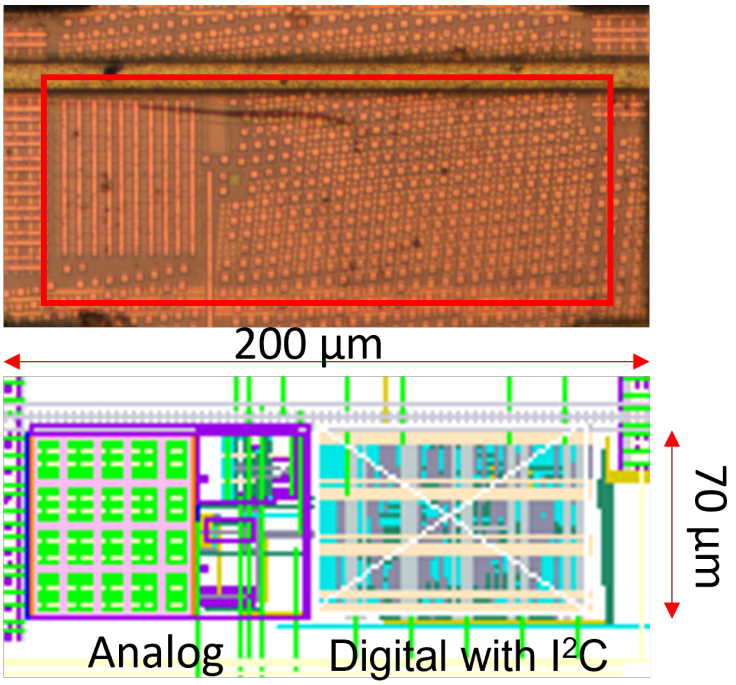


Figure 5.7: Die micrograph.

minimise any on-board noise and interference. An I2C driver with Arduino connections was added for data collection.

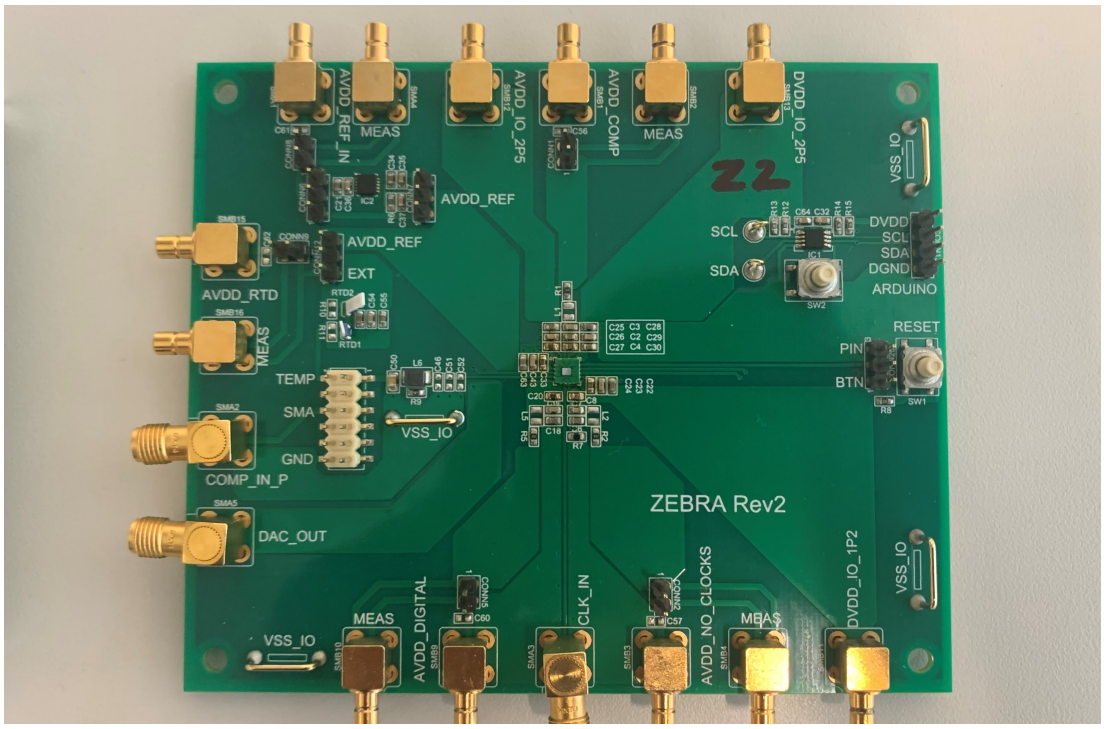


Figure 5.8: Photograph of a PCB board with an interposer.

The laboratory measurement equipment used to power the chip was similar to the one used in the first design. However, in this design, an Arduino was used for data collection purposes. Because the data was collected through an I2C interface it limited the minimum conversion time to 412.6 μs. The variable BDC latency, which is input-dependent, introduces harmonics in the output bandwidth due to the non-uniform sampling of the input signal when operating in continuous sampling mode and, as such, these are artefacts of the ADC interface.

5.3.1 Signal Reconstruction

The transfer function of the BDC is illustrated in Figure 5.9. Since the BDC is not producing a linear output code, the raw output data had to be first reconstructed before it could be further processed to obtain measurements such as SNR or INL. A two-step process was used here. Initially, a fitting curve was generated by substituting V_{out}, V_{in} and V_{REF} into the V_{RAMP} equations for a number of measured DC values and extrapolating for the full input range. In this case, any BDC errors were characterized

by C_p, the parasitic capacitance at the DAC output. Next, the RC approximation was calculated by treating the DAC as a simple RC circuit from equation (5.5), derived from equations (5.3) and (5.4). Here, n represents the number of DAC clock cycles, which in turn determines the BDC output code.

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f}, \tag{5.3}$$

$$V_{RAMP} = V_{REF}(1 - \exp(-\frac{nT}{R_{eq}(C_2 + C_p)})), \tag{5.4}$$

$$R_{eq}(C_2 + C_p) = -\frac{nT}{\ln(1 - \frac{V_{RAMP}}{V_{REF}})}. \tag{5.5}$$

Equation (5.5) has been used hereafter to represent voltage for the measurements in the following subsections.

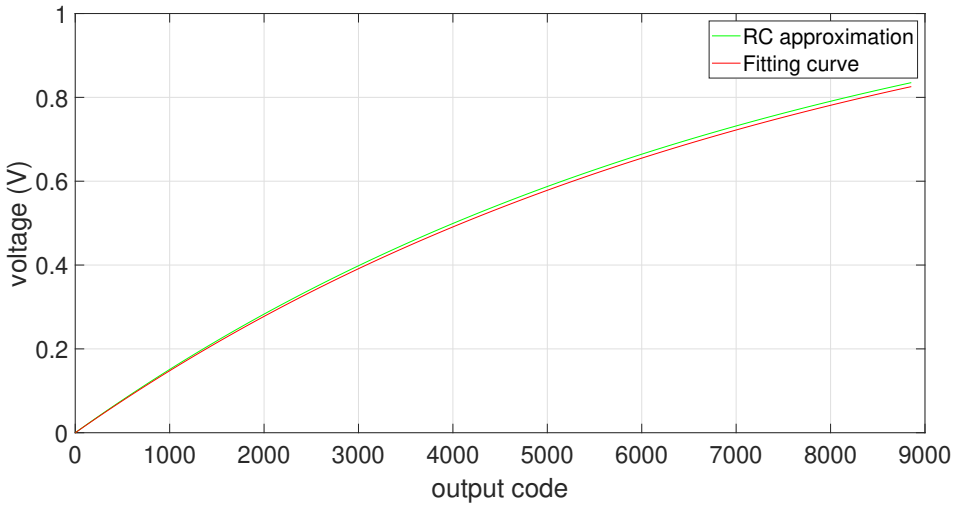


Figure 5.9: Output conversion, RC approximation and fitting curve.

5.3.1.1 Repeatability test

A repeatability measurement of the BDC was taken and the resulting histogram is illustrated in Figure 5.10. To measure the rms noise voltage, the output code was translated to voltage, as represented in Figure 5.11, showing a noise of 0.15 mV, translating to a

dynamic range of 65.6 dB.

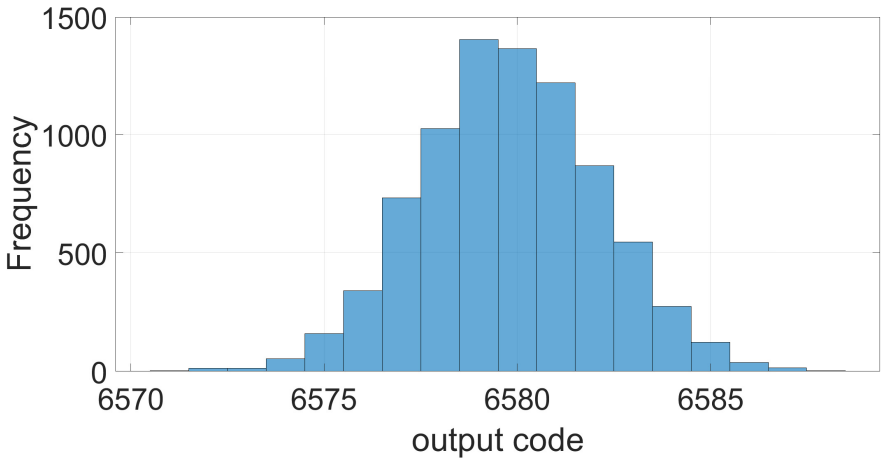


Figure 5.10: Histogram of the repeatability test results.

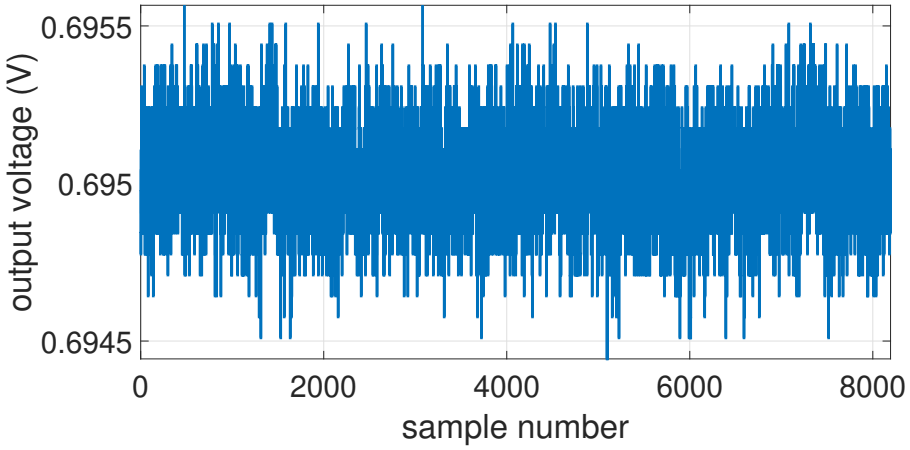


Figure 5.11: Repeatability test results showing rms noise of 0.15 mV.

5.3.1.2 Output spectrum

The SNR measured for a 25.4 mHz input with a range of 50-830 mV was 49.97 dB. The artifacts observed in Figure 5.12 manifest from the non-uniform sampling of the input signal, when operating the device in continuous conversion mode, due to the input dependent latency of the ADC. This has no impact on the performance when operating in the end application.

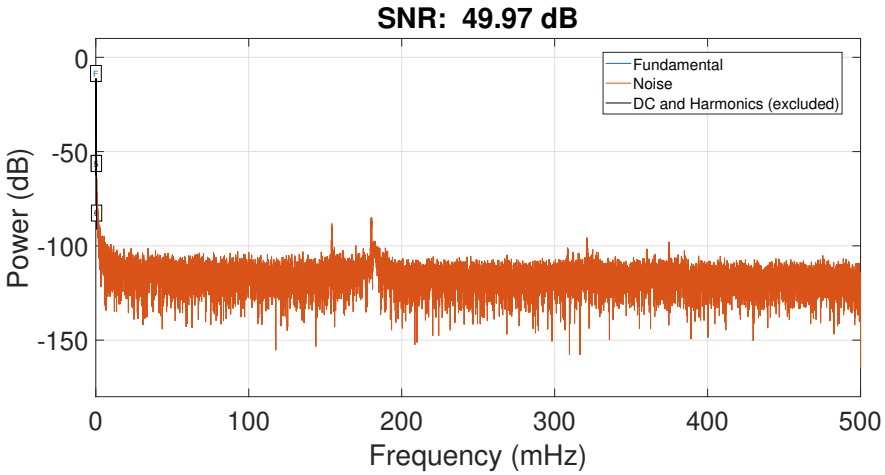


Figure 5.12: Measured output spectrum at full-scale input.

5.3.1.3 Power

Power consumption was measured for both a ramp-up only and the dual-slope modes. In both scenarios the voltage regulator was turned off and the blanking period, during which the comparator is disabled to prevent invalid decisions during DAC ramp-up, was minimized. With minimal blanking, the DAC consumed only an additional 0.012 μW of power.

In the ramp-up only mode, the BDC consumed 29.6 μW from the 1.2 V supply, of which 22 μW is consumed by the digital logic including the I2C interface, when clocked with a 20 MHz clock. The non-overlapping clocks and comparator consumed 3.2 μW and 3 μW, respectively, while the DAC consumed 1.44 μW.

In the dual-slope mode, the BDC consumed 26.5 μW from the 1.2 V supply of which 20.5 μW is consumed by the digital logic including the I2C interface, when clocked with a 20 MHz clock. The non-overlapping clocks and comparator consumed 3.2 μW and 1.43 μW, respectively, while the DAC consumed 1.42 μW.

5.4 Summary and Conclusion

This chapter presented a highly-digital counting-based BDC, where a traditional ramp generator was replaced with a switched-capacitor DAC to reduce area and power, greatly simplifying the design. Furthermore, a single internal capacitor was used to

eliminate any source of mismatch. This, in turn, resulted in a smaller DAC area and minimised the ripple, thus increasing the achievable resolution with the same averaging capacitor. While this thesis was mainly focusing on low-speed applications, the proposed approach aimed at increasing the conversion rate without significantly penalising performance. Although the power consumption is directly linked to the operating clock frequency, the overall achieved figure of merit was improved.

This BDC achieves an SNR-based Walden FoM of 0.048 nJ/Conv-step which is over 10 times better than the design implemented in Chapter 3, which also compares favourably with the state-of-the-art, as summarised in Table 5.1.

Table 5.1: Performance Summary and Comparison With Other Bridge-To-Digital Converters

	This work	**Chapter 3**	**CICC 2021 [115]**	**ISSCC 2018 [101]**	**VLSI 2017 [113]**
Readout Type	Counter ADC	SAR	VCO	SAR	ΣΔ
Technology [nm]	65	65	180	180	180
Area [mm^2]	0.014	0.01	0.05	1.7	–
Supply Voltage (V)	1.2	1.2	1.8	1.2	1.8
Input range	830mV	830mV	4mV	±68mV	±16mV to ±128mV
Power Consumption (μW)	30	7.4	20	2	19[a]
Conversion Time (ms)	0.41	45	1	4	62.5
SNR (dB)	49.97	56	31	54.2	66.4
DR (dB)	65.6	56.5	90	-	-
FoM$_{W,SNR}$ [nJ/conv]	0.048	0.65	0.69	0.019	0.7
FoM$_{W,DR}$ [nJ/conv]	0.008	0.61	0.0008	-	-

[a]including bias, ADC clocks, and digital decimation

The dynamic-range based Walden FoM is 0.008 nJ/Conv-step. Its wide input range of 830 mV and compact area of 0.014 mm^2 makes it suitable for environmental monitoring applications. These environmental sensors produce non-linear signals but, as long as

the ADC output is monotonic, the required information for the end application can be extracted without large computational resources.

While the FoM has improved significantly, the chip would benefit from an improved interface allowing the data to be collected at its full potential speed. The main results from this chapter were presented at the IEEE International Conference on Electronics Circuits and Systems on 20^{th} of November 2024 in Nancy, France.

Chapter 6

Summary and Conclusions

This chapter reviews the main objectives of this thesis. It starts by outlining the key research goals and emphasizes their importance within the broader context of environmental monitoring. Next, it summarises the contributions made to the field, including a list of publications. Finally, it suggests potential future work aimed at advancing this research, with the intention of inspiring ongoing development in the field.

6.1 Summary of Thesis

The objective of this thesis was to research Analog-to-Digital Converter (ADC) designs that interface with resistive sensors and propose new solutions. The introductory chapter emphasized the importance of environmental monitoring and discussed system-level considerations for gas sensors. It also outlined specific challenges in designing for Internet of Things (IoT) applications. One main challenge is achieving power efficiency, as many of these systems need to operate on batteries for extended periods. Another challenge is the requirement for a compact design, particularly for portable devices. Additionally, large IoT networks generate substantial amounts of data that must be processed either locally or in the cloud. When local processing is preferred, limited storage capacity can pose a challenge. Chapter 2 then outlined the most commonly used ADC architectures across various applications. It also introduced the more application-specific Bridge-to-Digital converters, highlighting the complexities involved

in digitizing a Wheatstone Bridge (WhB) output. This output is a low-voltage differential signal that must be accurately detected amidst higher common-mode voltages. For optimal performance, the ADC must provide high input impedance, gain, linearity, and minimal offset and noise, all while ensuring good power-supply and common-mode rejection ratios. Meeting these design challenges is difficult, even with a relaxed sampling rate of just a few kilohertz.

Subsequently, the thesis introduced three BDC architectures to address the identified issues. First, it discussed the design and implementation of a low-area, wide-input range SAR-based bridge-to-digital converter (BDC), highlighting both simulated and measured results. Next, it introduced a threshold detection-based ADC, which serves as an alternative to the previous design. Although the key architectural blocks remain unchanged, the logic was updated to further reduce power consumption. The thesis includes discussions on both schematic and extracted simulation results. Finally, it presented a highly-digital counting-based BDC, which features a redesigned switched-capacitor resistor DAC from the SAR-based BDC, to minimize mismatch effects. This design is utilised more efficiently to increase conversion speeds and expand the range of applications.

6.2 Contributions to state-of-the-art

The presented buffer-less bridge readout ADC designs were implemented in 65 nm CMOS technology. Instead of digitizing a low-voltage differential output signal from the Wheatstone bridge (WhB), a single-ended signal from a voltage divider output (built with a resistive sensor and a known resistor) is compared against a switched-capacitor resistor (SCR) DAC. In a manner similar to a WhB, two SCRs are tuned until the two resistor dividers' outputs are equal. The elimination of the sample-and-hold circuit significantly simplifies the sensor front-end. The input is connected directly to the comparator, creating a high impedance node, thus eliminating the need for the sensor to provide any charge or current, and removing the requirement for any input buffer in the signal path. These changes reduce the Wheatstone bridge to a simple resistor divider, requiring fewer external components, improving the power-to-area trade-off,

and enhancing flexibility with a wide input range of 830 mV, suitable for gas sensor applications. This work led to the following publications:

- A. Fordymacka and I. O'Connell, "A 0.01-mm^2 0.83-V Input Range SAR-Based Bridge-to-Digital Converter", IEEE Solid-State Circuits Letters, vol. 3, pp. 330-333, 2020, doi: 10.1109/LSSC.2020.3018427.
- A. Fordymacka and I. O'Connell, "A 0.01-mm^2 0.83-V Input Range SAR-Based Bridge-to-Digital Converter", Technical Paper, IEEE 47th European Solid-State Circuits Conference (ESSCIRC), Grenoble, France, 2021. (Virtual)

A counting-based BDC design eliminated traditional active gain elements, enhancing power efficiency and design simplicity. Furthermore, it reduced mismatches by using a single switched-capacitor resistor DAC. This work led to the following publication:

- A. Fordymacka, G. Salgado and I. O'Connell, "A Counting Based Bridge to Digital Converter Achieving a Walden FoM of 0.048 nJ/conv-step", 31st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Nancy, France, 2024.

System-level power efficiency was addressed by exploiting the slow-changing nature of gas sensor signals, minimizing conversion rates and the amount of output data needing further processing. This is achieved in the Threshold Detection ADC, which observes the input signal to ensure it stays within safety margins, allowing the microcontroller to remain in standby mode until an alarm occurs. Furthermore, this requires only one decision clock cycle, independent of the target resolution. This work led to the following publication:

- A. Fordymacka and I. O'Connell, "Threshold Detection ADC For Continuous Monitoring Applications," 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Lansing, MI, USA, 2021, pp. 571-574, doi: 10.1109/MWSCAS47672.2021.9531751.

6.3 Future Work

The completed work has revealed potential avenues for future research and commercial applications. The data converters presented are built upon each other, but monitoring applications could benefit from a hybrid data converter that combines both the SAR and threshold detection. In this approach, the input signal would be "trapped" between two thresholds until it surpasses a certain level. At that point, the input could be closely monitored using successive approximation. This design could ensure the system is power-efficient, generates only useful data, and can track the signal more effectively. To improve the conversion rate of the successive approximation, instead of providing the same number of EFM clock cycles for the DAC to settle during each approximation step, the number of cycles could scale down with the step amplitude difference.

Another important consideration is measuring the performance of the ADCs. The two implemented designs, the SAR-based BDC and the counting-based BDC, were limited by the way the output data was extracted from the chip. One design measured the output by directly observing the comparator, which had to be split into 12 bits. The other communicated through the on-chip I2C, where bandwidth constraints limited data capture. Incorporating memory into the system may improve future designs. This could simplify testing and provide on-chip history for applications.

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