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Behavioral Modeling of SAR ADCs in SIMULINK

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This paper presents a toolbox for the behavioral simulation of SAR ADCs in Simulink®. The models include the most limiting circuit effects such as sampled thermal noise, capacitor mismatch, finite settling, comparator noise and offset. A user friendly interface is also included to allow study and high-level design of SAR ADCs, which is illustrated by means of a design example. It is also shown that the proposed toolbox is several orders of magnitude faster than electrical simulators, while keeping a high accuracy.

Keywords— Analog-to-Digital Converters, SAR, Behavioral Modeling and Simulation.

I. INTRODUCTION

In recent years Successive-Approximation-Register (SAR) Analog-to-Digital-Converters (ADCs) have become the dominant low power ADC architecture [1]. Time Interleaved (TI) ADCs using SAR channels have also become the best performing ADCs at high frequencies with sampling frequencies up-to 90GS/s being reported [2]. The key building blocks of SAR ADCs are the capacitors, switches, state machines, and comparator latches. All of these blocks improve with CMOS process scaling leading to ADCs with lower power and faster speeds. The digital CMOS nature of these building blocks means SAR ADCs have minimal static power consumption and the ADC power consumption is proportional to the ADC conversion rate. As a sub-ADC advances in SARs have also enabled Hybrid ADCs with substantially lower power consumption than Flash based ADCs [3].

In spite of the above mentioned benefits, the efficient design of SAR ADCs requires using a suitable design methodology and CAD tools in order to maximize their performance with the minimum power dissipation. Simulation is a key tool supporting the design automation at different levels of the synthesis and verification flow. It is a common practice that SAR ADCs are simulated in electrical simulators with mixed-mode capabilities, like CADENCE® AMS-simulator. However, some important analog circuit limitations such as capacitor mismatch, finite settling time, and comparator noise, have forced the introduction of compensation techniques like calibration [4], redundancy [5], majority voting [6], noise-shaping [7], among others. These techniques are mostly implemented in the digital domain requiring extra conversion cycles, which might lead to long simulation times even at early stages of the design.

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A well-known alternative simulation approach is based on the so-called behavioral modeling technique, which has been previously applied to other kinds of ADCs, such as ΔΣ ADCs [8]-[9]. This approach essentially consists of emulating device and physical effects at a higher abstraction level, so that the simulation time can be drastically reduced in several orders of magnitude, while keeping a high accuracy compared to electrical simulation. However, to the best of the authors' knowledge, little work has been done in the behavioral modelling and simulation of SAR ADCs.

This paper contributes to this topic and presents a toolbox for the behavioral modeling and simulation of SAR ADCs in the MATLAB/Simulink® environment. The toolbox enables the simulation of SAR ADCs with two different Capacitive Digital-to-Analog Converter (CDAC) topologies by including their main circuit error mechanisms with a high level of accuracy and reduced CPU time as compared to electrical simulations. Additionally, a design example is presented to show the high capabilities and robustness of the proposed toolbox to quickly validate compensation techniques.

Following this introduction, the paper is organized as follows. Section II presents the proposed modeling of SAR ADCs, describing the behavioral models for the digital engine, CDAC and comparator. Section III gives an overview of the presented toolbox, which includes a Graphical-User-Interface (GUI) developed to guide designers through the different steps of the simulation. Section IV shows the high-level design flow of a 12-bit SAR, highlighting the capabilities of the toolbox. Finally, conclusions are drawn in Section V.

II. BEHAVIORAL MODELLING OF SAR ADCS

The working principle of SAR ADCs follows a successive digital approximation of the analog input voltage. To illustrate this process, consider the SAR ADC schematic shown in Fig. 1, which uses binary weighted CDAC, bottom plate sampling and unit capacitor c_u. The SAR-digital block is a state machine that controls all the conversion process. The first state is dedicated to the sampling of the incoming signal V_{in} onto the CDAC. In the second state, the SAR-digital connects the MSB-capacitor bottom plate to the positive reference, V_{rp}, and the remaining

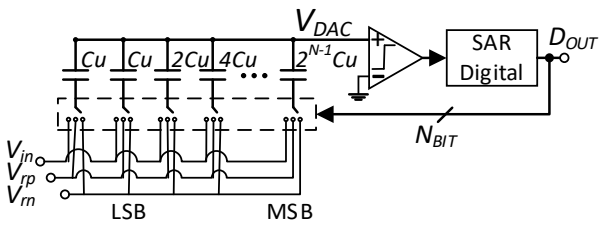


Fig. 1. SAR ADC Schematic.

capacitors to the negative reference, V_{rn}, and due to charge redistribution the V_{DAC} node converges to $-V_{in} + (V_{rp} - V_{rn}) / 2$. Before the second state ends, the comparator makes a decision whether V_{DAC} is above or below ground, setting the MSB-bit to '0' or '1', respectively. In the third state the bit trial process is repeated with the MSB_{-1}-capacitor, i.e. connecting it to V_{rp}, where V_{DAC} node now converges to $-V_{in} + (V_{rp} - V_{rn}) / 4$. The process continues through N-states for an N-bit ADC.

A. SAR-Digital engine

The SAR-digital engine can be easily modelled in the Stateflow® environment, where state machines are implemented with state transition diagrams and/or transition tables [10]. Fig. 2 illustrates the state transition diagram for a 4-bit SAR-digital (single-ended). The first state activates the sampling signal. In the second state the sampling signal is deactivated and D3 (MSB) is set to logic '1'. In the third state, D3 takes the value provided by the comparator ('0' or '1') and at the same time D2 is set to '1'. The process continues until the sixth state is reached, where the end-of-conversion (EOC) signal is activated. The resulting SAR-digital block can be used in Simulink® as a clock triggered unit, making possible the implementation of synchronous SAR ADCs. Note that a synthesizable Verilog/VHDL code can be also generated from the state transition diagram with the HDL-Coder [11].

B. Capacitive-DAC

The sampling control-signal generated by the SAR-digital can be used to trigger a sample and hold block and store the analogue input signal, as it is illustrated in Fig. 3. Real sampling networks introduce non-linear distortion and thermal noise [12]. The distortion is modelled with the general function block, which implements a polynomial expression of the form: $f(x) = a_1 \cdot x^1 + a_2 \cdot x^2 + \ldots a_i \cdot x^i$, where a_i corresponds to the *i-th* distortion term. On the other hand, thermal noise is originated due to random electron movement, so it can be modeled with a random number generator. It is assumed a normal distribution with zero mean value and a standard deviation given by the square-root of the well-known kT/C expression [12].

During the bit trials, different equivalent circuits around the V_{DAC} node are found. The general schematic shown in Fig. 4 provides a way to calculate the V_{DAC} node voltage as a function of the parallel-equivalent number of c_u connected to either v_{rp} or v_{rn}, c_{rp} and c_{rn}, respectively. Additionally, it can take into account parasitic capacitances associated to the top-plates, c_{tpp}, as described by:

$$V_{DAC} = \frac{c_{rp}}{c_{rp} + (c_{rn} + c_{tpp})} \cdot (V_{rp} - V_{rn}). \qquad (1)$$

Equation (1) can be implemented as a triggered MATLAB® function, where dynamic memory allocation can be used to make it configurable for any given number of bits. The bridge/split CDAC topology [4], also included in the presented toolbox, is modeled in a similar fashion.

To model process variations, every c_u is expressed as a normalized nominal value, i.e. 2, 4, 8 to 2^{N-1}, plus a given percentage deviation σ_{cu}. The deviation is a sample taken from an independent random number generator with a normal distribution and zero mean value.

Routing and finite on-switch resistance introduce *RC* time constants in the CDAC, leading to settling errors at the V_{DAC} output node. This limitation can be modelled as the step response of a first order RC circuit:

$$V_{DAC-st}(t) = V_{DAC} \cdot \left(1 - e^{-\frac{t}{\tau}}\right), \qquad (2)$$

where τ is the *RC* time constant. Equation (2) can be implemented with the Simulink block diagram shown in Fig. 5, where the error term is applied only to the current bit trial, i.e. assuming full settling from the previous state. The latter is a valid assumption given that CDAC continues its settling even during the comparator decision.

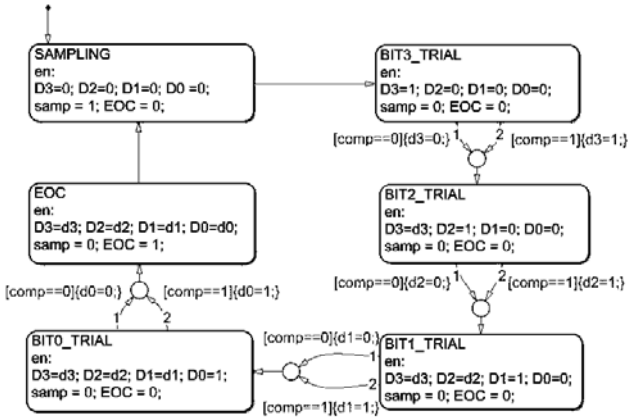


Fig. 2. State transition diagram of a 4-bit SAR-digital.

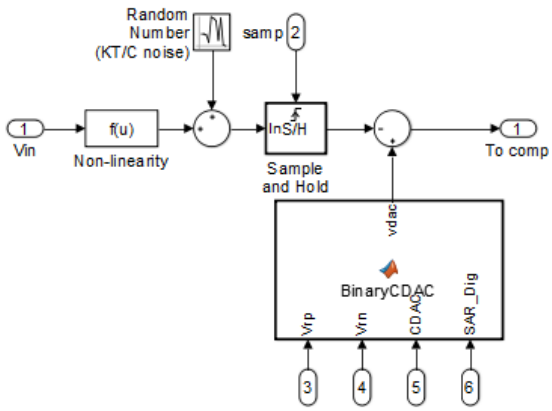


Fig. 3. Simulink CDAC Modeling.

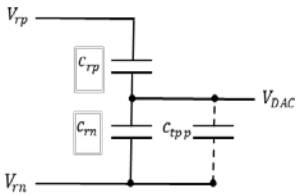


Fig. 4. Equivalent schematic for V_{DAC} generation.

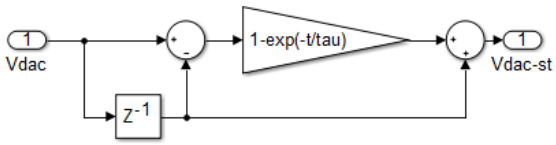


Fig. 5. CDAC finite settling modelling.

C. Comparator

Comparators implemented in SAR ADCs are typically made up of a high gain differential pair and a latch stage that stores the decision at the rising/falling edge of the clock signal. Fig. 6 illustrates the behavioral model of a fully differential comparator that emulates this circuit topology. $V_{DAC\text{-}N}$ is subtracted from $V_{DAC\text{-}P}$ and any possible DC-offset is modelled by the addition of a constant term, while the comparator input-referred noise is once again modelled by a random number generator. The compare block outputs '1' if its input is equal or lower than 0, and '0' otherwise. The latch effect is modeled with the sample and hold block.

III. Proposed SAR ADC Toolbox

A fully-differential SAR ADC model, built from the SAR-digital, CDAC and comparator models, explained in the last section, can be downloaded from [13][1]. The full model is accompanied by a GUI, in order to facilitate the study/design of SAR ADCs. The GUI, depicted in Fig. 7, allows the user to perform different ADC parametric analysis and to characterize main performance metrics such as DNL/INL, SNDR and ENOB. General ADC parameters such as, resolution, sampling frequency, input frequency and supply voltage, can be quickly set in the general parameters box. Under the CDAC parameters, the user can set the value for the sampling capacitor, mismatch, finite settling time, non-linear distortion term, and choose between binary or bridge CDAC. A dedicated comparator section allows users to set DC-offset and input referred noise, in LSB units. Additionally, the majority voting compensation technique described in [6] is also included, where the user can select the desired number of extra votes for the LSB_{-1} and LSB.

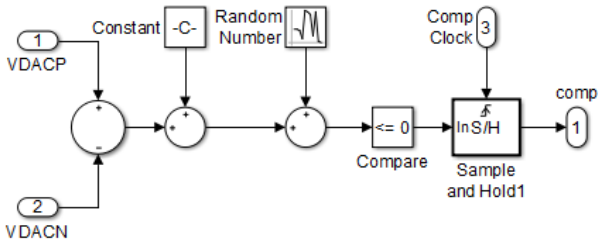


Fig. 6. Fully differential comparator model.

[1]The toolbox download link was not ready at the submission time. However, a copy of this can be requested to the main author.

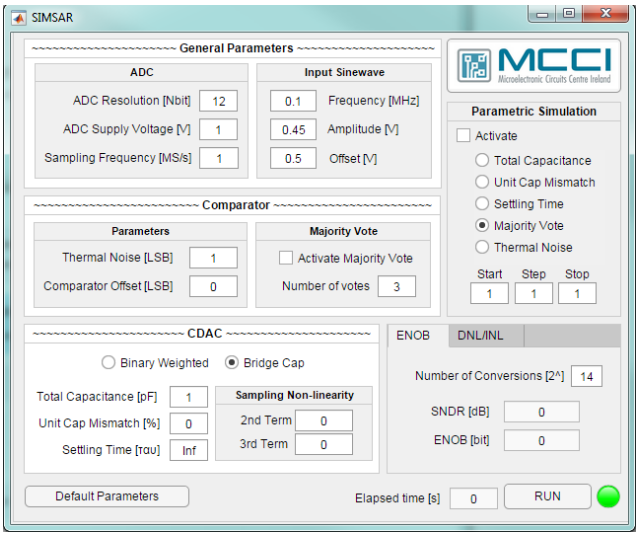


Fig. 7. Proposed toolbox' GUI.

The GUI source-code and Simulink models included in the toolbox can be easily modified to model additional features, e.g. the quantization error at the end of the conversion can be easily integrated and used as a comparator offset for the next conversion cycle, achieving the so-called noise shaping property [9]. Similarly, the full SAR ADC block can be easily used as the basic building block in time-interleaved ADCs, and/or hybrid architectures.

IV. Design Example and Performance Comparison

Consider the design of a 1.2V, 12-bit SAR. The high-level design flow is as follows. The first step is to identify the CDAC value necessary to achieve the targeted 73dB Signal-to-Noise-Ratio (SNR) at 1.2V supply. To this end, Fig. 8 shows the GUI results for the parametric analysis of CDAC, where it can be seen that 1pF represents a good trade-off between the target resolution and CDAC size.

The second step would be the analysis of the impact of the settling time over the DNL/INL metrics. As an illustration, Fig. 9 shows an extreme case where the time allocated for the settling

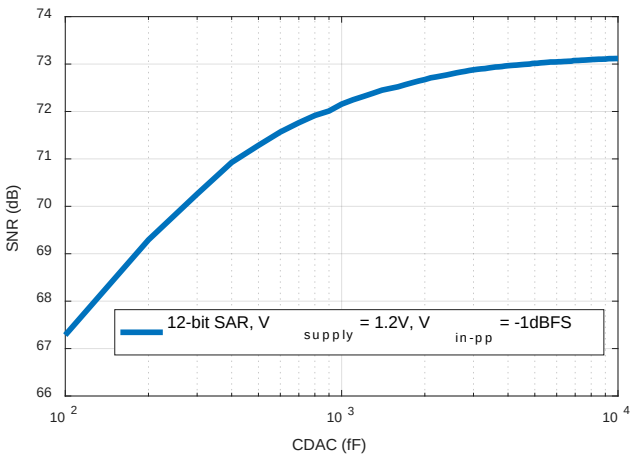


Fig. 8. CDAC parametric simulation.

is just 4.5τ, note that a larger error is introduced in the MSB transition, which reduces towards the LSB. A separate parametric analysis can be performed to identify the minimum number of RC time constants necessary to achieve a given DNL/INL, which is around 9τ for ±0.5LSB.

The third step in the design would be the mismatch sensitivity analysis trough Monte-Carlo simulations. To this end, it is first necessary to take a look at the targeted Process-Design-Kit (PDK) in order to identify the expected mismatch in the process. Fig. 10 shows a 200-run simulation considering σ_{cu} = 0.5% for both the binary weighted and the bridge CDAC. It is clear that the bridge CDAC shows higher sensitivity to process variations and must not be used unless lower mismatch is guaranteed. At this point an iterative process with the total size of the CDAC and σ_{cu} would start.

The final step is the analysis of the impact of the comparator noise, where a parametric analysis could be carried-out. However, at circuit-level, comparator noise is highly constrained by its power consumption budget. As an initial assumption the high-level designer can consider 1LSB as the comparator noise, and then reduce is noise figure using majority voting. As an illustration, Fig. 11 shows the parametric analysis for the number of extra votes, considering 1LSB of comparator noise. It can be seen that 5 votes represent a good trade-off between resolution and extra conversion states.

In summary, the designed 1.2V, 12-bit SAR ADC would need a 1pF binary CDAC, σ_{cu} = 0.5%, 9τ settling time allocation, 1LSB of comparator noise and 5 votes in the LSB_{-1} and LSB to achieve an effective resolution of 11.3bits.

A. *Simulation time performance*

In order to illustrate the simulation advantages of the proposed toolbox, the previously designed 12-bit SAR is simulated during 1024 conversion steps. A DELL PowerEdge C6145 running Linux Red Hat Enterprise Server 6.6 is used as the test hardware platform. Although it has multi-core capabilities, it has been software-limited to run in single-core. The toolbox runs in Matlab® 2016(b) and takes only 4s to complete the simulation. On the other hand, the equivalent transistor-level simulation in CADENCE® VIRTUOSO® IC6.17, with AMS-Simulator and SAR-Digital in Verilog, reports an elapsed simulation time in excess of 167ks (1d 22h 19m). The simulated SNR is the same in both cases, meaning that the proposed toolbox is 41750x times faster than the electrical simulator, while maintaining the same precision. Moreover, the schematic entry in the circuit simulator could take several days starting from scratch, while in the toolbox everything is implemented and ready to run.

V. CONCLUSIONS

A toolbox for the behavioral modeling and simulation of SAR ADCs in MATLAB/Simulink® has been presented. The effects of main building-block circuit nonidealities are included in the models, thus allowing to simulate SAR ADCs at system level with an accuracy comparable with electrical simulations. Moreover, the presented toolbox benefits from their implementation in MATLAB in terms of user-friendly signal processing capabilities and interface with circuit-design platforms.

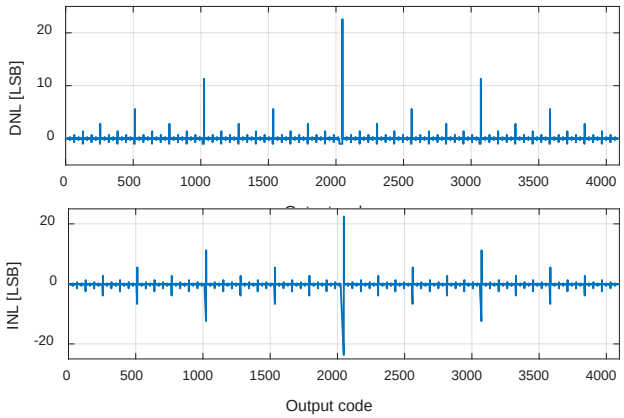


Fig. 9. DNL/INL plot with settling time allocation of 4.5τ.

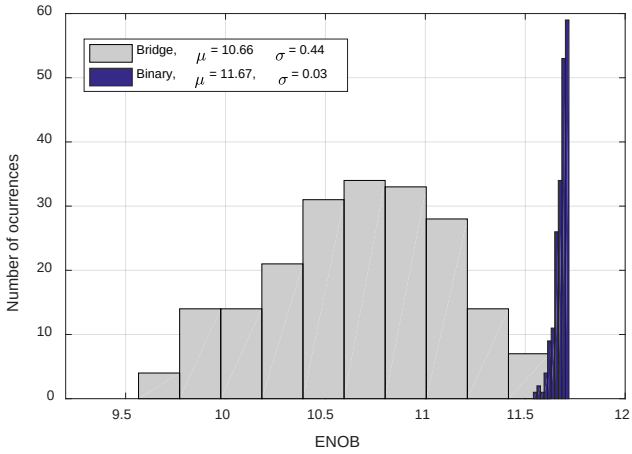


Fig. 10. Monte-Carlo simulation with σ_{cu} = 0.5%.

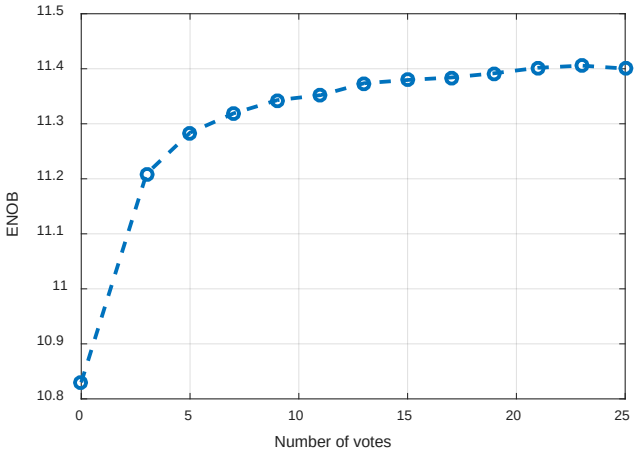


Fig. 11. Majority voting compensation.

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