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Investigating the transient response of Schottky barrier back-gated MoS_2 transistors

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Abstract. Molybdenum disulfide (MoS_2) MOSFETs have been widely reported to exhibit hysteresis behavior, which is usually attributed to charge trapping effects due to defective/sub-stoichiometric compositions in the material, or defects near, or at, the oxide/channel interfaces. It is also suggested that defective MoS_2 transistors show current limitations caused by the Schottky barrier junctions formed at the contacts. Here, we report on the static and dynamic device response of back-gated MoS_2 transistors directly fabricated on a SiO_2/Si substrate using chemical vapor deposition synthesis, without film transfer, and standard CMOS optical lithography. The devices exhibit an atypical hysteresis in the transfer characteristics, as well as a delayed response in the formation of the conducting channel in response to voltage pulses applied to the back gate. Analysis of the output characteristic is consistent with two back-to-back Schottky diodes, allowing the Fermi level pinning position at the Ni/MoS_2 source and drain contacts and blocking the MoS_2 hole channel. Capacitance-voltage characterization demonstrates that the grown MoS_2 thin film is p-type, resulting in a nominally-off, inversion mode, n-channel device. Analysis of the transient response and hysteresis as a function of device temperature, illumination and ambient conditions indicates that the dynamic response of the device is determined by the net charge in the MoS_2 film combined with the minority carrier generation lifetime in the underlying silicon substrate. The work demonstrates the strong dependence of the device response time on substrate, temperature, illumination, and net charge in the MoS_2 layer opening the possibility of applications in photo-detectors and sensors.

Keywords: Defects, hysteresis, MoS_2, Schottky barrier transistors, two-dimensional materials, reliability
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1. Introduction

The exfoliation of graphene, leading to the Nobel Prize in Physics in 2010 to A. Geim and K. Novoselov [1, 2], and the successful demonstration of molybdenum disulfide (MoS_2) field-effect transistor (FET) in 2011 [3] triggered a tremendous amount of research into two-dimensional (2D) materials. Due to the reduced thickness, these thin materials present an optimal electrostatic control of the channel providing better immunity to short channel effects than the planar silicon counterparts [4]. In addition, the wide variety of electronic and optical properties exhibited by thin semiconducting materials is also attracting interest in fields such as: photovoltaic cells [5, 6], supercapacitors [7, 8] or nanophotonics and quantum optics [9] are demonstrating a change towards to these promising options. Among the thin materials family, the transition metal dichalcogenides (TMDs) and especially MoS_2 present interesting properties like an indirect to direct bandgap transition as the film thickness is reduced from multilayer to monolayer due to quantum confinement and optical band gaps in the range of 1.2-1.8 eV [10], making them suitable for near-infrared absorption and emission with strong photoluminescence. Regarding electrical properties, according to the International Roadmap for Devices and Systems (IRDS) guideline [11], TMDs devices present advantages in terms of higher on/off ratios, enabling reduced power consumption, current leakage and good switching delay with respect to silicon devices.

Fundamental physics and devices on 2D TMDs have relied on the exfoliation method due to the high crystalline quality of natural and synthetic crystals. However, the critical limitations of the flake dimension and film uniformity have restricted its development beyond the fundamental studies. Scalable application of atomically thin TMDs requires wafer-scale deposition of films with well-controlled properties. Vapor deposition techniques have been most extensively explored due to their potential for high scalability and morphological control. Chemical Vapor Deposition (CVD) has emerged as the growth method used to produce large-area TMD films suitable for research and industrial purposes. However, the experimental results rarely accomplish the promising theoretical properties for these 2D materials. Since Novoselov *et al*. [2] demonstrated very poor properties in few-layer MoS_2 FETs (e.g. mobility of 0.53 $cm^2V^{-1}s^{-1}$), different strategies have been developed to overcome the device limitations: Dielectric engineering has been proposed to suppress Coulomb scattering and reduce the impact of Schottky barriers [12, 13, 14, 15, 16]; metal contact engineering [17, 18] and surface and defect engineering [19, 20] to improve the contact resistance and the Schottky barrier limitations or pulsed voltage measurements to achieve current hysteresis reduction [21]. In addition, material doping [22, 23, 24, 25], fabrication advances by atomic layer deposition [26], lithography alternatives [27] and double gate architectures [28, 29, 3] have been proposed as well. Unfortunately, despite these advances, defects and impurities (grain boundaries, corrugation, sulfur vacancies, oxygen incorporation, moisture molecules and oxide ions) still play an important role on the actual drop in performance of the fabricated devices. Predominantly, defects have demonstrated the influence of Schottky barriers underneath the contact pads by pinning the metal Fermi level [17, 18]. Additionally, depending on their energy positions inside the bandgap, defects can act as either donors or acceptors centers near the conduction and valence bands, or as generation-recombination centers (R-G) if they are located near the mid-gap energy. The presence of these defects, and their associated energy levels, can dominate the device performance. In this regard, it has been commonly reported that the effect of defects in exfoliated MoS_2 results in a n-type behavior [30]. The resulting devices are junctionless [31] accumulation mode n-channel MOSFETs [32, 33, 34, 35, 29] which usually present high power consumption limitations due to the normally-on characteristic.

In addition to defects which yield n- and p-type dopants in MoS_2, a number of papers have reported hysteresis in the transfer characteristics of MoS_2 channel MOSFETs, which is attributed to electron trapping and emission from oxide defects and interface or surface states [33, 36, 37, 35, 32, 38]. Hysteresis analysis have been carried out demonstrating carrier tunneling through oxide defects for the anti-clockwise behaviors [39] and trapping/detrapping of carriers in oxide and at the interface defects for clockwise operations [33], both with reversible effect. Other works have demonstrated the implication of the traps in the photoconductivity of these devices [34]. Theoretical and modeling works have also been addressed to shed light on these instabilities [40, 41, 42, 43]. However, due to the huge amount of variables (synthesis precursors, growth conditions, insulating and substrate materials, processing metals and annealing options) the limiting mechanisms and the defect implications on the performance and reliability of the device are as yet not entirely understood.

In this work, we report on the static and dynamic response of back-gated MoS_2 transistors, where the MoS_2 is grown by CVD directly on SiO_2/Si substrate and the devices are fabricated using standard lithography and etching without MoS_2 films transfer. Following an analysis of the static device characteristics, the hysteresis and transient response

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of the back-gated MoS_2 MOSFETs are reported. The results highlight the role of MoS_2 charged defects, and the silicon substrate, in the the hysteresis and transient response of the back gated MoS_2 MOSFETs.

2. Results and discussions

2.1. Structural characterization

The direct synthesis of large-area MoS_2 films on a n-type silicon substrate covered by a 100 nm-thick SiO_2 layer was accomplished *via* CVD through sulfurization of molybdenum trioxide (MoO_3) at a maximum temperature of 680 °C (see Methods for details). An optical image of the resultant deposition is provided in Figure 1.a. The CVD-grown MoS_2 and the SiO_2 substrate are easily distinguishable. Figure 1.b depicts the Raman spectrum of the MoS_2 layer excited by a 532 nm line laser at ambient conditions. The MoS_2 film exhibits two Raman characteristic bands at 387 and 410 cm^{-1}, corresponding to the in-plane (E^1_{2g}) and the out-of-plane (A_{1g}) modes, respectively. The difference of the peaks (Δ) remains between 21-23 cm^{-1} across the MoS_2 layer which is consistent with the presence of thin MoS_2 layers [44, 45, 46, 47]. These values are larger than expected for monolayer MoS_2 (18-19 cm^{-1}) [44, 45], but smaller than the typical value for bulk MoS_2 (26 cm^{-1}) [46], suggesting few-layer MoS_2. Additionally, the Raman spectrum presents a peak centered around 450 cm^{-1}. This controversial peak can be assigned to the combinations of different contributions [45]: i) One corresponding to the double frequency of the LA(M) mode (227 cm^{-1}) [47], attributed to disorder-induced Raman scattering or due to an increased level of partial oxidation on the MoS_2 samples [48]; ii) the first-order optical phonon peak A_{2u} which involves asymmetric translations of both Mo and S atoms in the c-axis direction [49, 50]; and, iii) the Raman peak D which can be ascribed to Mo-S vibrations for oxysulfide species [51]. The bands are attributed to bridging Mo-S-Mo species for reduced molybdenum compounds or Mo^{6+} oxysulfide species [51, 45]. X-ray photoelectron spectroscopy (XPS) analysis was used to measure binding energies of molybdenum (Mo, Figure 1.c) and sulfur (S, Figure 1.d) atoms. Figure 1.c shows two broad peaks positioned at around 229.2 eV and 232.3 eV, which correspond respectively to the main doublet Mo $3d_{5/2}$ and Mo $3d_{3/2}$ ($3d_{5/2}$:$3d_{3/2}$ ratio of 0.66 and a spin-orbit splitting of 3.10 eV) of Mo^{4+} chemical state [52, 53]. Also, a minor peak observed at 226.3 eV is attributed to S 2s component. S 2p peaks at 161.9 eV and 163.1 eV (Figure 1.d) are ascribed respectively to spin orbits of S $2p_{3/2}$ and S $2p_{1/2}$ ($2p_{3/2}$:$2p_{1/2}$ ratio of 0.5 and a spin-orbit splitting of 1.2 eV). These results are in good agreement with the reported binding energy values for MoS_2 [54]. Moreover, smaller contributions at around 235.3 and 234.0 eV coincide with the binding energy typically assigned to Mo^{6+} and Mo^{5+} oxidation states that correspond to the possible deposition of MoO_3 in the CVD synthesis process and/or the presence of suboxides species and S vacancies [55, 53, 56]. The Mo^{6+} and Mo^{5+} peaks found would indicate that some oxygen is incorporated in the grown MoS_2 film [57, 58, 59, 53], which was also demonstrated with the Raman results aforementioned. These results suggest the presence of defects distorting the stoichiometry of the synthesized MoS_2 films.

The determination of the thickness of the fabricated devices is carried out after the etching process through an atomic force microscopy (AFM) analysis. Figure 1.e. depicts the structure of the well-defined MoS_2 channel where triangular-shape MoS_2 domains are observed on the top layer. The AFM image reveals a MoS_2 channel of approximately 3 nm of height. Other devices along the sample have been characterized presenting similar thicknesses in agreement with Raman results. The structural studies have been complemented with a scanning electron microscope (SEM) characterization to verify the device homogeneity, the physical dimension of the channel and the effectiveness of the etching process. Figure 1.f corroborates a homogeneous channel and contacts.

2.2. Electrical characterization

2.2.1. Transistor characterization

Regarding the performance of the fabricated devices as field-effect transistors, Figure 2.a shows the transfer characteristic (I_{DS}-V_G) of a back-gated MoS_2 device with channel dimensions of 25 μm length and 25 μm width in logarithmic (left axis) and linear (right axis) scales, at different drain biases (grounded source). These curves reveal a clear n-type operation with close to 0 V threshold voltages, V_{TH} (corresponding to low density of fixed charges). According to the Schottky-Mott theory [60, 61, 62], for a defect-free Ni/MoS_2 interface, and the case where the MoS_2 is undoped with the Fermi level near mid gap, the expected barrier height should be close to zero, as $\Phi_{Ni} = 5.1$ eV and $\Phi_{MoS_2} = 5.05$ eV (electron affinity $\chi_{MoS_2} \approx 4.4$ eV and $E_g/2 \approx 0.65$ eV in a non-intentional doped material [63, 64]). This barrier height should, in theory, facilitate an ambipolar transfer characteristic [17]. However, in novel materials like 2D or III-V channel devices, it has been widely reported that the barrier height is a less sensitive function of Φ_M than expected in Schottky-Mott theory due to the effect of surface states at the interface between the semiconductor and the metal [17, 63, 18]. Furthermore, density functional calculations have confirmed that the metal-MoS_2 interaction pins the Fermi level at

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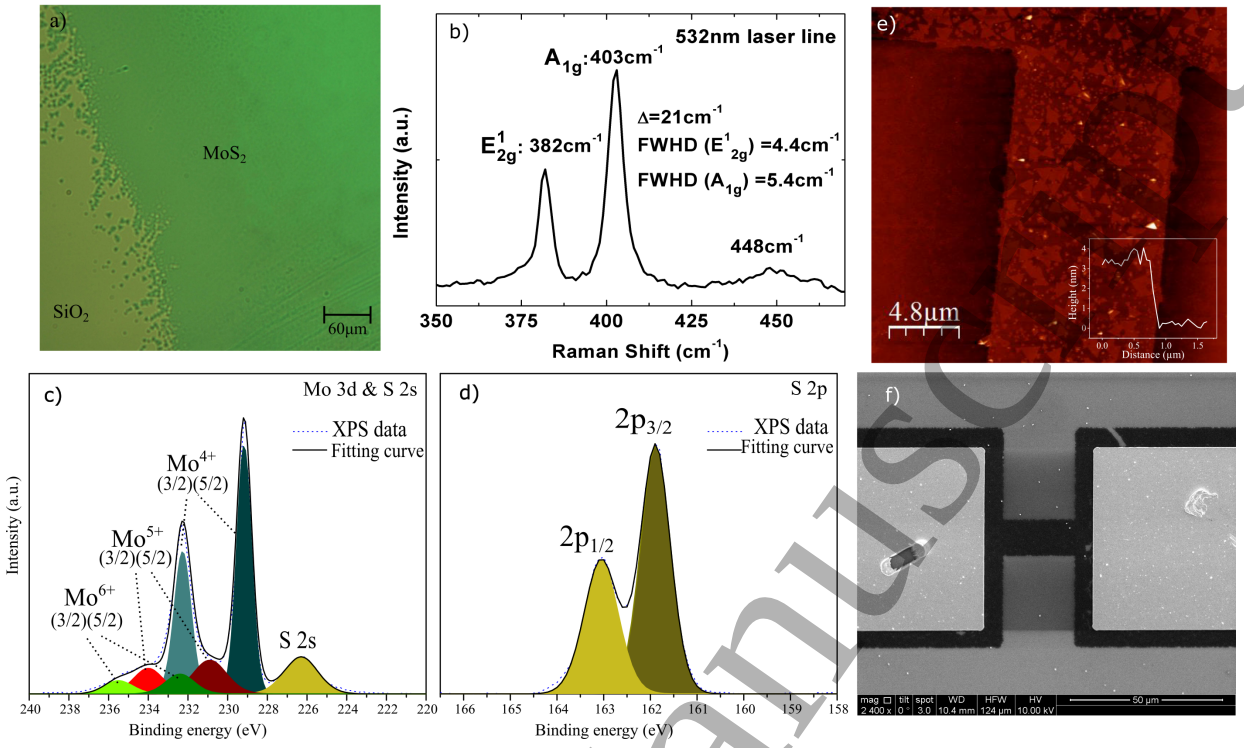


Figure 1. a) Optical image of a MoS_2 layer grown on a SiO_2/Si substrate. b) Raman spectrum of the MoS_2 layer using a 532 nm line laser at atmospheric conditions. c) and d) high resolution XPS spectra of Mo and S peaks. e) Atomic force microscopy image of a continuous $L = 25\ \mu m$ and $W = 10\ \mu m$ MoS_2 channel device. Inset: height profile of the MoS_2 channel. f) Scanning electronic microscopy image of a $L = 25\ \mu m$ and $W = 10\ \mu m$ back-gated device. Scratches observed in the contact pads are due to the electrical probe contact during the electrical characterization process.

0.1-0.3 eV below the conduction band edge of the semiconductor [65]. This Fermi level pinning has been attributed to the basic metal-MoS_2 interface physics [66]. The absence of ambipolar operation is therefore attributed to the suppression of hole current by the Schottky barriers. Figure 2.b shows the transfer characteristic for transistors presenting different physical dimensions on the same sample. Transconductance ($g_m = \partial I_D/\partial V_G$) is depicted in the right y-axis. Interestingly, g_m follows a monotonic increasing trend with no saturation due to channel series resistance. This observation should be attributed to the Schottky barrier narrowing by increasing the vertical field which implies a more probable tunneling for electrons from the contacts to the channel. Note that the dependence of the threshold voltage on the drain bias in Figure 2.a could also have its origin in the Schottky barrier [63]. A considerable device-to-device threshold voltage variability can also be inferred from Figure 2.b. Concerning this point, standard electrical parameters are presented in the Supplementary Material to allow comparison with other devices. Figure S1.a shows the threshold voltage variability for several devices with different physical dimensions with no clear trend as a function of the width or length. The field-effect mobility (μ_{FE}) is shown in Figure S1.b as a function of the physical dimensions for a fixed overdrive voltage ($V_{OV} = V_G - V_{TH} = 15$ V). The highest mobility of the characterized devices corresponds to $\mu_{FE} = 2.35\ cm^2V^{-1}s^{-1}$, which is comparable to the values typically reported for CVD grown MoS_2 devices in literature [67]. Finally, the subthreshold slope and the sheet resistance are depicted in Figure S1.c and S1.d, respectively. From the experimental extrapolation, material resistivity $\rho \approx 8.5\ \Omega.cm$ and contact resistance $R_C \approx 4.75$ MΩ are extracted ($V_{OV} = 5$ V and $V_{DS} = 0.1$ V).

2.2.2. Schottky barrier characterization

To investigate the Schottky barriers formation, Figure 2.c depicts the drain-source current-voltage characteristic of a 50 μm-length and 45 μm-width device in absence of back-gate bias (black square symbols). The curve shows a clear non-Ohmic rectifying behavior with exponential growing current at negative voltages confirming the formation of Schottky barriers in the metal-semiconductor junctions. To clarify this effect, the schematic illustration for two Schottky contacts in equilibrium condition resulting in two back-to-back junctions and considering a pinned metal work function is shown in Figure 2.d. According to the energy band diagram, the current through the

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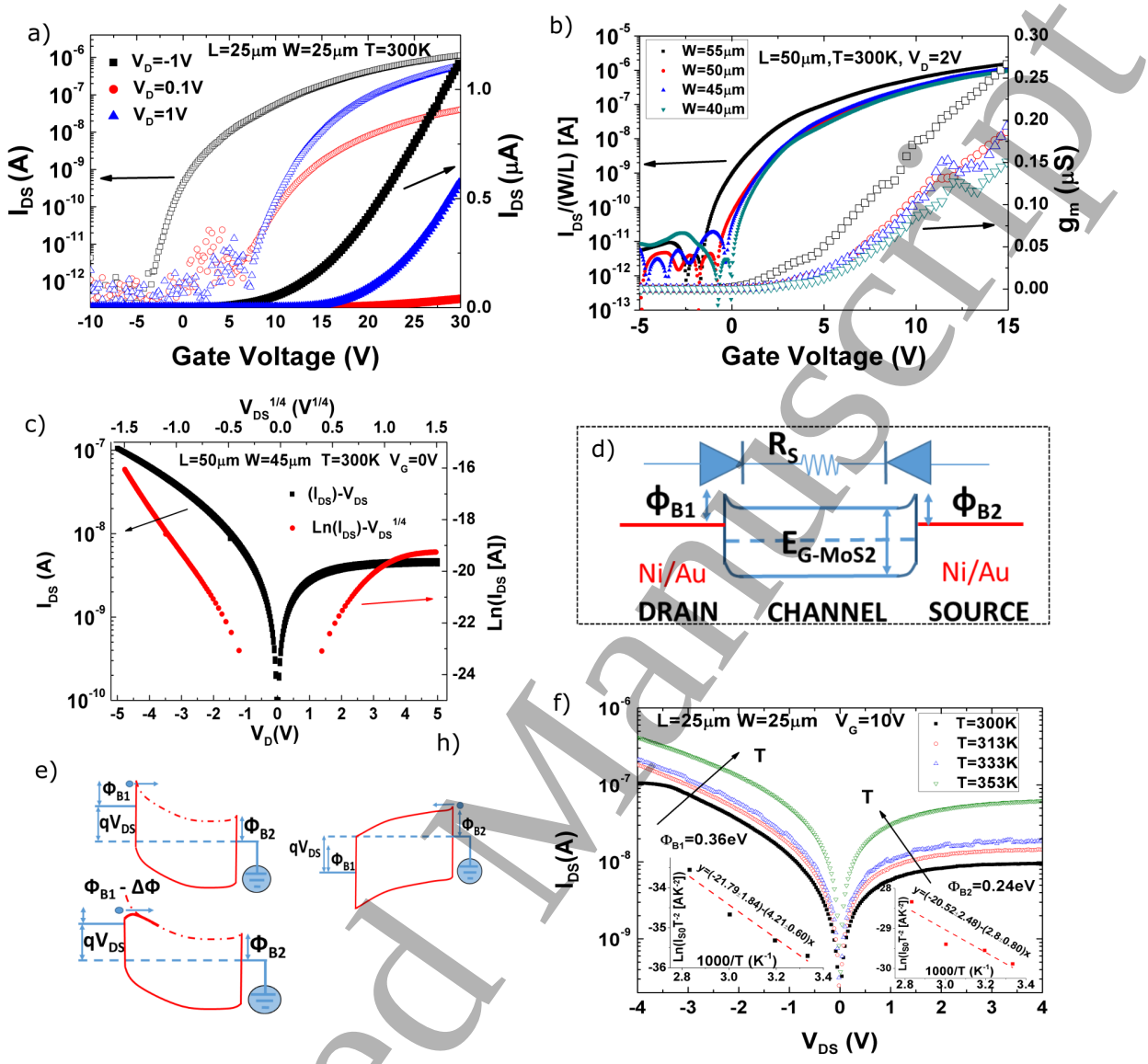


Figure 2. a) Transfer characteristic (I_{DS}-V_G) in logarithmic and linear scales for different drain biases. b) Transfer characteristic for different physical dimensions and the extracted transconductance (g_m). c) Output characteristic of a device with grounded gate bias ($V_G = 0$ V) in two different representations, I_{DS}-V_{DS} (black) and $ln(I_{DS})$-$V_{DS}^{1/4}$ (red). Drain currents I_{DS} are presented in absolute value. d) Schematic illustration of the device modelled by two back-to-back diodes and a channel resistance. e) Energy band diagram of the Schottky diodes under negative (top-left) and positive (top-right) drain biases. Energy band diagram when accounting the image force lowering effect under negative drain bias (bottom). Arrows indicate the electron flow. f) I_{DS}-V_{DS} behavior at different temperatures. The insets depict the fitting for the barrier heights extraction.

device will be limited either by the Schottky diodes or the corresponding channel series resistance. Energy band diagrams based on the two back-to-back Schottky barriers with negative and positive drain biases are presented in Figure 2.e (forced and grounded contacts are considered as drain and source, respectively). It is worth mentioning that regardless of the sign of V_{DS}, one of the Schottky diodes will always present a reverse configuration. Figure 2.e (top-left) depicts the case for negative drain bias. Under this condition, the drain/MoS_2 junction is biased in reverse while the MoS_2/source is in forward configuration (for electrons). The opposite case is presented in Figure 2.e (top-right), where a positive drain bias sets the MoS_2/drain junction in forward condition while the source/MoS_2 is in reverse. As observed, electrons have to overcome the corresponding reverse bias junction barrier in each case. According to the thermionic-emission theory [62], the current in a reversed Schoktty diode junction should saturate at the value:

$$I_0 = AA^{**}T^2 exp(\frac{-q\Phi_B}{kT}) \quad (1)$$

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where A is the contact area of the junction, A^{**} is the Richardson constant for thermionic emission, q is the magnitude of the electron charge, Φ_B is the Schottky barrier height, k_B is the Boltzmann constant and T is the temperature. This fact explains the behavior of the device when a positive voltage is forced: Although the drain/MoS_2 junction is forward biased, the current is limited by the reversed source/MoS_2 diode, Figure 2.d. However, this assumption cannot explain the current-voltage dependence observed at negative drain biases (Figure 2.c), neither considering the forward nor the reverse contributions of the diodes involved (in forward operation, the current should follow a linear fit with drain bias). Nevertheless, a departure from the ideal behavior can be explained by image force lowering effect [62, 63]. Increasing the reverse junction bias induces a reduction of the Schottky barrier and the current does not saturate but increases proportionally to $exp(q\Delta\Phi_B/kT)$, where $\Delta\Phi_B$ is the barrier lowering due to image charges. Energy barrier diagram taking into account this effect is depicted in Figure 2.e (bottom). Under these conditions, the corresponding value of $\Delta\Phi_B$ follows a $\Delta\Phi_B = \alpha V^{1/4}$ expression, where α is a constant depending on the donor/acceptor concentration and the relative dielectric constant of the material [63]. Figure 2.c demonstrates a linear dependence of $ln(\mathrm{I}_{DS})$ as a function of $V^{1/4}$ (red circle symbols), corroborating the barrier lowering effect at negative drain biases. This effect has also been observed in recent works on MoS_2 devices [63]. Therefore, the current through the device is limited by the reversed biased junction between the drain and the MoS_2 channel following the lowering barrier height effect at the negative drain biases and by the reversed biased junction between the source and the MoS_2 channel when the drain is positively biased. The current during the $\mathrm{V}_{DS} > 0$ V operation is saturated by the reversed junction and weakly affected by image force due to the absence of reversed bias in this interface (source is grounded) and the long distance to the drain ($L = 45$ μm). This fact is confirmed by reversing the contact configuration (not shown). Including the image force lowering effect, the reverse current under negative applied voltages can be expressed as [63]:

$$I_{DS} = AA^{**}T^2 exp[\frac{-q}{k_B T}(-\Phi_B + \alpha\sqrt[4]{V_{DS} - R_S I_{DS}})] \quad (2)$$

where α is a dimensional constant and R_S the series resistance of the channel.

To determine the height of the barriers, the Schottky diode behavior is characterized at different temperatures and low gate biases, Figure 2.f. According to the Equation 2, I_{DS0} values ($I_{DS}(V_{DS} = 0$ V)), calculated for zero-bias extrapolation at different temperatures, should follow a trend as $ln(I_{DS0}/T^2) = ln(AA^{**}) - (q\Phi_B/k_B T)$ when negative drain voltages are applied, Figure 2.f. The barrier Φ_{B1} can be extracted from the linear dependence [63]. According to the fitting in Figure 2.f (left inset), the barrier height value for this specific device is $\Phi_{B1} = 0.36$ eV for the reversed drain bias. In the case of a positive V_{DS}, the barrier which limits the current corresponds to the reversed source-semiconductor junction. This barrier height can be directly extracted from the reversed saturated current according to Equation 1, being for this specific device $\Phi_{B2} = 0.24$ eV (Figure 2.f, right inset). As Figure 2.c (bottom) depicts Φ_{B1} corresponds to the barrier height before subtracting the barrier height lowering effect. Therefore, the resulting barrier height corresponds to Φ_{B1}-$\Delta\Phi_B$ should be lower than Φ_{B2} according to the higher current for negative biases observed in Figure 2.c and Figure 2.f.

So far, the thermionic-emission has been considered as the main transport mechanism under these conditions of temperature and bias, statement which is validated by the fit of the experimental current (Figure 2.c) to the thermionic emission model (Equation 1 and Equation 2). Due to the absence of intentional doping (low acceptor/donor concentrations) and room temperature conditions, the contribution of other phenomena such as field or thermionic-field emission is discarded [62]. However, lowering the temperature or increasing vertical fields, these phenomena contribute to the transport mechanism. Figure S1 in the Supplementary Material (Section Schottky barrier characterization) validates that the main mechanism at room and higher temperatures is thermionic-emission while at low temperatures and at high gate biases thermionic-field emission contributes considerably to the current.

2.3. Device Instability

The $I_{DS} - V_G$ double sweep (forward/backward) characteristic of the same 50 μm-length and 45 μm-width device as in Figure 2.c is shown in Figure 3.a for different drain biases. A hysteresis cycle can be observed regardless of the selected drain bias. However, this reported behavior does not fit with the usual clockwise hysteresis, attributed to carrier trapping in MoS_2 devices [32, 33, 34, 35]. The observed crossing point in the hysteresis suggests an additional mechanism taking place in the carrier transport (not a pure clockwise or anti-clockwise behavior is observed). Figure 3.b shows the same operation when increasing the delay time between sweep points, implying longer sweep times. The shortest sweep time (black square symbols) presents the same behavior as the previous device: a cross point in the hysteresis. However, when increasing the delay time, the cross point disappears and pure clockwise hysteresis is observed. A zoom-in of the cross region is presented in the inset of Figure

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3.b.

To shed light on this unusual behavior, Figure 3.c shows the transfer characteristic at different temperatures. At relatively low temperatures (black squares and red circles), the drain-source current presents the mentioned crossing behavior, *i.e.* I_{DS} increases with V_G and it continues rising even when the voltage sweep changes the direction and decreases from the maximum (V_G = 30 V). This unexpected behavior suggests that the threshold voltage is being shifted to negative voltages or carrier injection is still taking place. However, this behavior is not permanent. During the reverse sweep at around $V_G \approx$10 V (at T = 255 K), the current suddenly drops crossing the value of the forward sweep and finishing the reverse sweep with a higher threshold voltage than for the forward sweep direction (arrows indicate the sweep direction). When increasing the temperature, the cross point is shifted upward and disappears at room temperature, where hysteresis presents a purely clockwise operation. Therefore, the crossing effect observed in the hysteresis is originated by a thermally activated mechanism. A detailed analysis of the temporal characteristic of the current as a function of temperature at high vertical field is presented in Figure 3.d. Note here the bias conditions and that the voltage step is applied at t = 0 s. In this representation, the contribution of the two competing mechanisms is inferred: i) An initial phenomenon showing a temporal current level increment and ii) a second one which is responsible for a current level decay. These two mechanisms explain the crossing effect in the hysteresis depending on the sweep time: for sweep times shorter than the time needed to reach the maximum current at a given temperature and bias condition (τ), the first mechanism prevails and devices show anti-clockwise hysteresis (not shown). However, if the sweep time is long enough to allow both mechanisms to take place, the hysteresis shows a cross point once the first mechanism ends (crossing effect in Figure 3.c). Finally, if the sweep time is long enough, the second mechanism will prevail over the first and devices will show clockwise hysteresis (higher temperatures in Figure 3.c). Due to the temperature dependence of the first effect, the hysteresis also depends on the temperature. Despite the origin of this initial effect not being clear, the second phenomenon causing a temporal current decay and a clockwise operation has been widely reported in MoS_2 devices [32, 33, 34, 35]. This effect is usually attributed to charging/discharging of carriers through oxide [33, 68] or interface traps [69]. In case of oxide traps, these are traps located within a few nanometers from the interface and thus can follow the change in the applied voltage by tunneling exchange with the channel. Illustratively, when a forward gate bias is applied, the traps whose energy levels are below the Fermi level are filled by electrons with different characteristic times. The trapped electrons contribute to the increase of negative charge (reduction of positive charge considering donor traps) and therefore, increase the threshold voltage. A schematic representation is shown in Figure 3.e, where oxide and intrinsic traps are taken into account. This effect can be partially or totally recovered by applying a negative voltage to the gate according to Figure 3.f. These observations are consistent with the behavior predicted by theoretical modeling [33, 68, 70]. These defects are associated with both extrinsic (diffused water molecules and the chemisorption of oxygen [71]), which can be desorbed at high temperatures or under vacuum conditions, [33, 32] and intrinsic defect at the interface due to oxygen and sulfur vacancies, or even defects due to a non-passivated surface bonds of the MoS_2 [72].

On the other hand, the phenomenon occurring at the initial times, competing at lower temperature and causing the cross effect is not common. The mechanism presents a clear thermal activation signature (Figure 3.d) suggesting a Shockley-Read-Hall (SRH) mechanism involved. Carrier tunneling through oxide defects or thermal activation of oxide ions have been reported for the anti-clockwise behaviors [39]. However these effects can be discarded in this work due to the negligible gate current and the reduced implication of the phenomenon by increasing the temperature, opposite to the expected behavior when taking into account the thermally activated oxide ions. Another possible explanation could consist in a slow generation of carriers in the channel at the initial times, low intrinsic carrier density or even carrier injection limitations to the channel through the Schottky barriers at source and drain.

To further analyze this initial effect, devices are characterized under microscope white light conditions. Figure 4.a shows the response of the device to a sequence of successive positive gate voltage pulses (up to V_G = 20 V) starting from a negative bias ($V_G = -10$ V) (Figure 4.a, top). As observed, (Figure 4.a, bottom) the black curve depicts the behavior previously reported, an initial current increase followed by the expected current decay once the trapping effect dominates. However, under microscope white light conditions (red line), this first phenomenon is suppressed and only the characteristic decay, attributed to the trapping/detrapping phenomena, is observed. Successive pulses present lower current due to the overall threshold voltage shift to positive voltages (the recovery periods at $V_G = -10$ V are shorter than the stress periods at V_G = 20 V). The same behavior is observed in the $I_D - t$ characteristic at two different temperatures in Figure 4.b. The exposure

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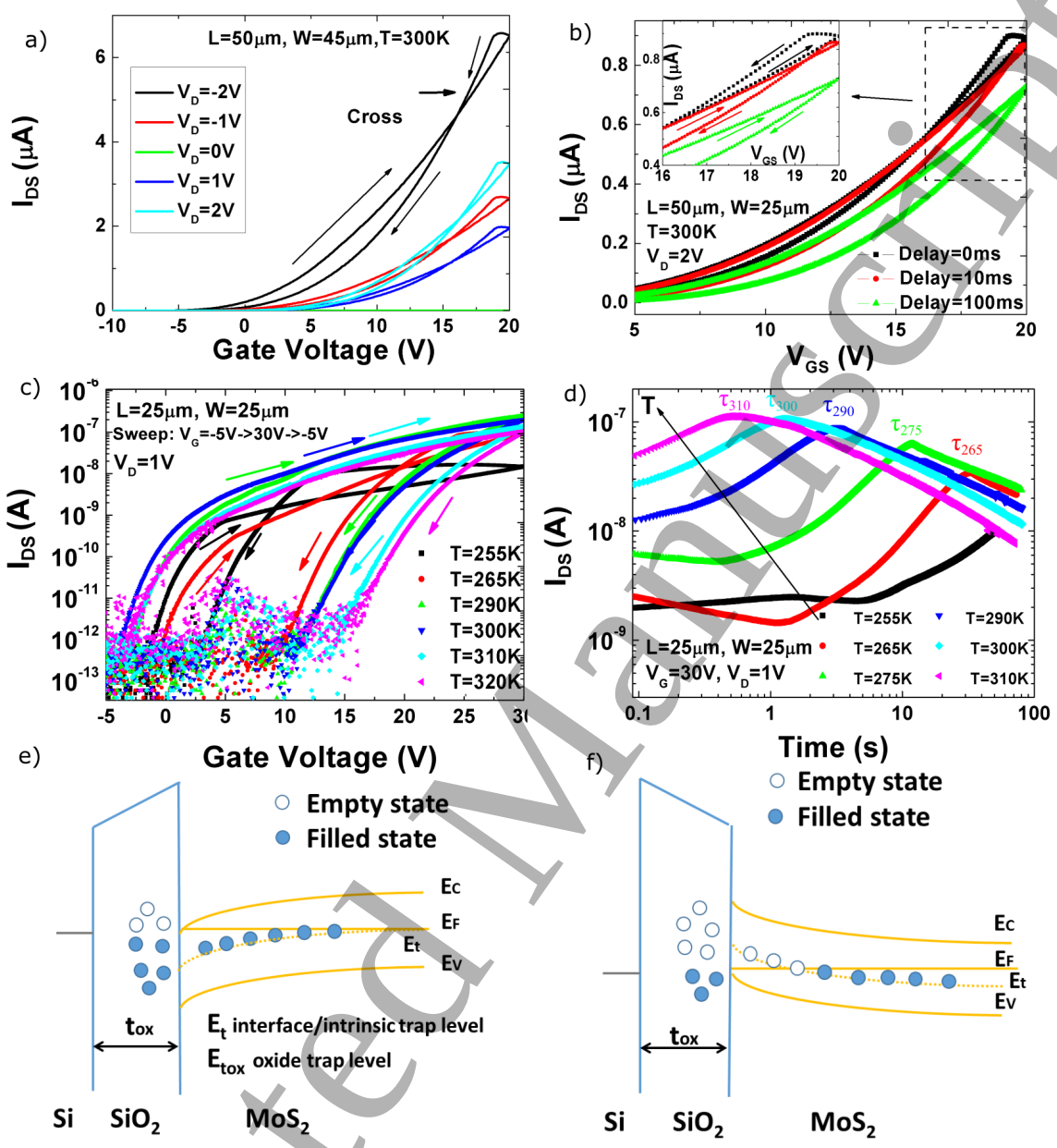


Figure 3. a) Transfer characteristic (absolute value) with double sweep (forward and backward) of a 50 μm-length and 45 μm-width device for different drain biases. b) Transfer characteristic for another device with a 50 μm-length and 25 μm-width as a function of the sweep delay time. Inset shows a zoom-in of the cross point area. c) Current hysteresis for different temperatures. d) I_D-t characteristic when a positive gate voltage pulse is applied at $t = 0$ s at different temperatures for the same device as in c). Energy diagram scheme of the trap behavior: e) When a positive voltage is applied at the back-gate. The bending of the energy bands allows traps (in the oxide and at the interface) to be filled with electrons once they are below the Fermi level; f) when a negative voltage is applied, the energy band bending makes electrons to escape from the traps.

to the light can generate electron-hole pairs when the energy of the light is larger than the semiconductor band-gap. The photogenerated excess of electrons can directly contribute to the current presenting a faster response to the voltage rise. This fact points to difficulties in the formation of the channel as the origin of the aforementioned initial current increase.

Capacitance-voltage (C-V) characterization is performed in order to gain further insight into the particular origin of the delay in the electron channel formation. This characterization is carried out directly on the fabricated MOSFET devices ($Si/SiO_2/MoS_2$),

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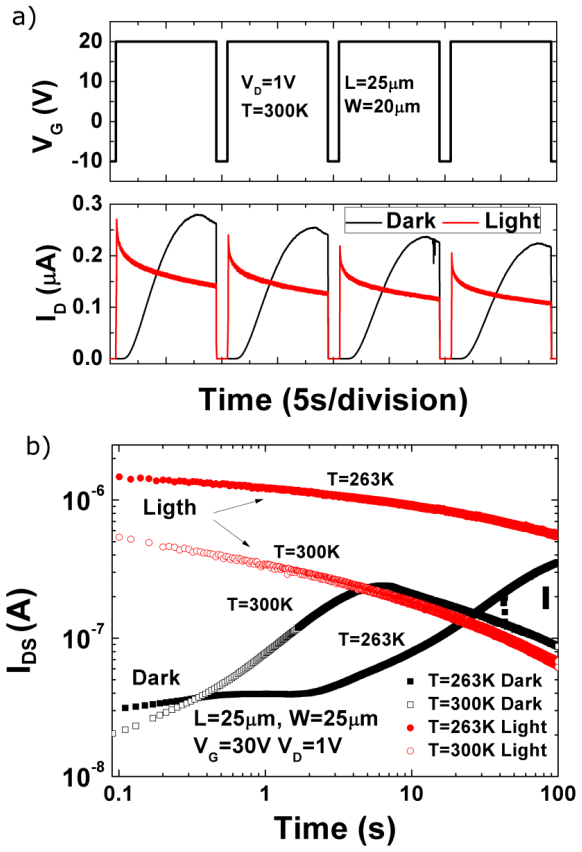


Figure 4. a) Gate voltage pulsed response under dark and illumination conditions. b) Comparison of the I_D-t characteristic at high gate voltage for dark and illumination conditions at different temperatures.

where the force and low biases are applied at the Si substrate and at the drain contact, respectively (Inset Figure 5.a). Figure 5.a shows the gate capacitance measured through the structure at low temperature. Two frequencies (low, f = 1 kHz, and high, f = 1 MHz) are recorded both for double voltage sweep measurements. The structure presents a clear accumulation channel, a depletion region and almost no inversion channel corresponding to the electron carriers (positive voltages at the back gate). It should be noted that the measured maximum capacitance (C_{ox} = 1.24 pF) agrees with the theoretical oxide capacitance value (C_{ox}) according to 100 nm-thick SiO_2 oxide and the area of the contact. The maximum capacitance at high frequency occurs for negative biases at the substrate (Figure 5.a), suggesting that the majority carriers are holes at the MoS_2/SiO_2 interface and electrons at the SiO_2/Si interface (in agreement with the n-type Si substrate). However, according to Figure 5.a, when positive voltages are applied at the back gate, the device is not able to form the inversion charge following the bias signal. This result could be initially in agreement with the time associated to form an inversion layer of holes at the he Si/SiO_2 interface. Due to the n-type doping characteristic, holes have to be thermally generated, a slow process taking into account a highly crystalline Si layer. To form the inversion channel, minority carriers must be thermally generated in the space-charge region (SCR) of the junctions and minority carrier generation lifetimes are manifestly longer than majority ones, presenting a slow generation rate and limiting the inversion charge response [73]. Note here that any of the two interfaces could impose the operation limit under these considerations, but initially the high quality n-type silicon substrate should present higher minority carrier lifetimes than the defective MoS_2 layer. If the source of the initial instability in the devices is the thermal generation of minorities, this effect can be relaxed by increasing the minority carrier density through higher temperature (n_i increases) or photo-generation conditions (photo-generated minority carriers). C-V characterization performed under microscope white light and high temperature conditions shown in Figure 5.b and Figure 5.c, respectively, validates this statement demonstrating that the photo (Figure 5.b) or thermal (Figure 5.c) generation enhance the inversion charge increasing the minority population. According to these results, the slow formation of the inversion layers, which requires time to thermally generate minority carriers, explains the initial current delay (current increase with time). Therefore, the observed current delay in the devices (τ in Figure 3.d) can be related to the inversion layer formation (minority carrier should be thermally generated). Section Device instability in the Supplementary Material demonstrates that this delay is governed by a SHR mechanism with an energy activation of 0.64 eV above the valence band suggesting thermal generation of minorities through generation-recombination of electron-hole pairs thanks to states in the mid-gap state. Moreover, the measured τ values (Figure 3.d) agree with the expected response time for minorities carriers in this doped silicon layer according to $\tau = \tau_g \cdot N_A/n_i$ [74], where $N_D = 10^{15}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3} and τ_g between 10^{-3} s and 10^{-4} s for this specific doping level at room temperature [75].

The I_D-V_G and C-V responses suggest that due to the limitation of high Schottky barriers blocking the holes current, the device should operate in inversion-mode. Therefore, an electron channel should be formed entailed by the thermal generation of the minority carriers at the Si/SiO_2 interface (holes). It is worth mentioning that due to this combination of phenomena the behavior of these devices corresponds to back-gated Schottky barrier field-effect transistors (SB-FET) operating with inversion channel rather

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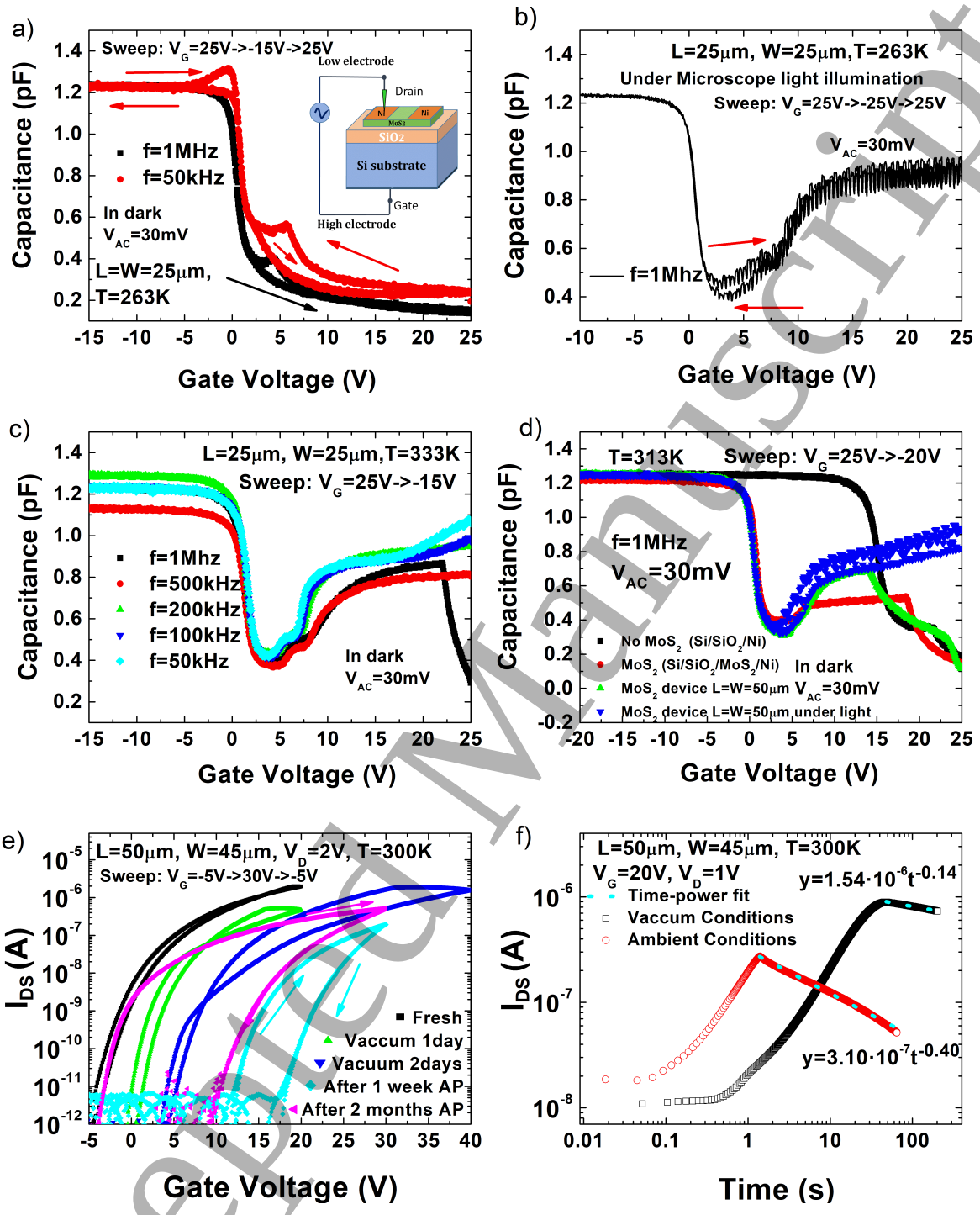


Figure 5. a) Capacitance-voltage (C-V) characteristics for two frequencies at low temperature and under dark conditions. b) C-V characteristic under microscope white light. Arrows indicate the sweep direction. c) C-V characteristic at high temperature under dark conditions. The black curve (the first measured) still presents an initial delay to reach the inversion layer. d) C-V characteristics for different structures with and without MoS_2 layer on top under different light conditions at 313 K. e) Transfer characteristic of one fresh device, under vacuum and in atmospheric pressure (AP). f) I_D-t characteristic of the device in vacuum and air conditions.

than the usual n-type transistors (junctionless), widely reported in literature, presenting accumulation-mode operations [63, 69, 35, 32, 76, 17, 30]. Moreover, this operation ensures normally-off devices with potential less power consumption than the normally-on ones, typically presented in literature.

However, due to the intriguing structure with two semiconductor interfaces further corroborations

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should be carried out. Figure 5.d shows the C-V characteristic of one reference structure without MoS_2 layer (in the same sample). As expected, the structure (Metal/SiO_2/n-type Si) presents a clear n-type behavior with accumulation, depletion and almost no inversion. Note that the high potential (Inset in Figure 5.a) is applied at the silicon gate, therefore the curve should be reversed. These results agree with the previous calculations with a high frequency CV obtained for frequencies above $1/\tau$ ($\approx$ from 0.01 Hz to 0.1 Hz). However, the depletion of the substrate is reached at more positive voltages than in the devices presenting the MoS_2 layer, Figure 5.b and Figure 5.c. This fact points to the different charge density at the surface below the contacts. In this regard, when the MoS_2 layer is presented, red curve in Figure 5.d, the depletion regime shifts to the left. Interestingly, higher inversion is observed in this case. This change in the C-V characteristic suggests additional mechanisms inducing unusual inversion channel at this high frequency (1 MHz). This effect is even clearer for a typical device with MoS_2 channel (Figure 5.d green curve). In this case, the maximum inversion capacitance is higher but the initial time τ to reach this capacitance level (attributed to thermal generation of minorities) is still present. As expected, if a source of artificial light is applied (blue curve), the minority carrier density increases and the thermal generation is not necessary to achieve the maximum inversion capacitance which is approximately the same as in dark conditions. Therefore, the MoS_2 layer has an important role on the response of the device where, despite the limitation that the silicon layer imposes, the maximum inversion capacitance reached is controlled by the MoS_2 layer. One possible explanation for this unexpected inversion level that the devices present at high frequency could reside in the charges and defects in the MoS_2 layer (as demonstrated in the structural characterization) and at the top interface (not passivated). It is reported that inducing surface charge of the same type as the silicon doping (negative in this case of n-type substrate), it will induce a corresponding charge opposite sign in the semiconductor at the oxide/Si interface and will give rise to an inversion region in the peripheral area (called peripheral inversion) [77]. The presence of an inversion layer in an area outside the region defined by the gate, provides a source of minority carriers to the inversion region in the area defined by the gate, with a resulting ac inversion response, which does not originate from the generation of minority carriers. This effect is expected if the surface charge is higher than the semiconductor charge associated with the maximum depletion width, $\approx 8 \cdot 10^{10}$ cm^{-2} for 10^{15} cm^{-3} Si substrate doping concentration [77], charge densities which within the range expected for a defective MoS_2 layer as suggested in the structural characterization. Moreover, this surface charge value could be in agreement with the calculated charge for the V_{FB} shift of 15 V ($\approx 10^{12}$ cm^{-2}) observed in Figure 5.d when the MoS_2 layer is presented in the structure. The other possible explanation for the observed inversion capacitance behavior is the formation of the electron channel in the MoS_2 layer being the limiting phenomenon in the device operation. It means that the MoS_2 layer also has to generate minority carriers (electrons) at the MoS_2/SiO_2 interface, presenting a p-type behavior. However, due to the reported defective characteristic of the MoS_2 in these devices, shorter carrier minority lifetimes than in silicon are expected and therefore faster response. Despite this, it is worth noticing that if a perfect peripheral inversion is achieved in the silicon, the limiting factor should be the electron carrier generated in the MoS_2.

To study the influence of the surface charge density on the device operation, Figure 5.e shows the transfer characteristic under different ambient conditions. When the device is under vacuum conditions, the hysteresis cycle is narrower because, while the initial time in the formation of the channel prevails, the carrier trapping phenomenon at interface decreases, suggesting a reduction of active defects. However, once the device is under atmospheric pressure (AP), the second phenomenon takes over and a wider clockwise hysteresis appears. Figure 5.f shows the temporal comparison with the I_D-t curves in both under atmospheric pressure and vacuum conditions corroborating the surface charge density effect. The decay part of the curve falls more abruptly (higher power exponent) on the device exposed to atmospheric pressure than under vacuum conditions due to the presence of higher active trap density. This part of the curve fits perfectly with a time power law observed in silicon transistors which is attributed to hydrogen and other species diffusion generating oxide and interface states [33, 78, 79]. In MoS_2 devices, this widely reported behavior has been attributed to the trapping of carriers at interface and oxide defects produced by dissociative adsorption of oxygen on the defective surface of MoS_2, moisture at room conditions and oxide species together with sulfur vacancies in the structure. However, the decreasing of active defects (and surface charges) under vacuum condition makes that the rising part of the curve takes more time to reach to the maximum current level (τ). This effect is consistent with less charge density at the surface resulting in a weaker peripheral inversion at the Si/SiO_2 interface and longer time to reach the same inversion charge density. Note that the higher current presented under

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vacuum condition is due to the lower threshold voltage.

Final corroboration of the influence of the defects on MoS_2 top surface and at MoS_2/SiO_2 interface on the operation and performance of the back-gated devices is demonstrated by fabricating and characterizing another sample grown under a slightly different synthesis process on the same Si substrates (additional synthesis data in the Supplementary Material). This sample presents a more defective MoS_2 layer where higher density of imperfections in the channel are easily discernible in the SEM characterization (Figure S4). The comparison with the previous sample also suggests a thinner MoS_2 layer (AFM profile, not shown). Figure 6.a shows the same pulses characterization as in Figure 4.a demonstrating shorter initial delay in this more defective sample. This result is consistent with higher charge density on the surface inducing higher peripheral inversion level at the Si/SiO_2 interface. Additionally, capacitance-voltage

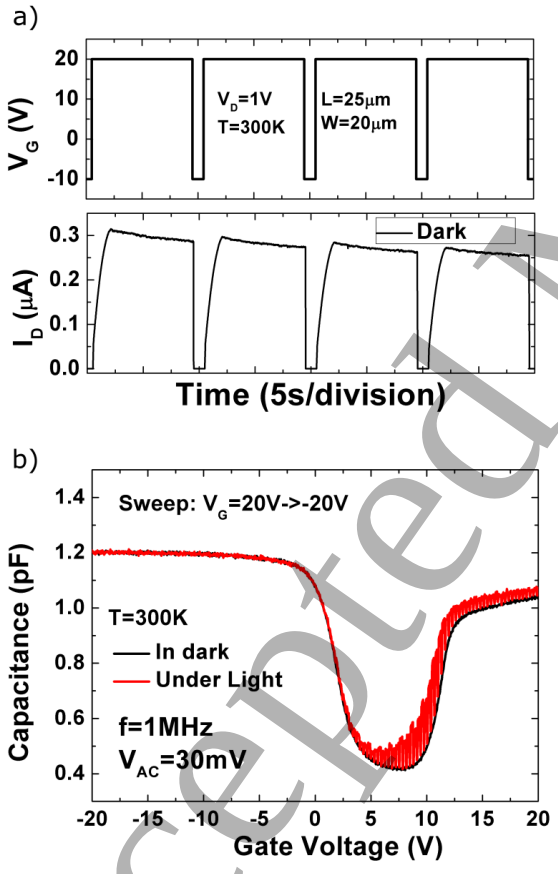


Figure 6. a) Gate voltage pulsed response under dark conditions for a more defective MoS_2 device. b) Capacitance-voltage (C-V) characteristics at room temperature under dark and microscope white light conditions (same device as shown in Figure 6.a).

characteristic of the same sample (Figure 6.b) presents a clear inversion channel even at room temperature and higher frequency. The capacitance in the inversion regime presents almost no differences between illuminated and not illuminated characterizations and the values are higher compared to the thicker MoS_2 device (Figure 5.c). A comparison is shown in Figure S5. These results indicate that the magnitude of the capacitance in inversion is not limited by thermal generation of minority carriers in the silicon, but is provided by a peripheral source of inversion charge (see inset Figure 5.a) at the Si/SiO_2 interface. The density of this inversion charge at the Si/SiO_2 interface is set by the negative charge density associated with the overlying MoS_2. This density of charge in the MoS_2 (bulk and surface) can vary from sample to sample, and also varies with the ambient conditions (as shown in Figure 5.f).

As a final remark, the results described in this work highlight that these devices present: i) a Fermi level pinning at the metal/MoS_2 interface which blocks the hole current resulting in an n-channel behavior in the transfer characteristic; and ii) a net p-type structure which requires the formation of an electron channel due to the inversion of the interfaces, entailed by the thermal generation of minority carriers and/or the a supply of minority carriers in an area peripheral to the contacted area. In this process, the defect density and sign in the defective MoS_2 and at the surface of MoS_2 (not passivated) play an important role in the formation of the channel. However, the thermal generation of minority carriers in the silicon layer can still delay the channel formation modulating the current hysteresis in the device which is also affected by the trapping/detrapping of carriers. The fact that isolated mechanisms such as the trapping/detrapping phenomena, peripheral inversion and the thermal generation of minority carriers affect the current in these devices opens the way to modulate the device to operate in a mode which utilizes one or more of the mechanisms responsible for the transient response depending on the intended application. The results suggest that a relatively slow response which is strongly dependent upon light and temperature could be achieved with passivated and/or by non-defective MoS_2 devices. Photo-detectors and temperature sensors could be the potential applications. On the other hand, inducing negative charges on the surface, improves the channel inversion resulting in faster response. Such devices can also operate as bio or gas sensors. From the electronic point of view, the current device, made with large-area grown MoS_2 films, have demonstrated normally-off operation with potential low-power consumption and with electrical parameters such as mobility, on/off ratio and on-resistance comparable to reported parameters in literature.

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3. Conclusions

The results in this work demonstrate that CVD grown MoS_2 MOSFETs can present a combination of a net p-type MoS_2 and Fermi level pinning at the metal/MoS_2 interface of the source and drain regions, where the pinning level is located in the upper half of the MoS_2 energy gap. These combined effects result in a nominally-off MOSFET, which requires the formation of a n-type inversion region for the on-state condition. In this condition, the MoS_2 MOSFET illustrates a complex time dependent and hysteresis response which is determined by the net charge in the MoS_2 film, the trapping/detrapping effects and the minority carrier generation lifetime in the underlying silicon substrate. In this process the defects in the MoS_2 play an important role determining both the time to generate the n-type inversion layer in the MoS_2 and the current decay due to carrier trapping. The connection of the net charge in the MoS_2 to the device response time to a gate voltage pulse, occurs because the charge density and type in the MoS_2 determines the corresponding charge density in the underlying silicon substrate. If the charge in the MoS_2 is negative, it creates a corresponding positive (inversion charge for n-type silicon) in the substrate, which can reduce, or potentially eliminate the time taken to form an inversion layer in the silicon, and also influences the hysteresis behaviour of the MOSFET. This interpretation is consistent with measurements under microscope white light, and increasing temperate, which both show a marked reduction in the device response time. Finally, measurements under vacuum and in air conditions demonstrate a marked change in the response time of the MoS_2 MOSFETs, consistent with the ambient impacting on the net charge density in the MoS_2 layer through interaction with oxygen, moisture and absorbates on the MoS_2 surface. Additionally, different samples have demonstrated that the device transient response following the application of a gate pulse is controllable by the defect density and by the MoS_2 growth parameters opening the door to engineer these mechanisms for specific target applications such as light-detector, gas or bio sensors.

Methods

3.1. Synthesis of MoS_2

Chemical vapor deposition through sulfurization of molybdenum trioxide (MoO_3) using elemental sulfur was carried out. The synthesis process for the MoS_2 growth was as follows: two alumina crucibles, one containing 0.6 mg of MoO_3 (Aldrich 99.5) and one containing 0.3 g of sulfur powder (Alfa 99.5) were placed in a quartz process tube (2 inch diameter). The quartz tube was introduced into a two-zone furnace (PlanarTech) placing the sulfur crucible upstream and the MoO_3 downstream. The substrate (10^{15} cm^{-3} n-type doped silicon covered by a 100 nm-thick thermal grown SiO_2 layer) was first cleaned with an IPA rinse followed by a piranha etch (three parts sulfuric acid to one part hydrogen peroxide) for 1 h. The pressure was set to 1 Torr during all the process. A flow of argon gas was initially used to purge the tube (300 sccm) for 20 min at room temperature and then 15 min to 150 °C in the MoO_3 stream. Afterthat, the argon flow was reduced to 100 sccm and the downstream and upstream furnaces were heated to 680 °C and 160 °C, respectively, as measured by a type-K thermocouple at the outer surface of the process tube. Growth time was 5 min for the MoS_2 film synthesis. Subsequently, the upstream furnace was turned off and the downward one was naturally cooled to 540 °C in 10 min followed by a fast cooling to room temperature in argon ambient.

3.2. Device Fabrication

Firstly, the sample was spin-coated with standard lift-off and image resist, and photo lithography was employed to define the source and drain patterns. Then, electron beam evaporation was used to deposit the Ni/Au electrodes. The thicknesses of the Ni and Au were 20 nm and 200 nm, respectively. A lift-off process was carried out to complete contact fabrication of the MoS_2 FET. Then, a new resist layer was deposited and a dry etching of the MoS_2 material outside the channel between S/D contacts was carried out. Finally, the resist mask was removed.

3.3. Experimental

The elemental composition analysis was carried out by fundamental X-ray photoelectron spectroscopy (XPS, Kratos Axis Ultra- DLD). Scanning electron microscope (SEM) characterization was performed in a FEI Quanta FEG 650 under high vacuum (0.1 mB) conditions using using an ETD (Everhart-Thornley Detector) for secondary electrons-topography. Raman spectra was obtained thanks to a Jasco NRS-5100 employing a 532 nm laser to excite the samples. A laser power of 4.4 mW with 30 s of exposure time with 5 accumulations were applied during the measurements. The topography and thickness of the MoS_2 samples were characterized using an atomic force microscope (NTMDT NTEGRA) in semicontact mode and with metallic tips. The air conditions electrical characteristics were measured in a semiautomatic Suss PA200 probe station with temperature capability. The low temperature characterization under vacuum conditions was carried out in cryogenic Lake Shore

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Janis ST-500 probe station working with liquid nitrogen. The dc characteristic were recorded using a Keithley SCS 4200 and an Agilent B1500 systems. The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were performed using either an Agilent 4294A or CV enabled B1500 LCR meter (MFCMU).

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Supplementary Data

Supplementary material for this article is available online.

4. ORCID iDs

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