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Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in $In_{0.53}Ga_{0.47}As$ capacitors

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This work looks at the effect on mid-gap interface state defect density estimates for $In_{0.53}Ga_{0.47}As$ semiconductor capacitors when different AC voltage amplitudes are selected for a fixed voltage bias step size (100 mV) during room temperature only electrical characterization. Results are presented for $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ metal–oxide–semiconductor capacitors with (1) *n*-type and *p*-type semiconductors, (2) different Al_2O_3 thicknesses, (3) different $In_{0.53}Ga_{0.47}As$ surface passivation concentrations of ammonium sulphide, and (4) different transfer times to the atomic layer deposition chamber after passivation treatment on the semiconductor surface—thereby demonstrating a cross-section of device characteristics. The authors set out to determine the importance of the AC voltage amplitude selection on the interface state defect density extractions and whether this selection has a combined effect with the oxide capacitance. These capacitors are prototypical of the type of gate oxide material stacks that could form equivalent metal–oxide–semiconductor field-effect transistors beyond the 32 nm technology node. The authors do not attempt to achieve the best scaled equivalent oxide thickness in this work, as our focus is on accurately extracting device properties that will allow the investigation and reduction of interface state defect densities at the high-*k*/III–V semiconductor interface. The operating voltage for future devices will be reduced, potentially leading to an associated reduction in the AC voltage amplitude, which will force a decrease in the signal-to-noise ratio of electrical responses and could therefore result in less accurate impedance measurements. A concern thus arises regarding the accuracy of the electrical property extractions using such impedance measurements for future devices, particularly in relation to the mid-gap interface state defect density estimated from the conductance method and from the combined high–low frequency capacitance–voltage method. The authors apply a fixed voltage step of 100 mV for all voltage sweep measurements at each AC frequency. Each of these measurements is repeated 15 times for the equidistant AC voltage amplitudes between 10 mV and 150 mV. This provides the desired AC voltage amplitude to step size ratios from 1:10 to 3:2. Our results indicate that, although the selection of the oxide capacitance is important both to the success and accuracy of the extraction method, the mid-gap interface state defect density extractions are not overly sensitive to the AC voltage amplitude employed regardless of what oxide capacitance is used in the extractions, particularly in the range from 50% below the voltage sweep step size to 50% above it. Therefore, the use of larger AC voltage amplitudes in this range to achieve a better signal-to-noise ratio during impedance measurements for future low operating voltage devices will not distort the extracted interface state defect density. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4774109]

I. INTRODUCTION

The scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) has been advanced in recent years with the introduction and optimization of high dielectric constant (high-*k*) gate oxide materials on silicon in conjunction with the metal replacement of doped polysilicon gate electrodes,[1,2] As scaling progresses beyond the 45 and 32 nm nodes, replacement of the silicon semiconductor channel material for an advanced gate stack is likely to improve the performance in future planar and nonplanar MOSFET architectures.[3] Compound semiconductor material systems such as $In_{0.53}Ga_{0.47}As$ are under investigation for their suitability to replace the silicon semiconductor as a result of their high electron mobility.[4] Detrimental scattering of electrons due to the presence of a high interface state defect density (D_{it}) at

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the high-k/$In_{0.53}Ga_{0.47}As$ interface is a major issue.[5,6] Significant advances have been made in recent times[7–9] at reducing the large and dominant mid-gap D_{it} in $In_{0.53}Ga_{0.47}As$ semiconductor MOS capacitors[10] (MOSCAPs) with sufficient effect to achieve band-to-band (unpinned) Fermi level movement, and this progress has been successfully transferred to equivalent material MOSFET devices.[11]

As further development and optimization of the high-k/$In_{0.53}Ga_{0.47}As$ interface continues, an accurate estimate of D_{it} is important to ensure performance enhancements can be predicted and achieved in resulting MOSFETs. An as yet open issue for these systems is the influence of the AC voltage amplitude parameter selection on the D_{it} extraction for AC impedance-based capacitance–voltage (CV) and conductance–voltage (GV) measurements at AC frequencies ranging from 20 Hz to 2 MHz.[12] The conductance method (CM),[13,14] and the combined high–low frequency capacitance-voltage method (HL),[14] manipulate some or all of the CV/GV data to obtain the D_{it} estimates and we assess these two methods in this work for selected oxide/$In_{0.53}Ga_{0.47}As$ systems.

Such admittance spectroscopy applied carefully to both Si (Ref. 15) and $In_{0.53}Ga_{0.47}As$ (Ref. 10) MOS devices has been effective to the present day in different material systems for extracting greater understanding of interface defects. Maximizing the AC voltage amplitude improves the signal-to-noise ratio (SNR), but continued transistor scaling reduces the operating voltage which necessitates a smaller voltage step size during electrical characterization. It would be reasonable to expect increased error and/or variability in the measurements as the voltage step size becomes comparable to, and less than, the AC voltage amplitude since this could reduce the SNR significantly. Therefore, we assess the effect of such changes on devices that are both the basis for, and the prelude to, functional III–V semiconductor MOSCAPs and MOSFETs.

II. EXPERIMENTAL DETAILS

This work looks at six samples in total, **S1–S6**, which are summarized in Table I. The full experimental details of (i) **S1**, **S2**, and **S4** are provided in Ref. 16, (ii) **S3** in Ref. 9, and (iii) **S5** and **S6** are identical to **S3** with the exception of the oxide thickness (~12 nm instead of ~8 nm) and the fact that **S6** is p-type.

All epitaxial $In_{0.53}Ga_{0.47}As$ semiconductor layers were grown by metal-organic vapor phase epitaxy (MOVPE) on heavily doped ($\sim 2 \times 10^{18}$ cm^{-3}) InP(100) substrates. Samples **S1**, **S2**, and **S4** had back contacts of Ti/Au (for the p-type sample) and Au/Ge/Au/Ni/Au (for the n-type samples), followed by a 30 s rapid thermal anneal (RTA) at 623 K in N_2. Samples **S3**, **S5**, and **S6** had no back contact formation as series resistance effects were deemed to be negligible.

All $In_{0.53}Ga_{0.47}As$ surfaces were initially rinsed for 1 min each in acetone, methanol, and isopropanol, prior to immersion in $(NH_4)_2S$ diluted in deionized H_2O (20 min, 295 K). The Al_2O_3 layers were grown by atomic layer deposition, using alternating pulses of trimethylaluminum ($Al_2(CH_3)_6$) and H_2O. Samples were loaded into the atomic layer deposition reactor within either 3 or 7 min exposure to ambient after removal from the $(NH_4)_2S$ solution. Top metal depositions were either by shadow mask (SM) or by a lithography lift-off (LO) process. Metal–oxide–semiconductor capacitors were formed with a variety of areas and shapes. A short summary of the material system details is provided in Table I, and further details can be found in Refs. 9 and 16.

III. ANALYSIS TECHNIQUES

First, we must consider the estimation of the oxide capacitance. The oxide capacitance (C_{ox}) is derived from Eq. (1),[14] where a dielectric constant (k) of ~8.6 is used for the Al_2O_3 oxide deposited by ALD,[17] and ε_0 is the permittivity of free space.

We assess only Al_2O_3 in this study because of its potential use as an intermediate k-value oxide to form a stable interface control layer between other high-k oxides (e.g., HfO_2) and $In_{0.53}Ga_{0.47}As$ that exhibit poor interfaces with high interface state defect densities.[18–20] A SiO_x interlayer is generally found for transition metal binary high-k oxides (e.g., HfO_2) on silicon.[21]

C_{ox} is directly inversely proportional to the oxide thickness (t)

$$C_{ox} = \frac{k\varepsilon_0}{t} = \frac{8.6 \times 8.85 \times 10^{-12}}{t} \quad \{F/m^2\}. \tag{1}$$

The oxide capacitance values derived from Eq. (1) using nominal ALD thicknesses approximately correspond to those obtained from the estimated thicknesses from physical characterization techniques, such as spectroscopic ellipsometry and high resolution transmission electron microscopy.[16] The oxide capacitance values estimated through different direct measurement techniques generally agree with the values obtained using Eq. (1), although variations can occur since there is always some error inherent in the k-value and

TABLE I. Summary of sample details for S1–S6. SM = shadow mask and LO = lift-off.

Sample name	Dopant type	Dopant element	Doping in cm^{-3}	$(NH_4)_2S$ % conc.	Transfer time (min)	Oxide thickness (nm)	Ni/Au thickness (nm)	Metal process
S1	N	S	4×10^{17}	10	~7	~8	60/40	SM
S2	P	Zn	4×10^{17}	10	~7	~8	60/40	SM
S3	N	S	4×10^{17}	10	~3	~8	70/90	LO
S4	N	S	4×10^{17}	5	~7	~8	60/40	SM
S5	N	S	4×10^{17}	10	~3	~12	70/90	LO
S6	P	Zn	4×10^{17}	10	~3	~12	70/90	LO

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thickness estimates. In addition, techniques used for estimating the oxide capacitance can often produce results different to those obtained when measuring the capacitance observed in strong accumulation.

We employed two methods for evaluating the interface state defect density for each sample: the CM[13,14] and the HL.[14]

In the case of some samples, we have also used secondary estimates of the oxide capacitance mainly to illustrate two points: (1) it is well known that using a different oxide capacitance will give a different extraction of D_{it} employing the CM and HL, but the effect on the D_{it} extractions for different values of oxide capacitance and for different values of AC voltage amplitude is unknown. Quantification would be informative; (2) if the estimated and employed oxide capacitance is slightly inaccurate (as discussed previously) and falls very close to or lower than the measured capacitance, how do the D_{it} extraction techniques handle these conditions?

The essence of the CM is contained in Eq. (2). When sweeping the applied voltage for fixed AC frequency values ($\omega = 2\pi \times$ AC frequency), we assume a zero deviation in the semiconductor band bending ($\sigma_s = 0$). Under this condition, $f_D(\sigma_s) = 0.4$, and q is the electronic charge ($\sim 1.602 \times 10^{-19}$ eV).

$$D_{it} = \frac{\langle G_p/\omega \rangle}{f_D(\sigma_s) q} \approx \frac{2.5}{q} \left(\frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \right) \{\mathrm{cm}^{-2}\mathrm{eV}^{-1}\}. \quad (2)$$

The measured capacitance (C_m) and conductance (G_m) in Eq. (2) are from the C_pG parallel circuit mode CV/GV measurements after checks for series resistance effects are complete and corrected if necessary.[14] As a comparative check, we also carried out equivalent measurements with no assumptions regarding the deviation in the semiconductor band bending and by sweeping the frequency at fixed voltage bias values. Similar D_{it} results were obtained and therefore we maintain focus here on results using Eq. (2) in order to compare with the HL extractions.

The HL,[14] unlike the conductance method, uses only the measured capacitance and not the conductance, as represented by Eq. (3).

$$D_{it} = \frac{C_{it}}{q} = \frac{1}{q} \left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right] \{\mathrm{cm}^{-2}\mathrm{eV}^{-1}\}. \quad (3)$$

The measured low and high frequency capacitance is C_{LF} and C_{HF}, respectively. The capacitance assigned to the interface state defect response to the AC frequency is C_{it}. The extracted D_{it} using the HL is very sensitive to the low and high frequencies employed and can underestimate D_{it} significantly as a result.[15] Ideally, a quasistatic capacitance should be used for C_{LF} to maximize the interface state defect response, and an extremely high frequency should be used for C_{HF} to ensure the interface defects cannot respond to the applied AC frequency. In practice, compromises must be made. For this study, we focus on $C_{LF} = 20$ Hz and $C_{HF} = 2$ MHz, which we will show give reasonably accurate results.

Equation (3) and thus the HL is very sensitive to the selection of C_{ox}, and when C_{ox} is approximately equal to or less than C_{LF} especially and/or C_{HF}, the method either fails entirely or gives anomalous results. In contrast, Eq. (2) and thus the CM relies on the square of the capacitance subtraction term and therefore is more robust when $C_{ox} \leq C_m$.

In estimating the energy position of interface state defect traps, we use the methods of Ref. 14 by taking room temperature high frequency 2 MHz CV data and assuming a negligible C_{it} response so that $1/C = 1/C_{ox} + 1/C_s$. We cross-check with other measurements at lower temperature and for difference device areas to see the effect of these on C_{it}. We then calculate C_s and the depletion width W. We also determine the Fermi level position with respect to φ_B and the surface potential at each gate voltage bias ψ_s, and from these, we determine the trap position in the energy gap. The trap energy position estimate is very sensitive to the semiconductor doping concentration and the estimated oxide capacitance. We know that such estimates have a resolution of ± 0.05 eV for silicon,[22] and at least the same for $In_{0.53}Ga_{0.47}As$.[16] Based on these assumptions, the trap energy position resolution with respect to maximum AC voltage amplitude change employed in this work is negligible at ± 0.006 eV.

The electrical measurements presented here were carried out using an *Agilent Technologies* E4980A Precision LCR meter and employed methods and techniques to achieve accurate CV/GV measurements over the entire AC frequency range of the meter. The quasistatic capacitance–voltage measurements were carried out using an *Agilent Technologies* B1500A Semiconductor Device Analyzer. The on-wafer measurements were performed at room temperature in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point ≤ 203 K). Extreme care was taken to remove parasitic capacitances from the measurements using robust calibration techniques that remained valid throughout the measurement process.

TABLE II. Main electrical measurement parameters for the CV/GV data used in this work. The 25 frequencies swept were 20 Hz, 40 Hz, 100 Hz, 350 Hz, 700 Hz, 1 kHz, 1 kHz, 2 kHz, 4 kHz, 6 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 60 kHz, 80 kHz, 100 kHz, 200 kHz, 400 kHz, 600 kHz, 800 kHz, 1 MHz, 1.34 MHz, 1.67 MHz, and 2 MHz. All measurements were carried out at each of the following 15 AC voltage amplitudes at a fixed step size of 100 mV (amplitude/step ratio in parenthesis): 10 mV (1:10), 20 mV (1:5), 30 mV (3:10), 40 mV (2:5), 50 mV (1:2), 60 mV (3:5), 70 mV (7:10), 80 mV (4:5), 90 mV (9:10), 100 mV (1:1), 110 mV (11:10), 120 mV (6:5), 130 mV (13:10), 140 mV (7:5), and 150 mV (3:2).

ID	V_g step (mV)	V_g start (V)	V_g stop (V)	# f	f start (Hz)	f end (MHz)	#AC	AC start (mV)	AC end (mV)
S1	100	−2	1.5	25	20	2	15	10	150
S2	100	2	−1.5	25	20	2	15	10	150
S3	100	−2	1.5	25	20	2	15	10	150
S4	100	−2	1.5	25	20	2	15	10	150
S5	100	−4	4	25	20	2	15	10	150
S6	100	4	−4	25	20	2	15	10	150

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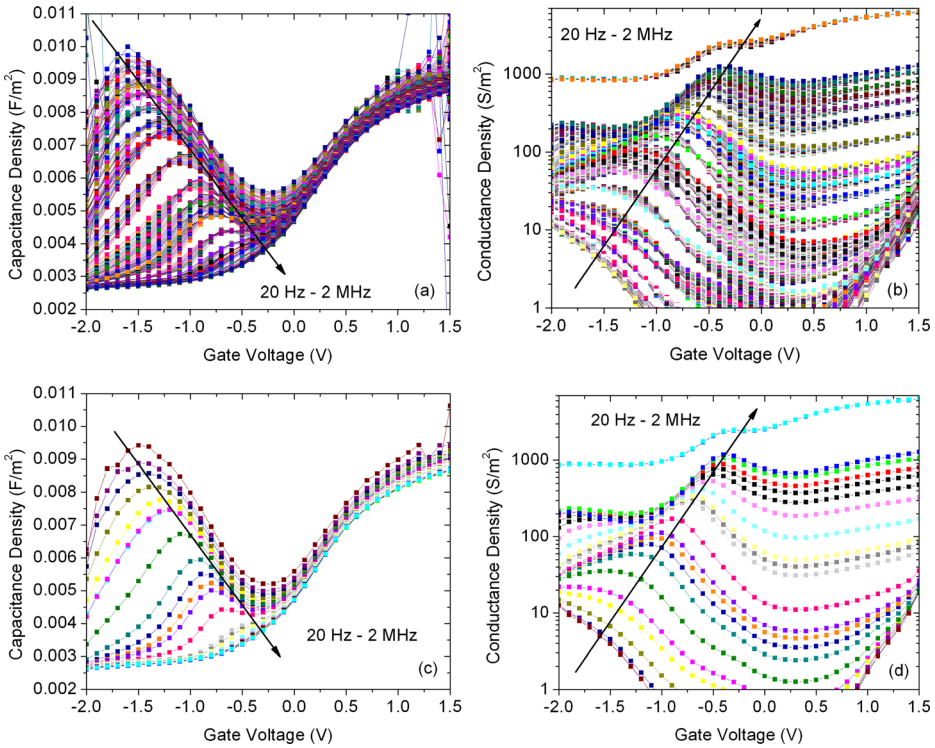


FIG. 1. (Color online) Sample **S1** (a) CV and (b) GV responses for 15 different AC voltage amplitudes (10–150 mV) for each of the 25 AC frequencies selected between 20 Hz and 2 MHz (see Table II). This illustrates the type of CV/GV measurements carried out for all samples **S1–S6** and D_{it} extractions are performed on this type of data set for all samples **S1–S6**. In order to differentiate between the AC frequency dispersion and the dispersive effects of the changing AC voltage amplitude on the CV and GV characteristics, we show 25 AC frequency (c) CV and (d) GV results for a single AC voltage amplitude of 50 mV as comparisons to (a) and (b), respectively.

We apply a fixed voltage step size of 100 mV for all voltage sweep CV/GV measurements at each AC frequency between 20 Hz and 2 MHz. We repeat each of these measurements 15 times for the equidistant AC voltage amplitudes between 10 and 150 mV. This provides the desired AC voltage amplitude to step size ratios from 1:10 to 3:2. This is done for all samples **S1–S6**. See Table II for more details.

IV. RESULTS AND DISCUSSION

Figures 1–4 illustrate the experimental CV and GV responses as a function of AC frequency and AC voltage amplitude (Fig. 1), the extracted interface state density values (Figs. 2 and 3), and a comparison of the low frequency (20Hz) and quasistatic (QS) CV responses (Fig. 4). Table III provides a summary of the main results of this work, which are also described individually in Figs. 5–10. Figure 1 shows sample **S1** (a) CV and (b) GV responses for 15 different AC voltage amplitudes for each of the 25 frequencies selected between 20 Hz and 2 MHz, as described in Table II. Figures 1(a) and 1(b) illustrates the type of CV/GV measurements carried out for all samples **S1–S6**. D_{it} extractions are performed on this type of data set for all samples **S1–S6**. In order to differentiate between the frequency dispersion at a single AC voltage amplitude and the dispersive effects of the changing AC voltage amplitude on the CV and GV characteristics, we show 25 frequency CV/GV results in Fig. 1(c) CV and in Fig. 1(d) GV for a single AC

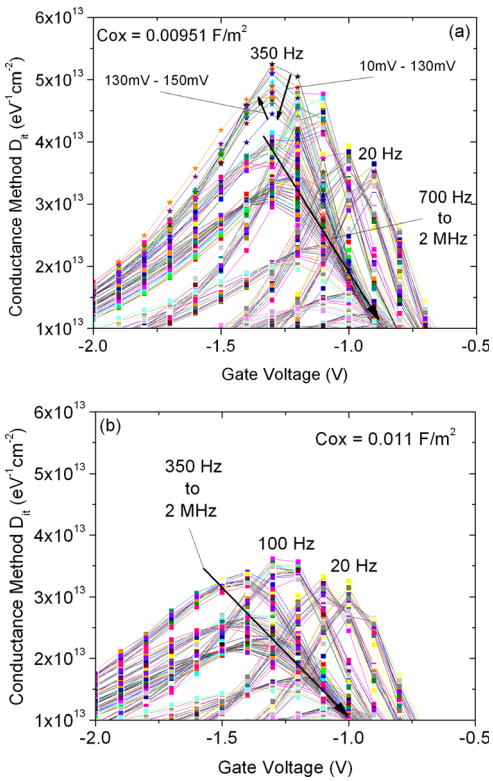


FIG. 2. (Color online) Sample **S1** D_{it} extractions using the CM [Eq. (2)] for a C_{ox} of (a) 0.00951 F/m^2 and (b) 0.011 F/m^2 for 15 different AC voltage amplitudes (10–150 mV) for each of the 25 AC frequencies between 20 Hz and 2 MHz (see Table II). This illustrates the CM analysis technique carried out for all samples **S1–S6**.

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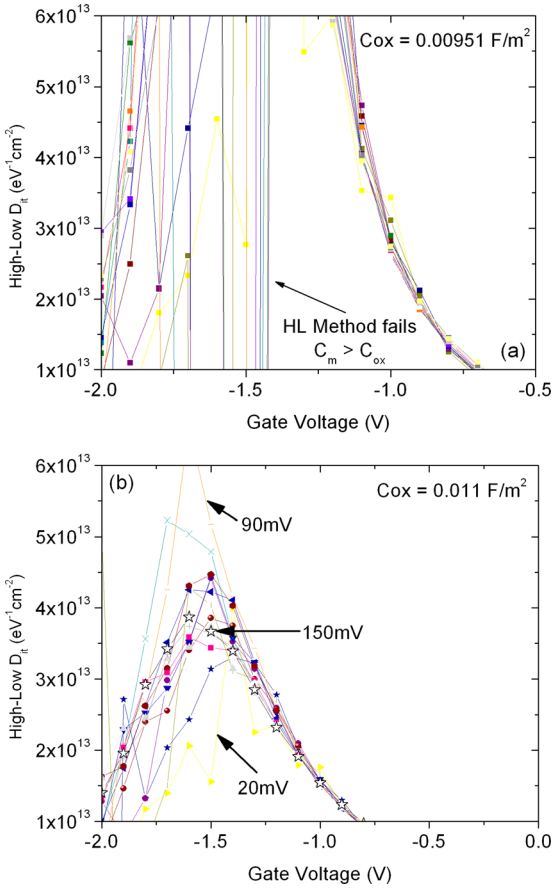


FIG. 3. (Color online) Sample **S1** D_{it} extractions using the HL [Eq. (3)] for a C_{ox} of (a) 0.00951 F/m^2 and (b) 0.011 F/m^2 for $C_{LF} = 20$ Hz and $C_{HF} = 2$ MHz at 15 different AC voltage amplitudes (see Table II). The D_{it} peaks for each AC voltage amplitude plot can be observed in (b) but not in (a) at $V_g = -1.5$ V. The anomalous behavior in (a) is due to C_{ox} being approximately equal to or less than C_{LF} and/or C_{HF}. An increased C_{ox} in (b) rectifies the anomalous behavior. Hence, the HL is not robust to lower values of C_{ox}. This illustrates the HL analysis technique carried out for all samples **S1–S6**.

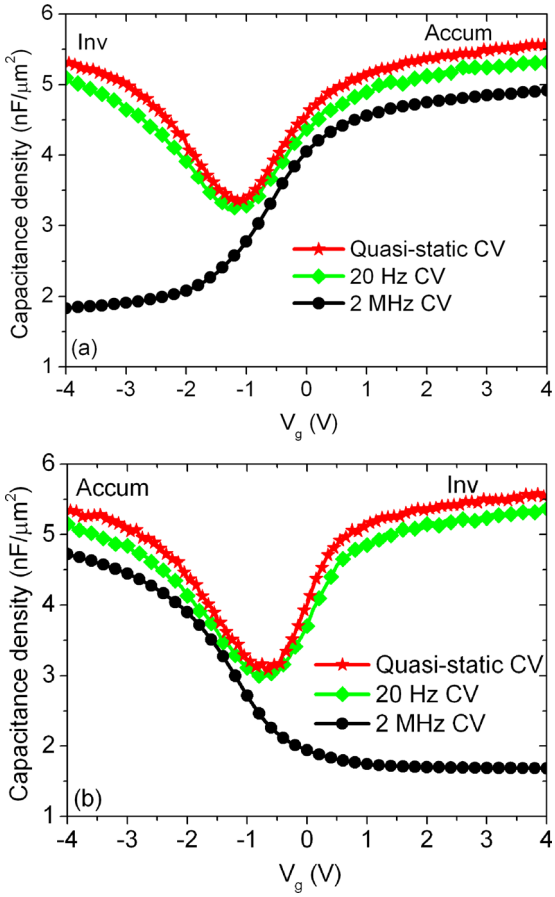


FIG. 4. (Color online) Illustration of how closely the 20 Hz CV approximates the quasistatic CV for samples (a) **S5** and (b) **S6**. Also shown are the appropriate 2 MHz CVs. This example shows that the 20 Hz CV can be used in the HL to give reasonable D_{it} estimates, and this is particularly useful for scaled devices with oxides <10 nm where a quasistatic measurement is not possible due to leakage effects.

voltage amplitude of 50 mV for comparison with Figs. 1(a) and 1(b), respectively.

Figure 2 shows sample **S1** D_{it} extractions using the CM [Eq. (2)] for a C_{ox} of (a) 0.00951 F/m^2 and (b) 0.011 F/m^2 for 15 different AC voltage amplitudes for each of the 25 frequencies selected between 20 Hz and 2 MHz, as described in Table II. The maximum D_{it} peaks for a clustered distribution can be observed at 350 Hz for (a) and 100 Hz for (b) at $V_g = -1.3$ V. Notice that the CM technique is robust to lower values of C_{ox}. Figure 2 illustrates the CM analysis technique carried out for all samples **S1–S6**.

Figure 3 shows sample **S1** D_{it} extractions using the HL [Eq. (3)] for a C_{ox} of (a) 0.00951 F/m^2 and (b) 0.011 F/m^2 for 15 different AC voltage amplitudes for $C_{LF} = 20$ Hz and $C_{HF} = 2$ MHz, as described in Table II. The D_{it} peaks for each AC voltage amplitude plot can be observed in (b) but not in (a) at $V_g = -1.5$ V. The anomalous behavior in (a) is due to C_{ox} being approximately equal to or less than C_{LF} and/or C_{HF}. An increased C_{ox} in (b) rectifies the anomalous behavior. Hence, the HL is not robust to lower values of C_{ox}. Figure 3 illustrates the HL analysis technique carried out for all samples **S1–S6**.

Figure 4 shows the accuracy of using a 20 Hz CV sweep to approximate to a QSCV sweep. The latter is generally not possible below a high-k oxide thickness of ~10 nm because the quasistatic CV extraction method necessitates a very low leakage current density which should have a value much less than the displacement current derived from the integral of displacement charge with respect to time resulting from the incremental applied voltage step on the MOS device. The derived capacitance is this incremental charge divided by the incremental voltage change. In Fig. 4, we see that there is little difference between the 20 Hz CV and the QSCV for both n-type **S5** (a) and p-type **S6** (b), indicating that for the $In_{0.53}Ga_{0.47}As$ MOS system a frequency of 20 Hz appears to be a reasonable approximation to a low frequency response and can be used in cases where gate leakage precludes the use of a full QSCV measurement.

Figures 5–10 show the extracted D_{it} for the most appropriate gate voltages and AC frequencies for each of the 15 different AC voltage amplitudes (10–150 mV). Figure 5 shows sample **S1** scatter plots for D_{it} extracted using the

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TABLE III. Summary of results in this work and how they change with C_{ox} selection and the AC voltage amplitude from 50% below the voltage sweep step size to 50% above it.

	CM D_{it} ($cm^{-2}eV^{-1}$) $\times 10^{13}$		HL D_{it} ($cm^{-2}eV^{-1}$) $\times 10^{13}$				
Name	C_{ox} (1)	C_{ox} (2)	C_{ox} (1)	C_{ox} (2)	C_{ox} (1) F/m^2	C_{ox} (2) F/m^2	Figure
S1	4.8 ± 0.3	3.3 ± 0.2	Void	4.4 ± 1.0	0.00951	0.011	5
S2	6.0 ± 1.5	3.0 ± 0.8	Void	1.5 ± 0.3	0.00951	0.0155	6
S3	0.6 ± 0.1	N/A	0.9 ± 0.05	N/A	0.00951	N/A	7
S4	2.5 ± 0.1	2.25 ± 0.05	Void	Void	0.00951	0.011	8
S5	0.27 ± 0.03	N/A	0.24 ± 0.05	N/A	0.00634	N/A	9
S6	0.23 ± 0.05	N/A	0.23 ± 0.05	N/A	0.00634	N/A	10

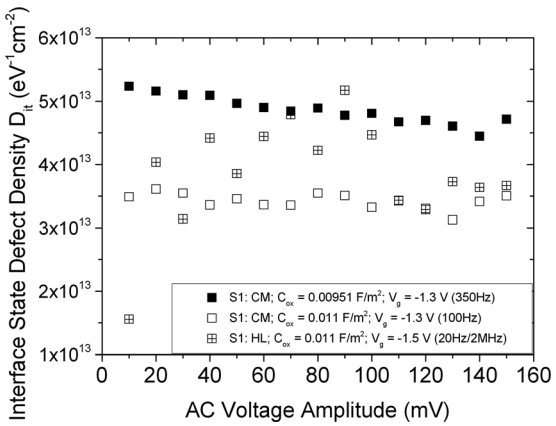


FIG. 5. Sample **S1** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00951$ F/m^2, $V_g = -1.3$ V ($E - E_v \sim 0.36$ eV), and at an AC frequency of 350 Hz; CM extractions carried out for $C_{ox} = 0.011$ F/m^2, $V_g = -1.3$ V ($E - E_v \sim 0.37$ eV), and at an AC frequency of 100 Hz; and HL extractions carried out for $C_{ox} = 0.011$ F/m^2, $V_g = -1.5$ V ($E - E_v \sim 0.36$ eV), and AC frequencies of 20 Hz (LF) and 2 MHz (HF).

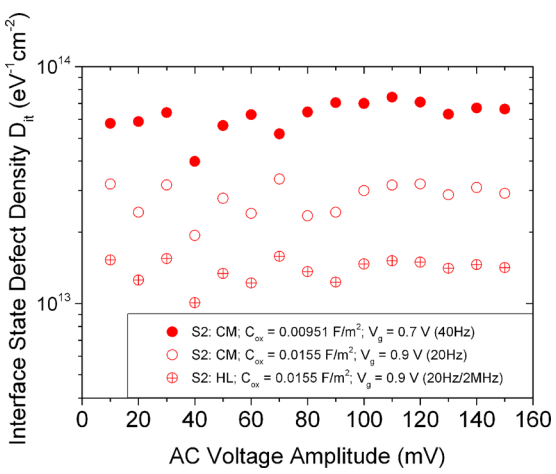


FIG. 6. (Color online) Sample **S2** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00951$ F/m^2, $V_g = 0.7$ V ($E - E_v \sim 0.36$ eV), and at an AC frequency of 40 Hz; CM extractions carried out for $C_{ox} = 0.0155$ F/m^2, $V_g = 0.9$ V ($E - E_v \sim 0.42$ eV), and at an AC frequency of 20 Hz; and HL extractions carried out for $C_{ox} = 0.0155$ F/m^2, $V_g = 0.9$ V ($E - E_v \sim 0.42$ eV), and AC frequencies of 20 Hz (LF) and 2 MHz (HF).

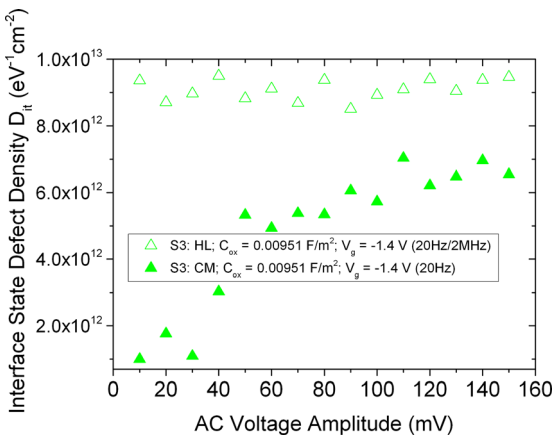


FIG. 7. (Color online) Sample **S3** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00951$ F/m^2, $V_g = -1.4$ V ($E - E_v \sim 0.33$ eV), and at an AC frequency of 20 Hz; and HL extractions carried out for $C_{ox} = 0.00951$ F/m^2, $V_g = -1.4$ V ($E - E_v \sim 0.33$ eV), and AC frequencies of 20 Hz (LF) and 2 MHz (HF).

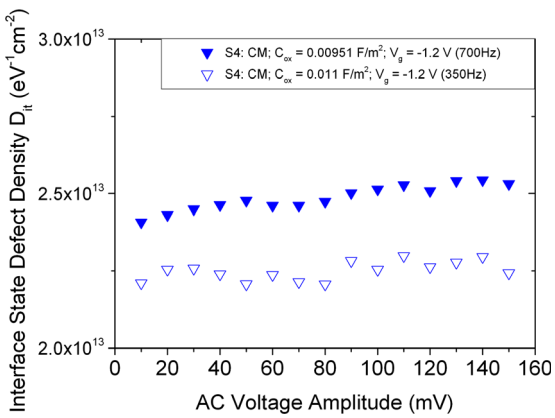


FIG. 8. (Color online) Sample **S4** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00951$ F/m^2, $V_g = -1.2$ V ($E - E_v \sim 0.41$ eV), and at an AC frequency of 700 Hz; and CM extractions carried out for $C_{ox} = 0.011$ F/m^2, $V_g = -1.2$ V ($E - E_v \sim 0.38$ eV), and at an AC frequency of 350 Hz.

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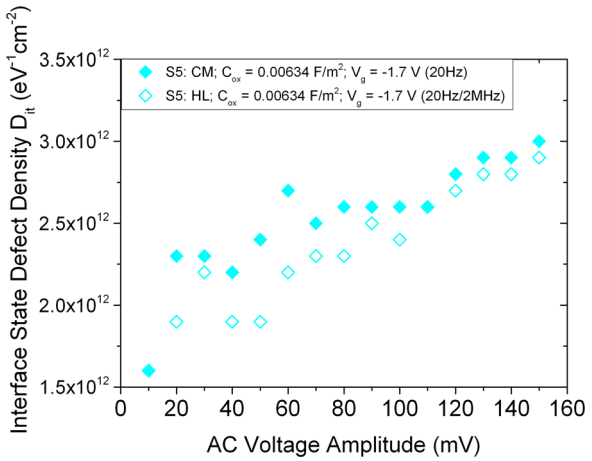


FIG. 9. (Color online) Sample **S5** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00634\,\mathrm{F/m^2}$, $V_g = -1.7\,\mathrm{V}$ ($E - E_v \sim 0.37\,\mathrm{eV}$), and at an AC frequency of 20 Hz; and HL extractions carried out for $C_{ox} = 0.00634\,\mathrm{F/m^2}$, $V_g = -1.7\,\mathrm{V}$ ($E - E_v \sim 0.37\,\mathrm{eV}$), and AC frequencies of 20 Hz (LF) and 2 MHz (HF).

CM and HL with the specified C_{ox} values. As discussed previously, the HL technique failed for $C_{ox} = 0.00951\,\mathrm{F/m^2}$ but was sufficiently remedied for $C_{ox} = 0.011\,\mathrm{F/m^2}$.

Figure 6 shows sample **S2** scatter plots for D_{it} extracted using the CM and HL with the specified C_{ox} values. The HL technique failed for $C_{ox} = 0.00951\,\mathrm{F/m^2}$ but was sufficiently remedied for $C_{ox} = 0.0155\,\mathrm{F/m^2}$. Figure 7 shows sample **S3** scatter plots for D_{it} extracted using the CM and HL with $C_{ox} = 0.00951\,\mathrm{F/m^2}$ (no further extractions were necessary with an increased C_{ox}).

Figure 8 shows sample **S4** scatter plots for D_{it} extracted using the CM only with the two specified C_{ox} values. The HL technique gave anomalous results for both values of C_{ox}. Figure 9 shows sample **S5** scatter plots for D_{it} extracted using the CM and HL with the specified $C_{ox} = 0.00634\,\mathrm{F/m^2}$ (no further extractions were necessary with an increased C_{ox}). Figure 10 shows sample **S6** scatter plots for D_{it} extracted using the CM and HL with the specified $C_{ox} = 0.00634\,\mathrm{F/m^2}$ (no further extractions were necessary with an increased C_{ox}).

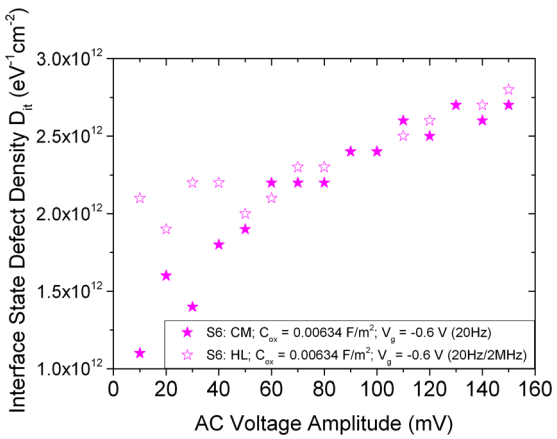


FIG. 10. (Color online) Sample **S6** extracted D_{it} for the most appropriate gate voltage and AC frequency for each of the 15 different AC voltage amplitudes (10–150 mV). Results are summarized in Table III. CM extractions carried out for $C_{ox} = 0.00634\,\mathrm{F/m^2}$, $V_g = -0.6\,\mathrm{V}$ ($E - E_v \sim 0.35\,\mathrm{eV}$), and at an AC frequency of 20 Hz; and HL extractions carried out for $C_{ox} = 0.00634\,\mathrm{F/m^2}$, $V_g = -0.6\,\mathrm{V}$ ($E - E_v \sim 0.35\,\mathrm{eV}$), and AC frequencies of 20 Hz (LF) and 2 MHz (HF).

From Table III, we see that for the most part, the AC voltage amplitude selected has little effect on the extracted D_{it} provided care is taken in the selection of C_{ox}, as overestimation of the oxide capacitance can lead to a reduced magnitude and shift of the peak mid-gap interface state defect density alongside a smoothing out of the response versus applied frequency and voltage (see Fig. 2), and underestimation of the oxide capacitance can lead to either complete failure of the extraction method or anomalous behavior (see Fig. 3).

It is worth highlighting the differences in the extracted D_{it} using both the CM and HL techniques for samples with and without the optimized passivation process and transfer time. Samples **S3**, **S5**, and **S6** were prepared by the optimized process and transfer time and therefore show D_{it} values an order of magnitude or more lower than samples **S1**, **S2**, and **S4** that were prepared using nonoptimized processes and transfer times.

V. SUMMARY AND CONCLUSIONS

Significant progress has been made in recent years to analyze and reduce the interface state defect density levels at the high-k/$In_{0.53}Ga_{0.47}As$ interface of metal–oxide–semiconductor capacitors for application as the gate stack in future field-effect transistors. The conductance method and the combined high–low frequency capacitance–voltage method are used extensively to investigate the interface state defect density levels in these and similar systems. While the selected oxide capacitance used in these extraction methods is known to have a significant effect on the interface state defect density level extracted—and we confirm that fact in this work—the effect of the selected AC voltage amplitude was unknown. It was also unknown whether changes to the selection of both these parameters would have a compounding effect on the extracted interface state defect density level. Overall we find that the selection of the AC voltage amplitude, especially for selected ratios from 1:2 to 3:2 with respect to the voltage sweep step size, has no significant effect on the level of interface state defect density extracted, and that it does not compound any error arising from the selection of the oxide capacitance regardless of whether you use the conductance method or the combined high–low frequency capacitance–voltage method. We also find that the conductance method is more robust to oxide capacitance selection. Therefore, an increased AC voltage amplitude up to a 3:2 ratio with respect to the voltage step size can be used in capacitance–voltage and conductance–voltage measurements for either the conductance method or the combined high–low frequency capacitance–voltage method to provide accurate interface state defect density estimates for the high-k/$In_{0.53}Ga_{0.47}As$ interface of metal–oxide–semiconductor capacitor gate stacks in future reduced voltage field-effect

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transistors. From a metrology perspective, this finding is significant, as the AC voltage amplitude can be increased without having a major impact on the extracted interface state defect density, and the increase in the AC voltage amplitude results in an improved signal-to-noise for impedance measurements.

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