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An Active Quench and Reset IC with Novel Hold-off Time Control Logic for Geiger-mode Avalanche Photodiodes

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This paper presents an active quench and reset circuit for Geiger-mode avalanche photodiodes (GM-APDs). The integrated circuit was fabricated using a conventional 0.35 μm CMOS process. Experimental results show that the circuit is capable of linearly setting the hold-off time from several nanoseconds to microseconds with a resolution of 6.5 ns. This allows selection of the optimal *afterpulse-free* hold-off time for the GM-APD via external digital inputs or additional signal processing circuitry. Moreover, this circuit resets the APD automatically following the end of the hold-off period thus simplifying the control for the end-user. Results also show that a minimum dead time of 28.4 ns is achieved demonstrating a saturated photon-counting rate of 35.2 Mcounts/s. © 2012 Optical Society of America

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Geiger-mode avalanche photodiodes (GM-APDs) are used in high sensitivity low-light sensing applications, particularly in applications where photon counting is necessary. In the Geiger-mode, the APD is biased above its breakdown voltage. When a photon is absorbed by the APD, an avalanche event is triggered and registered as a photon count. After every avalanche event, some residual charge is stored in traps in the APD. The release of this stored charge when the GM-APD is active may lead to an avalanche current correlated to a previous avalanche event, but not related to a new photon arrival. This is an unwanted source of noise and is typically termed "afterpulsing". The afterpulsing phenomenon can be minimised by allowing sufficient time for all trapped charge to dissipate before resetting the GM-APD. This is achieved using an appropriate control circuit whereby the APD avalanche current is quenched by lowering the bias voltage below the breakdown voltage, holding the bias below breakdown for a period of time before resetting the device to its original bias voltage to await the next avalanche event. The period of time that the device is held below its breakdown voltage is known as the hold-off time. If the hold-off time is set too short, then afterpulsing will significantly affect the photon counting statistics. If the hold-off time is too long, the counting rate will be limited. The hold-off time needs to be set appropriately for each individual GM-APD. The most popular method used for setting the hold-off time involved using monostables [1], [2]. The monostable can offer a wide range of hold-off times (from nanoseconds to microseconds), however accurate adjustment of the hold-off time is difficult. In [3], the delay line technique is used to set the hold-off time. This circuit consists of separate ramp voltage generators that are each used to create pre-defined pulse-widths for setting the hold-off time. This technique makes it easier to select an appropriate hold-off time, but it uses several capacitors that lead to an increased layout area. In addition, there are only a finite number of hold-off times available, thus requiring an increased layout area to obtain additional hold-off times. An additional limitation in all the techniques mentioned above is the requirement for a second monostable or pulse generator to reset the APD, which again adds to the complexity of the control circuit.

An accurate hold-off time control circuit was designed, simulated and described in [4]. In this paper, an active quench and reset IC (AQR-IC) is described which is an improved circuit on [4]. In this design, a ring-oscillator is used to replace the external clock described in [4] to simplify the end-user control. A counter in the circuit is clocked by the ring-oscillator after sensing the avalanche event. Using this counter the hold-off time can be controlled linearly. This circuit was fabricated using Austria Microsystems (AMS) 0.35 μm CMOS process and tested with a planar silicon GM-APD having a 27 V breakdown voltage [5], [6], [7]. Experimental results of the fabricated chip show that the circuit is capable of linearly setting the hold-off time from several nanoseconds to microseconds with a setting step of $\approx$ 6.5 ns. This circuit is also designed to reset the APD automatically at the end of the hold-off period without the need for another monostable or pulse generator. A minimum dead time of 28.4 ns is measured enabling a saturated photon-counting rate of 35.2 Mcounts/s with this AQR-IC.

Figure 1 shows the block diagram of the proposed circuit. The inverting input of the comparator is connected to the cathode of the APD which is biased at a voltage determined by V_{dd} and -V_{low}. A comparator is used to sense the avalanche current at the cathode of the APD. One PMOS and one NMOS transistor are used as the switches for quenching or resetting the APD. A ring-oscillator is used to generate clock pulses during the hold-off period and a counter is used to count the clock

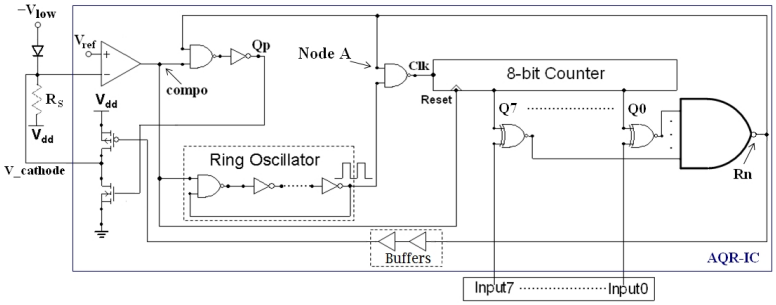


Fig. 1. Block diagram of the fabricated active quench and reset circuit

pulses to adjust the hold-off time.

Initially, when there is no avalanche current, *compo* is low, the ring-oscillator is inactive and the 8-bit counter is reset to 0 ("00000000"), both PMOS and NMOS transistors are turned off. When an avalanche event occurs, current flows through the sensing resistor R_S and a voltage drop is observed at the cathode of the APD. The comparator senses the voltage drop and *compo* goes from low to high. Q_p goes high to turn on the NMOS transistor and the cathode of the APD is connected to GND for quenching. Meanwhile, the ring oscillator is active and providing the clock to the counter.

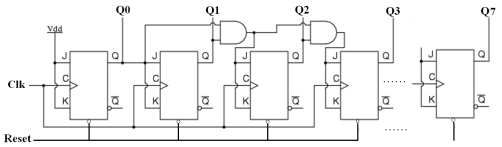


Fig. 2. Schematic of the 8-bit synchronous binary counter

The counter used here is an 8-bit synchronous binary counter consisting of 8 J-K flip-flops with the clock signal connected to the clock input of every flip-flop and the J and K inputs tied together as in Figure 2. The J and K inputs of the first flip-flop are connected to V_{dd}, the J and K inputs of the other flip-flops are connected to the output Q of each front end. When the reset signal *compo* is high, the clocks from the ring-oscillator are active and the counter counts upwards from 0 ("00000000") to 255 ("11111111"). Each output of the counter is connected to one input of an XNOR gate. The other input of the XNOR is connected to an external input (controlled by end user). When the outputs of the counter equals the external inputs, all the outputs of the XNOR gates go to logic "1" (high). Then R_n goes low which makes Q_p go low to stop the hold-off process and turn on the PMOS transistor thereby resetting the APD (buffers are used here to make sure the reset process starts after the hold-off process is finished). At this time, *Node A* goes low to block the clock from the ring-oscillator to the counter and the counter is stopped. This makes R_n remain low for resetting. When the cathode of the APD is reset back to V_{dd}, *compo* is low, the ring-oscillator is inactive and the counter is reset to 0 ("00000000"). Now the outputs of the counter do not match the external inputs, R_n goes high and the PMOS transistor is turned off to complete the reset process. The APD is then ready to detect the next photon. By setting the external inputs, the counting number can be determined and the hold-off time can be altered. The hold-off time setting step is decided by the counting speed which depends on the number of the stages of the ring-oscillator. A 41-stage ring-oscillator occupying approximate 25% of the IC core which is used here to give a stable setting step of around 6.5 ns for the hold-off time.

Figure 3 shows a photograph of the fabricated chip, the overall chip dimension is 1.7 mm × 1.4 mm which mostly occupied by the bond pads and decoupling capacitors. The dimensions of the IC core are 260 μm × 150 μm.

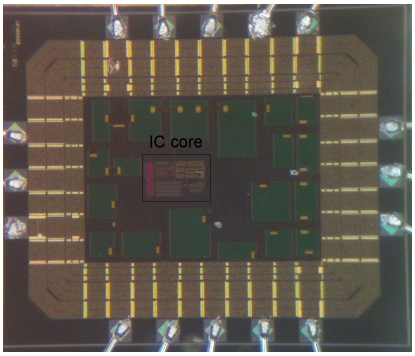


Fig. 3. Photograph of the fabricated chip

For the measurements, the AQR-IC is connected to a 20 μm diameter circular GM-APD developed by the Photodetection and Imaging Group at University College Cork. The APD is biased at 30 V (-V_{low} = -26.7 V) which is around 3 V in excess of its breakdown voltage. In Figure 4(a), the oscilloscope traces of the quenching pulse (Q_p) and the cathode voltage ($V_{cathode}$) are demonstrated with the hold-off time kept at 190 ns by setting Input7 to Input0 to 00011101. Figure 4(b) and Figure 4(c) show the cathode voltage ($V_{cathode}$) of the APD with the hold-off times set to 326 ns and 1.18 μs. The results demonstrate the accurate control of the hold-off time using external switches.

Figure 5 shows the results of varying the external input codes versus the resultant hold-off time. It shows when

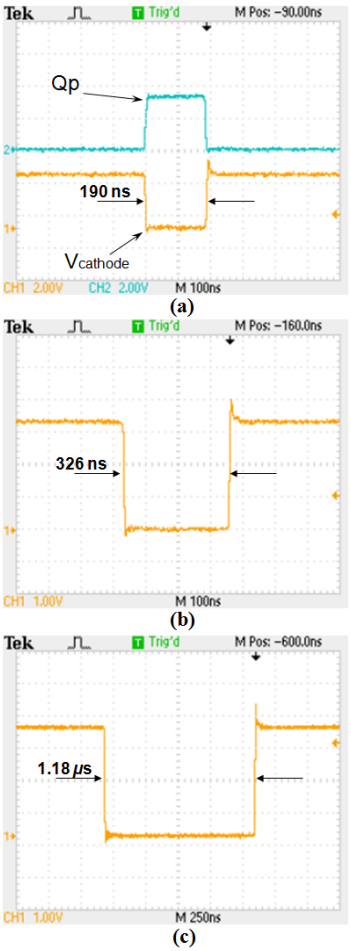


Fig. 4. (a) Quenching pulse (Qp) and APD's cathode voltage ($V_{cathode}$) with a hold-off time of 190 ns (00011101), (b) $V_{cathode}$ with hold-off time = 326 ns (00110010) and (c) $V_{cathode}$ with hold-off time = 1.18 μs (10110101).

the input code increases from 1 ("00000001") to 255 ("11111111") the hold-off time linearly increases from several nanoseconds to more than 1.6 μs with a setting step of about 6.5 ns. In Figure 6, A plot of $V_{cathode}$ is shown with Input7 to Input0 set to 00000001 when saturating light is directed at the APD, demonstrates the minimum dead-time between adjacent avalanche events in the GM-APD. It can be seen that the minimum dead-time is 28.4 ns corresponding to a saturated count-rate of 35.2 Mcounts/s with this AQR-IC.

In conclusion, an active quench and reset IC for Geiger-mode avalanche photodiodes fabricated using a conventional CMOS process is described. The experimental results show the hold-off time can be linearly set from several nanoseconds to microseconds with a resolution of 6.5 ns. The optimal *afterpulse-free* hold-off time for any GM-APD can be easily set by the end user through the circuit's digital inputs or via an additional signal processing circuit. A saturated photon-counting rate of 35.2 Mcounts/s is demonstrated from

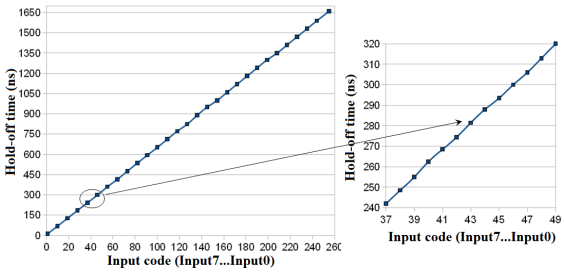


Fig. 5. External input codes versus hold-off time

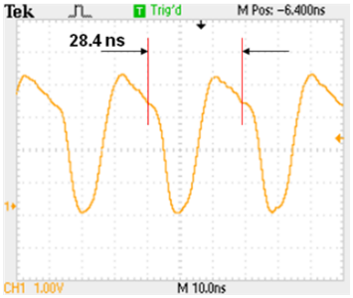


Fig. 6. Plot of $V_{cathode}$ for saturated count-rate

the measurement. The circuit uniquely incorporates a mechanism designed to reset the APD automatically at the end of the hold-off time thereby simplifying the control for the end-user.

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