Micro-transfer printing of micro-structured, ultra-thin light-emitting devices

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List of Acronyms

GaN	Gallium nitride
PICs	Photonic integrated chips
EL	Electroluminescence
HVPE	Hydride vapour phase epitaxy
AlN	Aluminium nitride
LEEBI	low energy electron beam irritation
KOH	Potassium hydroxide
OFN	Oxygen free nitrogen
QW	quantum well
μLED	micro-Light Emitting Diode
InGaN	Indium gallium nitride
SiO_2	Silicon dioxide
SiN_x	Silicon nitride
WPE	Wall-plug efficiency
IQE	Internal quantum efficiency
EQE	External quantum efficiency
QCSE	Quantum-confined stark effect
BOE	Buffered Oxide Etch

TMAH ..... Tetramethylammonium hydroxide

TP ..... Transfer Print

PDMS ..... polydimethylsiloxane

ICP ..... Inductive coupled plasma

PECVD ..... plasma-enhanced chemical vapor deposition

PR ..... photoresist

GRIN ..... Gradient refractive index

2DHG ..... two-dimensional hole gas

2DEG ..... two-dimensional electron gas

List of Publications

First author publications

1. **Z. Shaban**, Z. Li, B. Roycroft, M. Saei, T. Mondal, and B. Corbett, *"Transfer Printing of Roughened GaN-Based Light-Emitting Diodes into Reflective Trenches for Visible Light Communication"* , in Advanced Photonics Research, p.2100312, March 2022.

2. **Z. Shaban**, M.saei, B. Corbett and Z.Li *"Integration of high performance GaN LEDs for communication systems and smart society"* , in IEEE 72nd Electronic Components and Technology Conference (ECTC), pp. 2111-2115, 2022.

3. **Z. Shaban**, V. Zubialevich, E.A. Amargianitakis, F. Bilge Atar, P.J. Parbrook, Z. Li and B. Corbett *"InGaN/AlInN interface with enhanced holes to improve photoelectrochemical etching and GaN device release "*, in Semiconductor Science and Technology, March 2023.

Conference posters

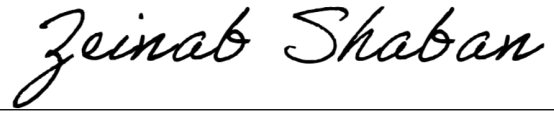
1. **Z. Shaban**, Z.Li and B. Corbett "Light enhancement of GaN LEDs by transfer from original substrate to reflective trench" , UK Nitride consortium, 2022.

2. **Z. Shaban**, Z.Li and B. Corbett "Stress management on GaN LEDs for Transfer Printing", Photonics Ireland conference, 2021.

3. **Z. Shaban**, Z.Li and B. Corbett "Controlling device bow for effective transfer of GaN LEDs to non-native substrates" , IPIC, 2020.

Declaration

I, Zeinab Shaban hereby declare that, unless otherwise stated, this work is my own, and that it has not been submitted for another degree, either at University College Cork or elsewhere.

Signed: 

Abstract

3D integration of optoelectronic devices is a crucial future technology, which can be applied in the areas of photonic integrated circuits, flexible displays, communication and more. Among the various technologies, micro-transfer printing has emerged as a precise and cost-effective way to assemble devices for 3D integration. To enable this technology, devices must be released from their native substrates, which open up a lot of possibilities. It can achieve integration with flexible or heat-conductive backplanes, as well as heterogeneous integration of multiple materials on a common platform, resulting in miniaturised chips. Also one can benefit from reclaiming and reusing the original substrates to reduce the production cost significantly. On the other hand, GaN devices exhibit unique optical properties in optoelectronics compared to other semiconductors, and GaN-based LEDs have established themselves in a variety of applications, due to their low power consumption, long lifetime, short response time, and high brightness. This thesis has focused on releasing high performance GaN LEDs and addressing their associated issue for micro-transfer printing.

The first part of this work is focused on releasing and transfer-printing of GaN LEDs grown on Si substrate. There are several factors that limit the performance and manufacturing of GaN LEDs on Si. One issue is related to the deformation of the released coupons due to their high inbuilt strain, which could result in transfer-printing failures as well as challenges during the post-print integration process. To address this issue, COMSOL software was used to study the stress effect on the devices. Experimentally, the intrinsic deformation of the released LEDs was compensated by using compressed SiN_x layers that resulted in flat devices after release. Another issue is related to the low light extraction for GaN LEDs on Si. To solve this problem, the underside of the released LEDs is roughened during the coupon preparation process prior to transfer printing. Furthermore, using the unique properties of transfer printing, the roughened

LEDs are printed inside a fabricated reflective trench with 10 μm depth to direct the light to the surface normal. Results showed that roughening along with the reflective trench increased the collected power by a factor of ~ 7 compared with LEDs on the original substrate.

A second part of this study examines the release of GaN-based structures from substrates (i.e. sapphire or bulk GaN) by photoelectrochemical (PEC) etching when pure chemical etching is not possible. A sacrificial layer which can obtain smooth etch surfaces and uniform etching with high selectivity is needed. Also, from the perspective of transfer printing, thick rather than thin sacrificial layers are preferred to facilitate the releasing and picking process. In this work, 300 nm-thick releasing layers comprising of InGaN/AlInN stacks are proposed for PEC etching. The presence of two-dimensional hole gas at the interface of InGaN/AlInN due to the strong polarization field are indicated by modelling and capacitance-voltage measurement. This resulted in a smoother surface with a three times higher etch rate compared to the conventional InGaN/GaN superlattice structures used for PEC etching. Moreover, various electrolytes and post-PEC treatment were studied to improve the surface smoothness.

Further work should be done to determine the impact of the adhesion layer in transfer printing on heat generation and device performance. Using the optimized sacrificial layer to release other structures like lasers should also be investigated.

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To
my beloved Mehrdad Saei for his support

Chapter 1

Introduction

The increasing complexity of photonic device applications necessitates the integration of many components on one substrate in order to create a compact, efficient, and cost-effective chip. Over the past decade micro-transfer printing (μTP) has emerged as a method for heterogeneously integrating components of different materials or fabrication platforms in order to achieve a variety of enhanced functions or applications [1]. It is necessary to release the devices from their growth substrate in order to utilize this technology. In this thesis, the focus is primarily on the release of devices from the growth substrate so that they can be printed using this technology. In particular, GaN LEDs are being released because integrated chips are increasingly demanding smaller and more efficient sources of light as applications in numerous industries become more complex [2]. LEDs based on gallium nitride (GaN) have gained a lot of interest for a variety of applications, especially in display and communication systems, due to their low power consumption, long lifetime, short response time and high brightness [3, 4]. An LED integrated directly onto a chip, for example, could provide a compact, low-cost, and reliable way to use LED for displays, sensors, or communications. This introduction provides an overview of integration techniques, with a particular emphasis on transfer printing technology and the process required to enable the transfer printing of devices. The development of GaN LEDs is discussed in this chapter as they are one of the main light sources used in a variety of applications. Moreover, the advantages and disadvantages of each substrate for GaN LEDs are discussed, as well as the methods for lift-off of GaN LEDs from their respective substrates.

1.1 Introduction of integration techniques

3D integration of optoelectronic devices is a crucial technology for the development of practical devices such as photonic integrated circuits, flexible displays and communications. Various optoelectronic devices need to be packaged or coupled, either optically or electronically, with a variety of components to become functional. Manufacturing costs associated with packaging processes are significant, and these processes are often associated with reliability issues. Many years of effort have been devoted to developing an accurate and cost-effective integration technology [5, 6]. There are three principal approaches to wafer-level integration, which can be categorized as monolithic, hybrid, and heterogeneous. The following section discusses various integration techniques for light emitting devices.

1.1.1 Monolithic integration

The monolithic integration method uses a single substrate to fabricate devices. The entire process is typically carried out at the wafer level. Lattice matching and epitaxial plane selection are vital requirements for this type of integration. As the optimal structure varies from device to device, the fabrication process needs to be adjusted accordingly [7, 8]. An example would be the development of highly efficient inorganic red, green, and blue emitting materials on a single wafer, which is still in its infancy and poses many challenges. Currently, the highly efficient blue and green emitting LED structures are GaN-based, while the efficient red emitters are AlGaInP-based [9, 10].

1.1.2 Hybrid and heterogeneous integration

A hybrid integration approach can be used to avoid the problems associated with monolithic fabrication by fabricating the devices on separate substrates. Afterwards, they are diced into individual chips and assembled. As a hybrid integration approach, flip-chip integration is the most commonly adopted in the industry due to its environmental friendliness (eliminating lead material and flux cleaning), low temperature process and fine pitch capability. [11–13].

This technique allows different devices to be integrated on a variety of substrates due to the separate fabrication processes of each wafer. By using this technique, individual components are integrated after the overall fabrication process has been completed. As a result, this process

offers the advantage of testing and characterizing a component or device prior to its integration. In this manner, the best-performing devices can be selected, while the non-functional components can be discarded, thereby enhancing the quality of the chip [14]. However, as flip-chip assembly requires precise alignment, it limits the possibility of scaling up and reducing the cost of photonic integrated chips (PICs) [15–17].

As a solution to this challenge, heterogeneous integration has been explored in recent years using die-to-wafer or wafer-to-wafer bonding, where the critical alignment of the devices is achieved by lithography. A heterogeneous integration process involves the integration of two or more different materials technologies on a single chip [18]. The process is generally carried out during the initial to mid-stages of the fabrication of the PIC chip [19]. The main advantage of heterogeneous integration is that it can perform the same functions as monolithic integration, meaning that it provides accurate submicron alignment since alignment is achieved through wafer-scale lithography. Additional benefits include reliable performance and low costs due to economies of scale. This makes it suitable for high-volume applications [20]. One of the minor disadvantages with heterogeneous integration methods such as die-to-wafer bonding is that individual components cannot be tested before they are integrated into more complex PICs, resulting in reduced yield [19]. In addition, wafer bonding also requires a very clean and smooth surface to be used [21].

1.1.3 Micro-transfer printing technology

Micro-transfer printing (μTP) is an emerging technology for heterogeneous integration of optoelectronics and electronics. This technology at the microfabrication and semiconductor level was developed by the Rogers' group at the University of Illinois in 2004 [22, 23].

This technology has become a promising candidate for the assembly of thin and small devices precisely and cost-effectively, combining the advantages of flip-chip and die-to-wafer bonding. With this technique, thin film devices with micron sizes can be transferred in a massively parallel manner from a native growth substrate to a non-native target substrate with an accuracy of $\pm$ 1 μm [24]. Similar to die-to-wafer bonding, this technology offers high accuracy integration, and like flip-chip assembly, it allows prefabrication and pretesting of devices before integrating them into a new target [6].

This technique primarily involves pick up ink from the donor substrate and printing it on the target substrate [25]. The pick-up and printing process can be done by adjusting the peeling

velocity of the stamp, because the adhesion strength of the device(s) to the stamp varies with the rate of peeling [23, 26]. The elastomeric stamp is typically made of polydimethylsiloxane (PDMS). Most stamps rely on a stable and rigid backplate (typically made of glass), a bulk elastomeric material forming a mesa on the backplate, and stamp posts extending from the bulk material away from the backplate. The schematic of printing process is shown in Figure 1.1.

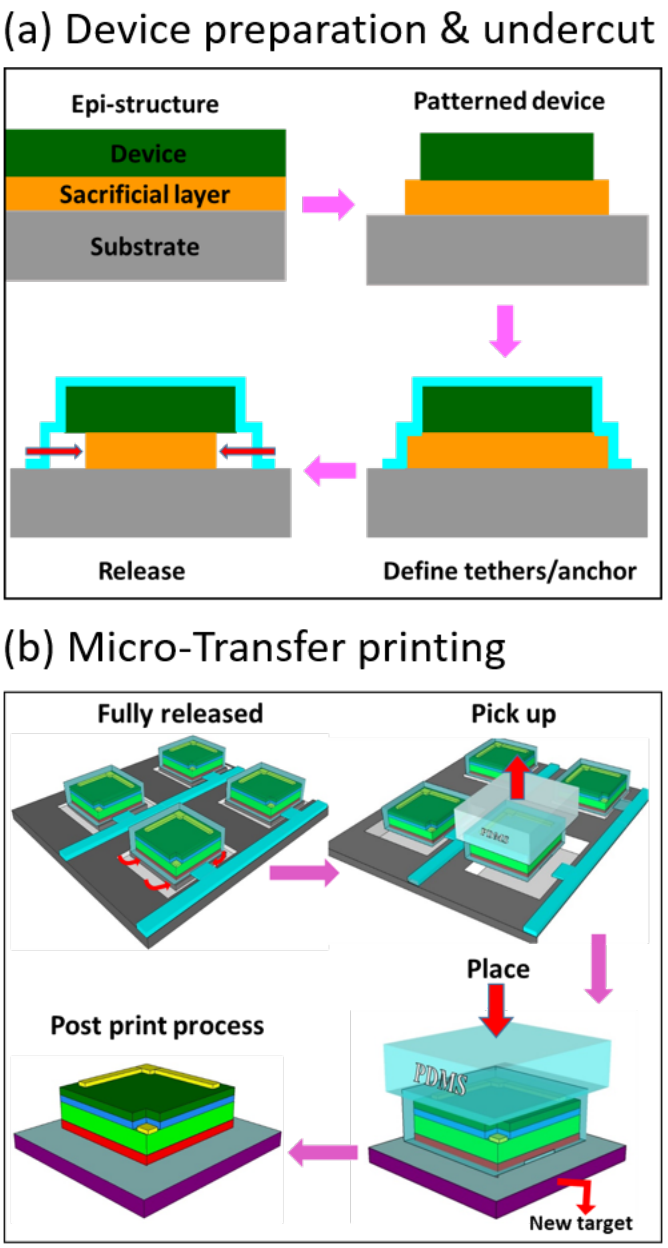

FIGURE 1.1: Process overview for transfer printing: (a) the preparation of the devices and the selective etching of the release layer while leaving the coupons suspended by tethers and securely anchored on the substrate, (b) schematic micro-transfer printing process for released LEDs.

To prepare the sample for transfer printing onto new targets, the fabricated devices have to be released from their native substrates. The releasing is enabled by incorporating a sacrificial layer in the epitaxial layer stack between the device layer and the substrate, which can be selectively etched.

To undercut, the devices are patterned on the source wafer. After that, they are protected by a passivation layer with local openings that allow access to the sacrificial layer, which is then underetched. After underetching the sacrificial layer, the suspended devices are anchored to substrate with tethers. Note that the undercut etching method is determined by the type of substrate. The purpose of this study is releasing devices from different types of substrates in a manner that is compatible with transfer printing and does not degrade the quality of the epitaxial layers, as well as to optimize the fabrication process to increase printing yield.

Once the devices have been released, a PDMS stamp with a post array (or a single post) whose size and patch matching the device array arranged on the source wafer is used to pick them up. During the pick-up step, a PDMS stamp mounted on transparent glass is aligned and brought into contact with the desired devices on the source wafer, and is then pulled back at a high velocity. The tethers of the anchoring system are broken at engineered locations by pulling rapidly, allowing the devices to be picked up and adhered to the stamp posts [27, 28].

In order to print the coupons, the stamp is moved over the target by automated systems, then the device is aligned to the desired location on the wafer, the stamp is lowered, and the coupon is printed. During the printing process, the stamp is slightly overdriven and sheared to the side, then slowly detached from the target. This results in a low adhesion strength between the device and the stamp, which leaves the device adhere to the wafer target. The bond to the wafer target can be a direct bond using van der Waals forces or can be enhanced by having a thin polymeric layer as a adhesive layer on the receiving substrate [29, 30].

Note that when the stamp is placed onto a target, the relative adhesive strength between the device and the stamp should be less than that between the device and the target [26]. In order to achieve this, micro-tips can be introduced as surface relief on the PDMS surface to allow for variable contact areas [31]. Shear loading is another method that can be used to modulate the adhesion of the stamp [32].

Micro-transfer printing technology offer several new possibilities due to the heterogeneous integration. It can achieve integration with flexible or heat-conductive backplanes, as well as heterogeneous integration of multiple materials on a common platform, resulting in miniaturised

chips. Also one can benefit from reclaiming and reusing the original substrates to reduce the production cost significantly. Over the last decade, researchers have continuously advanced the technology in order to demonstrate novel classes of devices developed from micro-assemblies. Thus, this technology has been applied to a wide range of applications including photovoltaics [33], optical communications [34], optoelectronics [1, 35], and displays [36]. There is no doubt that integration chips require smaller and more efficient light sources for many applications. Thus, the first part of this thesis focuses on the transfer printing of ultra-thin micron-sized GaN-based LEDs and the issues associated with their transfer printing and device efficiency. As such, the next sections will provide a brief history of the development of GaN based LEDs. The fundamental operating principle for LEDs is described, and the benefits and limitations of growing nitrides on different substrates are also discussed.

1.2 Light-emitting diodes

1.2.1 Brief history of GaN LEDs

The fundamental operation of a LED is generation of light when electric current is passed through it. This effect is called electroluminescence (EL) and was discovered by Henry Joseph Round in 1907 when he reported yellow electroluminescence from a piece of silicon carbide (SiC) [37]. It was nearly 20 years later that Oleg Vladimirovich Lossev rediscovered the same electroluminescence in forward-biased and reverse-biased point-contact diodes made from single-crystal SiC and conducted extensive studies on their characteristics. His observations of green light from a SiC metal-semiconductor rectifier under reverse bias and photographed of the first EL was published in Wireless World and Radio Review in 1924 [38]. The subsequent improvement in semiconductor films has led to the development of the first blue LED utilizing SiC films with proper p-n junctions. However, their low electrical to optical power conversion efficiency, due to the indirect bandgap of SiC, has diminished the utility of these devices [39, 40]. By the time the most efficient SiC LEDs had only an efficiency of 0.03% at 470 nm [41]. Thus, another material and process technology were required; gallium arsenide phosphide (GaAsP) diodes had already proven to be more efficient, and therefore work on SiC LEDs was discontinued.

Using GaAsP, Holonyak et al. started the era of visible LEDs operating at room temperature in 1962. In the following years, LEDs began to be mass produced and were initially based on

the red-emitting GaAsP material, which was closely followed by the green-emitting Gallium-Phosphide material [42, 43]. In their early days, these devices were used as indicator lamps and small displays in wrist watches.

In late 1960s, James Tietjen of Radio Corporation America (RCA) wanted to design a flat screen television. To accomplish this, he chose to utilize LEDs since they were a compact light source. A bright blue LED, however, was not available at the time to produce white LEDs using red-green-blue (RGB) pixels. The demand for producing the blue light push the researchers to find the materials which can generate blue light. Tietjen believed that the development of gallium nitride crystals would enable the production of blue LEDs due to its large bandgap. Thus, he assigned Herbert Maruska to develop a process based on hydride vapour phase epitaxy (HVPE) for growing thin films of gallium nitride [44]. In 1968, he succeeded in making single-crystalline GaN films [45]. It was found that GaN films always exhibit n-type conductivity without being intentionally doped, so the main challenge was how to achieve the required p-doping of the GaN to form a p-n junction LED [46]. Traditionally, p-n junction LEDs have been constructed from a sandwich of n-type and p-type layers, as exhibited in red GaAsPs and green GaP.

In 1969, Maruska attempted to dope gallium nitride with zinc, the element that provides p-type doping in GaAsP and GaP. He also experimented with magnesium, cadmium, mercury, and germanium, but none of these measures were successful. The lack of p-type GaN and poor crystal quality halted researchers from making blue LEDs for twenty years. The breakthroughs in GaN films began in 1986 with the significant improvement in the crystal quality achieved by coating sapphire with Aluminium Nitride (AlN) before growing GaN on top [47]. A process that is now widely accepted as a standard method of manufacturing high-quality III-nitride structures with reduced defect density. By then, new attempts had been made to produce an efficient p-type GaN. In 1989, Akasakis' group, revealed the first true p-type doping and p-type conductivity in GaN. A magnesium doping approach developed by Maruska and Rhines was used to achieve p-type doping, with the dopant being activated by low energy electron beam irritation (LEEBI) in this case [48]. After that Nakamura found that post-growth annealing had a similar effect on activating the dopant [49]. Following this breakthrough in 1989, advancements in p-type doping, particularly Mg activating dopants and superlattice doping, opened the way for efficient p-n junction LEDs. Eventually, Akasaki, H. Amano and S. Nakamura received the Nobel Prize in Physics in 2014 for their invention of high-efficiency blue light emitting diodes (LEDs) [50]. The invention of blue LEDs revolutionized lighting technology

and led to a wide variety of new applications since the complete coverage of the entire visible spectrum was now possible.

1.2.2 Fundamentals of LED operation

The simplest LED structure is based on a p-n junction as illustrated in Figure 1.2, where two heavily doped materials are grown subsequently. In p-n junctions, electrons from n-type materials will diffuse across their physical boundaries into the p-type layer, where they will recombine with existing holes. A similar process occurs with holes that diffuse to the n-type side. This results in a region near the p-n junction being depleted of free carriers. It is known as the depletion region. Depletion regions have no free carriers, so the only charge they have is from ionized donors and acceptors. As a result of these dopants, a region of space charge is created i.e. n-type donors and p-type acceptors which produce a potential known as diffusion voltage (V_D). The V_D is the potential that free carriers must overcome in order to diffuse to the neutral region of the opposing type of semiconductor. As a result of applying external bias, the p-n junction barrier is decreased or increased depending on whether forward bias is applied or reverse bias is applied. When forward bias is applied, electrons and holes are injected into regions of opposite conductivity type, increasing the flow of current. As the carrier diffuses into the opposite conductivity type, it will eventually recombine resulting in the emission of a photon [51].

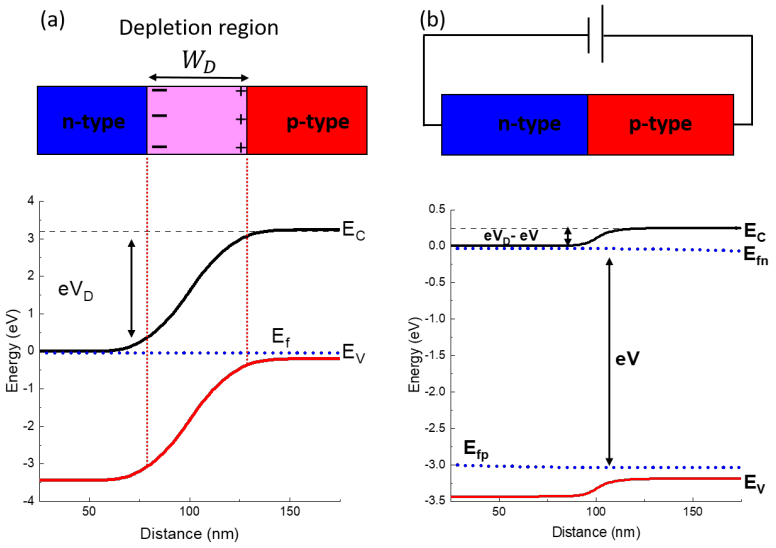

FIGURE 1.2: The GaN p-n diode under zero bias showing the depletion region and the corresponding energy band diagram. (b) a diode under forward bias (3 V) with a reduced depletion region width and changed energy band diagram.

The main disadvantage of the simple p-n structure is the diffusion of carriers. Eventually, carriers injected into semiconductors of opposing conductivity types will recombine. There is an associated diffusion length for each type of carrier before they recombine with one another. The Figure 1.3 (a) shows the distribution of carriers in a p-n junction under forward bias. After applying forward bias, majority carriers are free to diffuse widely across the junction to the opposite side. As soon as these carriers reach the opposite side of the junction, their identity changes to that of minority carriers and they can contribute to the recombination process over the distance of the minority carrier diffusion length (L_n). The carriers can diffuse a long distance to the opposite side of the junction, as illustrated in Figure 1.3 (a). As a result of the long diffusion distance, the carrier concentration is low and recombination occurs over a wide area.

Recombination rates can be calculated using the bimolecular recombination equation [52]:

$$R = Bnp \tag{1.1}$$

Where B represents the bimolecular recombination coefficient for the semiconductor, which measures the probability of radiative recombination in cm^3s^{-1}; for GaN, B is 2.2×10^{-10} cm^3s^{-1}. The electron and hole concentrations are represented by n and p, respectively. This means confining a high concentration of carriers in a very small area will result in increased radiative recombination and a reduction in the recombination lifetime. Typically, high-efficiency LEDs are designed around a heterostructure or quantum well structure in order to improve the recombination rate and optimize their efficiency. A schematic of a double heterojunction structure is shown in Figure 1.3 (b). It consists of a layer with a small bandgap (active region) grown between two large bandgap barrier layers. As a result, the thickness of the region where carriers recombine is determined by the thickness of the active region rather than the diffusion length, which is much shorter than a typical diffusion length. For instance, the diffusion length of electrons in p-GaN can range between 0.2 and 0.9 μm [53], while the thickness of the active region is in the range of a few nanometers. Therefore, carriers in these structures have a much larger concentration than those in homojunction structures. According to the Equation 1.1, higher carrier concentrations result in increased radiative recombination, for this reason high-efficiency LEDs are designed with double heterostructures [52] or quantum well (QWs) and today's best performing LEDs are considered to have multiple quantum-well regions sequentially deposited on one another.

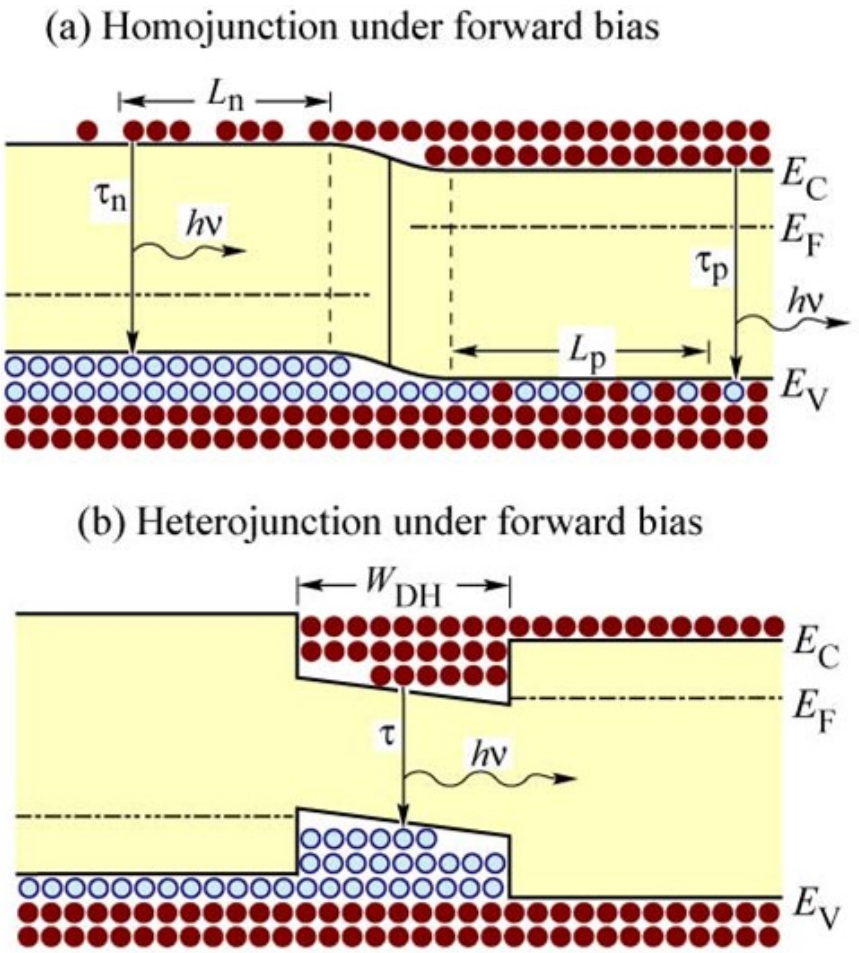

FIGURE 1.3: Under forward bias, the distribution of free carriers in (a) homojunctions and (b) heterojunctions. Adapted from [52].

1.2.3 GaN-based LEDs

Typical GaN LED structures consist of a thin p-GaN, active layer and n-GaN film on a substrate. In GaN LEDs, the p-type layer is mainly doped with magnesium (Mg) to create free holes, while the n-type layer is generally doped with silicon (Si) to create free electrons. A ternary indium gallium nitride (InGaN) alloy is used as the QW of visible GaN-based LEDs. Indium in these semiconductor materials can be tuned to emit light throughout the entire visible spectrum, while maintaining the direct bandgap. Figure 1.4 illustrates the bandgap energies of AlN (6.015 eV), GaN (3.41 eV), and InN (0.7 eV) as a function of lattice constant and demonstrates the wide range of wavelengths from deep-UV to the near-IR that III-nitrides can cover.

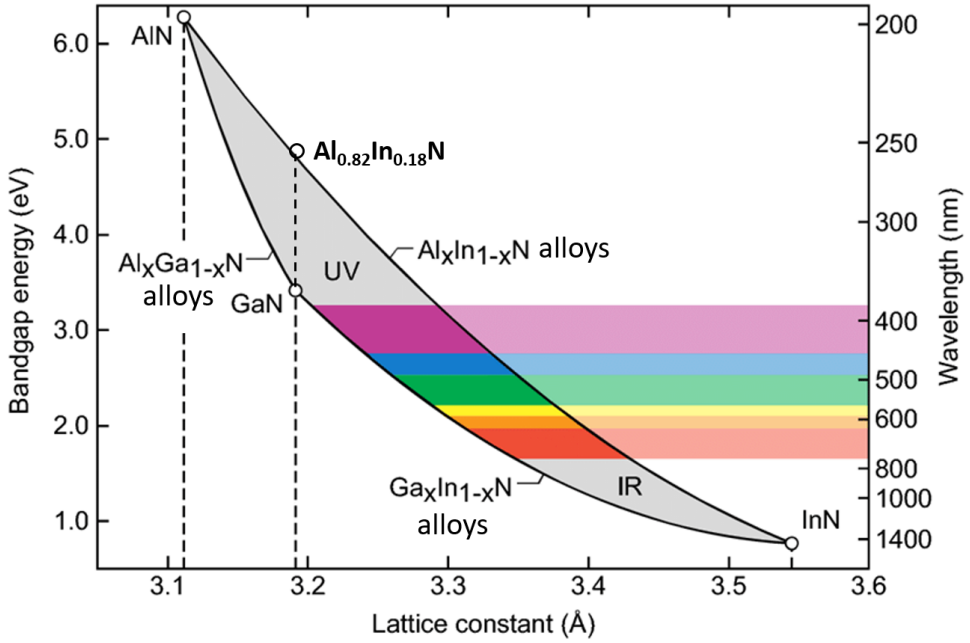

FIGURE 1.4: The band gap energy of nitride semiconductors and emission wavelength as a function of the lattice constant. Adapted from [54].

1.2.4 Efficiency of GaN LEDs

LED performance can be evaluated by analyzing their efficiency, which is mainly measured by four parameters: Internal Quantum Efficiency (IQE), Light Extraction Efficiency (LEE), External Quantum Efficiency (EQE) and Wall-Plug Efficiency (WPE).

Internal quantum efficiency (IQE) represents the number of photons (hv) emitted from the active region of the LED per second due to number of injected electrons per second. The IQE can be defined as:

$$IQE = \frac{P_{int}/(hv)}{I/e}, \tag{1.2}$$

Where P_{int} is the optical power emitted by the LED in the active region, and I is the current injected into the LED. Here hv represents the photon energy (h being Plank's constant). A higher IQE value indicates that a larger portion of the electrical energy is being converted into optical energy and emitted as light. The IQE of an ideal active region should be unity, however, different loss mechanisms come into play, limiting the IQE to be $< 100\%$. Ideally, all photons emitted by the LED active region should escape the LED active area (where 100% of the light would be extracted). However, internal light reflection and absorption reduce the amount of

light that can escape LEDs. The light extraction efficiency (LEE) is refers to the ratio of the number of photons emitted per second in to free space (P_{out}) to number of photons emitted per second from the active region P_{int}.

$$LEE = \frac{P_{out}/hv}{P_{int}/hv}\,, \tag{1.3}$$

The external quantum efficiency (EQE) is the overall efficiency of the LED and is defined as the ratio of the number of photons emitted, P_{out}, to the number of electron-hole pairs injected, I/e. EQE can be expressed as:

$$EQE = \frac{P_{out}/hv}{I/e} = LEE \times IQE\,, \tag{1.4}$$

The EQE takes into account both the IQE and the LEE, and provides a comprehensive measure of the efficiency of the LED. Finally, the wall-plug efficiency (WPE) is the overall energy efficiency of the LED semiconductor chip and is defined as the ratio of the optical output power, Pout, to the electrical power input, $I \times V$. WPE can be expressed as:

$$WPE = \frac{P_{out}}{I \times V}\,, \tag{1.5}$$

The transfer of electrical energy to optical energy is accompanied by losses both of electrons and photons, which reduce the WPE. In consequence, the WPE can be divided into the following components:

$$WPE = ELE \times EQE, \tag{1.6}$$

where ELE is the electrical efficiency, which is the amount of energy lost by electrons on their way to the quantum wells. These metrics provide a way to evaluate the performance of LED semiconductor chips and to determine how effectively electrical energy is being converted into optical energy and emitted as light.

Knowing the GaN crystal structure is essential for identifying the efficiency loss mechanisms. GaN has the wurtzite crystal structure (see Figure 1.5 (a)). Wurtzite is a hexagonal structure in which gallium atoms are covalently bound to nitrogen atoms. Each atom has four tetrahedral

bonds, and the electronegativity of nitrogen is stronger than that of gallium, indium, and aluminum, providing strong ionic properties. The structure of wurtzite is non-centrosymmetric and lacks inversion symmetry in the c-direction, it forms polar bonds, and it has alternating layers of gallium and nitrogen. As a result of these alternating layers, the charges within the bulk cancel each other out, but fixed sheet charges exist at the surface (negative at the Ga-face and positive at the N-face).

The GaN based LEDs are mainly grown on the [0001] direction. In this direction spontaneous polarization exists which leads to a polarization induced electric field. Induced internal electric field due to the polarization causes band-bending, called the quantum-confined Stark effect (QCSE) [55]. As a result of this property, the overlap between electron and hole wave functions is reduced (see Figure 1.5 (b)), which reduces radiative recombination and, consequently, IQE. Another factor contributing to the low radiative efficiency and IQE of GaN LEDs is the very high dislocation density which acts as nonradiative recombination centers [56]. Dislocation density is caused by a lattice mismatch between GaN and the substrate; therefore, the type of substrate will affect the number of dislocations.

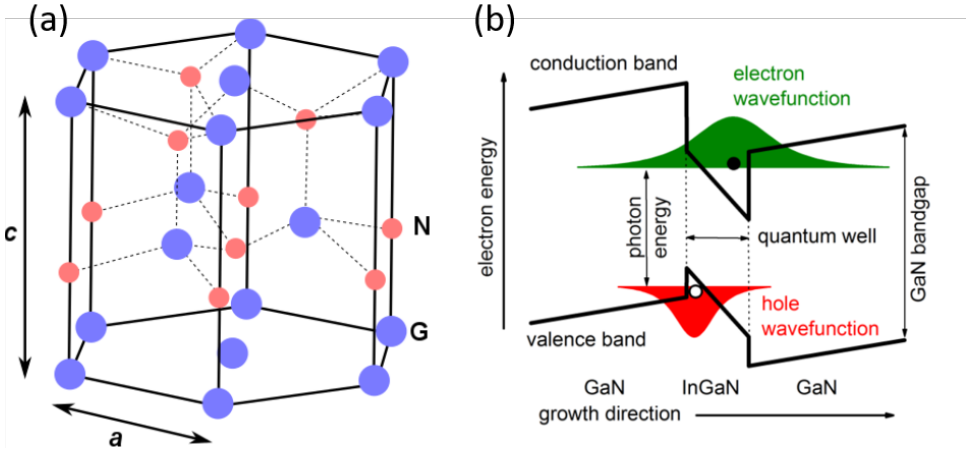

FIGURE 1.5: (a) The crystal structure of wurtzite GaN. Dashed lines indicate Ga-N bonds. (b) An illustration of the effects of polarization on an InGaN/GaN quantum well growing in the common Ga-polar or [0001] direction. Adapted from [57]

As the LED wafers used in this research were purchased from a commercial vendor, we were unable to control their IQE. In contrast, we could increase the EQE of μLEDs by increasing their light extraction efficiency. Even if the internal quantum efficiency of III-nitride LEDs is optimized, the external quantum efficiency is still largely determined by the efficiency of light extraction. Conventional GaN LEDs with flat emission surfaces suffer from low light extraction efficiency because of the large difference in refractive index between GaN (n$\sim$ 2.5)

and air (n$\sim$ 1) which results in low critical angle. Therefore, a significant portion of the light generated within the LED active region will be trapped within the semiconductors. Therefore, the enhancement of the light extraction efficiency for GaN LEDs is extremely important to achieve high external quantum efficiency. As part of this thesis, the focus was on improving light extraction in a manner that is compatible with transfer printing. Furthermore, the unique properties of micro transfer printing were used to improve the collected light from GaN LEDs.

1.3 GaN LEDs on various substrates

As stated earlier, the main step in transfer printing is the release of coupons/devices from their growth substrates. There are several different technologies that can be used to release devices depending on the type of substrate. Each substrate has its pros and cons. In the section below, we will discuss the advantages and disadvantages of each substrate and the methods that may be utilized to remove it.

1.3.1 Advantages and disadvantages of sapphire substrate

Sapphire is one of the most commonly used substrates for epitaxially growing GaN-based LEDs, since sapphire has a wide gap transparency, a robust structure, a low cost, and the ability to withstand high temperatures [58]. There is however a high thermal ($\sim -25.5\%$) and lattice ($\sim 13\%$) mismatch between sapphire and GaN, resulting in a high density of dislocations in the epitaxial layer of GaN, which can reach $10^9 - 10^{10}\ cm^{-2}$. These dislocations cause non-radiative recombination of electron-hole carriers, which ultimately leads to a reduction in the IQE of LEDs. Moreover, the large mismatch in coefficient of thermal expansion (CTE) between GaN ($5.59 \times 10^{-6} K^{-1}$) and sapphire ($7.5 \times 10^{-6} K^{-1}$) causes a high level of compressive stress in the grown film when it cools down from deposition temperature. An effective method of reducing stress is to employ a buffer layer, such as low temperature (LT) AlN [47, 59]. Poor thermal conductivity of sapphire also poses a problem when it comes to the LEDs, especially when the use of high-power and high efficiency LED is being considered. A LED chip's junction temperature can be up to approximately $70 - 100\ ^{\circ}C$. Luminous efficiency and device lifetime would be reduced by too high a junction temperature. As sapphire has poor thermal conductivity (k $\sim 0.35\ W(cm.K)^{-1}$) at $100\ ^{\circ}C$, impede dissipating heat, reducing the LEDs' lifetime [60]. To resolve this issue, it would be beneficial to remove the growth substrate and

place the device on a heat conductive backplane. Various methods are available for removing sapphire, including laser lift-off, electrochemical etching, and photo-electrochemical etching.

1.3.2 Advantages and disadvantages of Si substrate

The development of GaN LEDs on different substrates, such as Si, has also been explored due to their lower cost and higher thermal conductivity, even though there is a lattice mismatch of 16.9% between GaN and Si.

One of the industry's key goals is to keep LED manufacturing prices low. The choice of substrate has been shown to have a significant impact on manufacturing costs. For such cost reductions to be achieved, silicon wafers must be large enough (6 or 8 inches) to enable a large number of devices to be produced for a minimum number of growth and processing runs. Sapphire substrates show their limitations in this aspect, since it is difficult to produce high-quality large area wafers [61]. In addition, Si substrates have much higher electronic and thermal conductivity (k$\sim$ 1.5 $W(cm.K)^{-1}$) than sapphire, which enhances their superiority for the fabrication of high-power LEDs [62]. These advantages make Si an attractive alternative to sapphire for fabricating low-cost LEDs.

In spite of the advantages of Si as a substrate for GaN LED growth, GaN-based LEDs on Si substrates still pose some disadvantages. GaN-based LEDs have a low light extraction efficiency, which results in poor performance. Light absorption through the material, total light reflection, and the area of the electrode are the primary factors which influence the LEE. Firstly, while light absorption by materials is inevitable, some substrates are more absorbent than others, reducing the amount of light emitted. The energy gap of Si is 1.12 eV, which is less than the wavelength of visible light, resulting in the fact that more than half of the visible light generated by the active region of LED is absorbed by Si substrates, thereby reducing the EQE of LEDs [63, 64]. This issue can also be overcome by removing the growth substrate (here Si) during chip fabrication to prevent the absorption of light by the substrate. A wet chemical etch can be used to selectively remove Si, thereby resolving this issue. In this thesis, a wet chemical etching technique is utilized in order to separate the Si substrate. Additionally, roughening technique in conjunction with transfer printing is used to reduce the internal light reflections due to the scattering effect and increase LEE. The details will be discussed in the later chapters.

Another issue associated with GaN LEDs on Si is that the GaN layers grown on Si substrate have a high tensile stress, which can result in cracks in the epi-structure during the cooling process. Tensile stress results from a large mismatch in CTE (-115%) between GaN ($5.59 \times 10^{-6} K^{-1}$) and Si ($2.6 \times 10^{-6} K^{-1}$) as well as mismatch in their lattice constant (16.9%) [65]. Despite the fact that different buffer layers (i.e AlN and AlGaN) and stress-mitigation architectures have been implemented into structures to achieve net-zero stress structures. This approach, however, may not be suitable for GaN-on-Si materials intended for release because after the removal of epitaxial silicon substrate, the strain would be partially relaxed in the GaN epilayer, which results in crack generating [66] or such anchored GaN structures often exhibit a significant bow that persists or increases after release. The presence of such issues poses a challenge for transfer printing and 3D integration, and supports the case for robust design processes. Simulation and compensation layer has been introduced in this thesis to resolve this issue.

1.3.3 Advantages and disadvantages of GaN substrate

The growth of GaN-based LEDs on free-standing GaN has attracted considerable attention in recent years. It is due to the fact that, despite the foreign substrates (e.g., Sapphire, SiC, and Si), the free-standing GaN substrates are completely matched in terms of the lattice and the CTE to the GaN epilayers. This has significant benefits for the development of high-quality GaN films and high-efficiency GaN-based LEDs. Improved crystalline quality of epitaxial films on free-standing GaN substrates would reduce non-radiative recombination between defects and carriers, therefore increasing IQE [67, 68]. Furthermore, the superior thermal conductivity of the GaN substrate (k$\sim$ 2.1 $W(cm.K)^{-1}$) allows the heat generated in the active region to be dispatched quickly [69]. Although the growth condition of GaN LEDs on a free standing substrate still requires process development to achieve high quality device [70, 71], the cost of a free-standing GaN substrate is the main obstacle that must be overcome in order to realize the fabrication of commercial LEDs on such substrates [72]. Therefore, the capability of releasing GaN layer structures from GaN substrates will enable the use of the highest performing devices (light emitting diodes and lasers) while retaining the ability to recover the expensive substrate. As GaN substrates are chemically inert, they cannot be chemically etched; additionally, laser lift off is not compatible with GaN substrates. Thus, our research focuses on the photoelectrochemical (PEC) etching technique, which is applicable either to GaN substrates or sapphire substrates.

1.4 Thesis outline

- **Chapter 2: Process optimization of GaN LEDs based on Si**

  In this chapter, the fabrication process of μLEDs compatible with transfer printing is outlined and the most critical steps to enable transfer printing of devices are discussed in detail. This includes optimizing the anchor to maintain the device in place during the undercutting process and to prevent the anchor from being etched. Optimization of the release mechanism by employing wet chemical etching in order to prevent cracks in the devices. A particular emphasis is placed on the management of stress. This is because transfer printing is most effective with flat devices, but GaN device on Si is commonly bowed after release as a result of inbuilt strain. We have therefore studied this issue through simulation and addressed it experimentally in this chapter.

- **Chapter 3: Light extraction improvement of transfer-printed LEDs**

  To enhance the light extraction, we developed an original integrated method for roughening the backside of released LEDs using wet chemical etching during the coupon preparation process. Then, to demonstrate the capability of μTP technology, ultra thin GaN LEDs were printed onto various substrates including fabricated deep trenches with coated reflector to boost the directional light output and their light output power was compared. The key characteristics of μLEDs are measured and analyzed before and after printing process in order to ensure that the fabrication process does not compromise the quality of the devices. Finally, the potential of the fabricated μLEDs was investigated for visible light communication.

- **Chapter 4: Lift-off of GaN devices by photo-electrochemical etching**

  The objective of this chapter is to present a technique for releasing GaN devices from substrates where selective chemical etching is difficult. Thus, the mechanism of photo-electrochemical etching and the requirement for the thick sacrificial layer to facilitate the printing process are discussed. In order to meet this requirement, we introduce a novel sacrificial layer with a configuration of InGaN/AlInN/GaN. The optimization of the sacrificial layer is discussed and compared with a conventional sacrificial layer (InGaN/GaN). It is shown that the inbuilt polarization can induce the formation of 2DHG at the interface of InGaN/AlInN and, as a result, increase the PEC etch rate. Additionally, this chapter discusses the effects of electrolyte and post-treatments on achieving a smooth surface after PEC etching.

- **Chapter 5: Conclusion and future work**

  An overview of the most significant results of this thesis along with recommendations for future research is presented in this chapter.

- **Appendix**

  The Appendix contains schematics of the materials used in the thesis, further analyses of the C-V results discussed in Chapter 4, and experiments illustrating the PEC etching of LED structures.

Chapter 2

Process optimization of GaN LEDs based on Si for transfer printing

2.1 Introduction

The goal of this chapter is to optimize the design and fabrication process of blue GaN-on-Si μLEDs compatible to micro-transfer printing technology. Devices that are compatible with transfer printing have unique designs that make it possible to retrieve them from their original substrate using elastomer stamps. Devices need to be released from the substrate and anchored properly on the surface to enable an effective printing process. A tether and an anchor are required to hold devices during the entire fabrication process and to fracture when required during transfer printing. A wide variety of optoelectronic devices have been implemented using these design and process strategies [1]. For instance, after demonstration of the first printable red LEDs with (Al)InGaP substrates on GaAs [73], the same strategy was applied to InGaN LEDs on Si in order to enable printing these devices. The first printable InGaN LEDs based on Si were demonstrated in 2011 by Rogers et al. [74]. In that work, wet chemical etching was used to release the devices and a GaN tether was used to anchor them during the undercutting process. Following this, in 2017, Bower et al. demonstrated full-color μLED displays using printable red, blue, and green LEDs having sizes ranging from 3 $\mu m \times 10 \mu m$ to 8 $\mu m \times 15 \mu m$ [75]. Despite these advances on printable LEDs, there is still plenty of room to improve the fabrication process in order to facilitate printing and improve printing yields.

One issue dealing with preventing the device from collapsing and anchoring it to the substrate during the undercut, especially when devices must be left in solution for an extended period of time for roughening. It can be challenging as the anchor must be defined and formed along the [110] crystal direction of Si [74], but the direction is not known to a precision better than one degree. This can cause the anchor to be partially etched during the undercutting process.

In addition, there are several mechanical limitations associated with the manufacture of GaN-on-Si wafers. These are predominantly related to the high inbuilt stress of GaN devices. Residual stress in the GaN LED wafer when grown on Si is associated with significant lattice and thermal expansion mismatch between GaN and Si during wafer growth which is performed at $1000°C$. This can result in tensile stress being induced in the epitaxial material, which can result in wafer bowing or in extreme cases cracking, which can pose technical issues for device fabrication. To overcome this issue the wafer manufacturers include the thick buffer layer (normally comprising of AlN and AlGaN layers) to control stress in the epitaxial stack [76, 77].

This method, however, may not always be suitable for GaN-on-Si material intended for transfer printing, and the compensating inbuilt stress will become evident when the device is released from the substrate, because the underlying region of Si substrate, which contributes to compensate the stress, is removed by chemical etching. In addition, during fabrication process, a number of additional dielectrics and metal layers are deposited on the LED devices, which can introduce additional stress that results in bending of released epi-layers. It has been often seen that such anchored GaN structures show a significant bow that persists or increases after the devices are released, which will cause printing failures and challenges in the post-print integration process [78]. This is particularly challenging for large size devices, e.g.$>$ 100 μm [79]. The schematic of suspended GaN device is presented in the Figure 2.1. Such issues will not only cause printing failures and hinder high yield, but also cause challenges in the post print integration process. Therefore, managing the stress to achieve flat devices after releasing is highly desirable, especially for transfer printing.

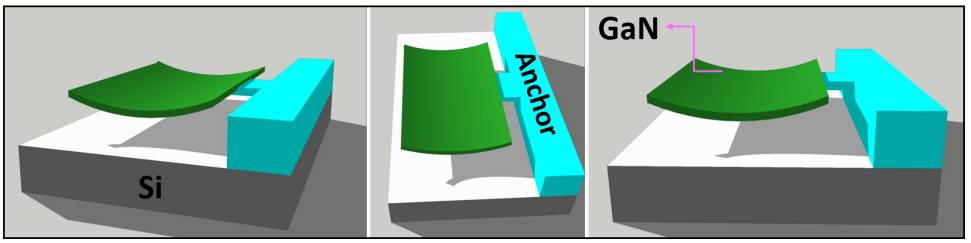

FIGURE 2.1: A schematic 3D view of a released GaN device anchored to a substrate that bowed as a result of the stress.

This chapter presents details of the fabrication process for GaN-on-Si μLEDs and techniques to address the above issues. The techniques used for fabricating efficient anchor/tethers, as well as the releasing process is described in Section 2.2. Moreover,to manage the intrinsic stress in GaN on Si, we proposed a stress compensation approach using SiN_x layers. By utilizing simulations, control of the residual stress by engineered SiN_x layers within the individual devices when released from the substrate could be compensated, resulting in a completely flat surface after transfer printing. Finally, simulation results are compared with experimental data. Methods will be discussed in Section 2.3.

2.2 Fabrication process flow of releasable LEDs

To produce releasable LEDs structure for transfer-printing, several unique considerations must be taken into account during process. Optimum anchoring is required to prevent etching. The size and type of tether need to be optimized to prevent device from collapsing during the undercut. Intrinsic stress and device bow need to be compensated to have successful printing. To meet all of these requirements efficiently, a process flow was developed. A brief outline of the process is described here with the steps described in some detail.

2.2.1 Wafer material

The InGaN based blue LED material grown on a (111) Si substrate was used due to its low cost and high chemical selectivity between GaN and Si that facilitates the releasing process. LED structures grown on (111) silicon wafer were sourced from commercial vendors. The detailed layer structure varied depending on the vendor but essentially the structure was common throughout. A cross-section schematic of the epi-structure used to fabricate the arrays of suspended InGaN LEDs for transfer printing is shown in Figure 2.2. The growth starts

with the deposition of AlN on the silicon substrate followed by a thick undoped GaN layer. Compensating AlN layers are included due to the different thermal expansion coefficient of GaN and Si and depend on the wafer diameter with the aim to minimize the wafer bow after cool-down from the growth temperature. After the compensating layers an n-doped GaN layer followed by multiple InGaN quantum wells emitting in the blue (450nm-480nm). The structure is completed with a p-doped GaN layer.

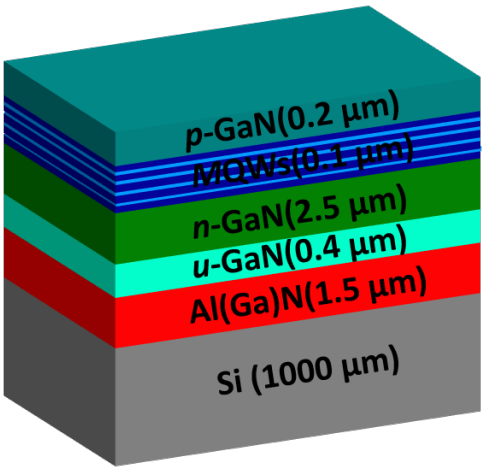

FIGURE 2.2: Schematic structure of the LED wafer.

2.2.2 Wafer surface cleaning

Cleaning a wafer's surface prior to fabrication is necessary to remove any adhering particles and organic/inorganic impurities. In addition, wafer surfaces cleaning before p-metal deposition is necessary to achieve a high quality ohmic contact.

On the p-GaN surface, carbon (C) and oxides may form during the epitaxial growth process, which act as barriers to hole transport and increase the p-contact resistivity. It is also possible for the surface to have residues of metal contaminants.

A solvent cleaning process with acetone and IPA, followed by DI rinse, is used to remove organic residues from wafer surfaces. Because solvents leave residues on wafer surfaces, the two-solvent method is used. Then to remove the native oxide, the sample dipped into buffered oxide etchant (BOE) for 5 minutes, as BOE can effectively etch silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), and rinsed with DI. Following that, samples were dipped in $1:1 = HCl:DI$ solution for 5 minutes to remove metal contaminants. Finally, the samples were cleaned with 45% potassium hydroxide (KOH) solution for 30 seconds as KOH is highly

effective in removing C. Oxygen free nitrogen (OFN) is used to dry the samples once they have been thoroughly rinsed with DI water.

2.2.3 P-contact deposition

Th fabrication process began with deposition of Pd p-contact by e-beam evaporation. To do this, semiconductor surface is patterned using a two level lift-off resist lithography. First the samples were baked at 150 $°C$ for 5 minutes to dehydrate the samples and adhesion promoter ($HMDS$) was spun at 120 $°C$. Pre-exposed photoresist ($PMGI\ SF11$) was then spun on the samples at 4000 rpm for 50 seconds and cured for 3 minutes at 180 $°C$. Following that imaging resist ($S1813$) was spun at 4000 rpm for 50 seconds and baked at 115 $°C$ for 1 minutes. The patterns were developed by exposing the samples through a chrome-quartz mask and dipping into developer ($MF319$). Samples were post-baked on hotplate for 3 minutes at 90 $°C$. Samples were dipped in Aqua-Regia for 30 seconds before metal evaporation to remove any dirt or oxide from the surface. Alloy such as bare Pd, Pd/Ni/Au and Ni/Ag/Ni can been used as p-contact. Here, the 40 nm Pd is then deposited as p-contact by electron beam evaporator and the samples placed in a solvent to remove the excess resist, leaving the patterned metal on the surface.

2.2.4 Mesa etch, insulation layer and metal deposition

To form the mesa, the samples need to be etched through p-GaN and MQW into n-GaN. An $S1828$ photoresist was spun at 4000 rpm for 50 seconds and developed, followed by baking at 90 $°C$ for 3 minutes to cure the photoresist. The patterned-photoresist was used as a mask on the sample. It is then etched by Cl_2 assisted inductive coupled plasma (ICP) to a depth of 900 nm to expose the n-GaN layer. After that, a 300 nm-thick SiO_2 insulation layer is deposited by plasma-enhanced chemical vapor deposition (PECVD). Then a third level of lithography was done to open a region for n-metal deposition and bond-pad, which were then etched by C_4F_6 assisted plasma etching. Afterwards, a two-layer lift-off resist of $PMGI\ SF11$ and $S1828$ was used to define the areas for the n-metal contact and bond pad. Initial test on different n-metals showed that $Cr/Pt/Au$ (70/30/200 nm) needs to be annealed at 250 $°C$ for 15 minutes in nitrogen ambient to form an ohmic contact, while Ti/Au (20/200 nm) forms ohmic contact without annealing. Moreover, it provides a lower resistance ohmic contact than $Cr/Pt/Au$ contact. Therefore, Ti/Au contact was chosen as the n-metal for the final devices. Note that the commonly-used Al-containing n-metal contact was avoided here as Al could be attacked by

the TMAH during the Si undercut process. Prior to loading for evaporation, the samples were treated with O_2 plasma to induce N-vacancies and enhance the ohmic contact. Afterwards, a Ti/Au of 20/200 nm layer was evaporated onto these open areas, serving as the n-contact as well as bond pads and finally, lifted-off the resist by MICROPOSIT Remover 1165. The functionality of the device was validated in this stage. The schematic of fabrication process flow is shown in Figure 2.3.

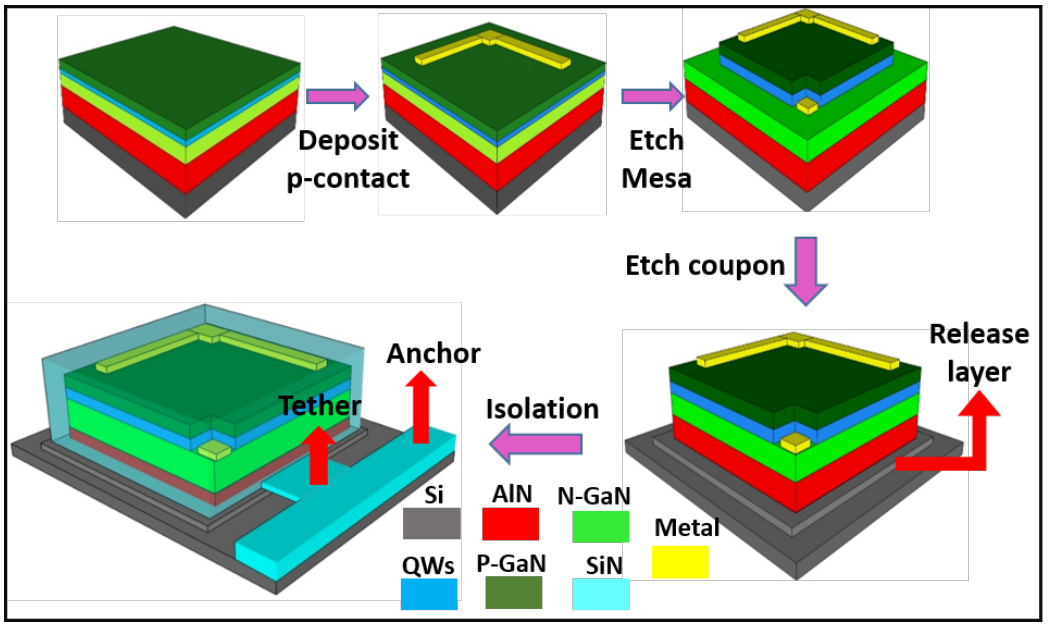

FIGURE 2.3: Schematic of the LEDs fabrication process.

2.2.5 Coupon and Si etch

To define the device lateral dimensions, a thick photoresist ($AZ4562$) was spun and patterned to protect the device for deep etching. ICP etching (gas: BCl_3/Cl_2) was used to etch through the epilayers till the Si substrate. Next, another level of lithography with $SPR220$ is done to define a larger platform of Si than the coupon size. In order to expose the fast-etching sidewalls of Si, ICP (gas:SF_6/C_4F_8) was used to continue etching deep into the Si substrate with a depth of 1 μm. Deep etching facilitates the etching process by exposing a larger surface of the material and assisting the solution to circulate underneath the suspended layers.

2.2.6 Define anchor and tether

Finally, to prepare the LEDs for releasing and the following transfer printing, 1 μm-thick SiN_x was deposited by PECVD. SiN_x is widely used as a hard mask in the microfabrication industry

due to its low etch rate (100 times less than Si) in alkaline KOH baths. In this step, the plasma frequency was adjusted to control the stress of the PECVD-deposited SiN_x layers to achieve flat devices. Detailed information will be provided in Section 2.3.

A final level of lithography was done to pattern and form anchors along the Si $< 110 >$ and tethers perpendicular to this direction. The anchor/tether system is used to support the suspended devices, preventing them from collapsing after releasing from the substrate. So careful designs are required to ensure that they are strong enough to anchor the devices, but also can break easily during the pick-up process. Different attempted configurations for tether and anchor design were tested to find the optimum size.

2.2.6.1 Tether tests

For devices with the size of 50×100 and 50×200 μm^2 for example , we found that narrow tethers of 10 microns in width are more likely to break due to stress during undercut, leading to device collapse, whereas tethers of 15 microns in width were stable during undercut, as illustrated in Figure 2.4.

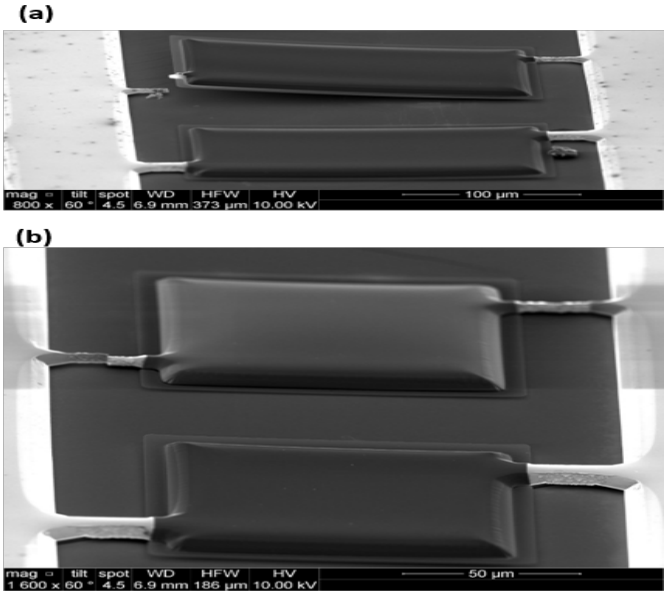

FIGURE 2.4: Comparison between two tether widths (10 and 15 microns) for various coupon sizes (a) coupon with size of 50×100 μm^2 and (b) coupon with size of 50×200 μm^2.

In terms of the number of tethers, we investigated two different sized devices, i.e. 50×100 μm^2 and 100×100 μm^2, with either one or two tethers, to check how it might affect the stability of devices during undercut. As seen in Figure 2.5 (a-b), In both types of devices, both samples with one and two tethers of the same width were found to be stable. Although one tether

was found to be sufficiently strong to hold the devices during the undercut, it cannot keep the devices in a flat position, especially for the long coupon like 150 μm as shown in Figure 2.5 (c). For small and short devices, however, such an issue is not significant. It should be noted that GaN epilayers were used as tethers in these tests. Despite the fact that a GaN tether with a sufficient width can support the device during the undercut, it was not successful in being picked up for printing due to its excessive thickness and and difficulty in breaking it. To resolve this problem, SiN_x is used as a tether for further experiments.

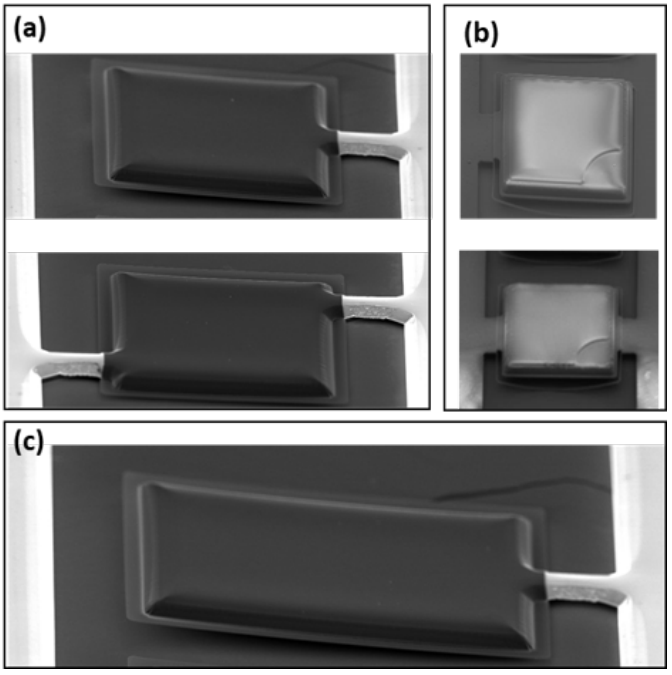

FIGURE 2.5: Comparison stability of devices with one and two tethers for different shape of coupons (a) coupon with size of 50×100 μm^2, (b) with sized of 100×100 μm^2. and (c) rectangular coupon with size of 70×150 μm^2.

2.2.6.2 Optimization of anchors to enable releasing and roughening the devices

Two type of anchors were explored to identify the stability of devices during the undercut and ease of transfer printing. Figure 2.6 illustrates the fabrication process for two different anchor types.

In first type of anchor, after mesa etch and metal evaporation, thick photoresist ($AZ4562$) was spun and developed, followed by dry etching to define the coupon with size of 100×100 μm^2, and form anchor with width of 30 μm along the Si [1-10]. Then, 1 μm-thick SiN_x was deposited by PECVD and then patterned using PR and dry etched to passivate the structure and form tethers perpendicular to the direction of anchors. This design has an anchor consisting of an

epilayer and SiN_x with a SiN_x tether. It then further etched into Si substrate (1.2 μm) to prepare the LEDs for releasing and the following transfer printing (see Figure 2.6). As it seen from schematic Figure 2.6 (d) due to the deep etch into Si substrate, Si-plane sidewalls of Si in anchor could be exposed to the solution during the undercut. Hence, small misalignment to Si crystal resulted in anchors being partially etched, so backside roughening of the device is impossible. As can be seen from Figure 2.6 (e), the majority of the anchor is etched during undercut.

This practical issue was addressed by proposing a novel approach and introducing another type of anchor system. The anchor in this design was fabricated with SiN_x and located on Si substrate. For this purpose, first LEDs with size of 100×100 μm^2 were defined by ICP etching through the epi-layers till the Si substrate. A larger Si platform of size 120×120 μm^2 was defined by lithography and then further etched ~ 1.2 μm deep into Si substrate for the purpose of release. Finally, to prevent the LEDs from collapsing during release, 1 μm thick SiN_x was deposited by PECVD and then patterned to form anchors and tethers. The anchors were orientated along the Si $< 110 >$ direction in which the etching rate of Si is much faster than that of Si $< 111 >$, therefore, devices which are tethered with anchors can be released from substrate using wet etch. In this design, anchors and tethers are fabricated from only SiN_x. Optical images of process including coupon etch, Si etch and isolated device with SiN_x are shown in the Figure 2.6 (f-h). Figure 2.6 (i) shows a schematic of a fabricated device with an anchor formed. This structure differs from previous ones in that the Si-plane sidewalls of anchors cannot be exposed to the solution. As a result, slight misalignment with respect to the Si $< 110 >$ will not result in a problem. This is because Si must be etched vertically in $< 100 >$ directions before it can be etched laterally underneath the anchor. Thus, a fully undercut device can remain in solution for a longer period of time without collapsing for roughening purposes. As shown in the Figure 2.6 (j), anchor remains intact and is not etched during undercut.

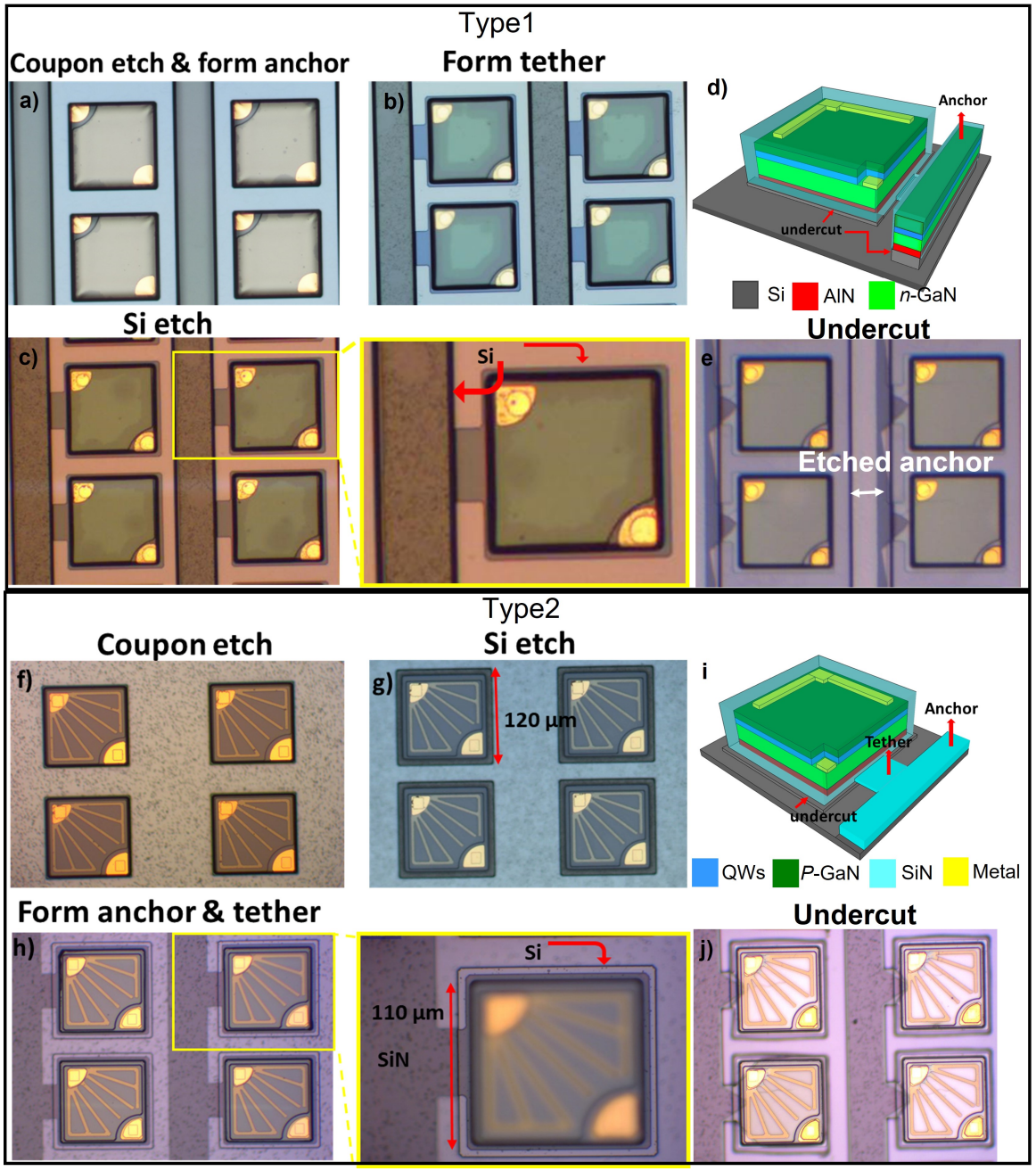

FIGURE 2.6: Optical images of anchor type 1 process flow (a) Etching a coupon and forming an anchor consisting of GaN epilayers. (b) Formation of tether using SiN_x. (c) Deep dry etching of Si (d) Schematic of fabricated LED (e) Released coupons with etched anchor after undercut. Optical images depicting the process flow of anchor type 2 (f) Coupon etch (g) Define a larger Si platform and dry etch (h) Form anchor and tether with SiN_x (i) Schematic of fabricated LED with SiN as anchor (i) Fully undercut coupons.

2.2.7 Undercut of LEDs from Si substrate

The anisotropic etching of Si enables wet chemical etching to be used to separate the GaN LEDs from the Si substrate, as will be demonstrated in this section.

A wet chemical etching process is known for its anisotropic effects, particularly in the case of specific wafer plane orientations on silicon wafers. Silicon has a cubic diamond lattice structure. In the cubic structure the crystal plans are perpendicular to the crystallographic directions. Figure 2.7 illustrates crystallographic directions that are commonly used for silicon etching and their corresponding perpendicular crystal plans. The atomic packing and available bonding in the crystal plane are the most crucial factors in the orientation-dependent etching of silicon. The low-index planes - (100), (110), (111) - and their position in the crystal lattice are depicted in Figure 2.7. The atomic lattice packing density in each plane is shown also in Figure 2.7. The $< 111 >$ direction shows the highest atomic packing density, while the $< 110 >$ direction shows less dense packing. Accordingly, $< 110 >$ exhibits significantly faster etch rates than the $< 100 >$ and $< 111 >$ directions. This can be explained by the density differences between the dangling bonds and the backbonds on the silicon surface [80]. The dangling bonds are located on the surface of a crystal plane, while the backbonds are located in the subsurface of the plane. A dangling bond is partially bonded to a silicon atom beneath it. As shown in the Figure 2.7 on the (100) plane, the atom from the center has two dangling bonds and two back-bonds. In the (110) plane, there are three dangling bonds and three back bonds (two of which are exposed) that can react. A crystal plane with a high density of dangling bonds will cause much instability, leading to an elevated etch rate. Unlike Si (110) planes, the Si (111) planes only contain one dangling bond. An atom on the (111) plane is supported by three equivalent Si-Si backbonds, which enhance the mechanical stability of the Si(111) surface, resulting in a slower rate of etching. This means that for anisotropic etching, the number of dangling bonds plays a crucial role in the etch rates of the different planes.

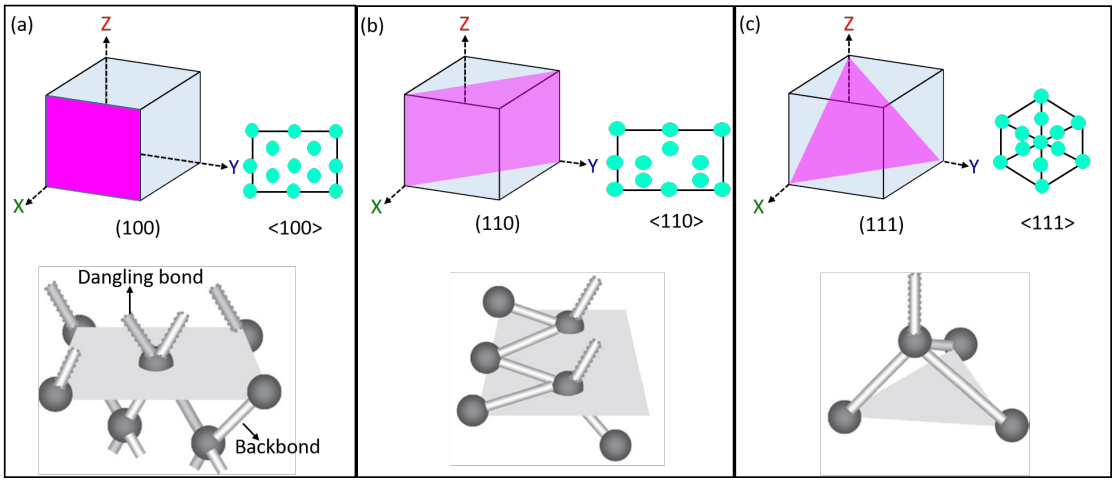

FIGURE 2.7: Silicon crystal atomic planes (3D cube) and crystallographic directions (atomic lattice) and their corresponding configuration of Si-Si covalent bonds for a)(100), b)(110) and c)(111) low-index planes, respectively. The highlighted atoms are those composing the highlighted plane. Dangling bonds are indicated by dotted lines. The covalent bonds inhibiting one atom are illustrated in part. Adapted from [81].

As stated before, the method for releasing these devices from the Si substrate exploits the significant differences in etch rates (>100×) [82, 83] for removing planes of Si(110) compared to Si(111) with wet chemical etching using potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). To take advantages of anisotropic etching of silicon, the arrays of devices are configured such that two sides of each device lie perpendicular to $< 110 >$ and anchored formed along the Si$< 1\bar{1}0 >$ and tethers perpendicular to this direction. In the $< 110 >$ direction, the devices are closely packed (spacing of $25\mu m$ for this example, but with values that can be as small as $2\mu m$). A schematic illustration of an array of devices anchored on a Si 111 wafer is shown in Figure 2.8.

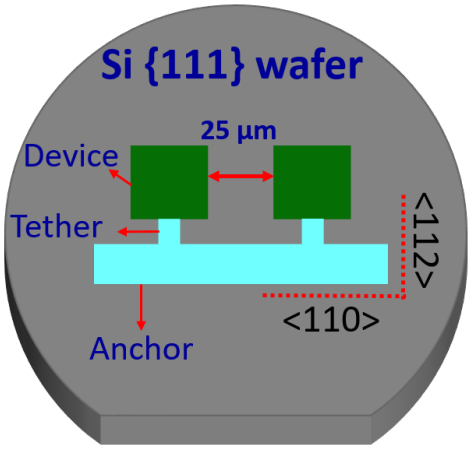

FIGURE 2.8: A schematic of devices with a designed orientation on a $< 111 >$ oriented Si wafer.

For undercutting the devices, once the devices were fabricated along appropriate directions, the samples were first immersed in BOE for 10 seconds to remove any oxide. Then, the devices are released from the Si substrate by removing a thin layer of Si underneath the GaN epi-layers using hot 5% TMAH wet etching. It has been found that the temperature of the solution plays a significant role in the etch rate and quality of the released devices. As can be seen from Figure 2.9 (a), undercut etching in TMAH at high temperature ($> 70°C$) resulted in micro-scale cracks on the epi-layers, especially for large size devices, which can be attributed to the high etch rate ($\sim 2.5\ \mu m/min$) causing fast strain relaxation. This cracking issue was resolved by performing the release etch at a lower temperature, i.e. $50°C$, which has an etch rate of ($\sim 1\ \mu m/min$).

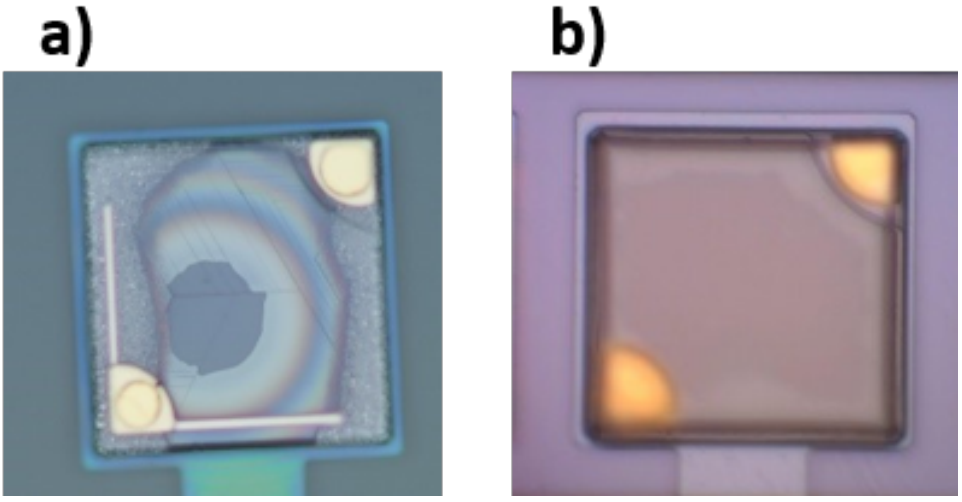

FIGURE 2.9: Optical images of devices after full undercutting using TMAH (a) at $70°C$ (b) at $50°C$.

As shown in Figure 2.10, during the etching process, anchors oriented along the Si $< 1\bar{1}0 >$ direction are minimally etched while the etching under the devices is fast. This is due to the fact that, the wet etching of Si with TMAH or KOH is highly anisotropic on $< 111 >$ oriented Si substrates, i.e., the etching rate of the $(1\bar{1}0)$ planes is much faster than that of the (111) planes or their projections.

As demonstrated in the Figure 2.10 (d) devices were held suspended above an air gap by a tether after completion of the undercut. The total thickness of the suspended devices after separating of the substrate (Si) is approximately 5 μm.

The backside of the released devices is usually flat and smooth when the undercut is just finished. By increasing the etching time, however, the AlN/AlGaN buffer layers are removed

and N-polar GaN is exposed to the etchant, leading to formation of pyramids on the underside surface. This roughening is beneficial for scattering the extracted light from LEDs and as a result increasing the light output power, details will be provided in the next chapter.

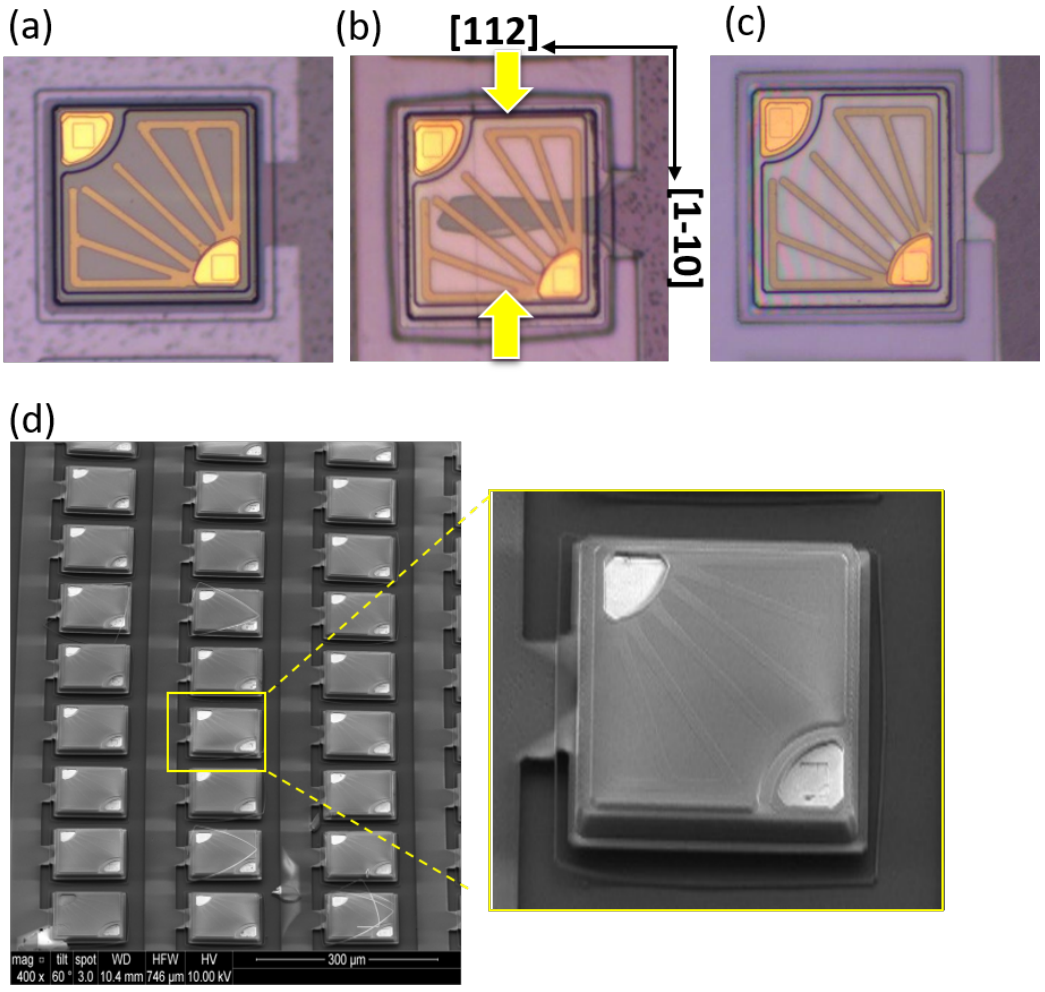

FIGURE 2.10: Optical images of device with size of 110 × 110 μm^2 (a) before undercut, (b) during undercut and (c) after fully undercut. (d) SEM image of array of released LEDs with detail of an individual device.

2.3 Stress management

As discussed previously, GaN devices suffer from significant bowing after release which makes transfer printing and 3D integration challenging, particularly when a robust design process is required. As such, managing the stress is extremely critical in order to achieve a flat device after the release. In order to minimise that bending we need to understand its effects through simulations and to control the bending through stress compensating layers. Therefore, to manage the intrinsic stress, for GaN-on-Si LED material, we proposed a stress compensation

approach utilizing SiN_x layers based on COMSOL simulation. It is worth noting that the stress of SiN_x can be controlled by the deposition condition. We will describe the method in the following section.

2.3.1 Methods

In order to estimate deformation and curvature which is generated during the device process, we used the commercial COMSOL software to simulate the thermal stress caused by the PECVD deposition of SiN_x layers on the devices. COMSOL combines Heat Transfer and Solid Mechanics physics for the Thermal Stress interface. The thermal stress interface solves for the stress and displacement due to thermal expansion. COMSOL requires the definition of the Young's Modulus, E, and the Poisson's ratio, ν, of each material to calculate the stresses, strains and deformations due to thermal expansion. The expansion is dependent upon the coefficients of thermal expansion, α, which need to be specified for this purpose. The coating temperature of layers also need to be determined to simulate the thermal induced bending of multilayer coatings.

A simplified LED structure is assumed, as shown in Figure 2.11, consisting of a 1.5 μm-thick AlGaN buffer layer and a 4 μm-thick GaN layer, is anchored with a 1 μm-thick SiN_x layer. The structure is 1.5 μm above the substrate.

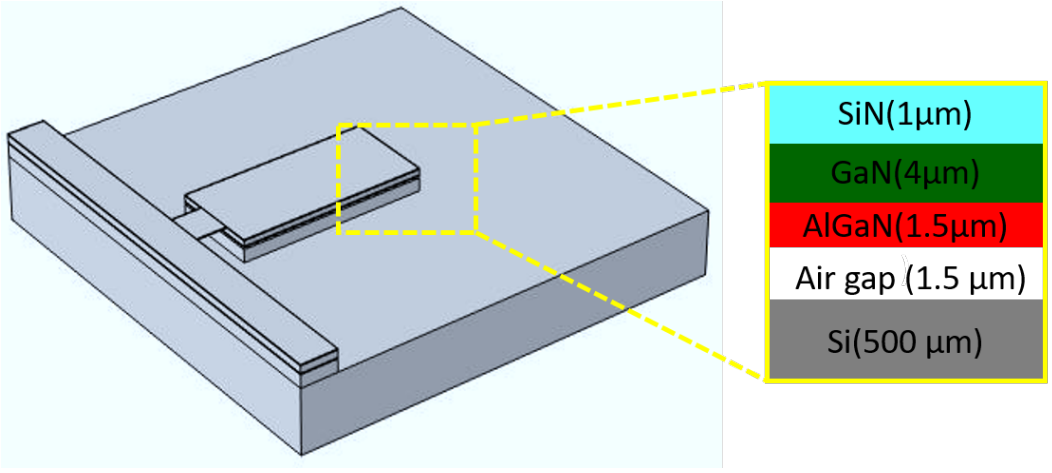

FIGURE 2.11: Schematic of released device used in COMSOL simulation.

The applied properties of materials for the simulation model are shown in Table 2.1.

TABLE 2.1: Applied material properties for the model.

Parameters	**Epi-layers**			**Deposited layer**
Material	Si	AlGaN	GaN	SiN_x
Thickness (μm)	500	1	4	1
Young's modulus (GPa)	180	185	210	230
Poisson's ratio	0.27	0.2	0.18	0.23
Thermal expansion coefficient (K^{-1})	2.59 $\times 10^{-6}$	5.2 $\times 10^{-6}$	5.59 $\times 10^{-6}$	1.55 $\times 10^{-6}$

All layers are active in their domains and all application modes share the same geometry, mesh and boundary. Note that to avoid computing power and fine meshing, a smaller size of Si substrate was chosen in the simulation. Simulators were run under steady state conditions. The stress within the epi-layers originating from epitaxial growth (called initial stress) is set according to the actual value in different LED wafers. The additional thermal stress of the LED is simulated when the high temperature (i.e. $300°C$) deposited SiN_x layer cools down to $20°C$. To incorporate the layer deposition on a deformed wafer the strain coming from the epi-layers has to be multiplied with the Young's Modulus and inserted as initial stress.

In order to calculate the initial stress of the wafer, a stylus profilometer was used to measure the GaN wafer bow at a scan length of 80 mm before and during fabrication. Figure 2.12 shows the curvature on the original wafer and the bow on the wafer during fabrication process.

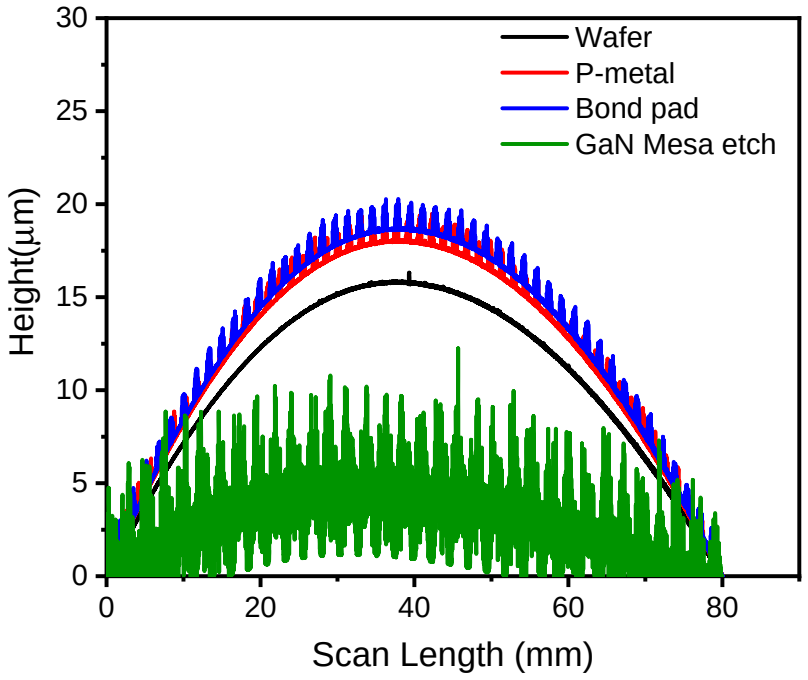

FIGURE 2.12: Wafer bow measurement on a GaN wafer performed using a stylus profilometer on a scan length of 80 mm during the fabrication process.

The stress of thin films was then computed using the Stoney Equation (2.1) in accordance with the wafer bow.

$$\sigma = \frac{1}{(6 \times R)}(\frac{E}{1-\nu})(\frac{t_s^2}{t_f}) \tag{2.1}$$

where t_s is the thickness of the substrate, t_f is the thickness of the film, E is the Young's modulus, ν is the Poisson ratio, and R is the curvature, which can be estimated using the wafer bow. The curvature radius, R, in the bowing epi-wafer is expressed as:

$$R = \frac{d^2}{8 \times h} \tag{2.2}$$

Where d denotes the diameter of the wafer and h denotes the bow of the wafer.

The calculated stress in each step of fabrication is presented in the Table 2.2.

TABLE 2.2: Calculated stress of wafer before and during microfabrication process of LEDs.

Fabrication process steps	**Calculated stress (GPa)**
Wafer/pre-stress	0.23
P-metal	0.28
Bond pad	0.29
GaN mesa etch	0.07

Figure 2.12 demonstrated that wafer is not completely flat and suffers from compressive stress before the process and it increases by deposition of metal and the protective layer, after etching the coupon stress will be released due to the fact that most part of the material is gone and smaller area can release the stress. As flat devices are required for high-yield transfer printing, so exact calculation of curvature in multilayered coating is essential for understanding the curvature generation depending on the process.

2.3.2 Investigation of the effects of initial wafer stress on device formation

In order to investigate the effect of the initial stress of the wafer before deposition, simulations were performed for a flat substrate (stress-free layer) and for a curved substrate with 70 MPa initial compressive stress. Note that in this instance, stress compensation was not considered in order to examine only the effect of initial stresses of wafer on device deformation. A coupon with a size of $70 \times 300\ \mu m^2$, with the same structures as in Figure 2.11, was considered for simulation.

The results show that the released coupon suffers from tensile stress, (bend upwards), with approximately 7.5 μm deformation for flat substrate, however, including the initial stress in the epilayer causes further deformation to nearly 10 μm after SiN_x deposition. Since our received wafer is not flat, the initial stress cannot be neglected for curvature calculation.

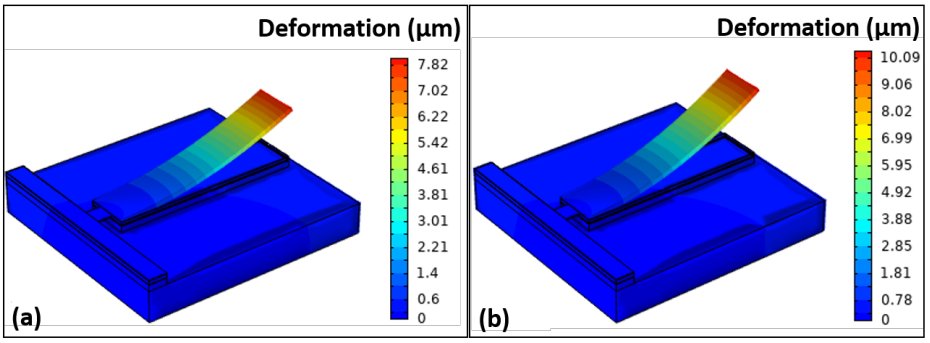

FIGURE 2.13: Deformation comparison of released LEDs with size of 70 × 300 μm^2 due to thermal stress a) SiN_x deposition on stress-free epilayer b) SiN_x deposition on wafer with initial compressive stress.

Furthermore, simulations were performed for rectangular coupons of different sizes (70 × 150 μm^2 and 70 × 300 μm^2 in order to determine if deformation will change with device size. As it can be seen from Figures 2.14(a,b) larger devices suffer from more deformation which is in good agreement with experimental data shown in the SEM image Figure 2.14(c).

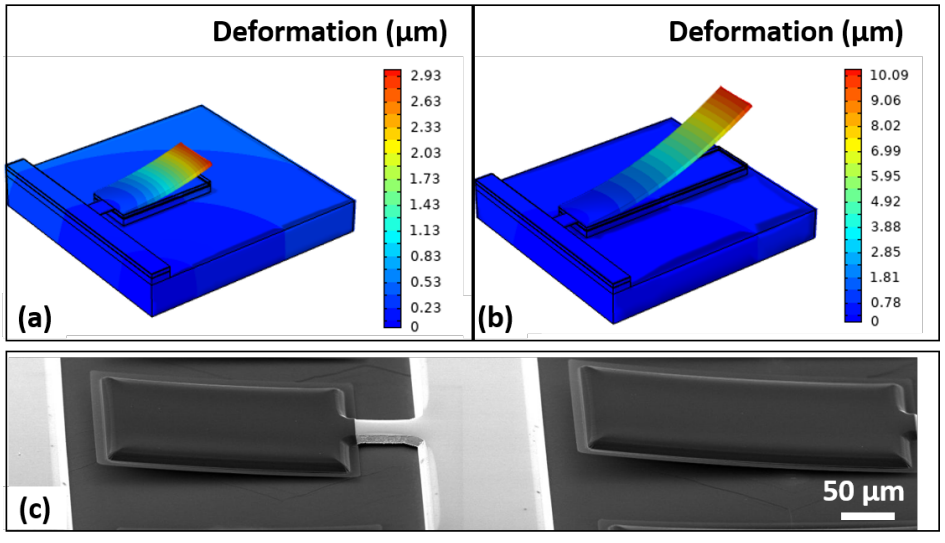

FIGURE 2.14: Deformation comparison of released LEDs due to thermal stress (a) Coupon with size of 70 × 150 μm^2 (b) Coupon with size of 70 × 300 μm^2. (c) SEM images of released LEDs with corresponding sizes.

2.3.3 Investigation of the effects of compensation layer on device flatness

To investigate the effect of stressed-deposited SiN_x on the released devices, thermal stress simulation was carried out for 1 μm SiN_x with neutral, tensile and compressive stress with respect to substrate. The geometry in the model was defined by using blocks of different materials with dimensions of 110 × 110 μm^2 and varying thickness. Figure 2.15 (a) depicts the schematics of the simulated structures. The stress within the epilayers originating from epitaxial growth is set to 70 MPa compressive stress to agree with the measured value in the LED wafers after mesa etch. A simulation of LED thermal stresses is performed when the SiN_x layer deposited at 300°C cools to 20°C, and the results are shown and analyzed.

It can be seen from Figure 2.15(b-c) that the SiN_x layer with neutral stress and with 200 MPa tensile stress cause upward deformation at the edge of the released coupon of 1.4 and 2.5 μm, respectively, while the same thickness of SiN_x with 200 MPa compressive stress reduces the deformation value to 0.5 μm (Figure 2.15(d)). Therefore, it can be concluded that by controlling the stress of the deposited SiN_x layers, the residual stress within devices, when released from the substrate, could be compensated resulting in a completely flat surface after undercut.

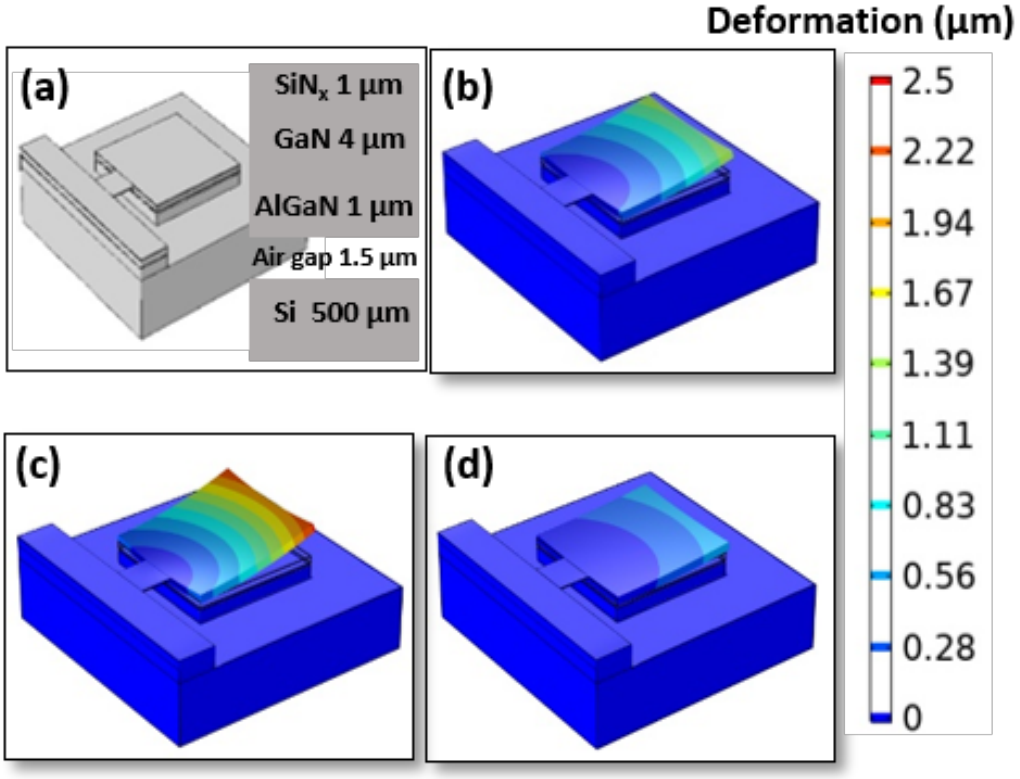

FIGURE 2.15: Simulated deformation comparison for the coupon of size 110 × 110 μm^2 by deposition of SiN_x with different stress. a) Simulation model,b) SiN_x with neutral stress, c) SiN_x with tensile stress, and d) SiN_x with compressive stress.

To compare the simulation results with experimental data, 1 μm of SiN_x with compressive and neutral stress was deposited by PECVD to the fabricated LED structures with size of 110×110 μm^2. It is noteworthy that the stress of the PECVD-deposited SiN_x layers could be controlled by changing the plasma frequency. To be exact, deposition of SiN_x with PECVD with low-frequency and high-frequency excitation resulted in films with compressive and tensile stress, respectively. To calculate the stress of the deposited thin film, the curvature of the substrate was measured prior and after deposition of SiN_x with a profilometer. A Stoney equation was used to determine the stress of a thin layer. After monitoring the stress on the deposited layer, the same fabrication process as Section 2.2 was followed to release the device from the growth substrate. Then, devices were individually transfer printed to a new Si wafer using a PDMS stamp. On each wafer, several devices are printed to evaluate the variation between devices and measure an average device bow. Figure 2.16(a) illustrates the schematic for the printed devices. During transfer printing, pressure is applied after the device is printed on the new target to ensure that all surfaces are in contact. When the PDMS stamp is retracted, the device is released onto the substrate, and if intrinsic stress is not compensated, it relaxes into a bowl-like shape. Optical image of devices with neutral stress SiN_x (Figure 2.16(b)) , shows Newton interference rings (circular interference pattern) due to the air gap between the device's bottom surface and the substrate. Interference fringe spacing indicates device bow as the air gap increases away from the device contact area [84]. Newton interference rings were not observed for devices with compressive stress SiN_x as shown in the Figure 2.16(c).

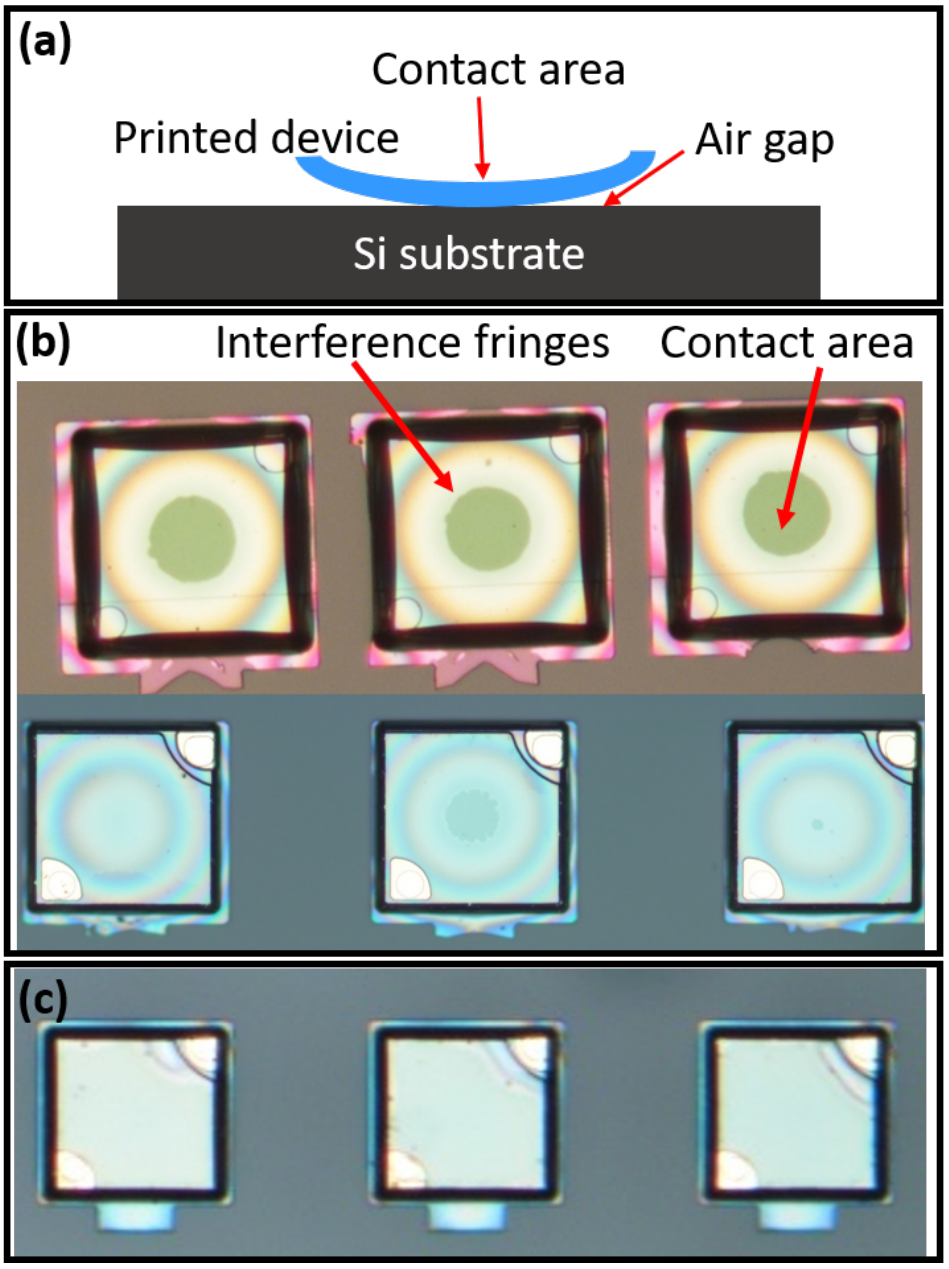

FIGURE 2.16: a) A schematic of a printed bowed device on Si.Optical images of printed coupon with size of $110 \times 110\ \mu m^2$ with deposited SiN_x with (b) neutral stress and (c) compressive stress.

Device deformation also was investigated by measuring the curvature using a profilometer and using white light interferometry of the transfer-printed devices. Note that the total thickness of transfer-printed devices including the epilayers and the SiN_x layer is now around 6 μm. As shown in Figure 2.17(a), the profilometer measurement confirmed upward deformation of the device with neutral stress. From Figure 2.17(b), it is clear that the device with neutral stress in the deposited SiN_x suffers from net tensile stress and deforms upwards, which is in good agreement with simulation data. Simulation results and experimental data confirmed

that the intrinsic deformation and curvature of the released LEDs can be compensated by incorporating compressively stressed SiN_x layers which lead to flat devices after releasing. It is worth noting that, while bowed devices can be printed, the process has large failure rate, whereas all compensated (i.e., flat) devices are printed successfully.

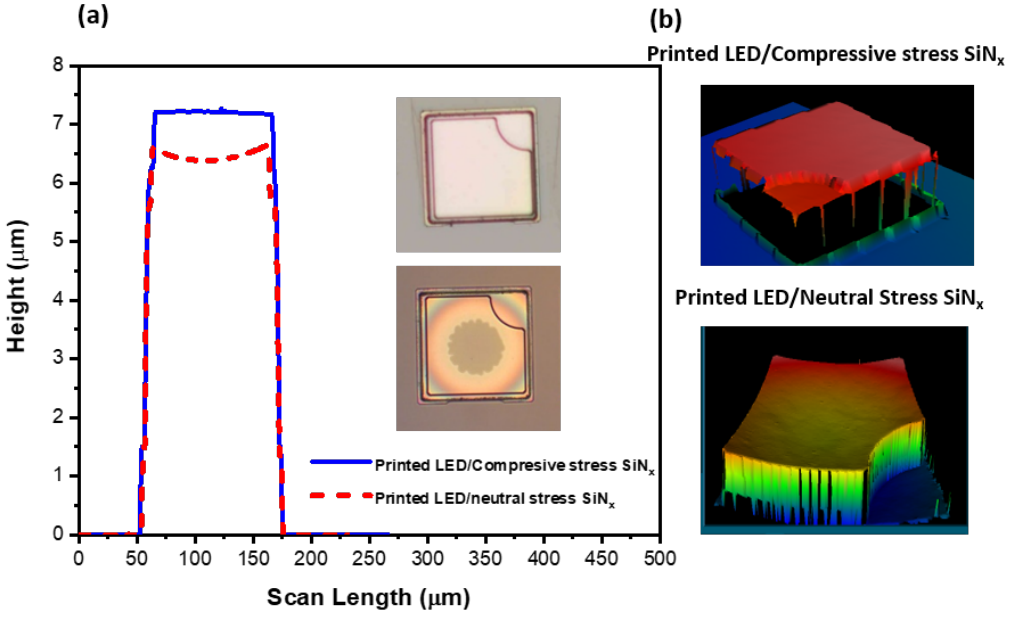

FIGURE 2.17: Device curvature with and without compensating SiN_x layer for device size of 110 $\times$110 μm^2; the inset shows optical images of printed LED swith compressive-stress SiNx(upper) and neutral-stress SiNx(lower). b) 3D images of the printed devices.

2.4 Conclusion

The results presented in this chapter shows the detailed fabrication process of GaN based μLEDs compatible for releasing and using in transfer printing technology.

To enable an effective printing process, GaN LEDs need to be prepared in a special way. This is so that they can be released from the substrate and anchored properly on the surface. A tether needs to be able to hold devices throughout the fabrication process and fracture when required during transfer printing. In order to accomplish this, precise engineering of their dimensions and material is crucial. It is seen that using SiN_x as a tether eases the printing process. For the tether to break and pick up easily during transfer printing, the underside of the tether must be etched completely. We have noticed that the etching of a wide tether takes longer than that of the entire coupon. This is due to the fact that the SiN_x tether is placed on a Si substrate. Therefore, the etching solution is not able to access the sidewalls of Si to etch

the tether laterally. As etching occurs from the edge of device, once the etching portion of the device is almost aligned with the edge of the tether (shown in Figure 2.18(a) with dashed line), the etching of the tether begins, since the solution can expose silicon underneath. Also, it is seen that etching of tether formed a triangle shape because (111) planes met and locked out the etching as the etching rate was too slow in this direction. Consequently undercutting the tether involves over-etching the coupon. Hence, it would be beneficial to locate the 2 tethers near the edge of the coupon instead of in the center (see Figure 2.18 (b)). In this case the etching of the tether will begin sooner and the triangle that appears in the tether during the etching of the coupon can also be removed.

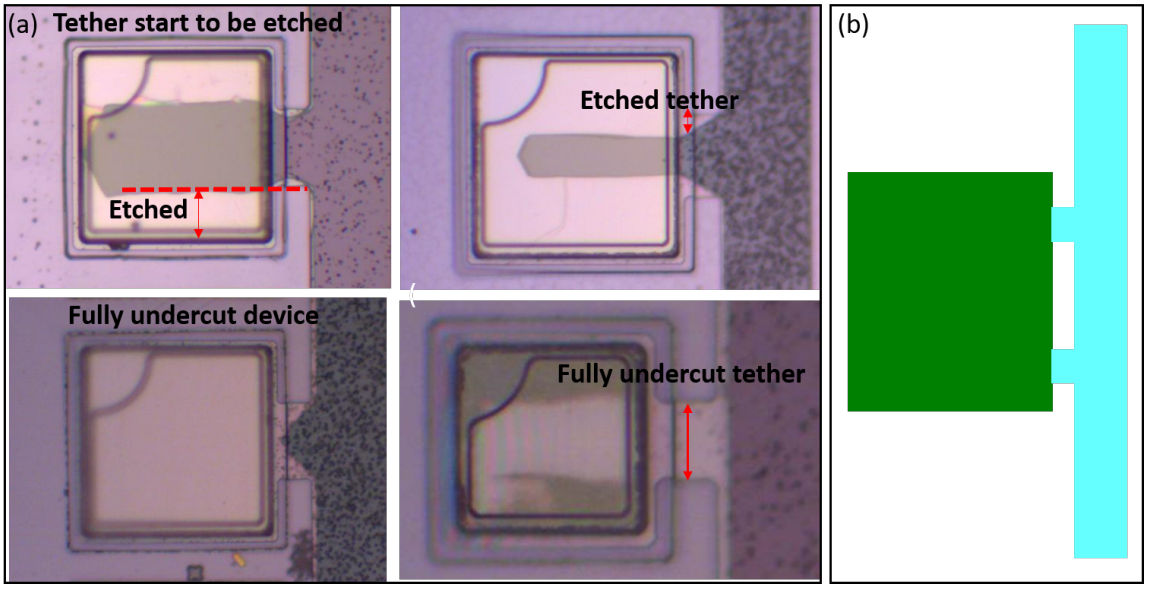

FIGURE 2.18: (a) Optical images of device during undercut with emphasizing the etching process in the tether. Dashed line indicated the alignment of etching part of device with the edge of tether (b) Suggested design of tether for future study.

In addition, we examined two types of anchors for assessing the stability of devices during undercutting and roughing. As opposed to epi-layers and SiN_x as anchors, SiN_x can be used as anchors because the Si plane is not exposed to the solution, and therefore anchors cannot be etched due to small misalignment.

Wet chemical etching using 5% TMAH is used to release the GaN LEDs based on Si substrate. It is seen that undercut etching in TMAH at high temperatures ($> 70°C$) can cause cracks on the epi-layers, which can be attributed to the high etch rate causing fast strain relaxation. By optimising TMAH undercut conditions, crack-free devices obtained.

As we have shown, specific considerations need to be taken into account when fabricating μ LEDs, which depend on the size of the LED and its initial stress on the wafer. As the stress

on the epilayer varies depending on the manufacturer, it is critical to make the appropriate measurements prior to beginning the process. It is seen that the deformation after release of larger devices is more severe than that of smaller devices. Therefore, a stress compensation layer is more essential for larger devices.

COMSOL simulation was used for calculation of the thermally induced curvature of layer coating on released devices. It was found that device bow can be controlled by changing the stress of SiN_x layer which is deposited on top of the device. Thus the stress of SiN_x on top of the coupon can compensate the tensile/compressive bow of the coupon which is generated in the device. According to COMSOL thermal stress simulation data and experimental results, it was determined that released GaN based LEDs without a compensation layer form concave surfaces suffering from tensile stress, while applying 1 μm of SiN_x with compressive stress reduced the curvature to an almost flat device after releasing. Simulation data determined that the type of initial stress of SiN_x plays an important role for obtaining flat surfaces.

Chapter 3

Light extraction improvement of transfer-printed LEDs

3.1 Introduction

The use of GaN LEDs based on Si has attracted significant interest for various applications, such as displays, communication and more. Despite good progress in fabrication of GaN LEDs on Si substrates, there are some factors that limit the performance of these LEDs. One of the major limitations of GaN LEDs on silicon is their low light extraction efficiency. Light extraction in GaN LEDs on silicon substrates refers to the process of efficiently emitting light from the LED device without significant loss due to absorption or reflection within the substrate material. However, silicon has limited transparency in the visible light range, which can pose challenges in achieving high light extraction efficiency in GaN LEDs on silicon substrates.

The two main approaches to improving LED efficiency are improving the internal quantum efficiency and increasing the light extraction efficiency. The former represents the number of photons generated by a certain amount of current flowing through the semiconductor device. It is mainly determined by crystal quality and epitaxial layer structure. The external quantum efficiency corresponds to the percentage of generated photons that are able to escape the chip and contribute to the overall lighting effect. High values of internal quantum efficiency have already been reported [85–87]. Taking into account light propagation in these devices the internal quantum efficiency for the device on Si was comparable to that on sapphire. Therefore, further improvements may be difficult to achieve, as a typical internal quantum efficiency (η_i),

value for blue LEDs has exceeded 70%. The maximum value of (η_i) for a GaN LED on Si has been reported to be 76% at 350 mA injection current [88]. There is, however, a lot of room in improvement of light extraction efficiency [89]. Light extraction, which is largely determined by Fresnel losses, is a major determinant of LED efficiency [90]. Due to the large index contrast between the GaN ($n \sim 2.5$) and the surrounding air, the escape cone for light is narrow, with critical angles ranging from 24° (air) to 38° (silicon) from normal, above which the majority of light is trapped by total internal reflection [91, 92]. As a result, only a small fraction of light can escape through the surfaces. Therefore, management of the light from these LEDs needs to be addressed to enhance the performance and their practical use in different applications.

Improving light extraction can be accomplished in several ways. To reduce the light absorption of the substrate, one way is increasing the reflectivity of the layers above the Si substrate and below the active region, for example, by inserting AlN/AlGaN distributed Bragg reflectors (DBR) between the intermediate layer and the LED structure. This has been tested by several groups and compared for a different number of Bragg mirror $\frac{\lambda}{4}$ pairs. However, the number of DBR periods is limited by the critical thickness of the nitride epilayer [93]. The thicker epilayer leads to stronger tensile stress during cooling from growth temperature to room temperature resulting in the generation of cracks in the epilayer due to the large thermal expansion mismatch between nitride layer and substrate. In fact, a major challenge of this method is the need for a high period number to achieve high reflectivity due to the fact that AlGaN/GaN has a high cracking risk and only offers a low refractive index change. Using alternative structure i.e ;lattice matched AlInN/GaN with a higher reflective index, enhanced the light intensity by factor of 3.6 when a 20-fold AlInN/GaN stack was used [94]. On the other hand, the DBR insertion increases the operating voltage and the series resistance. It should be noted that Bragg-mirror layers are effective only for backward light emitted vertically, and all light emitted laterally only partially benefits from these structures.

Another way to increase light extraction is topside patterning. The method, while effective for photo-excited devices, it is not technically feasible for electrically pumped LEDs because of the following reasons. Firstly because it is difficult to apply a topside contact to nano- and microscale patterns. Additionally, applying a remote p-contact too far away from the patterned area can cause current spreading problems [95]. Thirdly, etching patterns into or near the InGaN/GaN multiple-quantum-well layer (MQW) induces non-radiative defects that reduce light output [96]. lastly, the pattern must be very shallow (i.e., the p-GaN layer above the MQWs is typically $<$ 300 nm thick), which limits the aspect ratio of Gradient refractive

index (GRIN) features and the types of light-matter interactions that can be manipulated without etching into the active layer [97].

One of the most versatile methods of light extraction is substrate removal and thin film LED technology [98–100]. In thin film LEDs, the substrate is removed, and most light is extracted either directly or (ideally) after only one reflection at the backside. An essential prerequisite to this is the structuring of the surface in such a way as to prevent multiple reflections of light. Otherwise, all light propagating laterally will be extracted at the side facets following significant reductions in intensity due to the internal absorption. It has been reported that nitride films can be separated from sapphire and transferred to a variety of dissimilar substrates [101, 102]. Due to the relative hardness of sapphire and the lack of an effective wet-chemical etch, laser lift-off techniques were used followed by photo-electrochemical methods for roughening the backside of the device [103]. While, wet chemical etching can be used to remove the Si substrate. When the device has been roughened by either wet chemical etching or photoelectrochemical etching, flip-chip technique is commonly used to bond the device to other carriers [89, 104, 105]. As a result, the fabrication process will require a few additional steps.

In this project, we developed an integrated approach to roughen the backside of the GaN on Si LEDs using wet chemical etching during the coupon preparation process for transfer printing without any extra steps. This approach in conjunction with inserting a reflector between the LEDs and new target, the performance of LEDs can be improved. Moreover, in order to further enhance the collected optical power by redirecting the emission the released μLEDs were printed into silver-coated reflecting trenches formed in Si creating a 3D structure. The technique and results will be discussed in this chapter.

It is crucial that device performance must not be degraded during fabrication, including releasing, roughening, and micro-transfer printing, either electrically or optically. Thus, characterization was performed before and after transfer printing to ensure no effect was caused by the process. Details will be provided in Section 3.4. Finally, the potential of the fabricated LEDs for visible light communication has been discussed in Section 3.5.

3.2 Back side roughening to improve the light extraction

As stated before, only a small fraction of light could be extracted from planar GaN LEDs, thus proper light management was critical to achieving high device performance. A common

method is to make the surfaces rough to increase the ability of light to escape.

3.2.1 Surface Roughening of N-Polar N-GaN

The surface of the GaN epitaxies grown on Si substrates is usually Ga-polar. As soon as the devices are fully undercut for the purpose of transfer printing, the backside with the N-polar surface is exposed to solution. Accessing the N-polarity of GaN provides a good opportunity to roughen the surface. This is due to the fact that Ga-polar facet is very inert to most chemical etchants, while GaN with N-polarity can be selectively etched by water with the help of alkaline solution [106, 107]. Figure 3.1 illustrates the mechanism of etching N-polar GaN surfaces.

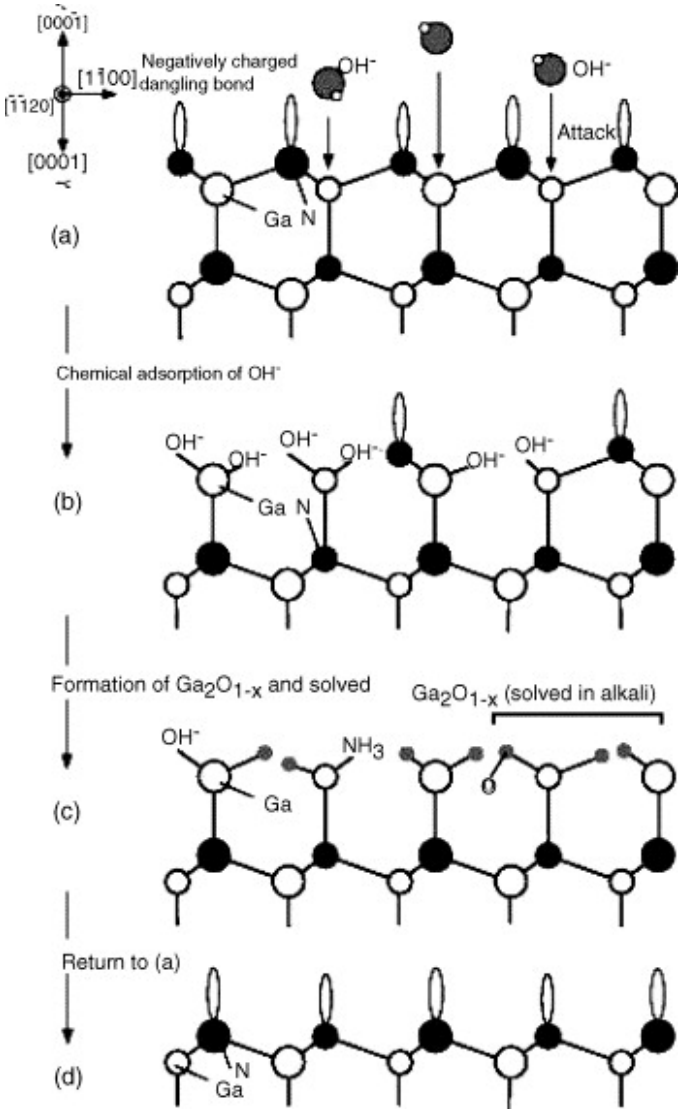

FIGURE 3.1: Schematic diagram of the cross section of N-polar GaN viewed along direction [$\bar{1}\bar{1}$20] to illustrate the mechanism of polarity selective etching.(a) Layer terminated by nitrogen with a negatively charged dangling bond on each nitrogen atom.(b) Hydroxide ion adsorption (c) Oxide formation (d) Oxide dissolution. Adapted from [108].

Initially, hydroxide ions (OH^-) are adsorbed on the N-polar surface of the sample (Figure 3.1(b)) and then react with Ga atoms following the reaction 3.1:

$$2GaN + 3H_2O \overset{OH^-}{\rightarrow} Ga_2O_3 + 2NH_3 \tag{3.1}$$

The Ga_2O_3 produced by this process is dissolvable by KOH, which acts as a catalyst. N-polar GaN can be etched by repeating the stages (a) to (d) in Figure 3.1. In the case of a Ga-terminated surface, etching could be initiated at step (c).

The polarity dependence of wet etching of GaN is attributed to the difference in bond structure [108]. As illustrated in Figure 3.2, each nitrogen atom in N-polar GaN has one dangling bond perpendicular to the surface, which allows hydroxyl groups to attack Ga atoms, resulting in a hexagonal pyramid-shaped etching surface, whereas each nitrogen atom in Ga-polar GaN extends three dangling bonds covering the Ga atoms below. The negatively charged dangling bonds repel hydroxyl groups away from Ga atoms, thus making Ga-polar GaN inert to alkaline etching [109].

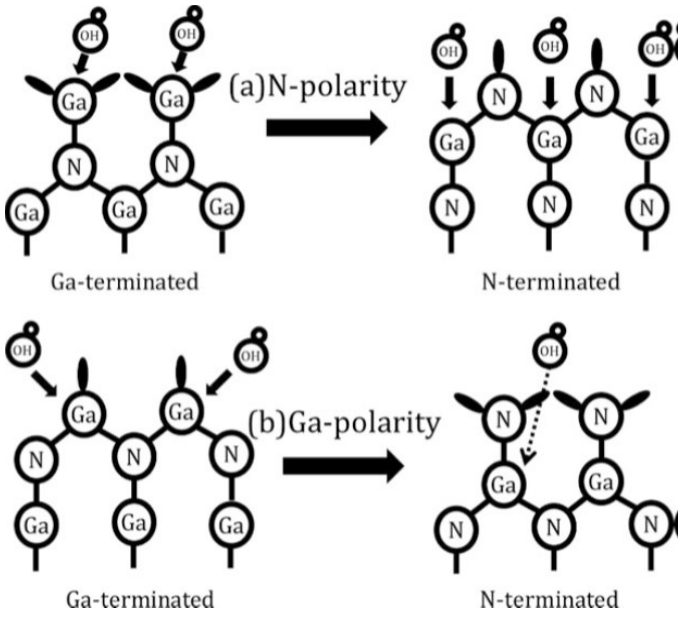

FIGURE 3.2: GaN etching of different polarities: (a) N-polar GaN can be etched by alkaline, and (b) dangling bonds of N atoms prevent Ga atoms from being attacking by alkalizing in Ga-polar GaN. Adapted from[109].

3.2.2 Back side roughening of released LEDs

Taking advantages of etching property of N-polar GaN, an integrated approach to roughen the backside of GaN-on-Si LEDs was developed here. When the Si layer underneath the device was completely etched by the TMAH solution (Figure 3.3(b)), the sample with suspended devices was dipped into the buffered oxide etchant for 10 seconds to remove any native oxide and SiN residual. The sample was then immersed into the same aqueous 5% TMAH solution at $50°C$ to form the pyramids. Note that while many types of etchants are available for silicon wet chemical etching, KOH and TMAH are the most commonly used [110–112]. The compatibility of TMAH with metal oxide semiconductor processes and its high selectivity with oxide mask have made it very popular [113, 114]. Additionally, It is reported that the etching rates of two orientations, (221) and (111), differed substantially between 25% KOH and 20% TMAH. For both of these planes, the etching rates in KOH solution were approximately half those in TMAH solution. There was no significant difference between the two etchants for the other orientations [115]. Additionally, KOH solution etching tends to etch the entire surface in N-polar GaN, including non-defective areas, which reduces the density of hexagonal pyramid structures on the surface [116, 117]. Note that to increase light scattering requires a high density of hexagonal pyramid structures. Also the diffusion of K^+ from the KOH-based solution into the MQWs is highly probable [118]. TMAH solution, on the other hand, exhibited better etching behavior with a high density of etched pits and better depth profiles and was free of contamination by alkaline metals [119]. It is for this reason that TMAH was preferred over KOH in this experiment. Moreover, the size of the pyramid was reported to decrease with an increase in the temperature of the solution. The isolated pyramids would eventually be etched away by further etching [120]. In addition, as stated in the previous chapter, high temperatures can cause cracks in the device, therefore $50°C$ was chosen in this experiment. The backside of the devices were fully roughened after around 50 minutes. SEM images (not shown here) revealed that the $AlN/AlGaN$ buffer layers were first etched by TMAH, after which the N-face GaN was exposed to etchant and pyramids were then formed on the bottom surface. As shown in Figure 3.3(c-d), the roughening on the backside (seen as dark color in the optical microscope images) began from the edge of device and extended to the center. As a result of the anisotropy etching of Si, the edge of the buffer layer were exposed to the TMAH and began to etch. Consequently, this part is exposed for a longer period of time, and after the device has been fully released and suspended, the buffer layer around the edge has been fully etched compared to the center part, which means that the n-GaN layer around the edge will be exposed to the TMAH sooner than the center

part, hence the roughening is directed. In other words, as the buffer layers at the edges were first exposed to TMAH etchant due to the anisotropic Si undercut etching, these areas were first roughened compared with the central areas, which explained why the roughening direction was the same as the Si undercut orientation, that is, along Si $< 1-10 >$. Figure 3.3(a-d) illustrate the optical images of array of LEDs with size of 110×110 μm^2 at each stage of the procedure, and magnified individual LEDs of each steps are shown in Figure 3.3(e).

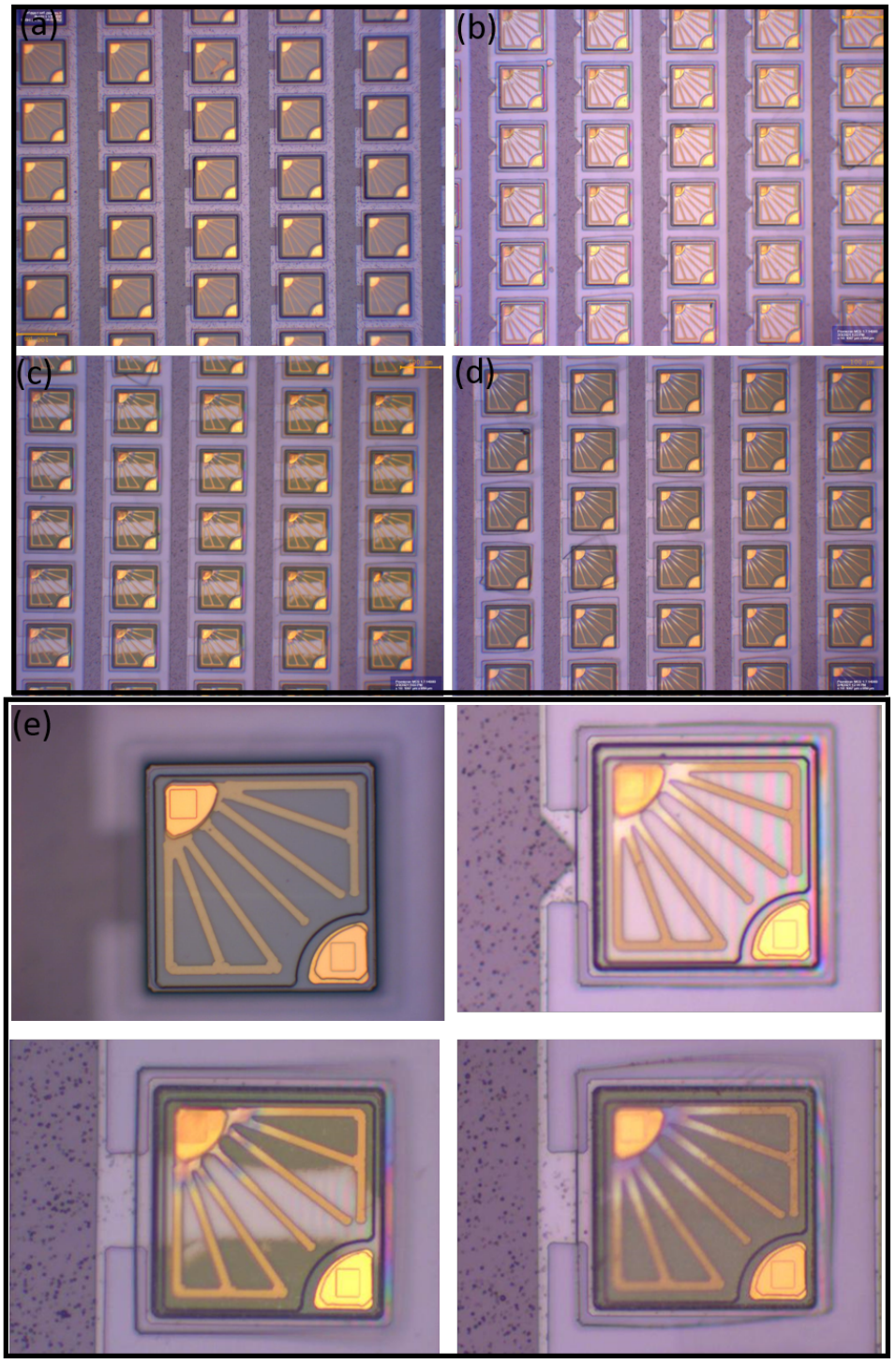

FIGURE 3.3: Optical images of array of LEDs with size of $110 \times 110\ \mu m^2$ (a) before undercut (b) after fully undercut (c) released LEDs with partially roughened backside, (d) with completely roughened backside and (e) showing the individual devices at each stage.

When the devices are fully roughened, the released LEDs were picked up using PDMS stamp, allowing characterization of the N-polar GaN surface using scanning electron microscopy (SEM). Figure 3.4 shows the completely roughened backside of the LEDs, where hexagonal-shaped pyramids of GaN with high density and various sizes were observed.

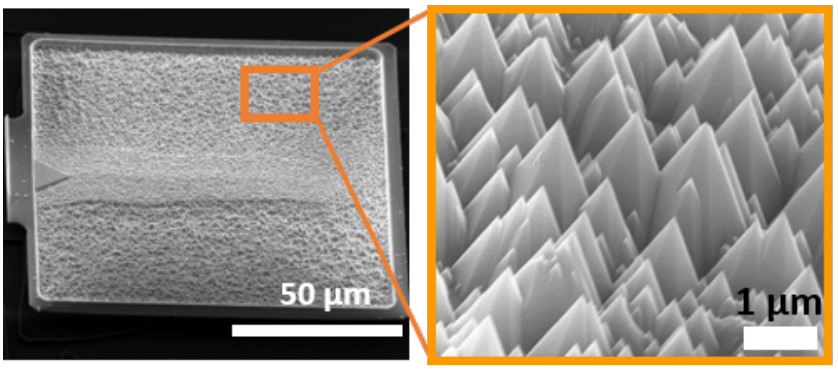

FIGURE 3.4: SEM images of released LED with size of $110 \times 110\ \mu m^2$ with roughened backside.

The non uniformity of pyramids could be attributed to the nonuniform defect distribution as the pyramids are initiated from dislocations. Several articles have demonstrated the mechanism for pyramid formation on N-polar surfaces [116, 121]. The formation of pyramids is attributed to facet-selective etching in which facets with different surface energies and etching rates compete with one another [122–124]. This study also has shown that the dislocation acting as the preferred spatial site for pyramid evolution initiated the etching process and accelerated the dissociation. In the dislocation and defect region, crystals have an irregular atomic arrangement, resulting in increased surface energy and instability. Dislocation and defects regions of a crystal are difficult to stabilize according to Morrison's thermodynamic argument [125, 126]. This results in elevated microscopic decomposition potentials for dislocation and defects regions compared to ideal decomposition levels. Consequently, these regions serve as critical etching initiation sites [125]. The Figure 3.5 illustrates the pyramid's evolution.

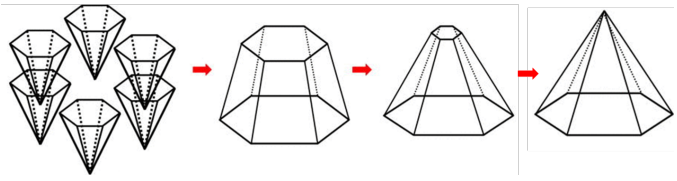

FIGURE 3.5: A schematic representation of the formation and development of the pyramid. Adapted from [124].

The exposed heads of dislocation would initiate the etching process, resulting in the formation of pits with V-shaped shapes within seconds, which assemble and encircle the truncated hexagon.

The hexagonal and dodecagonal geometric features of GaN crystalline structures are due to the inherent crystalline symmetry of GaN [124].

The face of hexagonal pyramids are $\{10\bar{1}\bar{1}\}$ planes with angle of around 58° with respect to the surface. It is worthwhile to note that the thickness of the etched GaN layers was around 1.2 μm (estimated from cross-sectional SEM of a cleaved device), which left enough n-GaN material for the contacts above. Considering that the thickness of n-GaN in the structure shown in Figure 2.2 was approximately 2.5 μm. With a roughened surface, the light can have a high probability to escape from the pyramid to the air after a few rounds of reflections.

3.3 Transfer printing of released LEDs

In order to compare the light extraction of printed LEDs, the released LEDs with and without backside roughening were micro transfer printed onto uncoated Si, Si with the reflective layer, and Si with the reflective trench.

3.3.1 Fabrication of reflective trench

The reason for using a reflective trench was to enhance the collected optical power in the forward direction by making the emission more directional. Therefore, to investigate the effect of a reflector trench to redirect the light into a photodetector with limited numerical aperture, square trenches ($\sim 230 \times 230\ \mu m^2$) with different depths were fabricated into a Si (100) substrate. To create the trenches, first, 300 nm SiN_x was deposited by PECVD on Si substrate as a mask. It is worth mentioning that our initial test showed that SiO_2 can be partially etched with TMAH, hence in final test SiN_x was used as a mask. Through photolithography, patterns of square shapes were transferred to the photoresist S1813 on the wafer. Using ICP system the exposed nitride is etched in CHF_3/O_2, resulting in a durable SiN_x mask suitable for deep etching of silicon in alkaline solutions. Before wet etching using TMAH, the photoresist is removed using a suitable photoresist stripper (1165). Then the samples immersed into 5% TMAH at $65°C$ for 5 and 9 min to form trenches with depths of 5 μm and 10 μm, respectively. The depth of fabricated trench was measured using profilometer (Figure 3.7(a)). The anisotropic wet etching of (100) Si in TMAH solution creates trenches with (111) faced sidewalls with an inclined angle of 54° with respect to the surface. A top-view optical image and SEM image of a trench with a depth of 10 μm can be seen in the Figure 3.7 (b,c) respectively. Then, the

patterned Ti/Ag (20/100 nm) was patterned and evaporated to serve as the reflector inside the trench, avoiding the location for subsequent metal tracks to avoid short circuit and capacitance effect after making interconnections. Figure 3.6 depicts process flow of the trench fabrication.

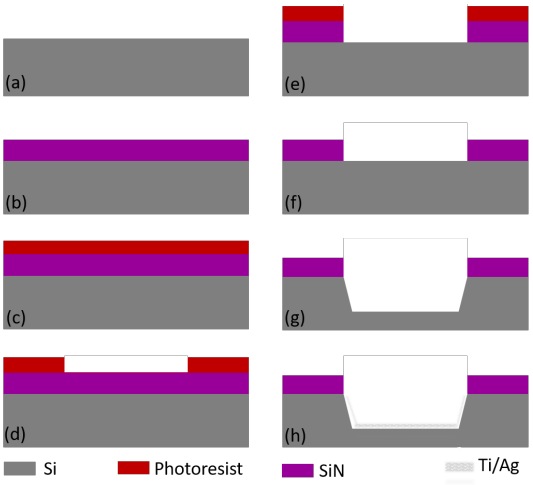

FIGURE 3.6: Schematic diagram of fabrication process of trenches (a) Silicon wafer, (b) SiN_x deposition, (c) photoresist deposition, (d) photoresist patterning, (e) dry etching of SiN_x, (f) remove photoresist, (g) wet etching of Si and (g) deposition of reflective layer.

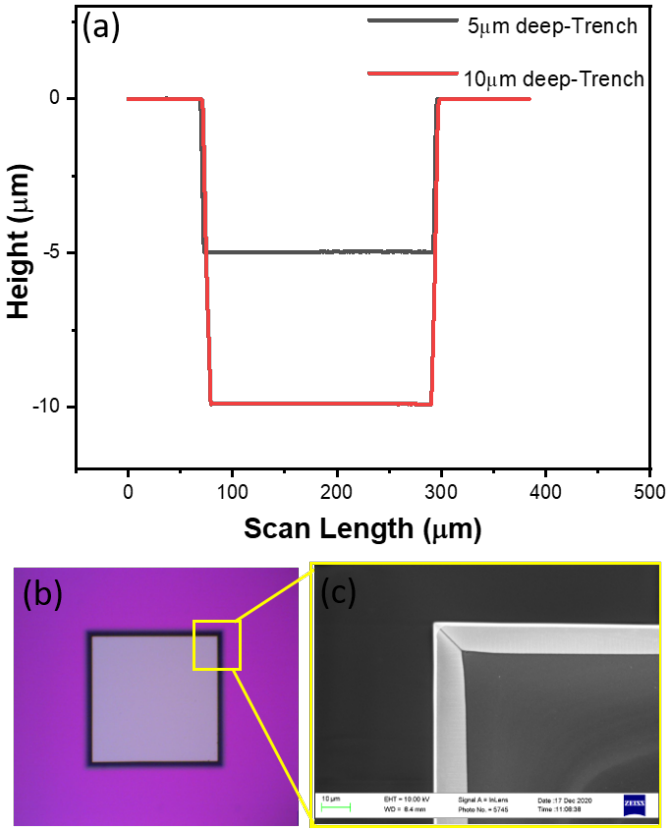

FIGURE 3.7: (a) Depth of fabricated trench in Si, (b) Top-view optical image and (c) SEM image of corner of trench.

3.3.2 Transfer printing of released LEDs

A layer of Intervia with thickness of 500 nm was spun as an adhesive layer on different carrier wafers, including uncoated Si, Si with the reflective layer and Si with pre-fabricated reflective trench. In the μTP process, a PDMS stamp with similar size to the devices is used to pick up the suspended LEDs from original substrate and print into a designated wafer. It should be noted that when using an adhesion layer such as Intervia, the backside roughening of the device did not cause any issue in transfer printing. Printing LEDs even in the deep trench had a high transfer printing yield as can be seen in the Figure 3.6 (d). Once the transfer printing is done, the Intervia was exposed to UV-light for 2 minutes, followed by a 3 minute baking at 100°C . Then, Intervia was hard cured in an oven for 30 minutes at 90°C followed by three hours at 175°C. As a result of curing, Intervia strengthened and LEDs appeared to be adhered to the new target firmly. Finally, to ease the probing and characterization the LEDs into the trench were electrically interconnected using photolithography and evaporation of Ti/Ag/Au (20 nm/2000 nm/200 nm). Note that the metal lift-off process requires thick photoresist due to the thickness of metal (> 2 μm). Therefore, we used a two-layer lift-off resist consisting of PMGI SF11 and S1813. Next, the pattern was developed by exposure to UV-light and subsequent development with MF319. It is necessary to expose samples placed inside trenches approximately three times longer than those placed on a flat surface. This is because the photoresist must be removed inside the trenches on a patterned area. Photoresist cracking has been observed in samples within trenches due to stress caused by $PMGI's$ thickness. In order to heal the cracks, the sample inside the trench was reflowed by backing it at 120°C for one minute. The failure to consider these points resulted in the formation of metal residues in trenches or the breaking of metal, as shown in Figure 3.8 (a) while adequate exposure and re-flowing the photoresist result in a clean trench with good metal interconnection Figure 3.8 (b).

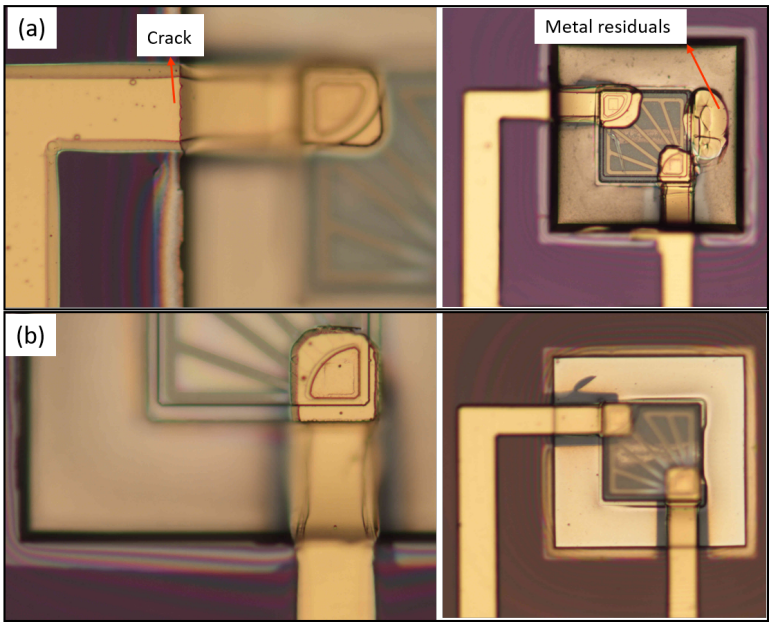

FIGURE 3.8: Optical images of metal interconnection of device into trench (a) before optimization of lithography step. (b) after optimization.

A schematic diagram of the transfer printing into the Si trench and their corresponded optical images are shown in Figure 3.9.

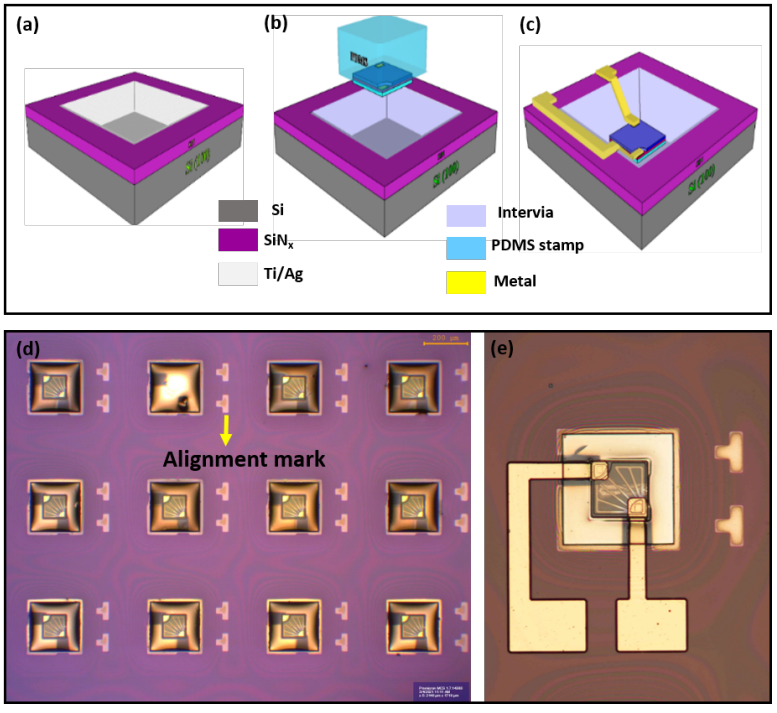

FIGURE 3.9: Schematic diagram of (a) Si trench with coated silver. (b) Transfer printing of device into reflected-coated trench coated with Intervia. (c) Metal interconnection after printing device. Optical image of (d) printed LEDs into trenches. (e) Metal interconnection

3.4 Characterization of LEDs before and after transfer printing

It is critical not to degrade the device performance during the fabrication process, including roughening and printing. As a result, testing the performance of devices is a necessity to ensure that the process does not adversely affect them.

3.4.1 Electrical characterization

To investigate how the roughening and the printing process affects the device performance, the current-voltage (I–V) characteristics of the μLEDs before undercut and after transfer printing with the roughened backside (on Intervia-coated Si) were measured with the test devices with large bond pads. The I-V curves under DC mode from 0 mA to 20 mA in forward bias condition are presented in Figure 3.10. It can be seen that the diode characteristic of the roughened μLEDs is improved, with the voltage at the injected current of 10 mA reduced from 4.06 to 3.8 V, showing a reduction of the series resistance after the undercut. This result is confirmed by measuring a large number of devices. The voltage decrease could be attributed to the small band gap shrinking due to self-heating resulting from the adhesive layer used for printing, whereas for devices before printing the Si substrate can dissipate the heat effectively.

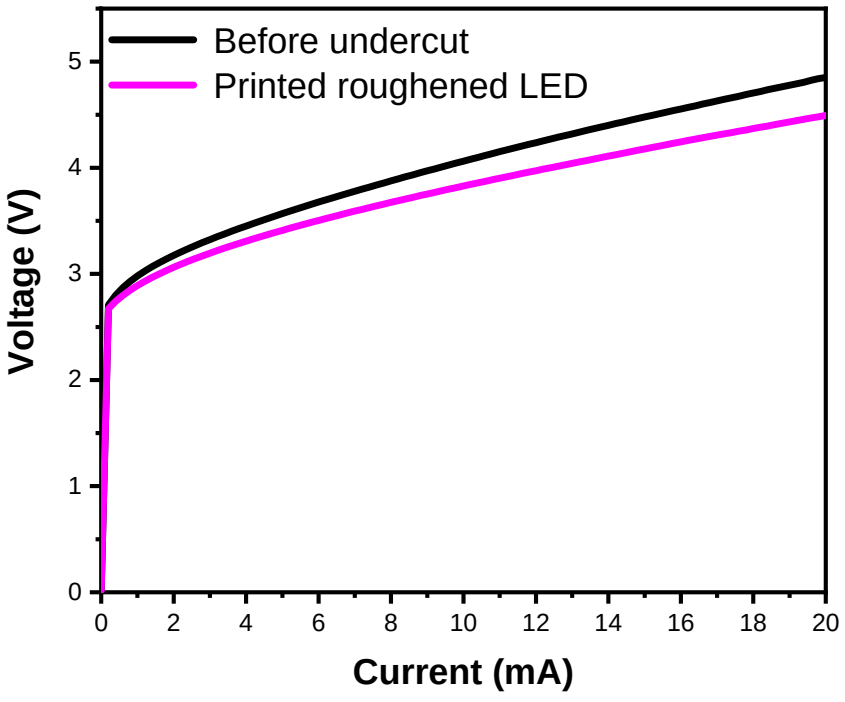

FIGURE 3.10: Current–voltage ($I-V$) characteristics of the 110×110 μm^2 blue LED before undercut and after transfer printing.

In addition, current leakage is measured in reverse bias, where the leakage current is reduced from 3.7× 10^{-4} A to nearly 4× 10^{-6} A at -4 V. Similar results were also reported by other groups [127, 128]. One possible reason could be attributed to the undercut etching which removes the interfaces (mainly the one between the AlGaN buffer layers and n-GaN layer). Therefore, any possible leakage paths through the dislocations at the interface are eliminated [128, 129].

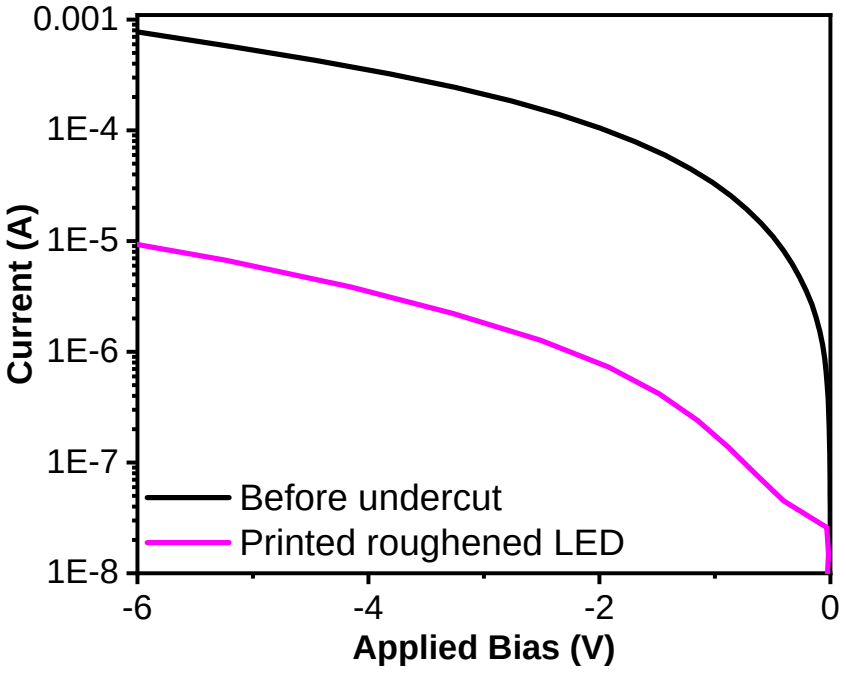

FIGURE 3.11: I-V curves under reverse bias.

3.4.2 Electroluminescence measurements

The electroluminescence (EL) spectra of different devices before and after printing is measured by an optical spectrum analyzer through an optical fiber at the top of the LED chip. As shown in Figure 3.12, a marginal redshift of the peak wavelength is observed from 448 to 450 nm after printing. Similar to the voltage drop shown in Figure 3.10, such a shift can also be attributed to the thermal effect of the adhesive layer (i.e., Intervia), which results in an increase in the device temperature. Transfer printing technology presents a common problem with heat dissipation because, regardless of the receiver substrate chosen, the process flows normally incorporate adhesion-enhancing layers on the receiving substrates to facilitate the release of LEDs from transporting stamps [130, 131]. Conventionally, these layers are organic materials, with poor thermal conductivity, κ (e.g for Intervia 8023, $\kappa \sim 0.19$ $\frac{W}{m.K}$). Due to these properties, adhesive layers can impede heat dissipation from operating devices even if the

substrate beneath the adhesive layer has a high thermal conductivity. To address this thermal issue, alternative transient layers of volatile liquids could be used instead of adhesive layers for appropriate printing [132]. Furthermore, recently, our group demonstrated the capability of printing devices directly onto the target without the use of adhesive. It helps to resolve the problem of heat dissipation [133].

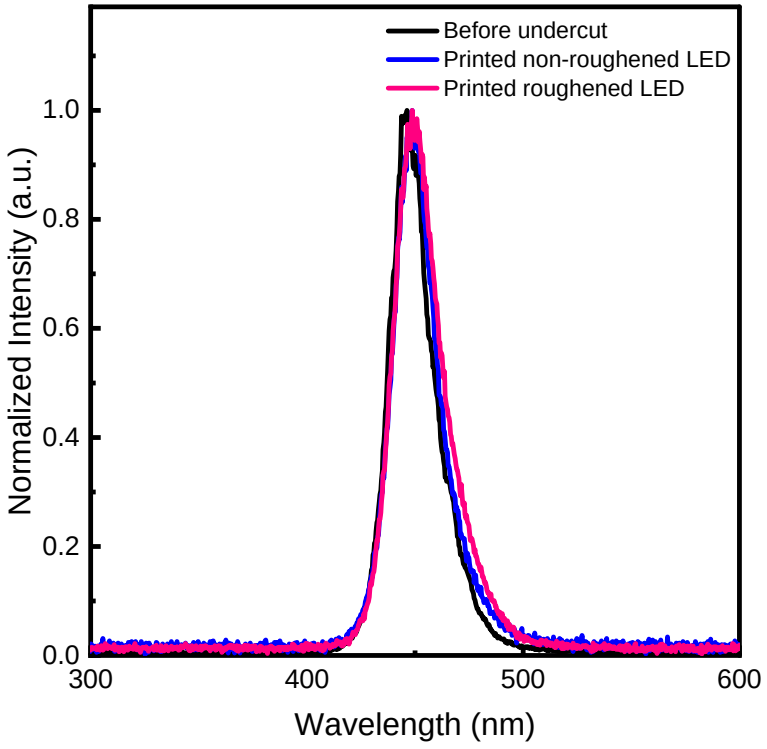

FIGURE 3.12: Electroluminescence spectra of non-roughened and roughened μLEDs before undercut and after printing on flat surfaces at 15 mA.

The EL spectra of the printed μLEDs under injection currents ranging from 5 to 60 mA is shown in the Figure 3.13.

As expected, the EL intensity of printed LED increases with increasing current density in the initial stage. Upon further increase in current density, emission intensity is saturated. At the higher current density level, a redshift of the wavelength is observed with increasing current density, owing to the reduced bandgap with junction-temperature rise. Along with the I–V curves, all of these indicate that transfer printing and undercut/roughening processes do not cause any issue for device quality.

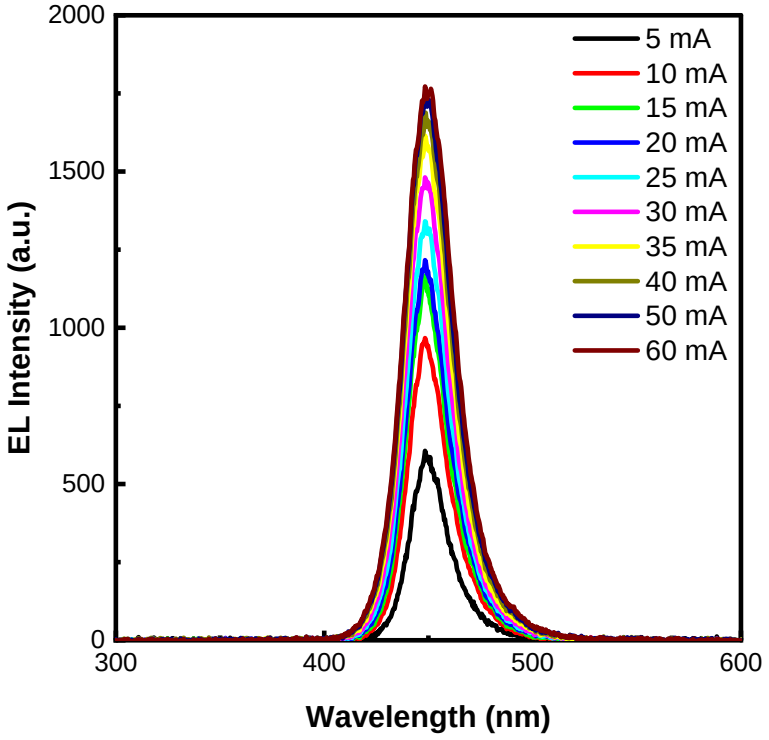

FIGURE 3.13: EL spectra of transfer printed roughened μLED operating under different currents.

3.4.3 Light extraction assessment

The light output power of LEDs before undercut and after printing was measured, where a lens was mounted 1 cm above the sample (numerical aperture of the setup was 0.5) to collect light into a photodetector placed above the lens.

The effect of backside roughening and the integrated Ag reflector on the light output power are shown in Figure 3.14 (a). When compared with LEDs on the initial Si substrate, transfer printing these devices (non-roughened) onto a new Si substrate with the adhesion layer (i.e., Intervia) increases light output by a factor of 1.2, which is attributed to the low refractive index of Intervia while printing onto a Ag reflective layer leads to improvement by a factor of 2.0. The addition of backside roughening with the Ag reflector results in a remarkable improvement in light output by a factor of 4.2, which can be mainly attributed to the scattering effect of the pyramids formed on the backside. This is confirmed by fluorescence microscopy images of the three LEDs in Figure 3.14 (b) where it is clear that the released LED with the roughened backside is the brightest image compared with the nonroughened LED.

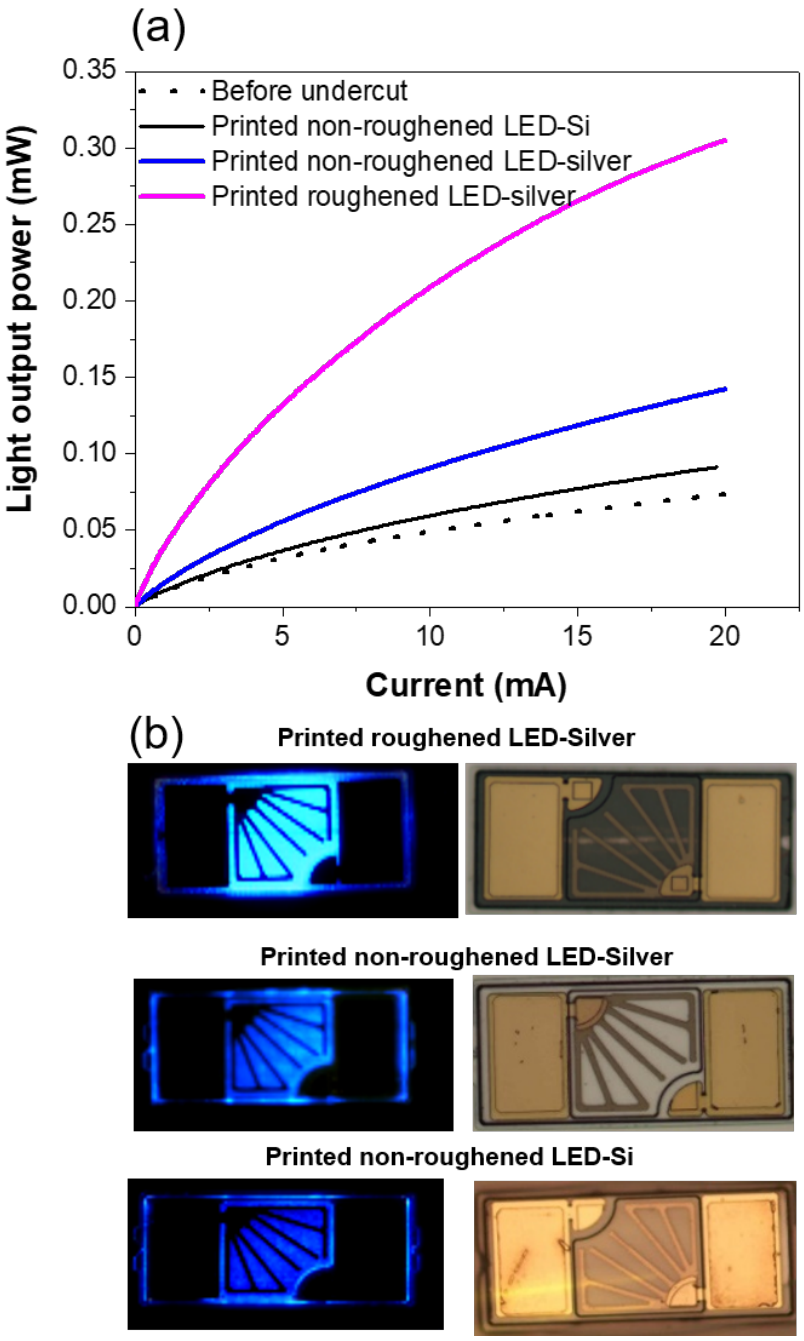

FIGURE 3.14: (a) Light output power collected into NA=0.5 of 110 × 110 μm^2 LED before undercut, non-roughened LED on Si and silver and roughened LED on silver. (b) fluorescent microscope images of printed LEDs and their corresponding optical image on the right.

To investigate the effect of the trench, the collected light output power of the device into the trench with depth of 5 μm and 10 μm and flat platform is measured for multiple devices. As can be seen from Figure 3.15 (a) printing LEDs into trenches with depths of 5 μm and 10 μm enhances the collected power by a further factor of 1.4 and 1.8, respectively, as compared to printed LED on a flat target. It is seen that the trench with the smaller depth is less effective in increasing the collected light. This is because the depth is comparable to the total thickness

of the LED, which is approximately 5 μm. Hence, some light emitted from the LEDs may escape from the trench without being redirected by the sidewalls, resulting in less power being collected than in the deeper trench. In general, an enhancement of collected power due to the trench can be attributed to light redirection by the sidewalls of trenches, meaning that a trench can reduce the angular distribution of light, hence increasing the convergence optical power. It can be seen from Figure 3.14 and 3.15 (a), that the light output collected for the roughened LED in the trench is over seven times that of the device on the initial Si substrate (before undercut).

It is known that the light emitted from LEDs is highly divergent, therefore it is desirable to shape the beam through the formation of a lens on top of the device for the further enhancement of directionality of light. For this purpose, printed LEDs into a cavity with depth of 10 μm was filled with a drop of transparent UV-epoxy resin with a refractive index of 1.5 and exposed to UV-light for 50 seconds to form a dome shape lens on top of the device. The collected optical power of the trench printed LED with polymeric lens is increased by factor of 1.1 when compared to that without a lens. This can be attributed to the increased critical angle achieved by the addition of the polymeric lens ($\theta = \arcsin(\frac{n_{lens}}{n_{GaN}})$), and higher critical angles mean a higher percentage of light can escape from the surface. In summary, it is seen that using a trench in conjunction with a lens improved the collected power by factor of 9 in comparison with the LED on original substrate as shown in Figure 3.15 (a). The schematic of the effect of trench and lens in redirecting light are shown in Figure 3.15 (b). The SEM image (left) and optical image (right) of a lit-up printed LED at 2 mA into a 10 μm deep trench are shown in Figure 3.15 (c). The light that hit, the trench sidewall is clearly visible in this image.

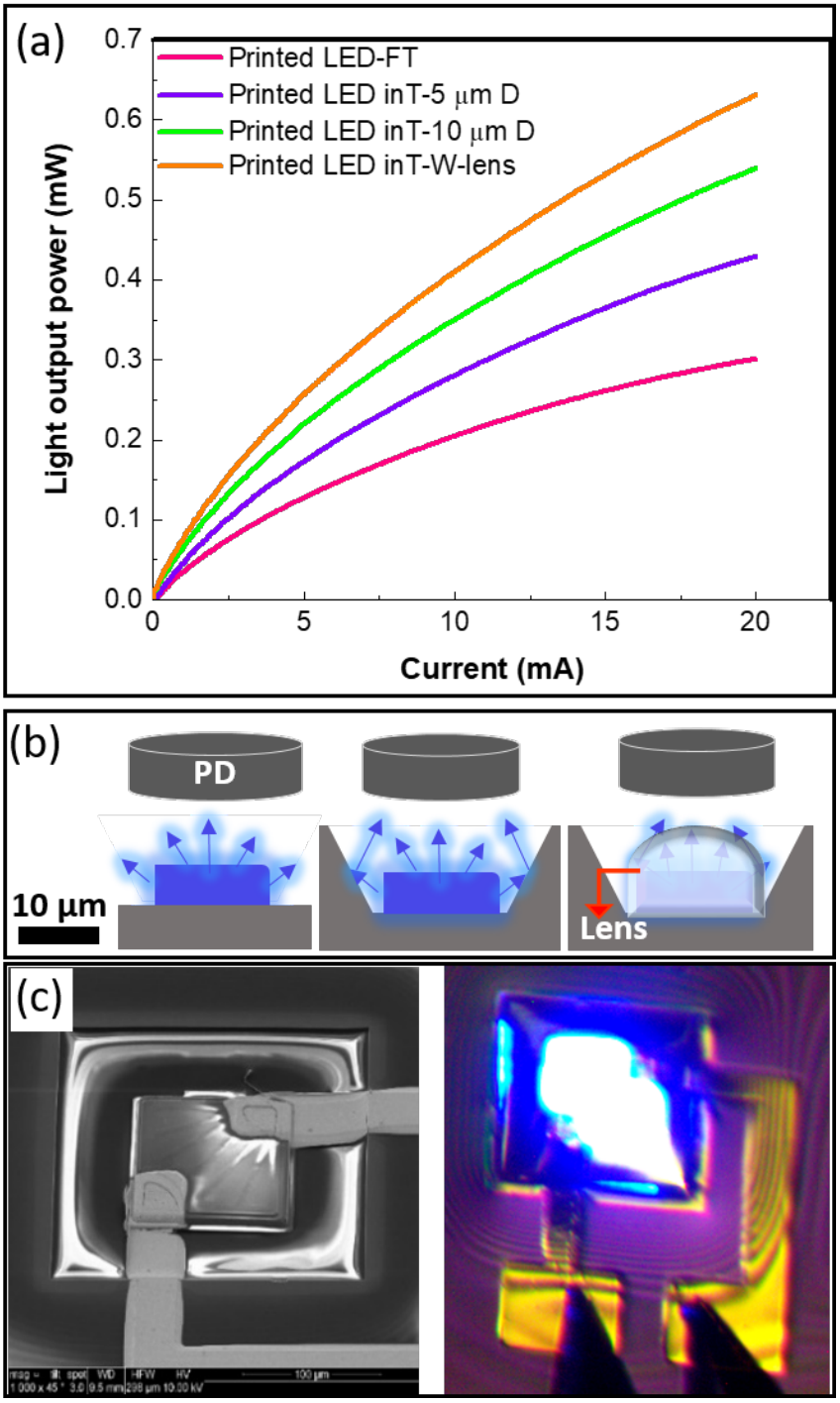

FIGURE 3.15: (a) Light output collected from $110 \times 110\ \mu m^2$ LED on original substrate, after printing on flat target (FT), in trench with depth of 5 μm (T-5 μm D) and 10 μm (T-10 μm D) and printed LED into 10 μm-deep trench with covered lens (c-W-lens).(b) Schematic of printed LED on flat target, into trench and into trench with lens to show the effect of sidewalls and lens in light redirection to photo detector (PD). (c) SEM (left) and Optical image (right) of a lit-up printed LED into 10 μm-deep trench at 2 mA.

3.5 Visible light communication performance of printed LEDs

Beside the advantages of LEDs for illumination, there is now the possibility of using LEDs in data communication especially for visible light communication (VLC). However, the optical modulation bandwidth of conventional broad-area LED is less than 20 MHz, which restricts the application of VLC [134, 135]. Here, micro-LED based on GaN can be advantageous. The combination of LED die sizes 10-100 times smaller in area than those of typical commercial GaN-based devices and their ability to sustain high current densities has facilitated high modulation speeds (> 1 Gb/s) [136–138]. It is reported that μLEDs with low optical power may defeat the purpose of free space VLC due to the low signal to noise ratio (SNR) [139]. Given the higher optical power of printed LEDs into trench, this further encouraged to demonstrate their performance in VLC.

The frequency response is one of the most significant parameters to be addressed in developing LEDs for use in VLC, and the cut-off or -3dB frequency is found to be correlated to certain diode parameters. Thus, to evaluate the potential of printed fabricated LEDs in VLC their frequency response was measured. The communication performance of the printed μLEDs was measured using signals generated from a vector network analyzer (VNA; 8753ES) combined with a constant current source (Keithley 2400) via Bias-Tee (mini-circuit-15 542) to be probed by a high-bandwidth ground-signal microprobe. The light output from the device was focused using an aspheric lens onto a high-speed photodetector (HSA-X-S-1G4-SI) and sent to a network analyzer to analyze the frequency response. Figure 3.16 illustrates the experimental setup for measuring LED bandwidth.

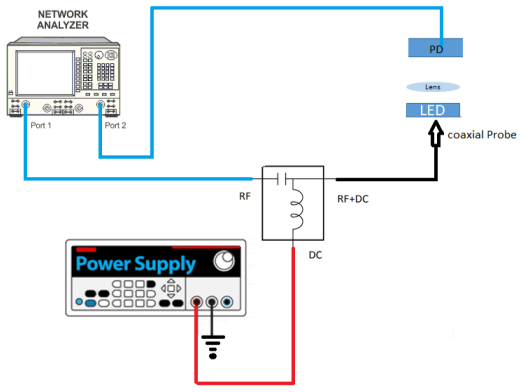

FIGURE 3.16: Setup configuration for bandwidth measurements

Figure 3.17 shows the frequency response and the extracted -3 dB bandwidth for the roughened LEDs in the trench at currents from 5 to 60 mA. It is seen that the frequency response and bandwidth increase with the injection current and the dependence can be related to the reduction of carrier lifetime.

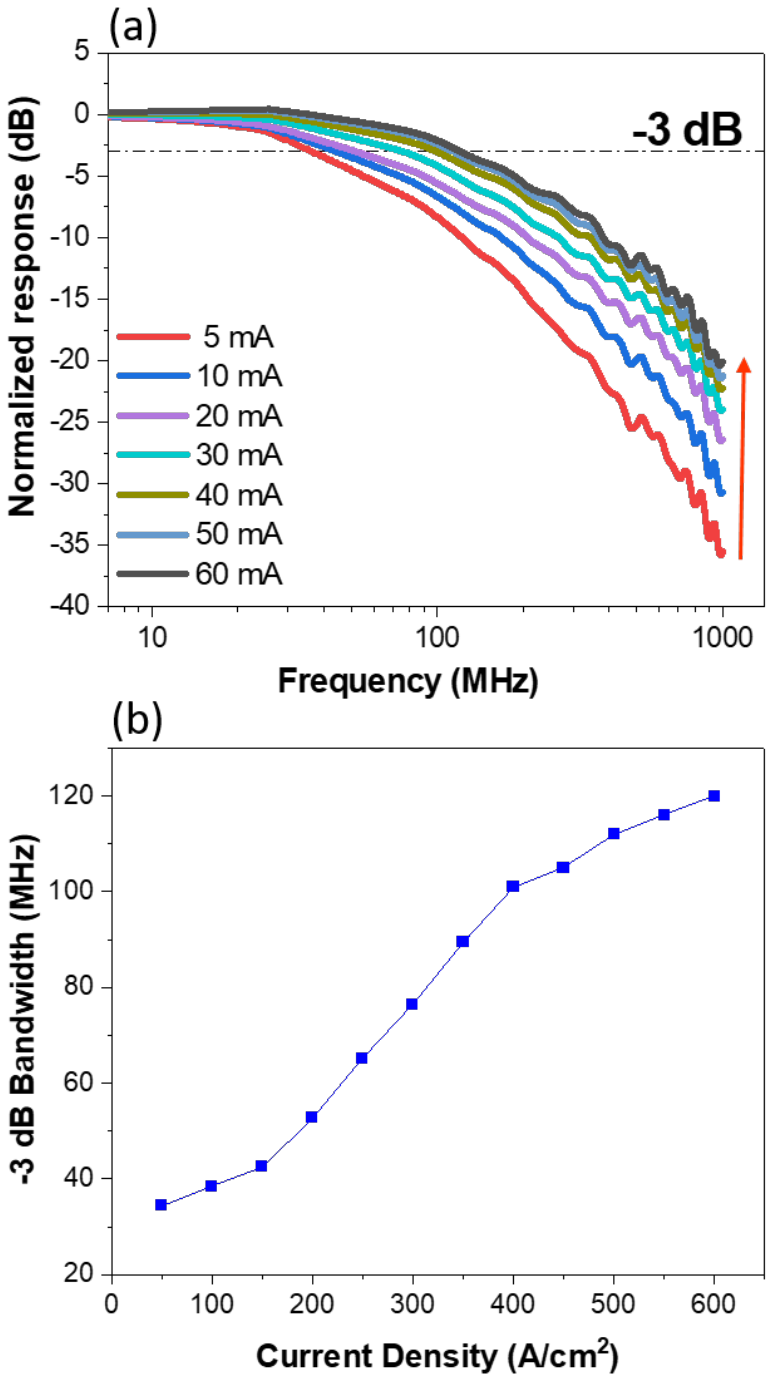

FIGURE 3.17: (a) Frequency response of the printed roughened blue LED with size of 110×110 μm^2 into reflective trench as a function of the injected current of the LED. (b) Extracted $-3dB$ modulation bandwidth versus current.

In fact, the -3 dB bandwidth of the LEDs can be related to the minority carrier lifetime (τ)

and Resistance-Capacitance (RC) time constant, which consist of differential resistance and geometric capacitance of the LED (i.e., $\tau_{RC} = R.C$), as described in the following Equation:

$$f_{-3dB} = \frac{\sqrt{3}}{2\pi\tau} = \frac{\sqrt{3}}{2\pi}(\frac{1}{\tau_r} + \frac{1}{\tau_{nr}} + \frac{1}{\tau_{RC}}) \tag{3.2}$$

where τ_r is the radiative carrier lifetime and τ_{nr} is the lifetime of nonradiative carrier. It is preferable to reduce the radiative carrier lifetime for enhancing f_{-3dB} bandwidth, but not nonradiative carrier life time, because carrier radiative lifetime is the dominant factor that limits the bandwidth modulation for LEDs with active areas close to micronsize or less[140]. In this case, τ_r is relative to the injected current density and can be written as:

$$\tau_r = \frac{1}{B \times N} \tag{3.3}$$

where B and N denote the radiative coefficient and the carrier density, respectively. Thus, by utilizing the Equation 3.3, the modulation bandwidth takes the following form when a bimolecular recombination mechanism is assumed:

$$f_{-3dB} = \frac{\sqrt{3}}{2\pi} \times \sqrt{\frac{BJ}{qd}} \tag{3.4}$$

Where J represents the injected current density, q is the elementary charge, and d is the active region thickness. Thus, Equation 3.4 implies that the higher -3 dB bandwidth can be realized by either increasing the operation current density, or reducing the size of the device to obtain higher injected current density [141, 142]. In our case, increasing the current density leads to bandwidth enhancement. The maximum -3 dB bandwidth of sample is 120 MHz, which corresponded to an injected current of 60 mA.

To compare the data-rate of transfer-printed devices, tests were made of the optical transmission of data. The SNR was estimated by subtracting the noise level from the signal power. For these measurements, the LEDs were probed with the setup shown in Figure 3.16. The DC current was mixed with an AC on-off keying modulation signal, although in this case the AC signal was a pseudo-random bit sequence (PRBS) of 27-1 bits. A digital data analyzer (MP1632A) was used to produce PRBS pattern with peak-to-peak voltage (Vpp) of 2V and the eye diagram was captured by an oscilloscope (DSO 80804A). The BER was estimated using the Q factor,

which was obtained directly from the eye diagram at the different data rates. The printed blue LEDs on a flat reflective platform were compared with those printed into the trench by measuring the bandwidth modulation and eye diagram with on–off keying (OOK).

It can be seen from Figure 3.18 (a) that the LEDs in the trench exhibit a higher signal-to-noise ratio (SNR) than that on a flat platform due to higher received optical power. In addition, the BER as a function of data rate for roughened LEDs and non-roughened LEDs on the flat platform and inside of the trench with depth of 10 μm is shown in Figure 3.18 (b). A lower BER is observed for the device into the trench, which is in good agreement with the SNR data. The roughened LED in the trench, operating at 40 mA, can achieve a data rate of 270 Mbps with a BER of $9.6\times\ 10^{-4}$ before reaching the $3.8\times\ 10^{-3}$ forward-error-correction (FEC) threshold. The lower data rate for the nonroughened LED (220 $Mbps$) on a flat platform is likely due to its lower optical power. Finally, the eye diagram of the roughened LED and nonroughened LED on the flat platform and inside of the trench at the data rate of 100 $Mbps$ and injection current of 40 mA are shown in Figure 3.18 (c). It can be seen that the eye diagram of the roughened LED into the trench is open and clear at 100 $Mbps$, which is related to the increased optical power, while the relatively noisy eye diagram for the non-roughened LED at this transmission speed is attributed to the lower SNR. Transmitting LEDs with a smaller divergence reduces optical crosstalk [143].Therefore, using the trench not only improves the light output power improving the SNR but also can be beneficial to reduce the optical cross talk in VLC applications.

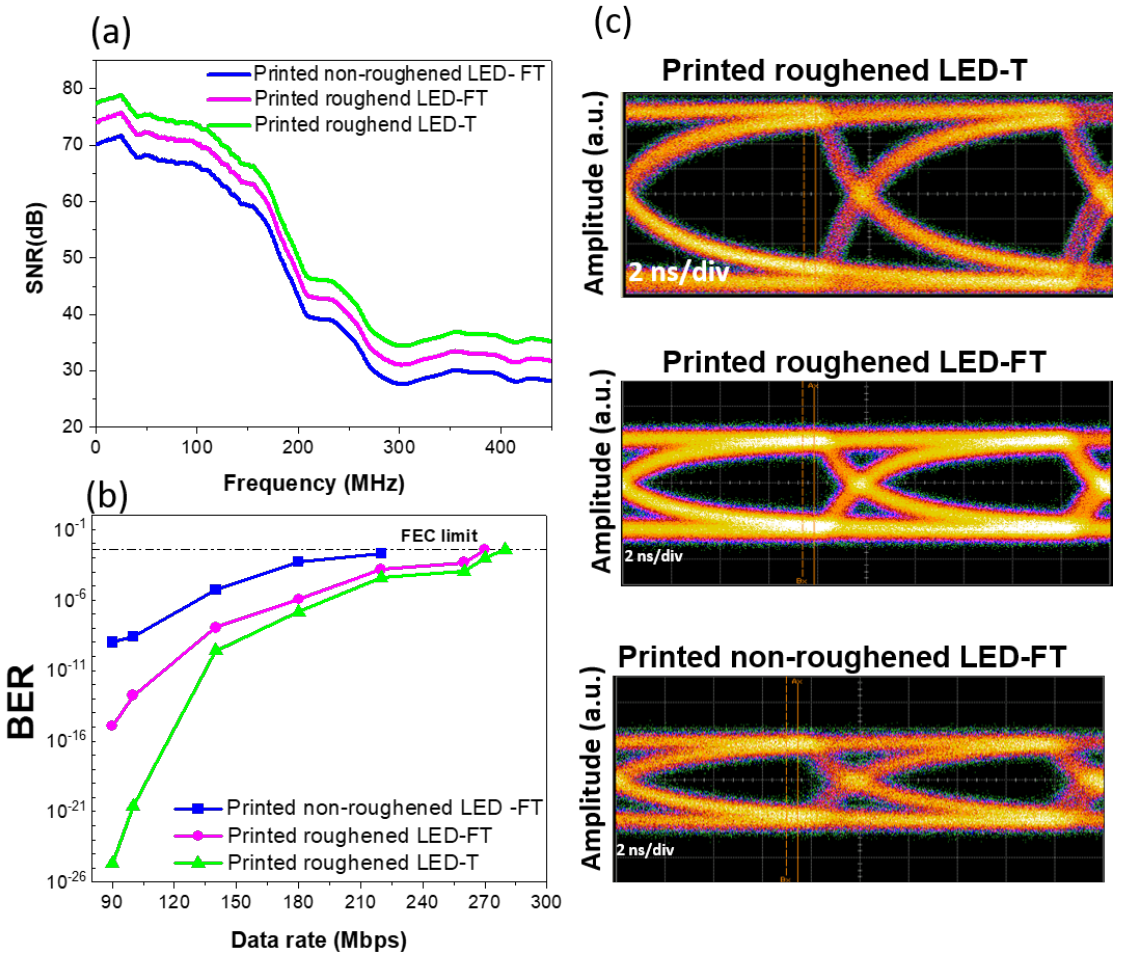

FIGURE 3.18: (a) Comparison of SNR of the printed nonroughened and roughened LED on flat silver platform and roughened LED into trench. (b) BER versus data rate of those devices. (c) Eye diagram of printed LEDs into trench and flat silver platform at data rate of 100 Mbps and injection current of 40 mA.

3.6 Conclusion

The capability of printing GaN LEDs on a variety of targets using micro-transfer printing was demonstrated, including 3D structures, which was a distinguishing attribute of this technology. To ensure that the quality of devices is not compromised during the process, the performance of $\mu LEDs$ was evaluated before and after printing.

The light extraction efficiency was improved by incorporating integrated backside roughening of the LEDs together with printing on the silver reflector. As a result, the collected light output power increased by a factor 4.2 when compared to LEDs before undercut. It is seen that output power of fabricated LEDs appeared to be rather low, it is important to note that this value is not representative of the actual output power. Our objective was to compare the output power

of fabricated LEDs with each other. A comparison of the power output of commercial LEDs using spherical integrated versus a detector with $NA = 0.5$ showed that the power output was 140 times higher when using integrating sphere. In this regard, the actual output power of fabricated μLEDs should be higher if an integrating sphere is used for the light output power measurement. While this may be the case, there is still potential for these LEDs to have greater output power.

One issue with this LED design was its use of fingers-shaped metal. Despite the fact that depositing finger shape metal will assist in spreading current, it covers approximately 15 percent of the surface, which prevents light from coming out. The problem can be resolved by using a transparent conductive layer, such as ITO, which spreads the current without covering the surface.

The external quantum efficiency results were also unexpected and have prompted us to explore the materials used for the fabrication of LEDs. As it can be seen from Figure 3.19 the external quantum efficiency increased by roughening from 4% to 13% at 0.2 A/cm^2 as compared to the LED before undercut which confirms the beneficial of roughening. There was, however, a rapid drop in efficiency. With increasing injection current density, efficiency drops, indicating severe carrier loss. However, this sharp drop in low current suggests there is insufficient electron blocking layer in the structure [144]. A fundamental problem exists with this material, and the output power will be enhanced if a higher quality material is used for fabrication of LEDs.

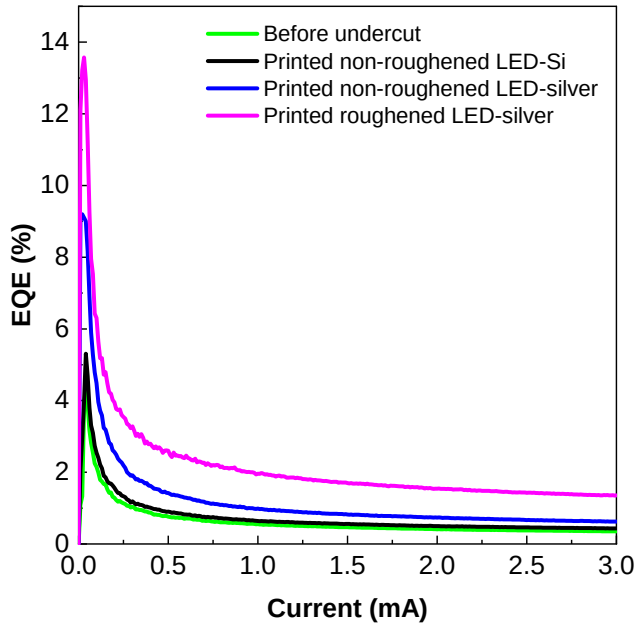

FIGURE 3.19: Comparison of external quantum efficiency of μLEDs before undercut, non-roughened μLEDs on Si and silver and roughened μLEDs on silver as a function of current.

Further enhancement of collected light output was achieved by printing roughened $\mu LEDs$ onto a deep reflective trench. Overall, using the trench with lens enhanced the collected power by a factor of 9 when compared with LEDs on original silicon substrates.

Finally, the potential of these devices for VLC was demonstrated where the results showed that the printed device in the trench improves the light output power a consequently the SNR. By incorporating quantum dots, effective down-conversion of light to other colors can be achieved. Arrays of such devices in conjunction with detectors can act as a high-bandwidth multicolor transceiver for VLC.

Chapter 4

Lift-off of GaN devices by Photoelectrochemical etching

4.1 Introduction

Over the past decades GaN-based alloys have been widely used in a variety of devices, such as light emitting diodes (LEDs) [145], lasers [146], and high power electronics [147], owing to their unique optoelectronic and mechanical properties. These materials are commonly grown on non-native substrates such as sapphire [148], SiC [149] and Si [150] due to their low cost. However, due to the lattice and thermal expansion mismatch between the nitrides and the substrates, such hetero-epitaxy leads to the formation of high-densities of dislocations and residual stresses in the epi-layers, which reduces the performance of devices [151, 152]. To achieve higher performance III-N devices can be grown on native GaN substrates but the cost of these substrates is a huge barrier for commercial applications. Therefore, release of GaN-based epi-layers from free-standing GaN substrates or high-quality GaN/sapphire templates can be beneficial by reclaiming and reusing the original substrates to significantly reduce the production costs [117, 153]. In addition, thin-film devices removed from bulk substrates exhibit superb optical performance due to their flexibility, thinness and transparency, which enables many new micro-cavity configurations [154]. It also facilitates the integration of thin-film devices with flexible or heat-conductive backplanes, as well as heterogeneous integration with other components, such as for multi-colour emission on a single chip using transfer printing [27, 155, 156]. Various techniques can be used to release devices from their original substrates, the method for releasing being determined by the growth substrate. For instance, the release

of thin-films of III-N heterostructures grown on silicon can be accomplished by wet etching, as explained in the earlier chapters, due to the high selectivity between nitrides and silicon [157]. Electrochemical (EC) [158] or photo-electrochemical (PEC) etching [159, 160] can been used for releasing GaN-based structures from substrates where selective chemical etching is difficult to achieve (e.g. GaN, sapphire, SiC, bulk (III-N)) [104]. PEC etching relies on photogenerated holes transported to the surface of the semiconductor to act as broken bonds and result in etching of the sacrificial layer. A lot of investigation has been done by using different sacrificial layers in PEC-etching. For instance, a thin ($\leqslant$ 50nm) InGaN layer has been used as the release layer [161, 162], to achieve uniform etching. However, such a thin layer usually does not allow the easy detachment of films as they can easily re-bond with the substrates by van-der-Waals forces. A thicker InGaN sacrificial layer is preferred but is much more difficult due to strain relaxation effects. The photo-generated holes cannot sufficiently diffuse and hence recombine before reaching the semiconductor-electrolyte interface [163]. As a solution, a superlattice structure of InGaN/GaN quantum wells (QWs) was implemented as a thick release layer in PEC etching [164, 165]. Despite the increased confinement of holes, material removal is rather non-uniform at the interface [166]. Therefore, a release layer for PEC-etching that can provide smooth surfaces and be suitable for the transfer-print process is desired. A smooth surface underneath the release devices is needed to minimize scattering loss as well as to have a better adhesion onto the target substrates [167, 168]. The purpose of this chapter is to develop a sacrificial layer that is compatible with transfer printing, and demonstrate that this sacrificial layer can be undercut using PEC etching, where substrates such as sapphire and freestanding GaN serve as the growth substrate. Hence, we introduce a novel sacrificial stack with InGaN/AlInN/GaN configuration. The structure is implemented in a relatively thick sacrificial superlattice structure for PEC etching. Details of the optimization of the sacrificial layer will be discussed and compared with the conventional (InGaN/GaN) sacrificial layer. Additionally, critical parameters will be optimized in the PEC etching process in order to achieve a smooth surface.

4.2 Principle of PEC etching

PEC etching is a particular wet etching process which takes advantages of light (photo) along with electrochemical (oxidation-reduction) reactions to etch. Along with the benefits of wet etching, PEC etch offers additional advantages, including bandgap selectivity [169], dopant

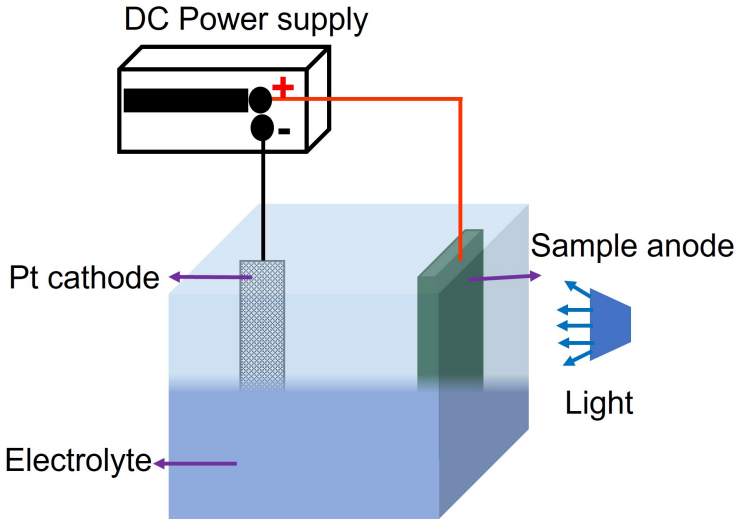

FIGURE 4.1: Schematic of PEC etching.

selectivity [170] and defect selectivity [171]. In order to create a controllable undercut into the epitaxial structure, band gap selectivity is particularly desirable. Structures based on materials with differing band gaps can be used to achieve band gap selectivity. It is possible to selectively etch a material with a narrower band gap by using light whose spectrum is absorbed by narrow-band gap materials, but not by wider band gap materials [160].

PEC etching combines the use of a light source to generate carriers within a material that then reacts chemically with the material to be etched. In PEC processing, the fabricated semiconductor is immersed in a conductive oxidizing electrolyte solution. On the n-side of the semiconductor, metal is deposited. The semiconductor acts as the anode while platinum (Pt) serves as the cathode. A schematic diagram of the PEC etching device is shown in Figure 4.1.

Electron-hole pairs can be generated by irradiating the semiconductor with light of energy. Holes oxidize the material to a soluble form in the electrolyte, and then the electrolyte dissolves the formed oxide. As an example, the following reaction occurs when GaN is etched with PEC etching [172].

$$h\nu \rightarrow e^{-}_{cb} + h^{+}_{vb} \tag{4.1}$$

$$2GaN + 6h^{+}_{vb} + 6OH^{-} \rightarrow Ga_2O_3 + 3H_2O + N_2 \uparrow \tag{4.2}$$

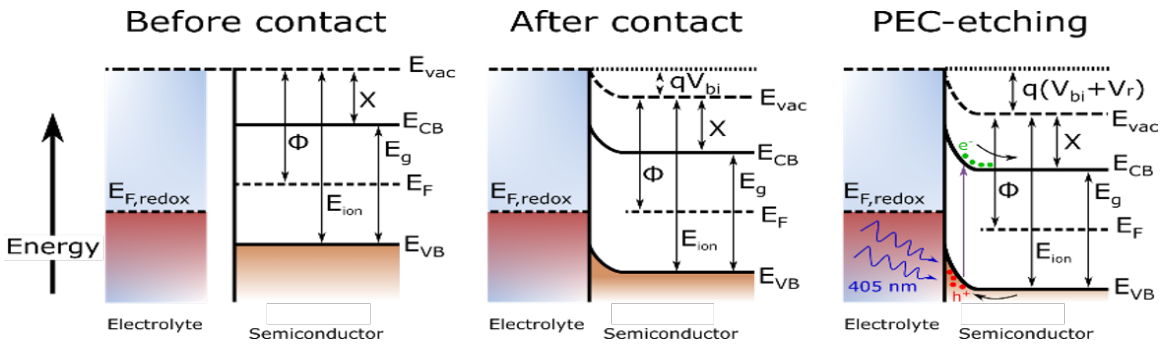

FIGURE 4.2: Schematics of energy bands of semiconductor and electrolyte (a -b) before and after contact and (c) during PEC-etching process where the photo-induced holes in the InGaN are trapped at the interface due to the band-bending.

$$Ga_2O_3 + 6OH^- \rightarrow 2GaO_3^{3-} + 3H_2O \tag{4.3}$$

Due to hole excitation by UV light at the anode of the GaN/electrolyte interface, GaN dissolves into Ga^{3+} ions where electrons flow out the circuit. It can be seen in reaction 4.2 that the oxidized Ga metal reacts with the hydroxide group to form gallium oxide and the oxidized nitrogen becomes N_2 gas. The formed oxide is then dissolved in an electrolyte (reaction 4.3).

This chemical reaction suggests that the actual etching catalyst is a hole. The holes must be confined to an appropriate area of the material in order for complete etching to take place. Therefore, PEC etching is a dopant-selective technique [173]. Figure 4.2 illustrates the band structures of a semiconductor immersed in an oxidizing solution. A Schottky junction is formed at the semiconductor-electrolyte interface where the bands bend upwards due to the existence of surface states which pins the Fermi level. Fermi level is pinned by unoccupied dangling bonds in gallium between 0.5 eV below the conduction band and around mid-gap (the position is determined by Ga/N ratio) [174]. Consequently, in n-type materials, the bands bend upward towards the interface, thereby restricting the number of holes at the surface. The formation of gallium oxide occurs at the semiconductor/electrolyte interface, and etching occurs at this interface.

4.3 Study of sacrificial layer

There is evidence from the chemical reaction that holes act as broken bonds in the PEC etching process, which is why structures that are able to confine and provide higher hole concentrations are highly desirable in the PEC etching process. There has been a recent discovery of a

two-dimensional hole gas (2DHG) in undoped GaN/AlN heterostructures. These observations demonstrate that the polarization can lead to the formation of 2D confined holes at negative polarization difference interfaces without the need for acceptor doping [175, 176]. Due to the high density of holes, this property of GaN heterostructures can be beneficial for PEC etching. The next section will discuss the details of polarization at the interfaces of heterostructures and the methods for creating holes or electrons.

4.3.1 Polarization

The wurtzite III-nitrides exhibit spontaneous polarization which is caused by the deviation of the GaN unit cell from the ideal wurtzite geometry and the strong ionic character of the covalent bond between gallium and nitrogen [177]. In the ideal structure of wurtzite, all bonds possess the same length and bond angles are equal. Therefore spontaneous polarization is zero. However, the lattice structure and ionicity of the bonds in GaN crystals are asymmetric. The bond along the c-axis is longer than the other bonds, and the bond angles deviate from the ideal. As a result, spontaneous polarization occurs.

Additionally, piezoelectric polarization is induced in heterostructures by lattice mismatches between layers. As an example, if AlGaN is grown on GaN along the [0001] direction and the GaN layer is sufficiently thick, there will be tensile strain at the interface because AlGaN has a lower a lattice constant than GaN. Due to the strain, the bond lengths and angles are altered, resulting in piezoelectric polarization [178].

Piezoelectric polarization is generally described by a tensor, however, it can be simplified for biaxially strained epilayers growing in the [0001] direction by expressing it as :

$$P_{pz} = 2\varepsilon_{xx}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{4.4}$$

with piezoelectric coefficient e_{31} and e_{33}, and elastic constants C_{31} and C_{33}. ε_{xx} is the isotropic in-plane strain, given by $\varepsilon_{xx} = \frac{a-a_0}{a_0}$, where a_0 is the relaxed in plane lattice constant of layer and a is the lattice constant of strained layer. Since $e_{31} - e_{33}\frac{C_{13}}{C_{33}} < 0$ is valid for AlGaN, InGaN, and AlInN, over the whole range of compositions, Equation 4.4 implies that the piezoelectric polarization is negative for tensile strained crystals and positive for compressive strained crystals. This means that the piezoelectric polarization for a layer under tensile stress is in the $[000\bar{1}]$ direction, while that for a layer under compressive stress is in the [0001] direction.

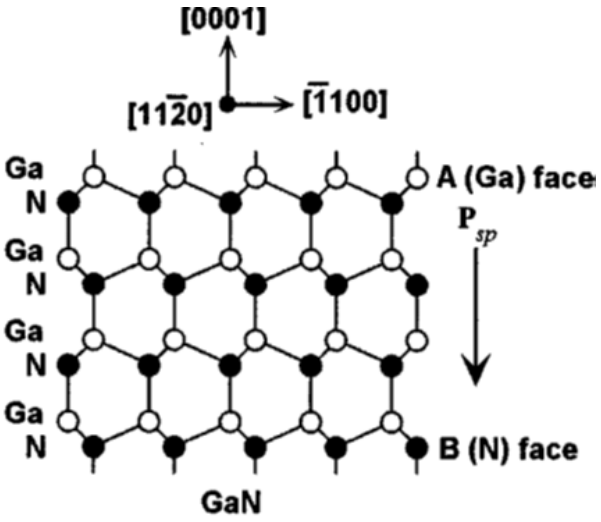

FIGURE 4.3: Spontaneous polarization field direction of GaN. Note that open circles refer to the Ga. Adapted from [179]

Note that the orientation of spontaneous polarizations is defined on the basis that the positive direction leads from the metal (cation) towards the nearest nitrogen atom (anion) along the c-axis . It means that for GaN and its alloy the spontanous polarization field is directed to the $[000\bar{1}]$ as indicated in Figure 4.3.

As a result, the orientation of piezoelectric and spontaneous polarizations is parallel when the layer is under tensile stress, while anti-parallel when it is under compressive stress. In Figure 4.4 the directions of the spontaneous and piezoelectric polarization are given for Ga-face, N-face, of AlGaN/GaN, InGaN/GaN and AlInN/GaN heterostructures. In Figure 4.4, P_{SP} stands for spontaneous polarization, P_{PE} stands for piezoelectric polarization, and σ denotes charge density.

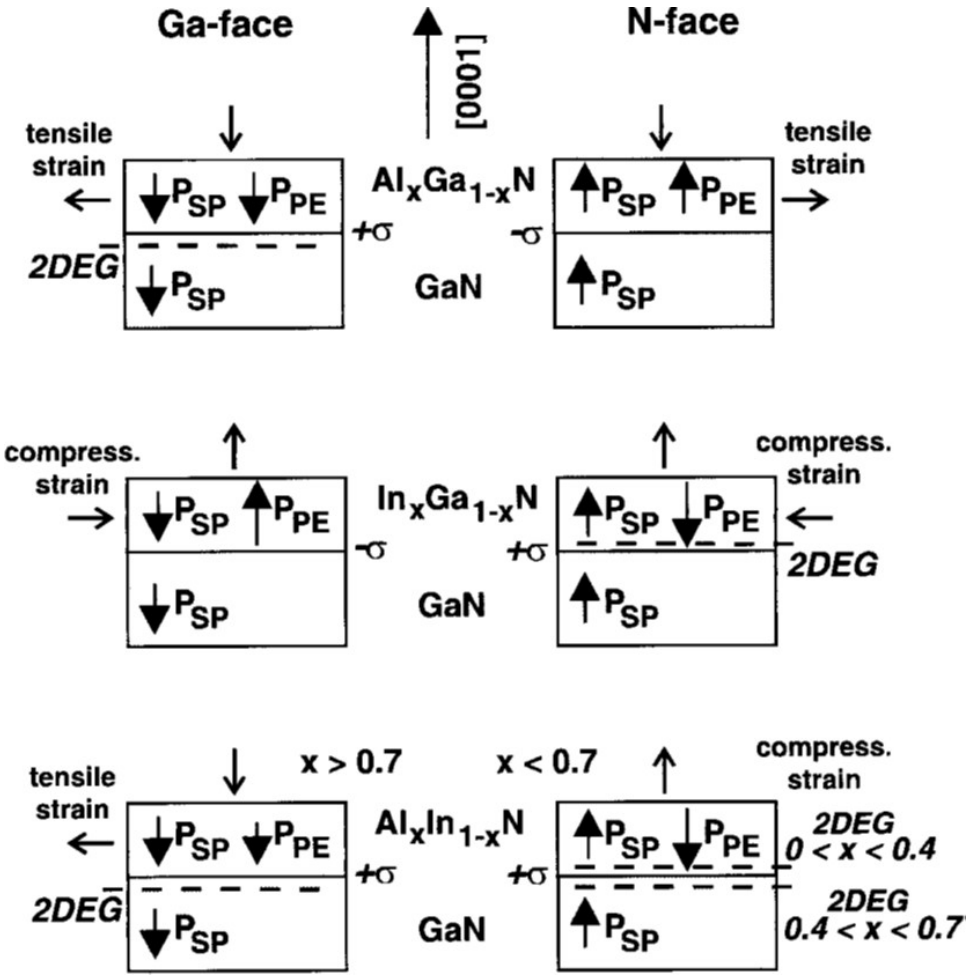

FIGURE 4.4: The orientation of the spontaneous and piezoelectric polarizations in pseudomorphic grown wurtzite AlGaN/GaN, InGaN/GaN, and AlInN/GaN heterostructures with Ga- or N-face polarities. In the case where the polarization induced charges is positive, a 2DEG can be confined close to the interface in the layer with a smaller bandgap. Adapted from [178]

The net polarization field inside one layer is the sum of spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pz}), $P = P_{sp} + P_{pz}$. For instance, for AlGaN/GaN, the total polarization of both layers is directed towards the substrate for Ga-face and towards the surface for N-face polarity crystals (see Figure 4.4). In compressively strained InGaN/GaN for Ga polar, P_{sp} points toward the substrate, while the P_{pz} orientated towards the surface. In this case, the P_{sp} can be partially or completely compensate by the P_{pz}.

With respect to a gradient of polarization in space, polarization induces a charge density that is given by:

$$\rho_p = \nabla P \tag{4.5}$$

As an analogy, at an abrupt interface of a top/bottom heterostructure, polarization may decrease or increase within a bilayer, resulting in a fixed polarization charge density at the interface.

$$\sigma = P_{top} - P_{bottom} = P_{sp}(top) + P_{pz}(top) - P_{sp}(bottom) \tag{4.6}$$

where the P_{top} is the net polarization of the top layer and P_{bottom} is the spontaneous polarization of the bottom layer. When the polarization induced sheet charge density ($+\sigma$) is positive, free electrons will tend to compensate the polarization induced charge, resulting in the formation of a two-dimensional electron gas (2DEG). In this case, the conduction band in the triangular quantum well will drop below the Fermi level, thereby confining the electron carriers. By contrast, a negative sheet charge density ($-\sigma$) will cause an accumulation of two-dimensional hole gas (2DHG), and the valance band edge is shifted upward to cross the Fermi level close to the interface. As an example growing $In_xGa_{(1-x)}N$ on GaN along the [0001] direction can provide the 2DHG. Note that the amount of polarization induced sheet charge density at $In_xGa_{(1-x)}N/GaN$ interface depends on the In-content (x) and the thickness of the $In_xGa_{(1-x)}N$. Thus by applying Equation 4.6 to $In_xGa_{(1-x)}N/GaN$ and assuming linear interpolation between their physical properties, we can calculate σ as follows:

$$\begin{aligned}\sigma(x) &= P_{sp}^{In_xGa_{(1-x)}N} + P_{pz}^{In_xGa_{(1-x)}N} - P_{sp}^{GaN} \\ &= P_{sp}^{In_xGa_{(1-x)}N} - P_{sp}^{GaN} + 2\frac{a(x)-a_0}{a_0}(e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)})\end{aligned} \tag{4.7}$$

where $e_{31}(x)$ and $e_{33}(x)$ are the piezoelectric coefficient of $In_xGa_{(1-x)}N$. $C_{13}(x)$, $C_{33}(x)$ are the elastic constants of $In_xGa_{(1-x)}N$. a_0 is the relaxed in-plane lattice constant of InGaN while $a(x)$ is the lattice constant of strained $In_xGa_{(1-x)}N$ on GaN. Calculations in SiLENSe are based on the material parameters listed in the Table 4.1 and all the InGaN and AlInN parameters were estimated assuming Vegard's law.

TABLE 4.1: Applied material parameters for the calculation [180]

	GaN	AlN	InN	$Al_xIn_{(1-x)}N$
Lattice constant (A^0)				
a	3.189	3.112	3.548	3.112 x + 3.548 (1-x)
c	5.185	4.982	5.76	4.982 x + 5.760 (1-x)
Spontaneous polarization (C/m^2)				
P_{sp}	-0.029	-0.081	-0.032	-0.081 x- 0.032 (1-x)
Piezoelectric constant (C/m^2)				
e_{31}	-0.49	-0.6	-0.57	-0.6 x - 0.57(1-x)
e_{33}	0.73	1.46	0.97	1.46 x + 0.97(1-x)
Elastic constant (GPa)				
C_{13}	100	127	108	127 x + 108 (1-x)
C_{33}	392	382	399	382 x + 399 (1-x)

Polarization charge density bound at the heterointerface of the $In_xGa_{(1-x)}N/GaN$ and $Al_xIn_{(1-x)}N/GaN$ heterostructure grown on Ga-face GaN as a function of alloy content is shown in the Figure 4.5. As can be seen in Figure 4.5 a low indium content in InGaN alloys will result in a high piezoelectric charge density at the InGaN/GaN interface, and consequently the formation of 2DHG. Furthermore, it is possible to form 2DHG or 2DEG by changing the composition of AlInN at the AlInN/GaN interface.

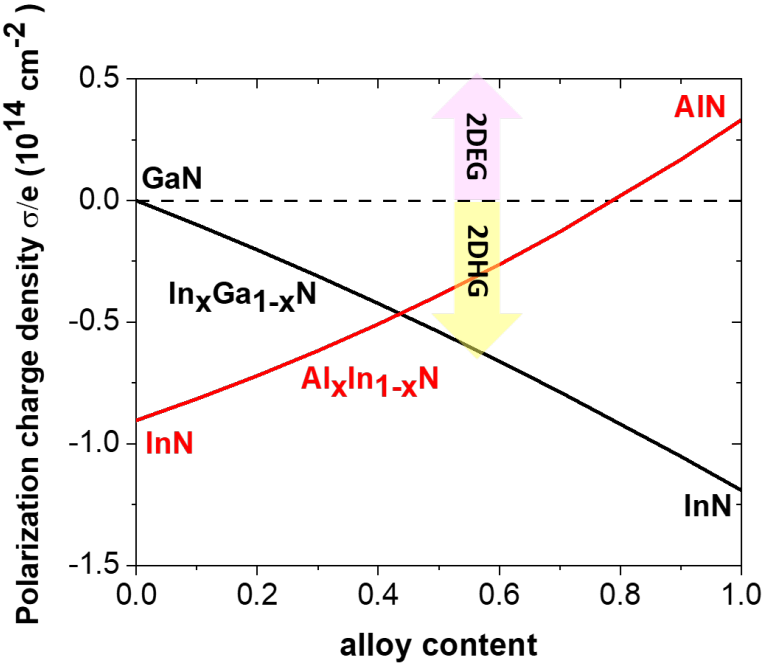

FIGURE 4.5: The density of polarization charges bound at the heterointerface of InGaN/GaN and AlInN/GaN heterostructures grown on Ga-face GaN. Positive signs indicate the presence of a 2DEG, while negative signs indicate the presence of a 2DHG.

As stated before, free electrons tend to compensate a positive polarization induced sheet charge which is bound at the hetero-interfaces i.e AlGaN/GaN . The sheet electron concentration $n_s(x)$

located at the interface of the nominally undoped AlGaN/GaN structure can be calculated by the following equations[180, 181]:

$$\begin{aligned} n_s(x) &= \frac{\sigma(x)}{e} - (\frac{\varepsilon_0\varepsilon(x)}{d_{AlGaN}e^2})[e\phi_B(x) + E_F(x) - \Delta E_C(x)] \\ n_s(x) &= 1 + [\frac{\varepsilon(x)d_{GaN}}{\varepsilon(0)d_{AlGaN}}]^{-1}[\frac{\sigma(x)}{e} - (\frac{\varepsilon_0\varepsilon(x)}{d_{AlGaN}e^2})] \times [e\phi_b^{eff}(x) + E_F(x) - \Delta E_C(x)] \end{aligned} \tag{4.8}$$

$\varepsilon(x)$ is the relative dielectric constant of $Al_xGa_{(1-x)}N$, d_{AlGaN} and d_{GaN} are the thickness of barrier and cap layer respectively. $e\phi_B(x)$ is the effective Schottky barrier energy. $E_F(x)$ is the Fermi level with respect to the GaN conduction band energy. In Equation 4.8, it is shown that the value of the sheet carrier concentration is dominated by the total polarization induced sheet charge which can be controlled by the alloy composition of the barrier. As well as the alloy content, according to the Equation 4.8 the concentration of free carriers is affected by the thickness of the barrier and cap layer. The concentration of sheet carriers will decrease with increasing Schottky barrier height and decreasing barrier thickness. Hole concentration density can also be calculated using the same principle of polarization. It has been reported that the sheet density of holes in InGaN/GaN or InGaN/InN varies with the thickness of the InGaN layer [182, 183]. As shown in the Figure 4.6, hole gases are difficult to confine in thin layers of InGaN ($< 5nm$) [182]. The high density of 2DHG at undoped pseudomorphic InGaN /AlN has recently been reported by Chaudhuri et al [184].

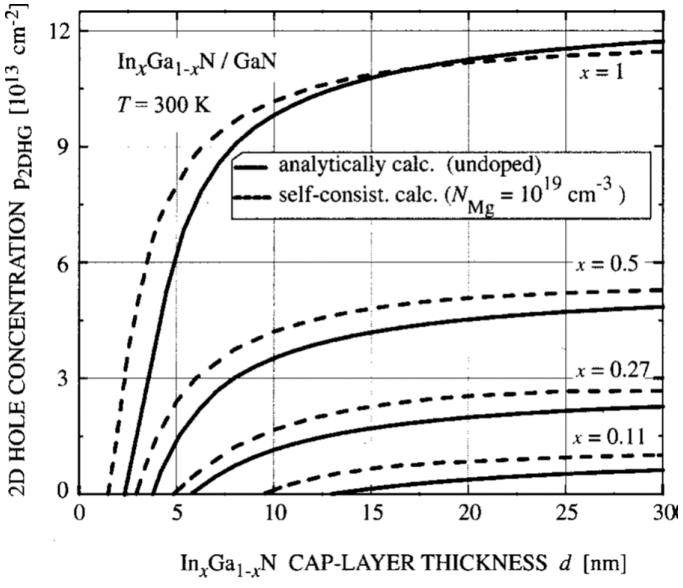

FIGURE 4.6: The dependence of the 2DHG density on the thickness of the InGaN capping layer for different indium contents x of the capping layer. Adapted from [182]

It is notable that misfit dislocations are a common phenomenon in heteroepitaxy, a process in which a thin film is grown on a substrate with lattice parameters that differ considerably. As long as a hetero-epitaxial film is thinner than a critical thickness h_c, it can be grown pseudomorphically on a substrate, while thicker films result in a relaxation of misfit strain via plastic flow. The critical thickness of InGaN with 20% indium content is around 4 nm [185]. Therefore, it should be noted that although thick InGaN is beneficial for the formation of 2DHG, it may result in relaxation issues.

AlInN is one of the important nitride-based alloys which can be lattice-matched to GaN for an alloy with an In content of 18% with a bandgap of of 4.4 eV [186, 187]. Research on AlInN has extensively utilized this lattice matching property to develop AlInN/GaN distributed Bragg reflectors [188, 189], high-electron-mobility transistors [190, 191] and integration as barriers in quantum-well LEDs [192]. Furthermore, a lattice-matched AlInN/GaN interface does not represent an exception to the rule for producing polarization and Yoshida et al. investigated the accumulation of holes (top interface) and electrons (bottom interface) at undoped GaN/undoped AlInN/ undoped GaN interfaces [193].

The properties of AlInN and the possibility of formation of dopant-free holes at the its interface motivated us to investigate the interface of InGaN/AlInN and its effect on the PEC etching process as a sacrificial layer.

4.3.2 Band diagram simulation

Here, we investigate an interface of InGaN grown on AlInN for the formation of a 2DHG in the InGaN. The nominal indium concentration in the InGaN layer was 17% with a bandgap of of 2.8 eV to achieve selective etching and 18% in AlInN layer to obtain lattice-match conditions with GaN. Figure 4.7 (a,b) illustrates the structures compared here: GaN (10 nm) / InGaN (2 nm) / (10 nm) GaN and GaN (10 nm)/ InGaN (2nm) / AlInN (variable) / (10 nm) GaN . Here, we keep the thickness of InGaN constant and vary the barrier (AlInN) thickness. AlInN thicknesses of 7.5, 15 and 30 nm were considered. The energy band diagrams for the structures above were simulated under an applied bias of 2 V using commercially available SiLENSe, a self-consistent one-dimensional Poisson solver from STR Inc [194]. This software is intended for modeling of LED heterostructures based on direct-bandgap wurtzite semiconductors –group-III nitrides and group-II oxides. This software implements a one-dimensional drift diffusion model that accounts for the specific characteristics of the wurtzite materials - a strong piezoelectric

effect, possible spontaneous electric polarization in epitaxial layers of III-nitride. The simulation parameters used were based on the standard values defined within the built-in database of the software SiLENSe, which are reported in Table 4.1. It should be noted that these "standard" values are based on relevant literature reviews on the lattice parameter [195], elastic constant [196], polarization constant [197], energy gap [198] and bowing parameter [199]. The magnified band diagram together with the calculated hole concentration for each structure are presented in Figure 4.7 (c-d).

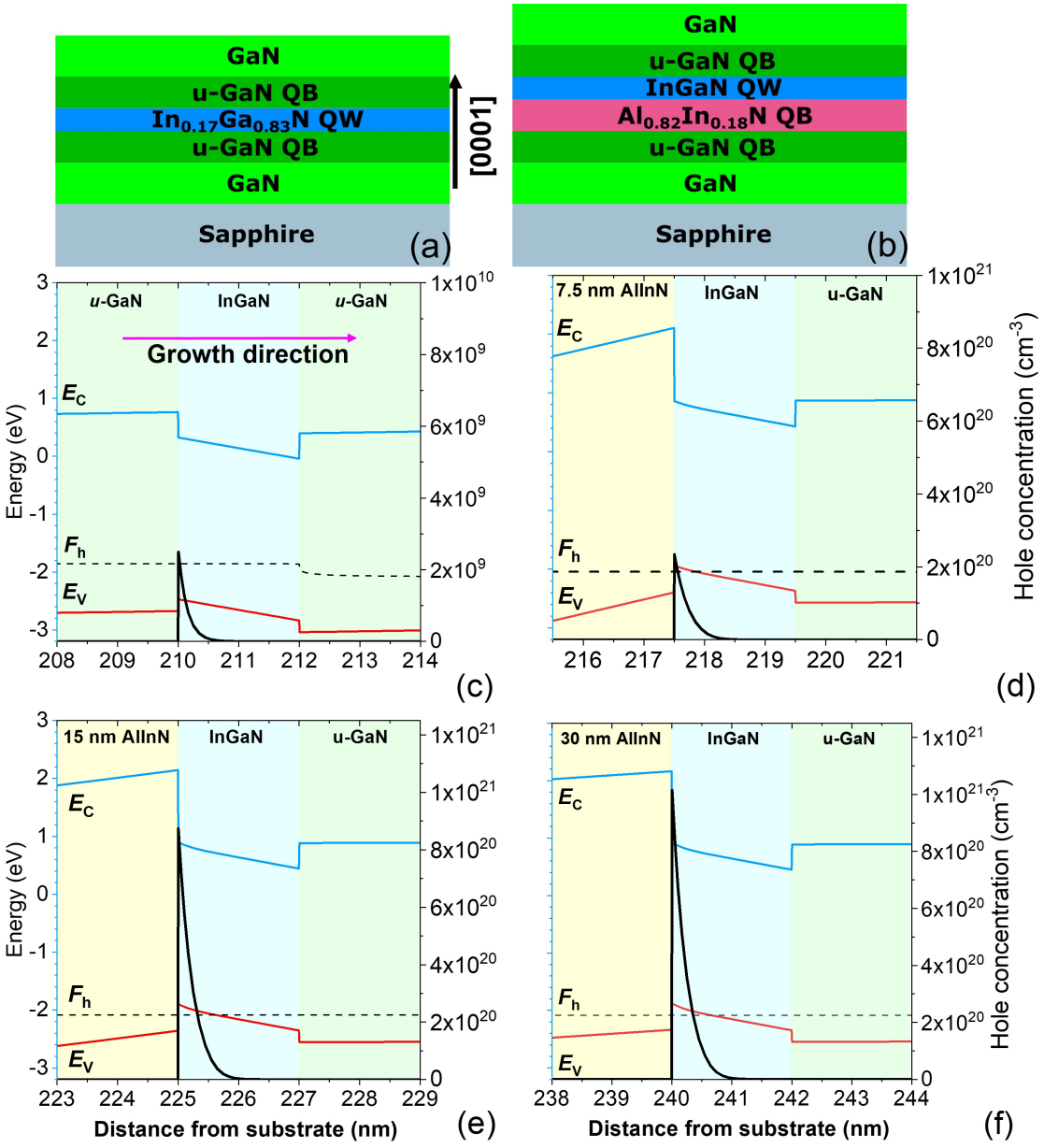

FIGURE 4.7: Cross-sectional schematic of structures without AlInN (a) with AlInN (b) as barrier. (c-f) Magnified of simulated energy band diagrams and calculated hole concentrations at a bias of 2 V applied to the GaN for AlInN layer thicknesses of 0, 7.5, 15 and 30 nm respectively are shown. The dashed line shows the Fermi level.

The net polarization field is the sum of spontaneous polarization (P_{sp}) and the lattice-mismatch induced piezoelectric polarization (P_{pz}), i.e. $P = P_{sp} + P_{pz}$. At the InGaN/GaN interface, the polarization discontinuity is $P = P_{sp}^{InGaN} + P_{pz}^{InGaN} - P_{sp}^{GaN}$, while for the InGaN/AlInN interface, assuming that AlInN is lattice matched with GaN, $P = P_{sp}^{InGaN} + P_{pz}^{InGaN} - P_{sp}^{AlInN}$. The sign of the net polarization of InGaN is opposite to AlInN resulting in a net increase in charge at the interface. The calculated net polarization field in the InGaN layer is 1.7 MV/cm for the InGaN/GaN structure but increases to 2.5 MV/cm for InGaN/AlInN. As depicted in Figure 4.7 (d-f), the presence of the AlInN underlayer and the polarization induced at the interfaces results in an electric field across the AlInN layer lifting of the energy for the InGaN QW bringing the valence band maximum to the Fermi level thereby increasing the 2DHG densities of $1.3 \times 10^{13} cm^{-2}$ at the the InGaN/AlInN (7.5 nm) interface, while the hole density is only 37 cm^{-2} for the conventional InGaN/GaN structure. A lower density of 2DHG for thin InGaN is in agreement with previous results reported [184]. As can be seen in Figure 4.8 with increasing AlInN thickness, the corresponding hole density increased to $1.9 \times 10^{13} cm^{-2}$ (15 nm) and $2.3 \times 10^{13} cm^{-2}$ (30 nm). The values for 2DHG have been calculated by integrating the peak area of the hole concentration in Figure 4.7. As can be seen from results, inserting AlInN barrier is beneficial to enhancing 2DHG, with fixed thickness of InGaN layer.

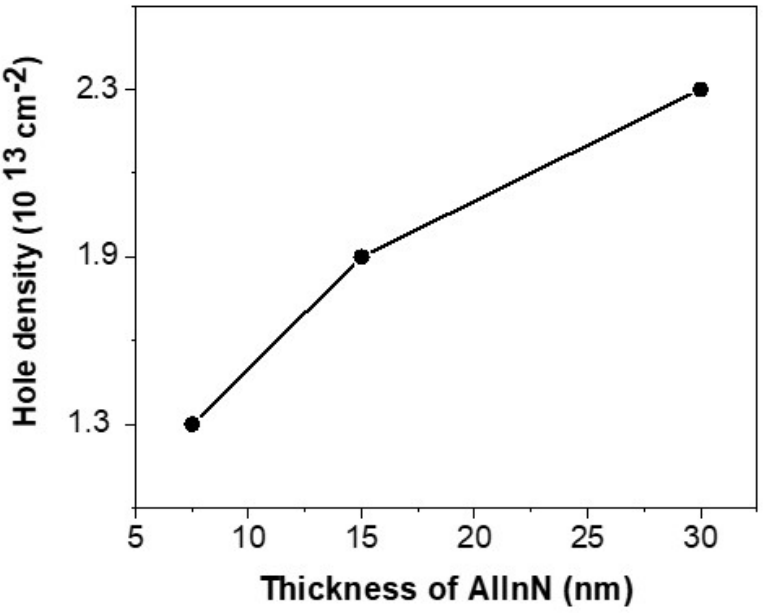

FIGURE 4.8: Hole density as a function of AlInN thickness for a fixed thickness of InGaN of 2 nm.

Moreover, the induced triangular shape of the energy bands in the InGaN layer leads to a reduced overlap of the electron and hole wave functions. Hence, electron and holes are separated to opposite sides of the QW reducing the recombination probability. Therefore, due to band

bending and the two-dimensional hole carrier channel, a large number of holes are available to reach the InGaN-electrolyte interface and finally contribute to the etching process.

4.3.3 C-V measurement

Capacitance-Voltage measurements of Schottky diodes can be used to as a characterization method for structures with 2DHG and 2DEG. Thus, to confirm the existence of a 2DHG at the InGaN (2nm)/AlInN interface, two structures, without and with, a 10 nm-thick AlInN layer (labelled as S1 and S2) were grown by metal-organic chemical vapour deposition (MOCVD) on c-plane AlN/Sapphire templates and capacitance-voltage (C-V) measurements performed. The growth was carried out by the MOCVD group at the Tyndall National Institute.

To prepare the sample for measurement, first samples were cleaned with BOE, HCl and KOH diluted in water. Then a photolithography process was done to pattern the wafer with variable diameter contacts. A thin layer of (50 nm) Pd was deposited using evaporation to form a Schottky contact to 10-nm of GaN. Note that C-V measurements must have two contacts: one Schottky and one ohmic. Pd on undoped GaN forms a Schottky contact, so that is what is used. After the metal deposition a following lithography step was done to expose n-layer around the contacts to avoid current spreading and get better IV characteristics. Note that GaN is undoped in principle, but there is an n-doping background present. Ti/Au (20 nm/200 nm) forms the n-contact pad on the lower GaN layer. Optical image and a schematic of the undoped structures used in C-V measurements are shown in Figure 4.9.

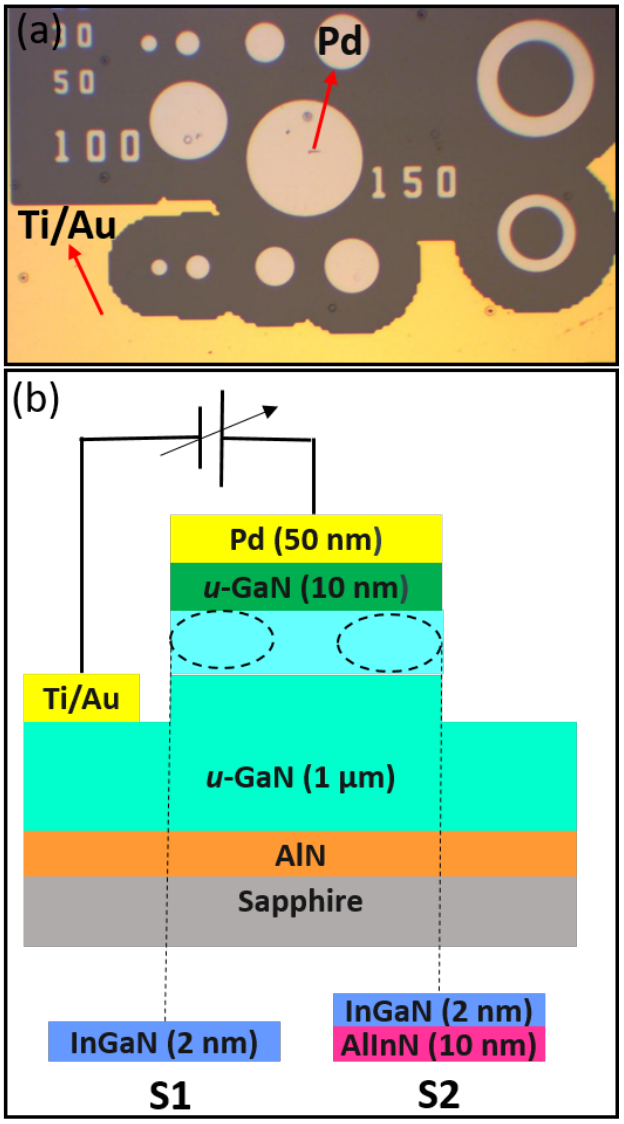

FIGURE 4.9: (a) Optical image and (b) a schematic of the structures used in C-V measurement.

The system used to obtain the capacitance measurements was an Agilent B1500 with a CV enabler connected to an Attogard cascade prober. This machine allows to drive voltage and add a small AC signal with different frequencies. The dependence of capacitance on frequency is shown in the Appendix A.2.2. However, in this case the ac modulation level of 25 mV and the high scan frequency of 1 MHz were used to ensure that all interface states cannot respond to AC signals, but only follow DC gate biases. The voltage was swept from -3 to 3V with a step of 0.1V. An analysis of the size dependence of capacitance is also presented in the Appendix A.2.1. C-V measurement for circle-shaped Schottky contacts with 150 diameter are performed at different temperatures 300 K and 223 K in order to confirm that the formed carrier is related to polarization and not due to the impurity doping.

Figure 4.10 presents capacitance as a function of voltage. Solid line indicates the capacitance at room temperature, whereas dashed line indicates that of 223 K temperature.

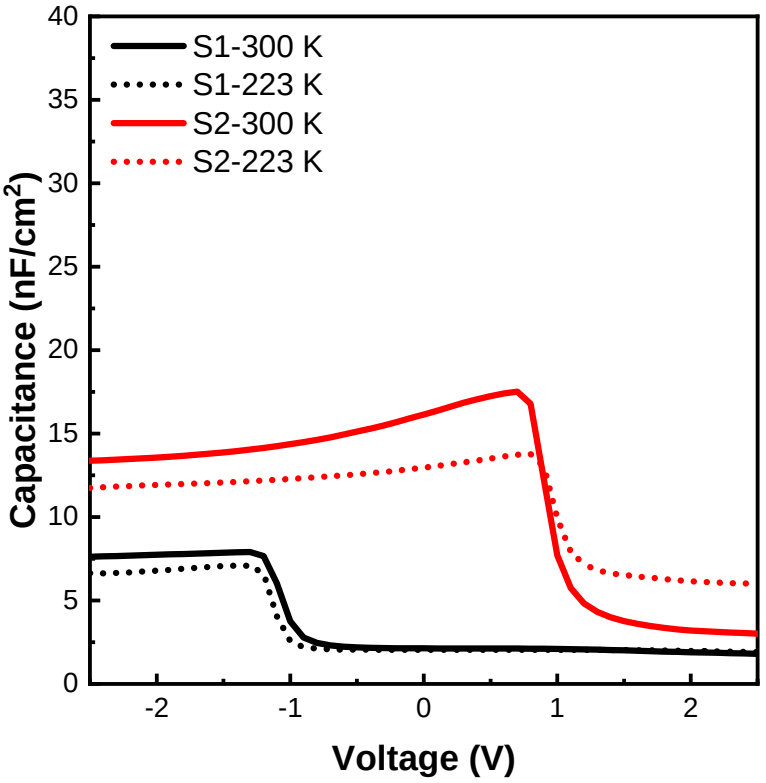

FIGURE 4.10: C-V characteristics of samples without (S1) and with (S2) 10 nm AlInN measured at 223 K and 300 K as a function of bias.

Applying a positive bias on the Pd results in a reduction of the capacitance in both samples implying an increased depletion layer confirming the assumption that the free carriers in both structures are holes. The nearly flat capacitance at negative bias indicates the formation of 2DHG at the interface.

At zero voltage, the structure with AlInN layer exhibits a higher capacitance (15 nF/cm^2) attributed to the increased 2DHG. With reverse bias applied, capacitance has a small decrease but it is almost constant below -2V, which is a result of the localized holes at the interface. When, for example, 0.5 V is applied the capacitance does not change and the carriers remain stationary, so higher voltage is needed to force holes away from the interface.

However, at 0 V bias in the sample without AlInN the capacitance is much lower (2 nF/cm^2). In this structure, there are relatively few free holes, almost none, as indicated by the simulation as well. A negative bias is applied to the structure and holes are attracted. This means there is no 2D hole gas within the structure, but rather holes absorbed from other layers and form capacitance. In this case, this structure has a capacitance that is at least two times lower than

the structure with AlInN. More significantly it can only be induced with an external bias in contrast to the structure with AlInN. Note that the voltage shift in S2 compares with Sample 1 is caused by the high hole density in S2, requiring a higher voltage for depleting the structures.

Additionally, the C-V measurements were conducted at a low temperature (223 K) in order to determine whether capacitance is temperature-dependent. In the case of C–V curves from a Mg-doped GaN layer, the capacitance value is strongly influenced by temperature [200, 201] due to the the high activation energy of magnesium. Mg has a large activation energy (150 meV to 250 meV) [202, 203], which results in a low probability of acceptor ionization, so in order to activate the Mg doped GaN layer, the samples tend to anneal. By reducing the temperature, in C-V measurement the holes can freeze out, causing the capacitance to be strongly impacted. Conversely, the C-V profile of the polarization-induced 2DHG is temperature independent due to the fact that the 2DHG is temperature independent [200]. For comparison, the 2DHG is calculated at two temperatures. Since the capacitance is defined as $C(V_{applied}) = edQ/dV$ the 2DHG densities can be obtained by integrating the CV curves. In accordance with this equation, 2DHG for S2 at 300 K and 223 K is around $3.3\times10^{11}cm^{-2}$ and $2.3\times10^{11}cm^{-2}$ respectively. As shown in the Figure 4.10 and calculated 2DHG, the C-V characteristics are almost independent of the temperature. It is evident that the 2DHG density is independent of temperature. However, the net hole density does not match with the hole density calculated in simulation that was approximately ($1.3 \times 10^{13}cm^{-2}$). This may be attributed to the compensation of hole gas with electron gas at the interfaces. This results in a reduction in measured capacitance and consequently a reduction in measured 2DHG. In order to understand its causes, further investigation is required.

4.3.4 PEC etching of designed sacrificial layers

Our theoretical and experimental analysis indicated that hole formation could be favoured for a layer of InGaN grown on a layer of AlInN. We thus experimented with PEC etching on such structures. Four structures (labelled as A, B, C and D) were designed in this work for the PEC etching process, all of which were grown by metal-organic chemical vapour deposition (MOCVD) on c-plane AlN/Sapphire templates. The epi-layers consist of a 500-nm unintentionally-doped GaN (u-GaN)/ 1.5-μm-thick n-doped GaN (n-GaN) buffer layer, 4 pairs of either InGaN/GaN or InGaN/AlInN/GaN stacks as the sacrificial layers, followed by 1 μm u-GaN capping layer. The sacrificial layer in sample A is the conventional InGaN/GaN (2 nm/10 nm) while samples B, C and D is GaN(60 nm)/InGaN(2 nm)/AlInN with AlInN thickness of (7.5, 15 and 30 nm) ± 1nm respectively. The nominal indium concentration in the InGaN layer was 17% to achieve selective etching and 18% in AlInN layer to obtain lattice-match conditions with GaN. The structures are depicted in Figure 4.11.

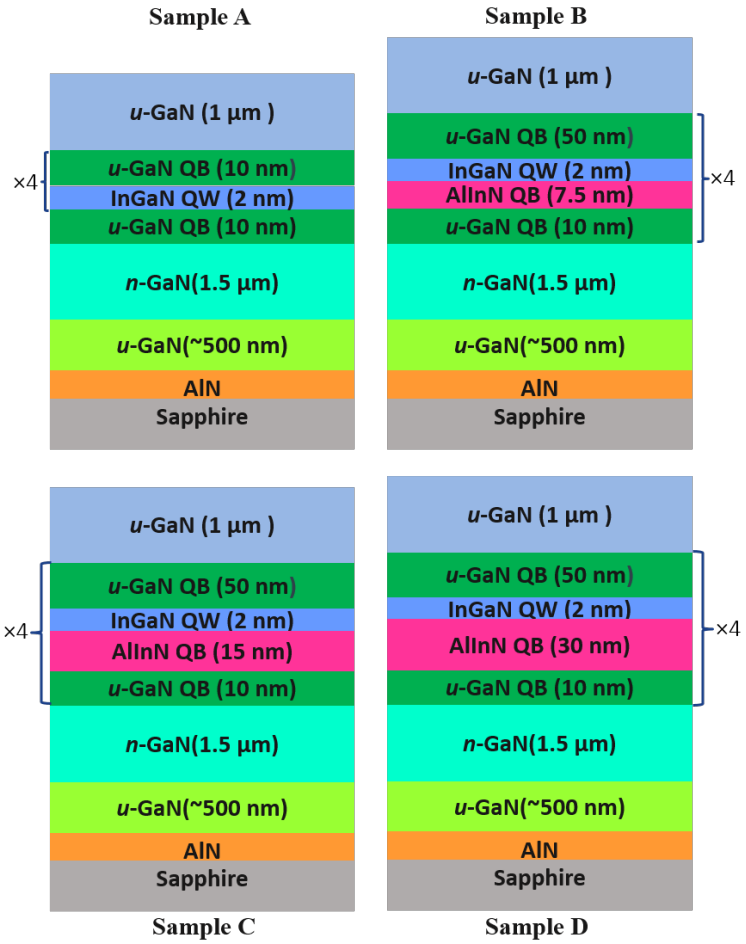

FIGURE 4.11: Cross-sectional schematic showing the four types of structures utilized in PEC-etching experiments.

To prepare samples for PEC etching, first the wafers were cleaned with acetone and IPA, then thoroughly rinsed by de-ionized (DI) water. After that the wafer was dipped into BOE for 5 minutes and rinsed by DI. Then the samples were put into $1:1$ = HCl:DI for 5 minutes and rinsed. Finally, the samples were dipped into 45% KOH solution at $90°C$ for 30 seconds and the thoroughly rinsed by DI and dried up by OFN.

After surface treatment, 300 nm SiN_x was deposited by PECVD as a hard mask. Lithography was then performed for patterning array of mesas with size of 50 μm × 50 μm and 20 μm × 100 μm. This was followed by inductive coupled plasma etching through the sacrificial layers to the top of the n-GaN current spreading layer. A mixture of In and Ga was used as contact pad on the n-GaN. Then photoresist was removed using 1165 solution as this would dissolve during the PEC etch. A schematic of the flow process and the of sample for PEC ethcing is depicted in Figure 4.12.

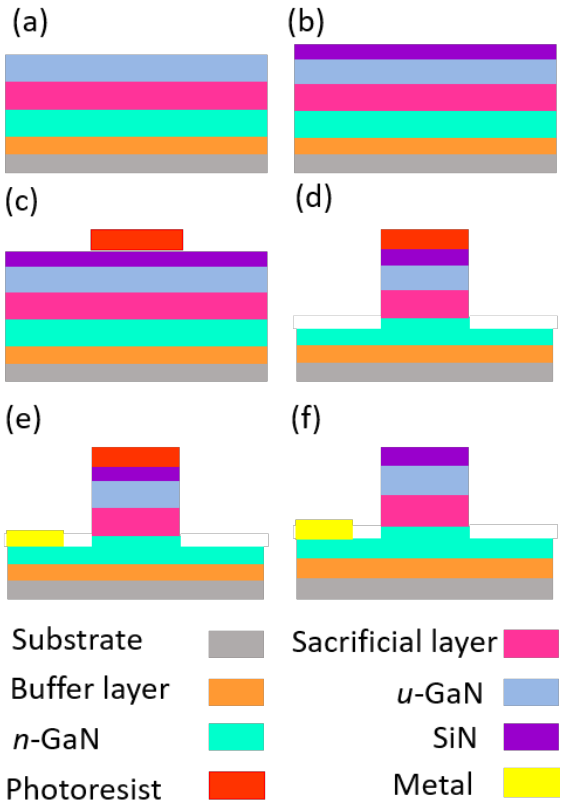

FIGURE 4.12: Schemtatic of the process flow. (a) epitaxial structures of sample (b) SiN depostion (c) Lithography for mesa patterning (d) dry etch to the n-GaN (e) Metal deposition (f) remove photoresist.

The PEC etching was performed by dipping the samples into electrolyte solution at room temperature. The electrolyte used was either KOH or HNO_3 solutions. The PEC etching process uses an applied bias and the illumination of sample with an external optical source

[159]. The energy of the excitation photon is higher than the bandgap of the sacrificial InGaN but less than the bulk GaN materials to achieve the band-gap selective PEC-etching. Here, the samples were illuminated from the front side by a focused $405 - nm$ LED (Nichia) with a power density of 105 mW/cm^2. An external dc bias fixed at positive 2.0 V was applied on the n-GaN of sample as the anode contact, and platinum mesh (Pt mesh) in the electrolyte solution was used as the ground electrode. After etching, the samples were rinsed in DI water and dried and checked by optical microscope. The released films were picked up using PDMS, allowing characterization of the N-polar GaN surface using atomic force microscopy (AFM) and scanning electron microscopy (SEM). The schematic of setup used for PEC etching is shown in the Figure 4.13.

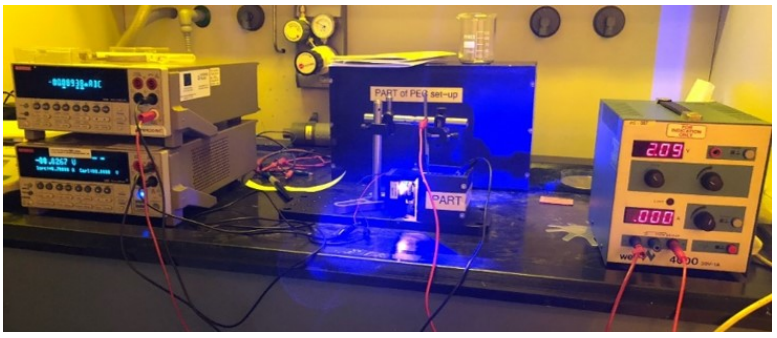

FIGURE 4.13: PEC setup used in these experiments.

4.3.5 Investigate the effect of AlInN

To investigate how the different sacrificial layers affect the releasing process, and to determine the effect of AlInN thickness, PEC etching on four structures (A, B, C & D) with corresponding AlInN thicknesses of 0, 7.5, 15 and 30 nm, respectively was carried out under the identical conditions, i.e. using 0.1 M KOH with bias of 2 V.

The optical images and SEM cross-section during PEC etching and backside morphology of the center of mesas after fully undercut are shown in Figure 4.14. As depicted, the undercut formation is apparent in all the samples meaning that enough carriers were photo-generated, and finally, able to contribute in the etching process. The lateral etch rates are 0.5 (A), 1.8 (B), 2.3 (C) and 2.5 $\mu m/min$ (D), respectively. All the structures with AlInN (sample B, C & D) exhibit a higher etch rate than that without AlInN (sample A). With increasing AlInN layer thickness etch rate first increased ($1.8 \rightarrow 2.3$ $\mu m/min$) and then saturated ($2.3 \rightarrow 2.5$ $\mu m/min$). This result agrees with simulations exhibiting increasing hole densities versus

the AlInN-thickness. An increased etch rate in the presence of AlInN indicates that electrons and holes are less likely to recombine before reaching the electrolyte.

Based on the optical and SEM images in Figure 4.14, the best surface morphology after releasing was observed in Sample B with 7.5nm thick AlInN. The etching homogeneity became worse with increasing AlInN thickness, where a rougher surface was observed. Possible reason might relate to the challenges in growing thick AlInN layers with MOCVD. Due to the different optimal growth conditions for AlN and InN, the AlInN layer suffers from composition in-homogeneity and poor surface morphology [204]. Such issue would become more severe with increasing thickness, which eventually has implication on the homogeneity of PEC etching. One observation is that 'whiskers' are formed on the etched surface and the density becomes higher for thicker AlInN samples. These dislocation-related whiskers indicate the degradation of the crystalline quality in thicker AlInN samples. Therefore, it can be concluded that although thicker AlInN is beneficial for enhancing the PEC etch rate, it results in rougher interfaces and in-homogeneous etching. Following optimization of the thickness of AlInN, the LED structures were grown on sapphire with a sacrificial layer consisting of Sample B and the results are shown in the Appendix A.3.

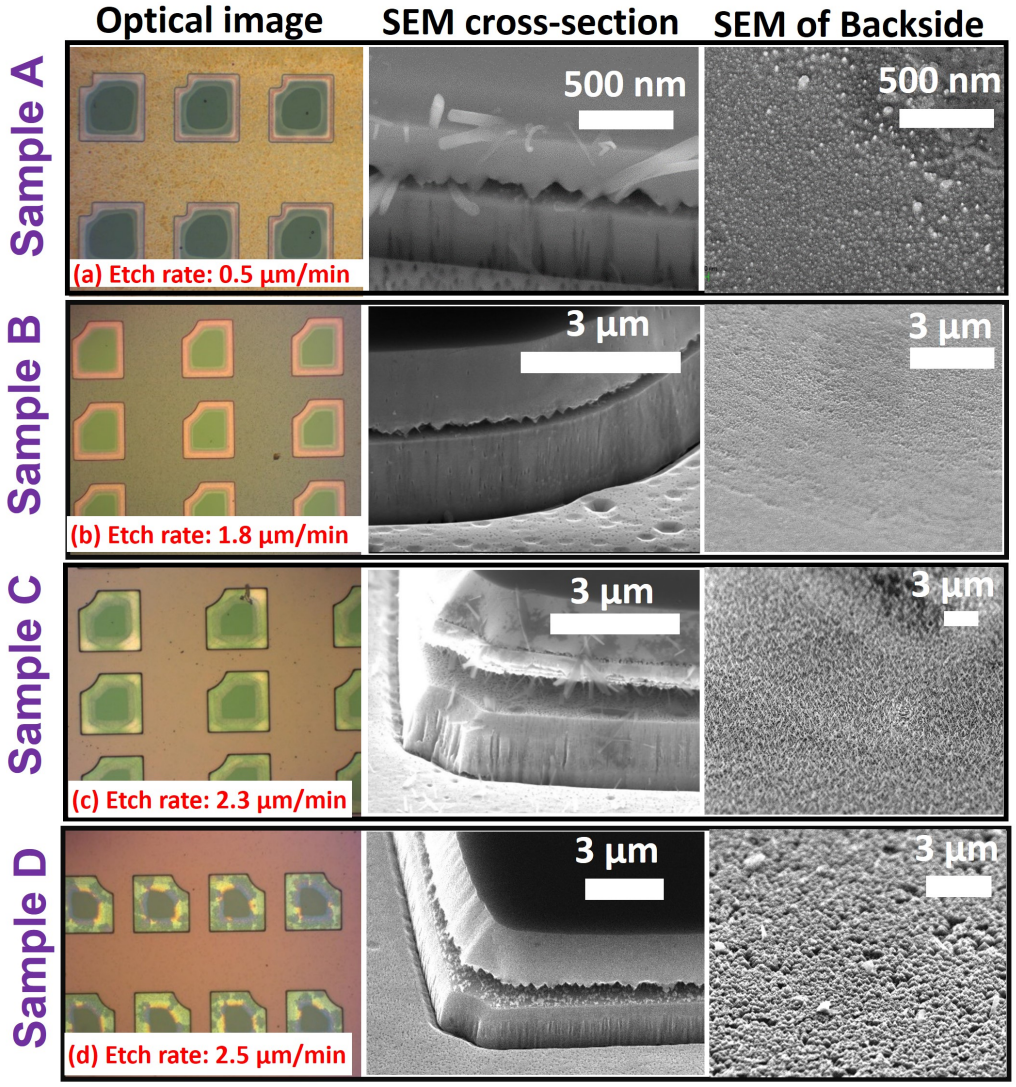

FIGURE 4.14: Optical (top-view) and SEM (cross-section and center of backside) after PEC-etching of samples (a) w/o, (b) 7.5 nm, (c) 15 nm and (d) 30 nm AlInN with size of 50×50 μm^2 under front-illumination with a power density of 105 mW/cm^2, a bias of 2 V and 0.1 M KOH solution.

4.3.6 Effect of electrolytes in the PEC-etching

As stated previously, a smooth surface underneath the release devices is critical to minimize scattering loss for variable applications. Therefore, in order to improve the surface morphology of the backside of the released devices, the effect of different electrolyte on PEC etching has been studied.

We have first investigated the effects of different KOH concentrations on PEC etching (etch rate and surface morphology) on Sample A. Figure 4.15 (a-c) presents the optical (top-view) image of Sample A during PEC etching and the SEM image of its backside in the center after

PEC etching at various KOH concentrations. For comparison, the etch rate of Sample A at the each concentration under similar illumination and bias conditions are plotted in the Figure 4.15 (d). It is seen that by reducing molarity of KOH from 0.1 M to 0.01 M, the etch rate is reduced from 0.5 $\mu m/min$ to 0.2 $\mu m/min$, but the backside looks smoother (Figure 4.15), in both samples pyramids were formed on the backside. However, with further reduction of concentration, the etch rate became too slow and less than 1 μm was etched after 1 hour.

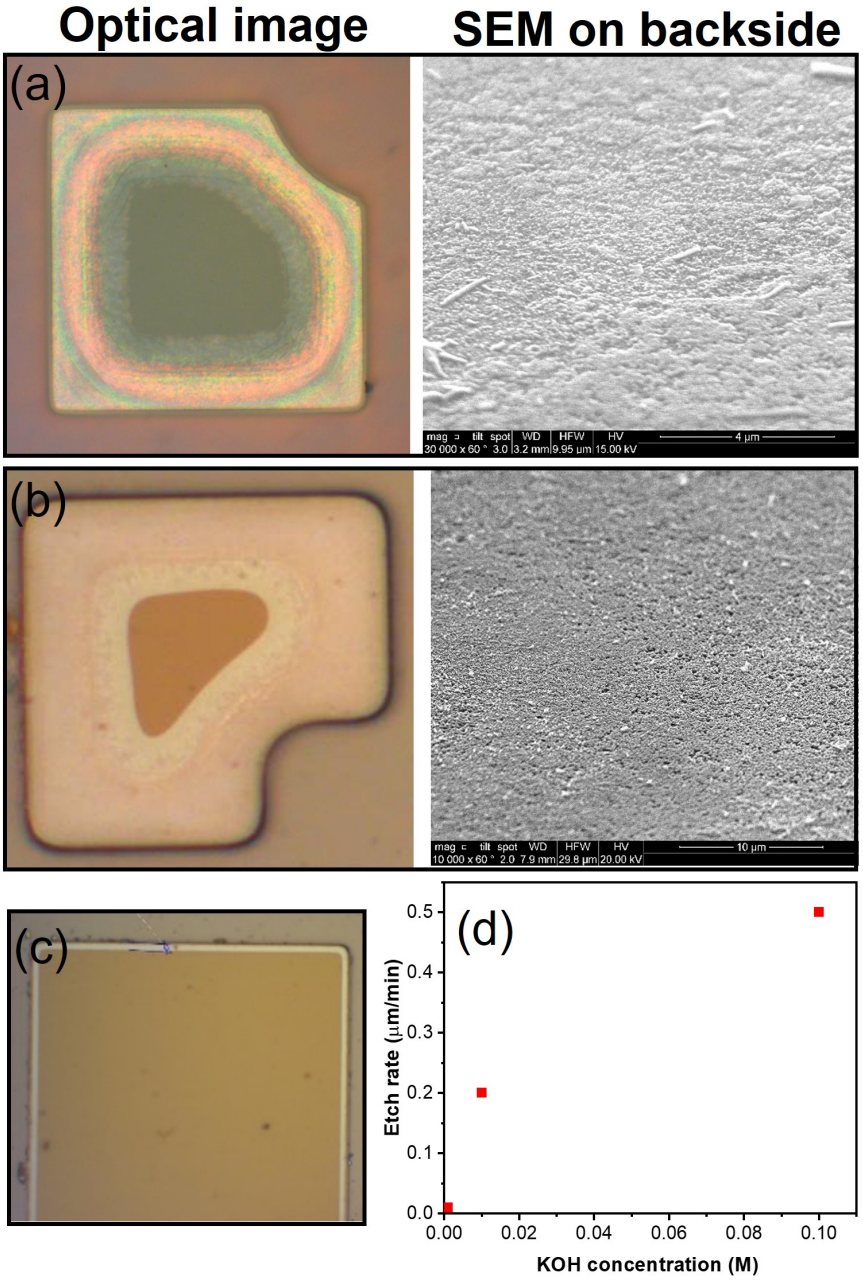

FIGURE 4.15: The optical (top-view) image of sample A with size of 50×50 μm^2 during PEC etching and the corresponding SEM image of its backside in the center after fully undercutting in (a) 0.1 M KOH (b) 0.01 MKOH (c) 0.001 M KOH and (d) shows the etch rate of sample A versus the molarity of KOH.

Then to compare the different electrolytes on etch rate and etched surface morphology, KOH and HNO_3 were employed using samples with Structure A while keeping the other conditions identical. The results above are also consistent with reports from Youtsey et al. that lower KOH concentrations result in smooth surfaces [205]. Therefore, a concentration of 0.01 M was used for both KOH and HNO_3 in this study.

As seen in Figure 4.16 (a), using KOH resulted in the formation of pyramid-like surface which is related to the exposure and etching of N-face GaN. This phenomenon was also observed in PEC etching with structure B as shown in SEM cross-sectional images in Figure 4.14. However, it was not observed when etching with HNO_3 as shown in Figure 4.16 (b). Note that KOH can chemically etch N-face GaN in addition to the photo-assisted etching. The acidic electrolyte does not chemically etch the material leading to different morphologies in an acid and a base solution. Figure 4.16 (c,d), show that RMS roughness of etched surface over an area of 5 $\times 5\mu m^2$ was reduced from 7 nm with KOH to 5.3 nm with HNO_3, revealing that using an acidic electrolyte can result in smoother surface. This result is confirmed by measuring a large number of devices. SEM images in Figure 4.16 (d), shows small particles on the etched surface after etching by HNO_3. As a results of our initial tests using other acid solutions, such as H_2SO_4 and HCl, we also observed these particles in the PEC etching procedure. Based on literature and our energy dispersive X-ray analysis, suggests that these particles might be gallium which could be formed during PEC etching process.

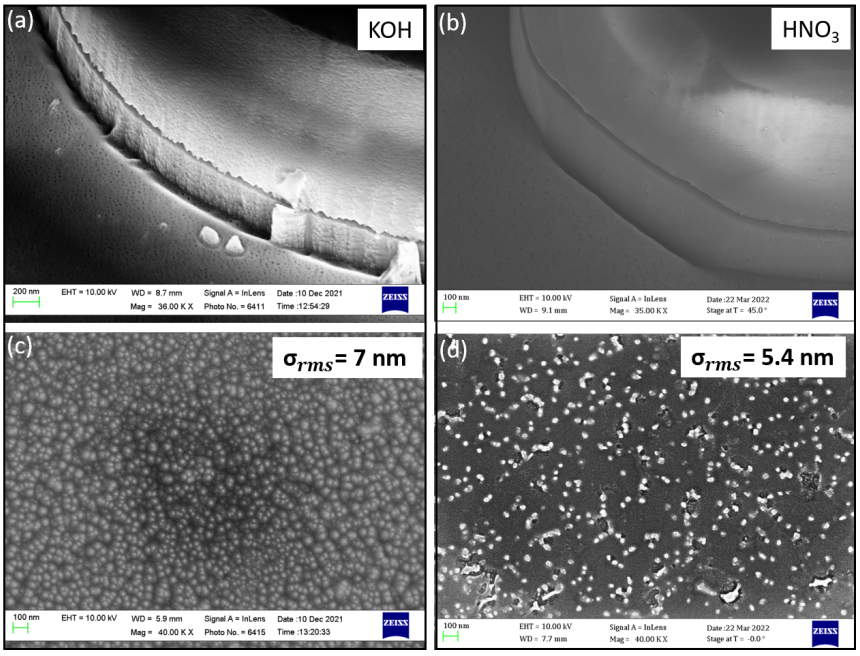

FIGURE 4.16: SEM images of mesa sidewall after PEC-etching sample A in (a) KOH and (b) HNO_3. (c-d) The center of the backside of released devices after etching.

To further reduce RMS roughness, a post treatment can be beneficial to remove Ga oxides. The solubility of those oxides varies between acidic or basic solutions depending on whether they dissolve to form a soluble complex [206]. Although KOH or TMAH is reported for post treatment to remove the residuals [207], these solutions could result in a rough surface due to the chemical etch of N-face GaN. Here, HCl (60 °C) for 15 minutes was used to dissolve these residuals, followed by dipping into acetone for 20 minutes to remove induced $GaCl_3$ particles. As seen in Figure 4.17 (b) the particles were sufficiently removed with the measured roughness reduced to 4.4 nm over an area of $5\mu m \times 5\mu m$ after post treatment.

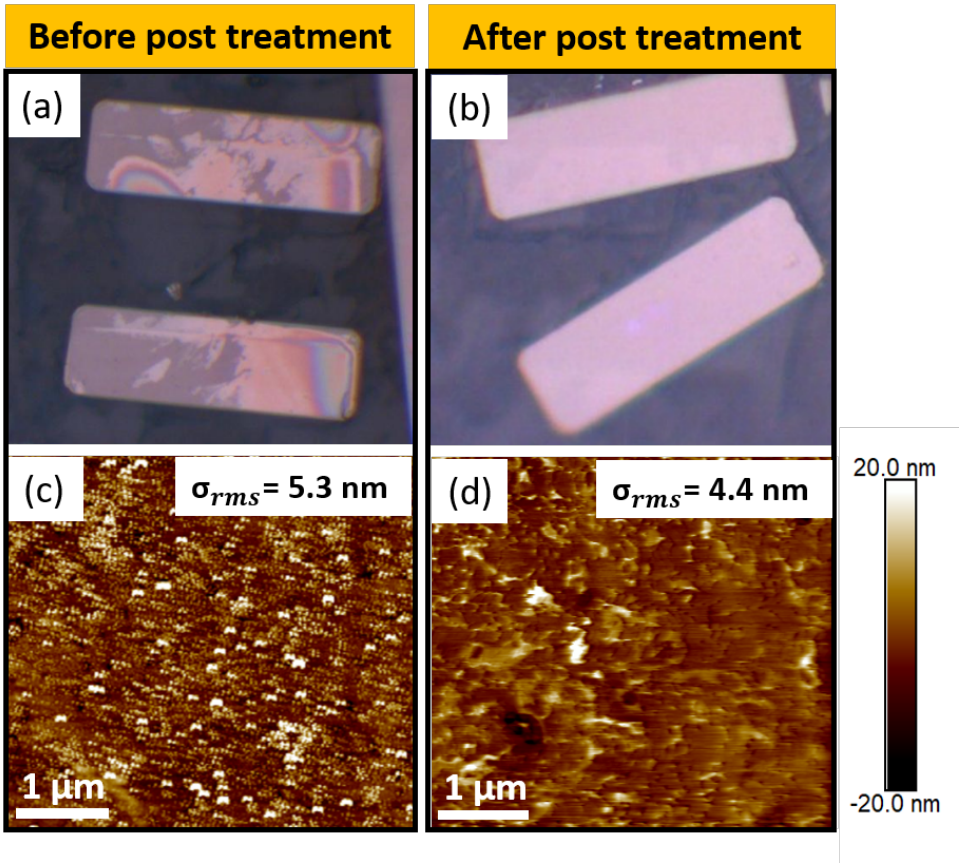

FIGURE 4.17: Optical images of the backside of released devices with size of 20 $\mu m \times$ 100 μm after PEC etching using HNO_3 (a) before post treatment (b) after post treatment and (c-d) their corresponding AFM scan of the center over $5 \times 5\mu m^2$.

4.3.7 Comparing conventional sacrificial layer with Sample B

It has been shown that HNO_3 as an electrolyte produces a smoother morphology for conventional sacrificial layers, so Sample A with conventional sacrificial layers was compared with Sample B with AlInN (7.5nm)/InGaN (2nm) in this condition, and PEC etching was carried

out under identical conditions, using 0.01 M HNO_3 and a bias of 2 volts and illumination power of 105 mW/cm^2 at 405 nm.

As depicted in Figure 4.18 (a), the photocurrent initially decreases exponentially and then declines slowly towards a steady value due to the complete undercut of films in the focused region. Since a large area of the sample was dipped in the solution, the non-zero current here is attributed to the photo-generated carriers by the scattered light outside of the focused region. It has been found that the etch rate for Sample B was about three times higher than that in Sample A, which was also reflected by the photocurrent level during etching as well as the total etching time. Note that photocurrent is proportional to the reaction rate at semiconductor/electrolyte interface, according to Faraday's law of electrolytes.

The fully undercut devices were picked up by PDMS and the backside morphology was examined by AFM, as shown in Figure 4.18 (b). The surface of Sample A after PEC etching exhibits a high density of islands, with the RMS roughness of 5.3 nm over an area of 5 $\mu m\times$ 5 μm, whereas Sample B exhibits terrace-like morphology, with RMS roughness of 2.5 nm over a similar area. Taking into account that the as-grown surface exhibits a roughness of 1.9 nm over an area of 5 $\mu m \times$ 5 μm, the etched surface from Sample B is quite smooth. This is due to the high density of polarization charges in combination with the photo-induced holes facilitates the etch rate, improve the uniformity of the etching, leading to a smoother released surface.

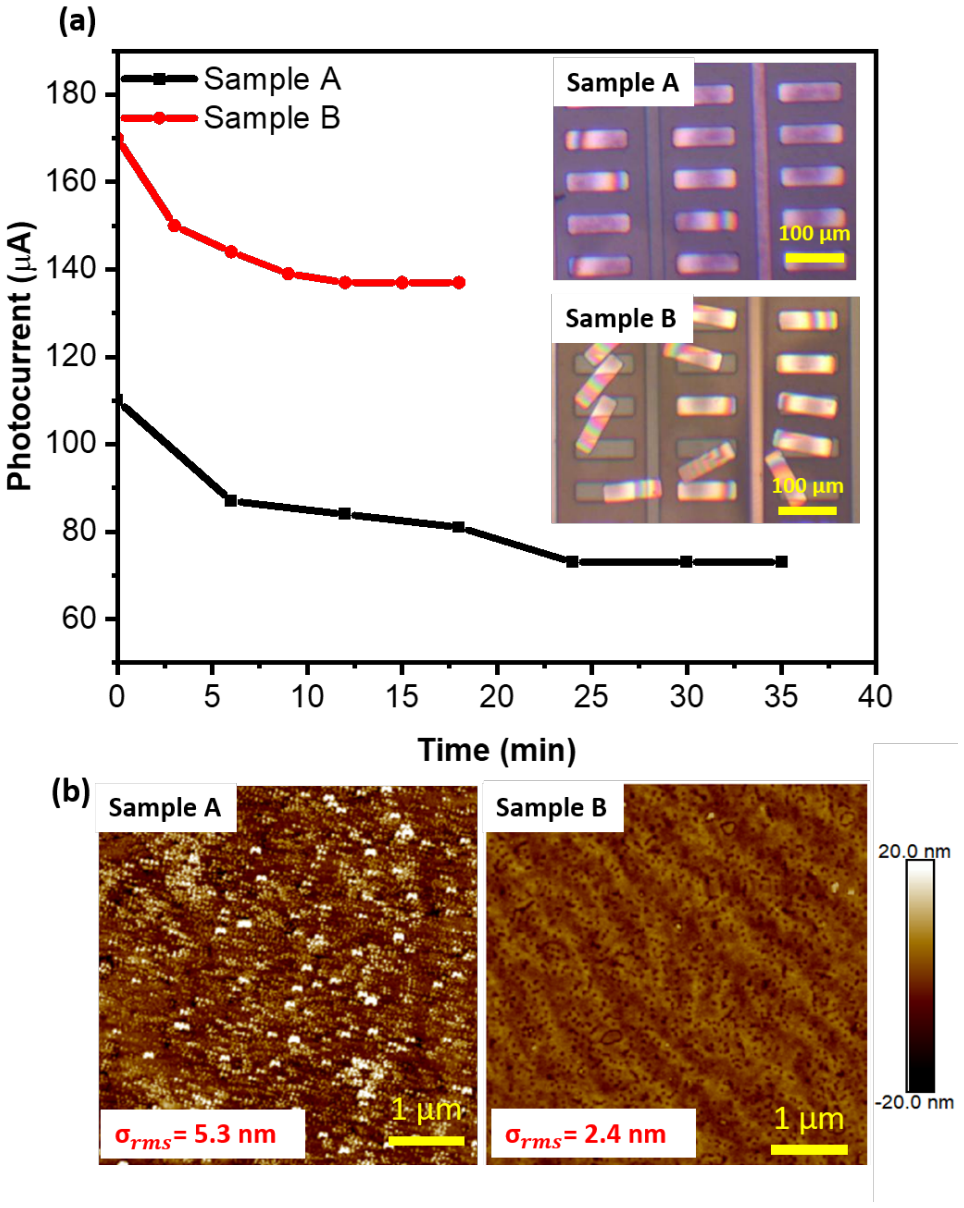

FIGURE 4.18: (a) Photocurrent vs time for sample A (without -AlInN) and sample B (with 7.5-nm-thick AlInN) with size of 20 $\mu m \times$ 100 μm. The inset shows optical images of the two samples after 20 min PEC-etching in HNO3. (b) AFM images of the center of their backside surfaces.

4.4 Conclusion

In summary, a sacrificial stack with InGaN/AlInN/GaN configuration is introduced for enhanced hole carrier confinement at the InGaN/AlInN interface for the PEC etching process. Simulations and C-V measurements indicate the presence of a high density 2DHG at the interface of InGaN/AlInN due to the strong polarization difference. The effect of thickness of barrier (AlInN) was investigated and it has been shown that increasing the thickness of the barrier results in the enhancement of holes. However, further investigation is required to optimize the thickness of quantum wells (InGaN). Simulating the hole concentration as a function of the thickness of InGaN for a fixed barrier thickness (7.5 nm AlInN) was conducted in the same manner as described in Section 4.3.2. The peak of hole concentration increases by increasing the thickness of InGaN, and when the thickness is thicker than 6 nm, the peak hole concentration will be saturating (see Figure 4.19). Thus, it is worth investigating experimentally the effect of thickness of InGaN between 4 to 6 nm in the future. This can result in a higher hole concentration while simultaneously being within the range of critical thickness in order to avoid relaxation issues.

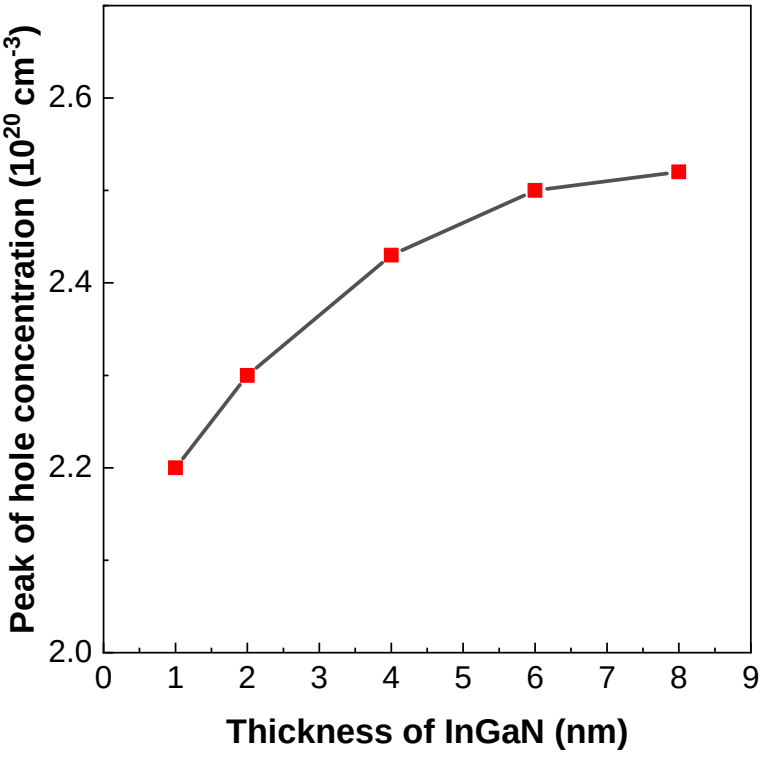

FIGURE 4.19: The dependence of the peak of hole concentration on the thickness of InGaN for a fixed thickness of AlInN (7.5 nm).

PEC etching experiments with varying AlInN thickness reveal that a 7.5-nm AlInN layer provides the most favorable balance between etch rate and surface morphology. Thicker AlInN layers result in a poorer surface morphology, despite a faster etch rate.

We found samples with (InGaN/AlInN) sacrificial layer exhibit almost three times higher lateral etch rate and much smoother RMS roughness on the etched surface when compared to the conventional InGaN/GaN release layers. Our study on the type of electrolyte showed that using HNO_3 electrolyte results in smoother surfaces because it prevents the formation of pyramid-like surfaces on the N-face GaN layer when compared to conventional electrolyte KOH. A post treatment in HCl can be used to remove the residual oxides after PEC etching, to further reduce the roughness. Additionally, the optimum structure with AlInN has been used to remove the LED structure from a growth substrate (for example, Sapphire), which is described in Appendix A.3.

Not only the (InGaN/AlInN) structure can be used as a sacrificial layer to lift-off GaN devices on sapphire or GaN substrate but also the dopant-free 2DHG at InGaN/AlInN interface could be potential platform for p-channel GaN electronic devices.

Chapter 5

Conclusion and future work

5.1 Results overview

The integration and combination of high performance electrical and optical devices with miniature structures is in demand for a wide range of applications, from displays to communication systems. Therefore, this study explores the use of μTP technology to integrate and improve the performance of GaN-based μLEDs with miniature structures on various substrates. The goal was to address not only performance-related issues, but also the challenges of releasing the devices from the original substrate and improving the printing process.

As GaN based LEDs grown on Si have been widely utilized within these applications due to their scalability, low manufacturing cost, and compatibility with existing Si (standard IC) manufacturing lines, we focused in Chapters 2 and 3 of this thesis on the development and transfer printing of GaN LEDs on Si. In order to develop and fabricate μLEDs suitable for transfer printing, a wide range of experimental techniques were employed in a cleanroom laboratory. μLEDs arrays were fabricated using a combination of wet and dry methods centered around four main steps: photolithography, patterning, exposure and development. The transfer printing requires suspending μLEDs, which was accomplished by wet chemical etching using TMAH to selectively remove Si. Undercutting requires that the device be anchored to the substrate in order to prevent collapse. A preliminary attempt to design an anchor and a tether with GaN (epitaxial structure) revealed that some practical issues can occur during the process. First, anchors can be partially etched during the undercut, so the device cannot be placed in solution for a prolonged period of time to allow roughening. In addition, thick material is difficult to

break during transfer printing.Therefore, to resolve this problem, we introduced the original method and demonstrated that using SiN_x as a tether eases printing, while using it as an anchor allows it to survive for a long period of time during the undercut process.

LEDs bowing due to strain was another issue associated with printing that had to be addressed. To manage the intrinsic stress in GaN on Si, we proposed a stress compensation approach utilizing SiN_x layers based on COMSOL thermal stress simulation. Our simulation results indicate that larger devices are subject to more deformation. It has also been demonstrated that engineering and controlling the stress of SiN_x as a compensation layer affects the net deformation of the device. In other words, for a device with size of 110×110 μm^2 , 1 μm of SiN_x layer applied with neutral stress and 200 MPa tensile stress results in 1.4 μm of upward deformation at the edge of the released coupon, whereas the same thickness of SiN_x with 200 MPa compressive stress results in 0.5 μm upward deformation. This deformation can be reduced further through precise control of the stress of the SiN_x layer. The stress of deposited SiN_x by PECVD was controlled experimentally based on the simulation results. It is shown that device with neutral stress in the deposited SiN_x suffers from net tensile stress and deforms upwards, which is in good agreement with simulation data. While incorporating compressively stressed SiN_x layers results in flat devices after releasing.

The steps needed to tackle the low light extraction of $\mu LEDs$ were introduced. The performance of fabricated LEDs was enhanced by utilizing a variety of techniques. In order to increase the possibility of light rays escaping, and to prevent internal reflection, the backside of the μLEDs was roughened using hot TMAH. Then, roughened devices printed onto a Ag reflective substrate. A roughening technique combined with an Ag reflector results in an increased light output by a factor of 4.2 when compared to μLEDs before undercut. In order to enhance the collected optical power by redirecting emission in the forward direction, the released LEDs were printed into fabricated silver-coated reflecting trenches with different depths that were formed in silicon. It worth noting that printing into 3D structures is a distinguishing feature of transfer printing technology, and it is the first time it has been accomplished. It has been shown that the light output collected for the μLED in trenches of 10 μm depth is over seven times greater than for the μLED on the initial Si substrate. Furthermore, it has been demonstrated that the formation of polymeric lenses on top of devices inside trenches can increase the collected light output by 1.1 times when compared to devices without lenses. Overall, using the trench together with the lens enhanced the collected light output power by factor of nine

in comparison to the LEDs on the original substrate. Additionally, the electrical and optical performance of devices was discussed, as well as their potential for application in VLC.

Chapter 3 focused on releasing GaN devices on GaN or Sapphire using PEC etching. Thus, the introductory of the mechanism of photo-electrochemical etching, importance of a thick sacrificial layer for transfer printing and confining 2DHG at the interface of stack GaN layers due to the polarization was provided. A novel sacrificial stack with a configuration of InGaN/AlInN/GaN is presented to be suitable for transfer printing. The structure is implemented in a relatively thick sacrificial superlattice structure for PEC etching. The bandgap diagram simulation and C-V measurements were performed to compare these structure with conventional InGaN/GaN sacrificial layer. It is shown that 2DHG concentration can enhance by implanting AlInN as a barrier at interface of InGaN/AlInN due to inbuilt polarization. A GaN layer has been successfully lifted-off using PEC etching with InGaN/AlInN/GaN sacrificial layers. A study was carried out to investigate the effect of AlInN thickness on lateral etch rate in PEC etching. Increasing the thickness of AlInN from 0 nm to 30 nm led to an increase in etch rate from 0.5 μm to 2.5 μm. However, slightly better results regarding homogeneity of undercut and smoothness of released surface were obtained with AlInN layer thickness of 7.5 nm. The possible reason for that is generally a smoother surface during the sacrificial stack growth process, as it gets rougher during AlInN growth. The PEC etching results of an InGaN/AlInN/GaN sacrificial layer and conventional InGaN/GaN sacrificial layer revealed that, not only is the etch rate for the InGaN/AlInN/GaN sacrificial layer three times greater, but the RMS roughness of the etched surface is also smoother than when using InGaN/GaN. In addition, it was found that the use of HNO_3 instead of KOH was beneficial to prevent the formation of pyramid-like surfaces on the n-face GaN.

5.2 Future work

It is outlined in each chapter what is necessary to improve the design and performance of GaN devices in the future study. From an application point of view, future work involving the transfer printing of LEDs and other devices onto new substrates, the innovative capabilities that micro-transfer printing technology offers for the integration of different devices should be exploited.

The integration of several colors of μLEDs on a single chip is highly desirable for a number of applications, such as displays, VLC, and so on. Micro-transfer printing is a technique that can accomplish this. Transfer printing of green μLEDs has been demonstrated in a similar manner to that of blue μLEDs, however better quality materials and further optimization of light output power are only required to make these devices suitable for a variety of applications. The transfer printed green and blue μLEDs inside of trench is shown in Figure 5.1.

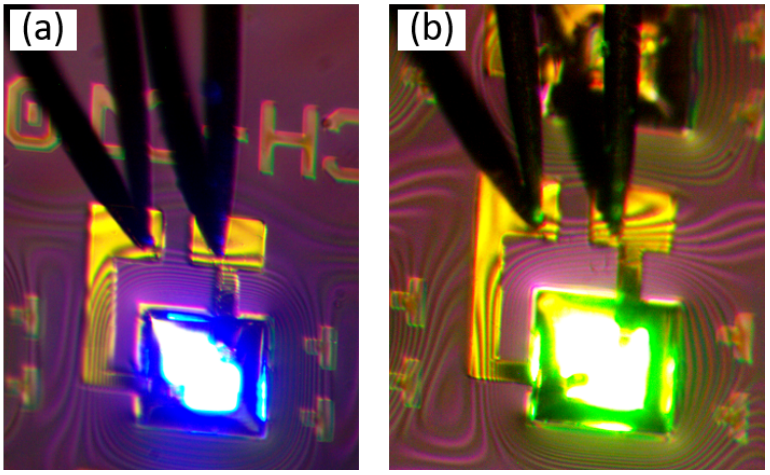

FIGURE 5.1: Optical images of lit-up printed μLEDs with size of 110 $\mu m\times$ 110 mum into trench a) Blue LED at 2 mA b) Green LED at 5 mA.

Integrating the blue and green LED in a single platform can act as dual-color transceiver in VLC. Additionally, the size of μLEDs can be further reduced. This is because the smaller LEDs are able to be modulated at higher speeds, making them ideal for applications related to VLC.

Additionally, the optimized sacrificial layer (InGaN/AlInN/GaN) can be used to release the high quality GaN devices on GaN substrates by using PEC etching, such as LEDs or lasers. It is possible, for instance, to integrate the released laser into a photonic integrated circuit using micro-transfer printing in order to achieve a miniature and compact device for high-speed communication. Other possibilities include transferring the released high-power μLEDs into flexible substrates that can be implanted with miniaturized optoelectronic systems for wireless optogenetics.

Appendix A

Appendix

A.1 Sample structures

In the following Figures, schematic representations of the sample structures that are used in this study are provided.

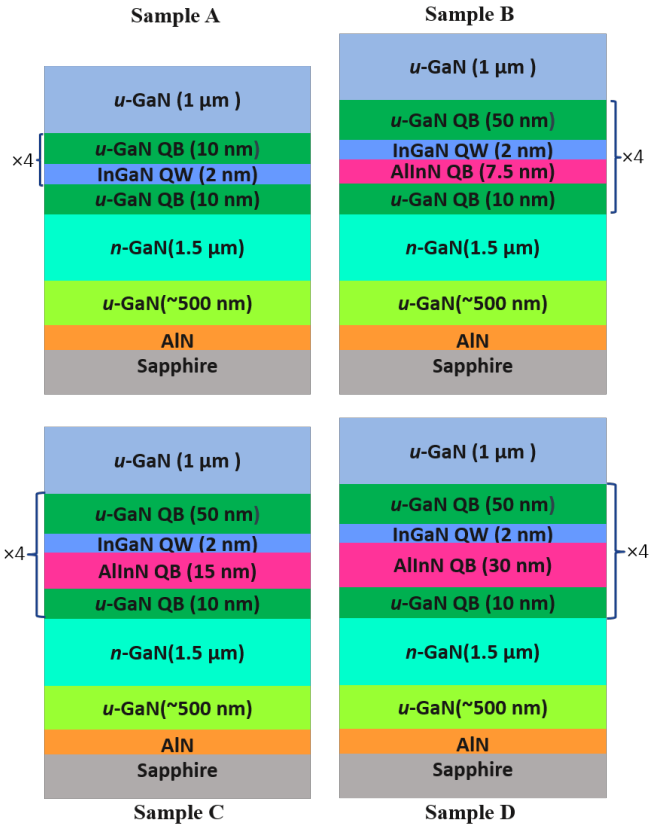

FIGURE A.1: Schematic of four types of structures used in PEC etching experiments

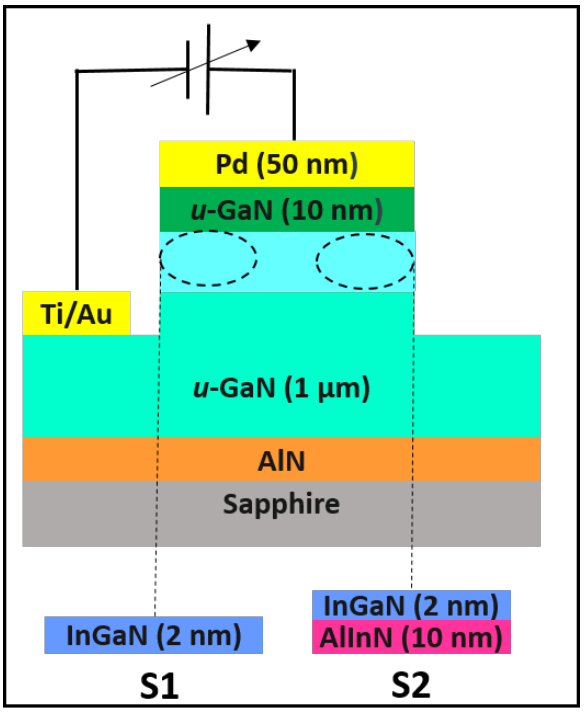

FIGURE A.2: Schematic of the C-V measurement structures.

A.2 Analyses of the C-V measurement

A.2.1 Size dependency of capacitance

To examine the size dependence of capacitance, the capacitance of Sample 2 was measured for two different sizes with diameters of 150 and 100 μm. In Figure A.3, capacitance is shown as a function of voltage for two different sizes.

Based on the Equation A.1, the ratio between two capacitance equals the ($\frac{C_2}{C_1} = \frac{A_2}{A_1}$). In this case, the capacitance of a circle with a diameter of 150 μm is 2.2 times greater than that of a circle with a diameter of 100 μm.

$$C = \frac{\epsilon_0 \epsilon_s A}{d} \tag{A.1}$$

As shown in Figure A.3, the capacitance of a device with a diameter of 150 μm is 2 times higher than that of a device with a diameter of 100 μm, which is almost in accordance with the expected result.

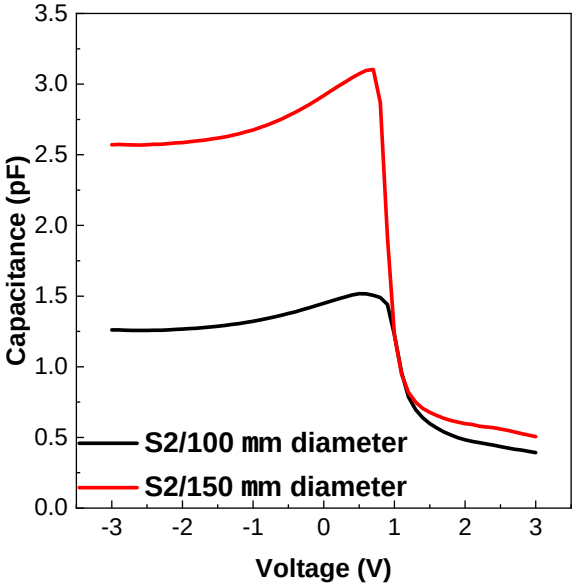

FIGURE A.3: C-V characteristics of the sample (S2) as a function of bias for various sizes.

A.2.2 Effect of frequency on capacitance

Figure A.4 shows the C-V characteristics of Samples 1 and 2 with Schottky contacts of 150 μm diameter, measured at various frequencies. As indicated in Figure A.4 (a), at the low frequency range less than 100 kHz, capacitance is seen to have a peak that is seen to decrease dramatically as frequency is increased. The presence of a peak in the C-V measurement is due to the deep traps [208]. At greater than 400 kHz, the peak of capacitance disappears. This means that the AC response of the interface traps decreases with increasing frequency. Contrary to Sample 1, the capacitance of Sample 2 shows no peak at low frequency, which may indicate that there may be fewer traps (dislocations) in Sample 2 compared to Sample 1. Both samples exhibit a slight reduction in capacitance when the frequency is increased. This is due to the carriers not being able to return fast enough to follow the signal at high frequencies. This is related to the impedance. The relationship between the capacitance and the impedance of a capacitor (ZC) is $C = \frac{1}{j\omega Z_c}$ where ω is the angular frequency equal to $2\pi f$ with f being the frequency. Therefore, it is evident that when frequency is decreased, capacitance measurements are affected. For this reason, C-V measurement outlined in Chapter 4, was conducted at 1 MHz to ensure that all interface states were unable to respond to AC signals.

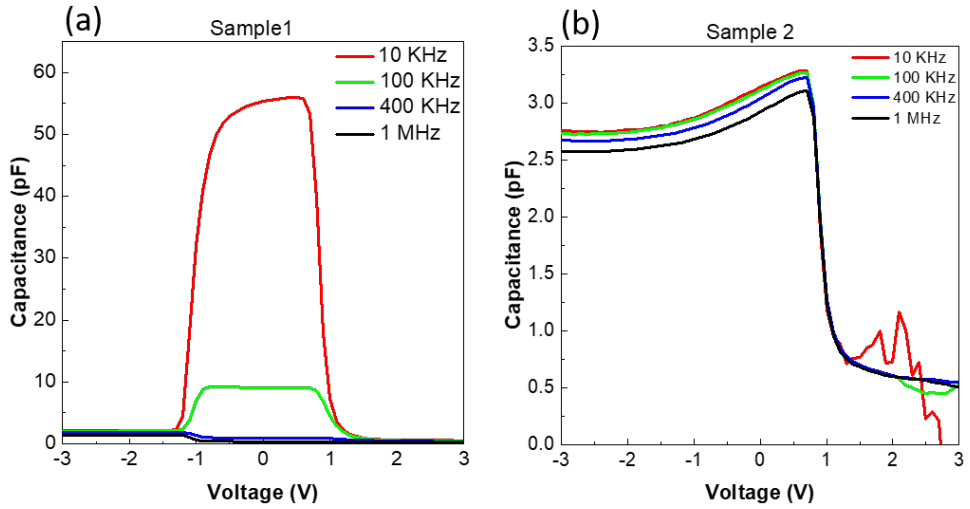

FIGURE A.4: C-V curves of (a) Sample 1 and (b) Sample 2 with Schottky contacts of 150 μm diameter measured at various frequencies from 10 kHz to 1 MHz.

C-V measurements at low frequency indicated that Sample 1 appeared to have a higher trap density than Sample 2, so the leakage current was measured at reverse bias for both samples. A positive supply was connected to the Pd while a negative supply was connected to the Ti/Au on n-GaN. As shown in Figure A.5 Sample 1, exhibits greater leakage than Sample 2, which is consistent with low frequency C-V results.

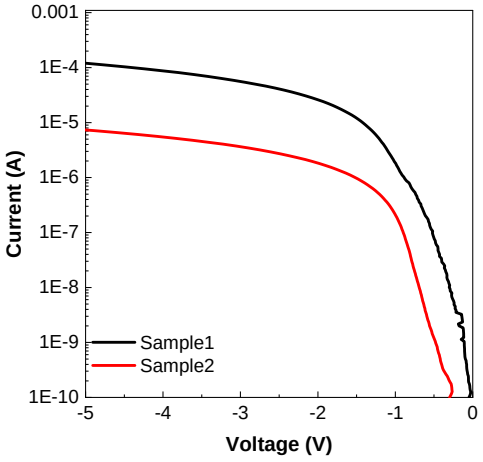

FIGURE A.5: I-V curves under reverse bias for contact of 150 μm in diameter.

A.2.3 C-V results validity and carrier concentration

To ensure the C-V measurement is valid, the normalized conductance and impedance was measured. The conductance data can serve as an indication of possible measurement problems. It is typical for the conductance to be very low. This indicates that there is very little current

leaking across the capacitor and that most of the current is displacement current. If the conductance (G) is on the same order as the reactance (ω C), there might be a problem with the capacitor. A reverse-biased diode may be going into breakdown or there may be a shunt path across a capacitor. The normalized conductance vs voltage or impedance phase vs voltage can provide this information. The impedance can be calculated as below.

$$Z = \frac{1}{G + 2\pi f C j} \tag{A.2}$$

where G represents the conductance, f represents the frequency, and C represents the capacitance. A phase of impedance can be calculated by Arctan (2πfC/G). Normalized conductance is obtained by normalizing the (G/2πfC).

Figure A.6 shows the impedance phase and conductance as a function of voltage for Sample 1 and Sample 2. From the Figures A.6 (a) and A.6 (b), it can be seen that the phase of the impedance for Sample 1 changes from -7 degrees to -57 degrees as the bias voltage is swept, and for Sample 2, it changes from -2 degrees to -80 degrees. The zero degree indicates that the impedance has no capacitance. The impedance is purely capacitance when it is 90 degrees. As the normalized conductance is not too high, the capacitance can be measured accurately. Thus, the measurement is reliable.

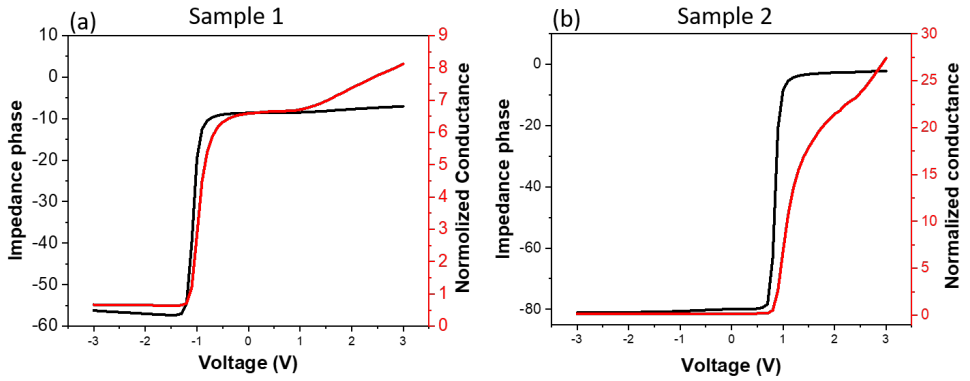

FIGURE A.6: Impedance and normalized conductance as a function of voltage (a) Sample 1 and (b) Sample 2.

The carrier concentration in C-V measurement can be extracted from the linear part of the reverse-bias $1/C^2 - V$ plot. It is clear from Figure A.7 that $1/C^2$-V does not exhibit the straight line, so the charge concentration does not remain constant. The carrier concentration of the linear part of $1/C^2$-V of Sample 2 in reverse bias is calculated according to the Equation A.3

$$N_D = \frac{2}{q\epsilon_0\epsilon_s A^2 \frac{d}{dV}\left(\frac{1}{C^2}\right)} \tag{A.3}$$

where q is the elementary charge, A is the area of the contact and ϵ_0 is the permittivity of free space and ϵ_s is the dielectric-constant of material. The calculated hole concentration (N_D) for sample 2 is around $2.3 \times 10^{16}\ cm^{-3}$.

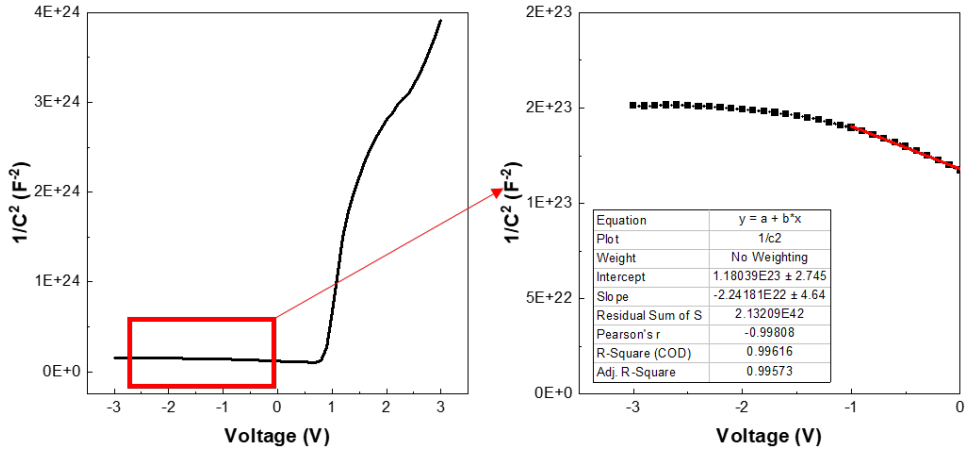

FIGURE A.7: $1/C^2$ as a function of voltage for sample 2.

A.3 Lift-off of LEDs using PEC etching

In order to demonstrate the capability of optimized sacrificial layer (InGaN/AlInN), a structure as shown in Figure A.8 was developed by the MOCVD group at Tyndall National Institute, in order to lift-off the full LEDs on top of it by PEC etching.

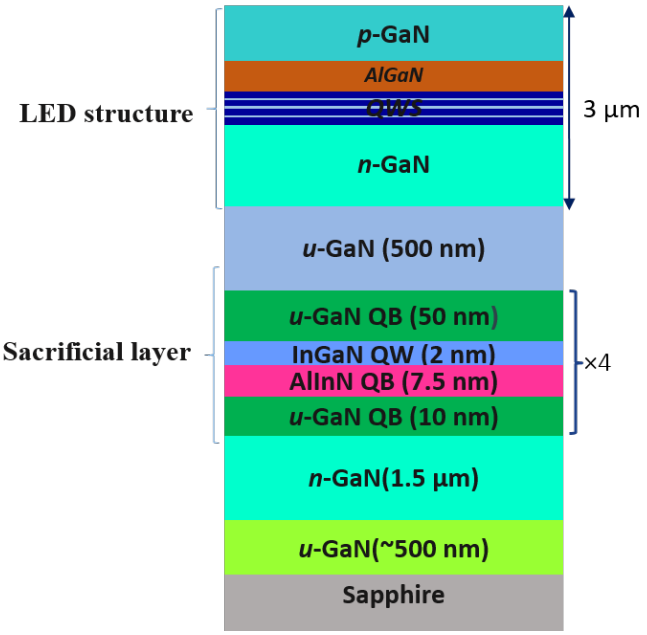

FIGURE A.8: Cross-sectional schematic of LED structure on sacrificial layer.

In order to prepare the sample for PEC etching, a coupon with size of 100 $\mu m \times 100 \mu m$ was etched according to the same procedure as described in Section 4.3.4. PEC etching was performed under identical conditions, namely with 0.1 M KOH, 2 V bias, and 105 mW/cm^2 for approximately 60 minutes. Figure A.9 illustrates an optical image of the LED and SEM image of it after being undercut completely with PEC etching.

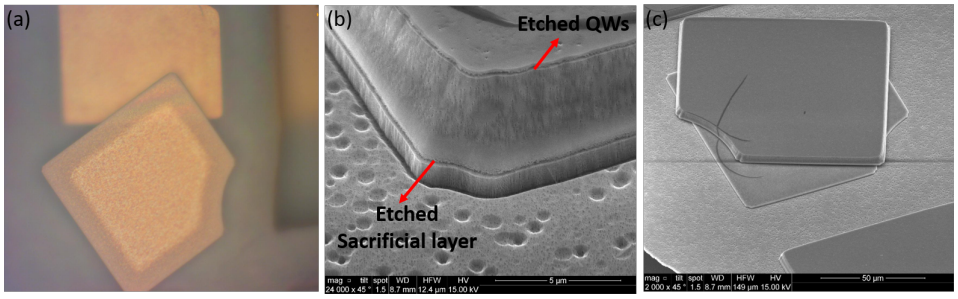

FIGURE A.9: (a) Optical image of released LED after being fully undercut (b) SEM cross section and (c) SEM (top-view) of released LED.

The SEM image confirms that LEDs can be fully undercut using this sacrificial layer. Additionally, from Figure A.9 (b), it can be seen that QWs were attacked by the chemical solution.

Therefore, a passivation layer is required to protect the sidewall of the device during undercutting.

Despite the fact that we were able to release LEDs with the designed sacrificial layer by PEC etching, there was one issue with this growth structure. It is found that part of wafer fully peeled off during the undercut (see Figure (a)). As it can be seen from Figure A.10 (b) the n-GaN layer exhibits both V-pits and high density of porous structures, which are small holes or voids in the material. It is reported that doped GaN layers which is exposed to electrolyte can be electrochemically or PEC etched and made porous. These porous initiate at the surface and grow vertically into structure [209]. These dislocations allow the electrolyte to penetrate to the GaN/Sapphire interface, where etching and peeling off occur. The peel off issue is not observed for samples that are grown on sapphire with a thin layer of AlN inserted between the sapphire and GaN, so to avoid this issue, the structure should be grown on sapphire with thin layer of AlN.

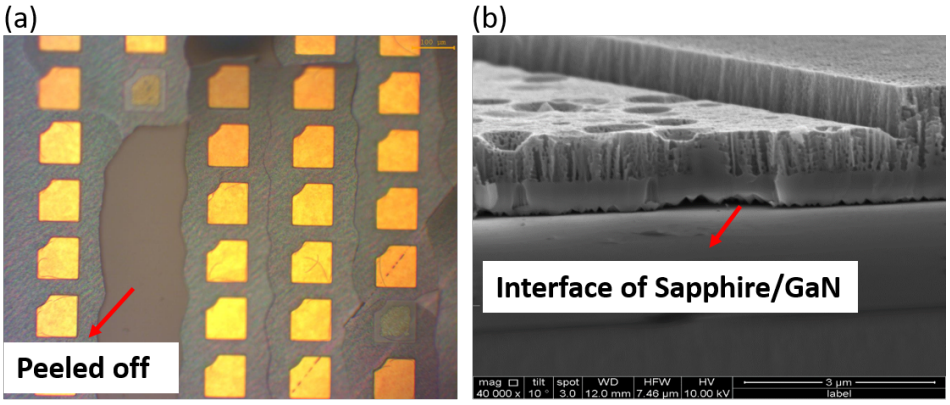

FIGURE A.10: (a) Optical image of LED during the PEC etching when part of device peeled off(b) SEM cross section of interface of sapphire/GaN.

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