Development of InAlN HEMTs for space application

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Declaration

I hereby state that all of the work undertaken in this thesis is original in content and was carried out by the author. Work carried out by others has been duly acknowledged in the thesis. The work presented has not been accepted in any previous application for a degree.

Signed: ……..

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Abstract

This thesis investigates the emerging InAlN high electron mobility transistor (HEMT) technology with respect to its application in the space industry. The manufacturing processes and device performance of InAlN HEMTs were compared to AlGaN HEMTs, also produced as part of this work. RF gain up to 4 GHz was demonstrated in both InAlN and AlGaN HEMTs with gate lengths of 1 μm, with InAlN HEMTs generally showing higher channel currents (~150 c.f. 60 mA/mm) but also degraded leakage properties (~ 1×10^{-4} c.f. < 1×10^{-8} A/mm) with respect to AlGaN. An analysis of device reliability was undertaken using thermal stability, radiation hardness and off-state breakdown measurements. Both InAlN and AlGaN HEMTs showed excellent stability under space-like conditions, with electrical operation maintained after exposure to 9.2 Mrad of gamma radiation at a dose rate of 6.6 krad/hour over two months and after storage at 250°C for four weeks. Furthermore a link was established between the optimisation of device performance (RF gain, power handling capabilities and leakage properties) and reliability (radiation hardness, thermal stability and breakdown properties), particularly with respect to surface passivation. Following analysis of performance and reliability data, the InAlN HEMT device fabrication process was optimised by adjusting the metal Ohmic contact formation process (specifically metal stack thicknesses and anneal conditions) and surface passivation techniques (plasma power during dielectric layer deposition), based on an existing AlGaN HEMT process. This resulted in both a reduction of the contact resistivity to around 1×10^{-4} $\Omega.cm^2$ and the suppression of degrading trap-related effects, bringing the measured gate-lag close to zero. These discoveries fostered a greater understanding of the physical mechanisms involved in device operation and manufacture, which is elaborated upon in the final chapter.

Acknowledgements

I would like to express my gratitude to my two academic supervisors, Prof. Peter Parbrook at the Tyndall National Institute and Dr. Andrew Barnes at the European Space Agency. Peter has mentored me throughout my time as his student in addition to providing direction for the majority of the project, for which I am very grateful. His expert knowledge on materials science, crystal growth and device physics have been invaluable, and I owe much of what I have learnt in the last few years to his patient and thoughtful communication. Andrew introduced me to the European Space Agency (ESA) and supported me during my time spent there in 2013-2014, fulfilling a major personal career goal. With his support and that of Dr. Fabio Vitobello I was welcomed into the Materials and Components Division and able to make use of the world-class test facilities at the European Space Research and Technology Centre (ESTEC), as well as gaining first-hand experience of the European space industry which I know will continue to be valuable throughout my career.

The majority of my research was undertaken at the Tyndall National Institute, part of the University College Cork, Ireland. The people in Cork are some of the most welcoming I have ever encountered. The city feels like a second home and reminds me a lot of my native Yorkshire with its beautiful countryside, rich traditions and the glowing sense of a proud community. The staff and students at the Tyndall National Institute are no exception, and I feel grateful to have worked with so many professional and helpful researchers from Cork and all over the world. My knowledge of and hunger for a career in science and technology have been enriched by interacting with a range of disciplines at Tyndall, made possible by a friendly atmosphere that encourages the incubation of novel ideas.

Dr. Donagh O'Mahony worked on the project for the first three years, developing the fabrication process, designing devices and being in constant communication with our project partners at ESA. I thank Donagh for always being approachable and his professionalism and patience when teaching me the majority of technical skills I have developed throughout this project. III-nitride HEMTs had never been produced at Tyndall as of September 2011, and using the process Donagh developed we were able to produce radiation-hard and thermally stable devices capable of RF gain and with high breakdown voltages – something I am very proud of. The rest of Brian Corbett's III-V Materials and Devices Group provided useful input also through the weekly meetings arranged by Pleun Maaskant, who deserves to be thanked more often for his tireless efforts in promoting useful discussion.

I was based in Peter's Nitride Materials Group where I was quickly and forcefully taken under the wing of Dr. Tom Sadler. I was lucky to have Tom growing my epilayers for the first two years of the project, and his expansive and thorough knowledge of not only

nitride materials but also every other conceivable topic left me on the losing side of many arguments. He once declared over a pint of Blarney Blonde, “I might actually at one point have been the best grower of InAlN in the world”, - and by God I think he might’ve been right. Tom is now handling the financial affairs of the British state, ensuring there will still be a place worth going back to if I ever decide to return home. I like to think the solid friendship of Peter, Tom and Haoning Li and I cermented the foundations of the Nitride Materials Group and allowed it to develop into the thriving hub of world-class research it is today.

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Publications resulting from this thesis

A) Journal publications

1. M. D. Smith, T. C. Sadler, H. Li, V. Z. Zubialevich and P. J. Parbrook, "*The effect of a varied NH_3 flux on growth of AlN interlayers for InAlN/GaN heterostructures*", Appl. Phys. Lett. **103**, 081602 (2013); DOI: 10.1063/1.4818645
2. M. D. Smith, E. Taylor, T. C. Sadler, Vitaly Z. Zubialevich, K. Lorenz, H. N. Li, J. O'Connell, E. Alves, J. D. Holmes, R. W. Martin, P. J. Parbrook, "*Determination of Ga auto-incorporation in nominal InAlN epilayers grown by MOCVD*", J. Mater. Chem. C **2**, 5787-5792 (2014); DOI: 0.1039/C4TC00480A
3. M. D. Smith, D. J. O'Mahony, M. Conroy, M. Schmidt, P. J. Parbrook, "InAlN HEMT Ti/Al/Ni/Au Ohmic contact optimisation assisted by in-situ high temperature transmission electron microscopy" Appl. Phys. Lett. **107**, 113506 (2015); DOI: 10.1063/1.4930880
4. E. Taylor, M.D. Smith, T.C. Sadler, K. Lorenz, H.N. Li, E. Alves, P.J. Parbrook, R.W. Martin, "*Structural and optical properties of Ga auto-incorporated InAlN epilayers*", J. Cryst. Growth. **408**, 97-101 (2014); DOI: 10.1016/j.jcrysgro.2014.09.031
5. M. D. Smith, D. J. O'Mahony, F. Vitobello, M. Muschitiello, A. Costantino, A. R. Barnes and P. J. Parbrook, "*A comparison of the ^{60}Co gamma radiation hardness, breakdown characteristics and the effect of PECVD SiN_x capping on InAlN and AlGaN HEMTs for Space Applications*", Semiconductor Science and Technology **31,** 025008 (2015)

B) Conference publications (oral presentation)

1. M. D. Smith, T. C. Sadler, H. Li, V. Z. Zubialevich and P. J. Parbrook, "*Optimization of AlN interlayers for InAlN/GaN HEMTs grown by MOCVD*", UK Semiconductors annual summer conference, University of Sheffield, 2012
2. M. D. Smith, T. C. Sadler, and P. J. Parbrook, "*Improved carrier mobility in InAlN/AlN/GaN HEMT devices for space applications*", European Space Agency 6th Space Agency – MOD Round Table Workshop on Wide Band Semiconductors and Components, ESTEC, Noordwijk, October 2012
3. M. D. Smith, D. J. O'Mahony, F. Vitobello, A. R. Barnes and P. J. Parbrook "*Direct comparison of thermal stability, radiation hardness and breakdown characteristics of InAlN and AlGaN HEMTs, with and without SiN passivation*", UK Nitrides Consortium (UKNC) annual winter meeting, Nottingham, 2012

C) Conference publications (poster presentations)

1. M. D. Smith, T. C. Sadler, H. Li, D. J. O'Mahony and P. J. Parbrook "*Initial investigations into InAlN HEMT reliability and the effects of including an AlN interlayer*", UK Nitrides Consortium (UKNC) annual winter meeting, Cardiff, 2012
2. M. D. Smith, T. C. Sadler, H. Li, V. Z. Zubialevich and P. J. Parbrook, "*Optimization of AlN interlayers for InAlN/GaN HEMTs grown by MOCVD*", UK Semiconductors annual summer conference, University of Sheffield, July 2012
3. M. D. Smith, D. J. O'Mahony, L. Floyd and P. J. Parbrook, "*Theoretical comparative study of InAlN/GaN and AlGaN/GaN devices based on preliminary material data*" European Space Agency 6th Space Agency – MOD Round Table Workshop on Wide Band Semiconductors and Components, ESTEC, Noordwijk, October 2012
4. M. D. Smith and E. Burrows, "*High Efficiency RFID System to help Automate Recycling*" International Microwave Symposium 2013, Graduate Student Challenge, Seattle, 2013
5. M. D. Smith, D. J. O'Mahony and P. J. Parbrook, "*Developing Ohmic and Schottky contacts for GaN-based RF transistors*" UK Semiconductors annual summer conference, University of Sheffield, July 2012
6. D. O'Mahony, M. D. Smith, P. Maaskant, B. Corbett F. Vitobello, A. R. Barnes and P. J. Parbrook, "*Influence of Au thickness on the structural and electrical propertiesof Ti/Al/Ni/Au Ohmic contacts for InAlN/GaN HEMTs*" European Space Agency 7th Space Agency – MOD Round Table Workshop on Wide Band Semiconductors and Components, ESRIN, Frascati, October 2014

D) Journal publications pending review

1. M. D. Smith, D. Thompson, V. Z. Zubialevich, H. Li, C. Trager-Cowan and P. J. Parbrook, "*Nanoscale fissure formation in $Al_xGa_{1-x}N$/GaN heterostructures for HEMTs and their influence on Ohmic contact formation*", to be submitted to Journal of Physics D
2. M. D. Smith, D. J. O'Mahony, K. Cherkaoui, and P. J. Parbrook, "Optimisation of InAlN high electron mobility transistor SiN_x plasma-enhanced chemical vapour deposition conditions for effective surface passivation", to be submitted to Applied Physics Letters

1. Introduction and outline

Space exploration projects such as the upcoming European Space Agency (ESA) led Jupiter Icy Moon Explorer (JUICE) mission are essential to further humanity's understanding of our place in the universe. With the advent of the exoplanet era Jupiter is considered a gas giant archetype, the study of which could provide answers to the origins of planets and life in our solar system and beyond[1]. Spacecraft probing extra-terrestrial bodies are subject to extreme thermal, sonic and radiation conditions often periodically throughout a mission lifetime, and no direct maintenance may be performed. Electrical components used to record, process and transmit data must remain stable, ensured through accelerated life testing and system characterization under space-like conditions. Local shielding or advanced design of existing Si- or III/V-based technologies may be used, limited by the effect of increased complexity and weight on mission cost and feasibility.

Group III-nitride electronics are an attractive alternative due to the intrinsic robustness offered by the material system. The wurtzite crystal structure and high degree of bond ionicity of AlN, GaN, InN and the associated alloys results in an electronic direct band gap range from 0.7 to 6.2 eV. The high breakdown field and electron saturation velocity of III-nitride materials expand the limits of operation of RF power amplification devices in terms of power handling and frequency response, improving the bandwidth and simplicity of circuits compared to Si and III-V technologies. The wider band gaps typically used relative to Si (1.1 eV) and III-Vs (< 2.5 eV) enables a higher power per unit size, increasing the system compactness. The band gap is direct, allowing the system to be used in optoelectronics applications. Furthermore the wide band gap and high thermal conductivity allow for operation under adverse ambient conditions such as high temperature or radiation environments[2].

III-nitride light-emitting devices have established GaN-based technologies as a rapidly emerging industry covering a broad range of applications. GaN was used to create blue LEDs developed in the 1990s, which earned the inventors the Nobel Prize[3]. GaN laser diodes are widely used in optical disc data storage, with Blu-Ray disc sales reaching 350

million in 2010[4]. Currently the ambient lighting and display markets are limited to LEDs by manufacturing costs and the so-called 'green gap', i.e. a lack of efficient LEDs that emit green light. The efficiency of green InGaN LEDs has surged with the advent of semi- and non-polar III-nitrides[5]. The continued development and cost reduction of GaN based technologies will allow them to fulfil the potential justified by the accreditation of the 2014 Nobel Prize for Physics, and they are expected to dominate the multi-billion dollar[2] lighting and display markets in the years to come.

Commercially available AlGaN/GaN heterostructure field-effect transistors (HFETs) or high electron mobility transistors (HEMTs) display competitive power handling capabilities, fast switching speeds and long lifetimes, with advanced development since the first GaN-based transistors in 1993 [6, 7]. GaN-based HEMT suitability for space-based applications is an active research topic, and a GaN monolithic microwave integrated circuit (MMIC) amplifier was recently included within the X-band communication subsystem of the ESA Proba V Earth observation mini-satallite[8]. Research-led development of AlGaN/GaN HEMT performance and reliability has identified common device failure routes and physical mechanisms governing operation. Crystallographic defects such as threading dislocations are reported to both facilitate Ohmic contact formation and degrade device leakage, and associated defect states contribute to stability limitations. Strain relaxation at the heterointerface under operational or conditional stress results in permanent loss of piezoelectric polarisation component and defect centres, severely degrading carrier density and mobility, respectively. Virtual gate effects result in a device current-slump at radio frequencies (above ~ 10 kHz).

The InAlN/GaN heterostructure exhibits similar properties to AlGaN/GaN with the possibility of a strain-free heterojunction at the lattice-matched barrier composition of $In_{0.18}Al_{0.82}N$[9-11]. Theoretically $In_{0.18}Al_{0.82}N$/GaN HEMTs intrinsically evade degradation and failure routes identified in AlGaN/GaN devices without sacrificing device performance. Predominantly due to the high aluminium content and the associated degree of bond polarity, spontaneous polarisation in $In_{0.18}Al_{0.82}N$/GaN heterostructures generates 2-dimensional electron gas (2DEG) densities competitive with AlGaN/GaN structures without the need for a strain-induced piezoelectric component. Furthermore

favourable band properties again resulting from the high aluminium content in $In_{0.18}Al_{0.82}N$ barrier layers allow for reduction of barrier layer thickness and corresponding improvements in device performance[12].

This work focuses on the comparison between operating mechanisms, production routes and device performance of AlGaN and InAlN HEMTs, with an emphasis on reliability for space applications. III-nitride material was grown by metal-organic vapour phase epitaxy (MOVPE) on sapphire substrates, both in-house and by an external vendor. Wafer level characterization examining a broad range of structural, compositional and electrical properties was performed prior to device processing, with HEMT devices and test structures were fabricated using a lithographic process. AlGaN HEMT fabrication techniques obtained from the scientific literature were modified for use with InAlN where necessary. Feedback between in-house device level characterization and process development resulted in optimisation of InAlN HEMT device performance and highlighting of the differences in behaviour between AlGaN and InAlN HEMTs. Advanced device characterization and reliability analysis including thermal stability, gamma ionizing radiation hardness and breakdown properties were explored in the ESA European Space Technology Research Centre (ESTEC) in Noordwijk, Netherlands. Following identification of critical factors limiting InAlN/GaN HEMT performance and reliability, alternative fabrication techniques were employed in order to suppress their effects.

InAlN HEMTs were shown to share the same basic operating principles with AlGaN HEMTs, with the differences arising due to the similar but distinct material properties of InAlN and AlGaN. MOVPE growth is more challenging for InAlN owing to the greater difference in the atomic properties of In and Al compared to Al and Ga, generally stemming from their atomic size. This limits the growth conditions available for optimisation of semiconductor crystal quality, with the alloy composition at the lattice-matched condition, $In_{0.18}Al_{0.82}N$, highly sensitive to temperature. The high Al content in the barrier layer allows for high 2DEG densities without heteroepitaxial strain, an advantage of the InAlN HEMT system over AlGaN. From a device fabrication perspective this results challenges in InAlN HEMT manufacture, as the wide band gap and thermo-chemical robustness make $In_{0.18}Al_{0.82}N$ more difficult to process and

characterise than AlGaN, typically with around 30% Al barrier layer alloy composition in HEMTs. The surface properties of $In_{0.18}Al_{0.82}N$, coupled with the ability to scale the barrier layer to just 5 nm (for improved DC performance), resulted in the InAlN HEMTs presented in this work suffering from parasitic surface leakage and trapping effect and hence being subject to intrusive virtual gate effects and reduced breakdown voltages. A revised InAlN HEMT surface passivation scheme was demonstrated and show to successfully suppress virtual gate effects, with successful identification and compensation of the effects that prevented a direct transfer from AlGaN HEMT manufacturing processes. III-nitride HEMTs were shown to be robust against exposure to radiation and high temperature environments, with a link established between device performance optimisation and reliability.

Chapter 2 provides an introduction to the III-nitride HEMT technology and provides justification for the investigation of InAlN HEMTs as a candidate for applications such as in the space industry. The material properties of III-nitrides are discussed, as well as the advantageous characteristics they afford HEMT devices. The concepts used to qualify HEMT performance and structural characteristics are introduced, providing a context for results presented subsequent chapters. The physical mechanisms governing charge transport are discussed with reference to the scientific literature, covering the semiconductor heterojunction, metal contact boundaries and surface effects. Finally the factors limiting III-nitride HEMT performance are discussed, with elaboration on the failure mechanisms active under radiation and high temperature environments.

Chapter 3 gives an overview of the experimental procedures used to generate the results presented in subsequent chapters. The physics behind MOVPE of AlGaN/GaN and InAlN/GaN heterostructures is introduced, as are the steps taken to ensure GaN buffer layers were semi-insulating. The methods used to structurally and electrically characterize III-nitride epistructures were described, including their limitations. A description of the baseline HEMT fabrication process is given, as is a summary of the device performance corresponding to the results presented in Chapter 5.

The results and analysis of investigations into MOVPE of InAlN/GaN and AlGaN/GaN heterostructures is given in Chapter 4. For AlGaN/GaN heterostructures, produced to

provide context for the challenges presented by MOVPE of InAlN/GaN, the effect of an increased Al barrier content was explored. Nanoscale surface fissures associated with heteroepitaxial strain relaxation were detected under non-optimised growth conditions and linked to anomalous electrical behaviour. For InAlN/GaN heterostructures the optimisation of growth of a 1 nm AlN interlayer was explored, shown to improve electrical performance under the right conditions. The main challenge proved to be balancing the resistive interfacial roughening with carrier recombination into surface states at reduced InAlN barrier thicknesses. The origin of Ga auto-incorporation in InAlN layers grown by MOVPE was explored and a procedure to suppress it was demonstrated.

Chapter 5 shows the results of radiation hardness, thermal stability and off-state breakdown experiments. The robustness of III-nitride HEMTs was demonstrated by the maintaining of operation after storage at 250°C for four weeks and after exposure to 9.2 Mrad of 1 MeV gamma radiation at a dose rate of 6.6 krad/hour. Well optimised commercial AlGaN HEMTs from an external source showed remarkable stability and confirmed the suitability of III—nitride technologies for RF power amplification in space-like conditions. InAlN HEMTs show potential to surpass AlGaN HEMTs in terms of maintaining high performance in adverse environments. However, InAlN HEMTs were shown to be more susceptable to non-optimised device fabrication techniques, principally surface passivation by SiN_x.

Significant improvements made to InAlN and AlGaN HEMT fabrication procedures and the physics behind the changes are presented in Chapter 6. The sensitivity of both InAlN and AlGaN HEMT Ohmic contact resistivity to metallisation schemes and anneal conditions are explored, with an optimised Ti/Al/Ni/Au technique demonstrated alongside an explanation of the mechanisms involved, principally interfacial roughening at the metal-semiconductor interface. The issue of InAlN HEMT surface passivation is addressed with reference to previous chapters. The PECVD condition of SiN_x was optimised to suppress virtual gate effects without degrading DC performance, and an alternative Al_2O_3 atomic layer deposition scheme was explored. Virtual gate effects are linked to a temperature-independent leakage route facilitated by quantum mechanical tunnelling between surface defect states.

Finally a conclusion and outlook for the future is given in Chapter 7. InAlN HEMTs in this work demonstrated their potential as candidates for devices in next generation space-based applications requiring good reliability and stability under adverse conditions. Performance and reliability are generally enhanced compared to equivalent AlGaN HEMTs, although effective surface passivation is challenging principally due to the high sensitivity of InAlN HEMTs to surface electrostatics. Generally InAlN HEMTs may be produced using existing AlGaN HEMT manufacturing technologies, although many of the intrinsic properties that make InAlN/GaN heterostructures attractive impact on effectiveness of epitaxial and fabrication processes. Experimental results and extrapolation of data from the scientific literature suggests advanced optimisation InAlN HEMT performance and reliability can allow for full exploitation of stability offered by the lattice-matched heterostructure and production of devices ideally suited for use in space-based applications.

2. III-nitride transistor principles

2.1 Suitability of III-nitride HEMTs for space applications

This section explores the performance and reliability of transistors utilizing III-nitride semiconductor material. The motivation for the development of a HEMT technology based on the III-nitride material system has been widely discussed in the literature (e.g. [13], see Table 2.1) and is primarily related to the wide bandgap and high chemical bond strength compared with existing HEMT materials such as AlGaAs/GaAs. This has led to considerably improved performance of GaN-based HEMTs compared with conventional III-V devices. The outstanding performance, recent progress in reducing the cost associated with the nitride wafer supply and improved epitaxial quality of III-nitride HEMTs in recent years has led to their use in defence and communication sectors.

The requirements for electronic devices with potential for use in the space industry differ from those to be used in more commercial applications. Production cost is less of an issue, as the cost analysis is dominated by the fuel required to deliver the payload beyond the Earth's gravitational pull. In this sense III-nitride HEMTs are attractive, as the high maximum operating temperatures and power density relax the requirement for complex cooling and circuit matching systems that add weight and cost to a mission. An additional constraint for space-based applications is the unavailability of any direct maintenance to be performed during a mission lifetime. Therefore device reliability is important both to reducing circuit complexity and prolonging the time available for transmitting useful scientific data. In a similar sense high power density and fast electronic switching speeds allow for improved data streaming, increasing the likelihood of major astrophysical discoveries and further justifying the existence of government-funded space programs to a sometimes sceptical public.

The properties that make the III-nitride material system a viable option for consideration in space applications are shown in Table 2.1 [2]. Figure's of Merit (FOM) are metrics used to quantify the overall performance, and are explained in detail in [14] and [15]. The high electron velocity and mobility provide high frequency performance, which combined with the high sheet carrier concentration result in high power densities. The

large band gap and high operating temperature allow for reliable operation under the extreme radiation environments and thermal cycling encountered when undertaking space reconnaissance. Therefore in addition to being of general benefit in communications systems for satellites, the advantages of GaN may reduce payload requirements in missions such as the Solar Orbiter where high temperature exposure is likely and also on missions such as LAPLACE (to Jupiter) where the effects of the planet's radiation belts are an issue.

Table 2.1: Summary of properties relevant to HFET operation for GaN compared with Si, SiC and GaAs. FOM is Figure of Merit, i.e. Baliga[14] and Johnson[15] (from[2]).

Material	Mobility ($cm^2/V.s$)	Relative dielectric constant	Band gap (eV)	Baliga FOM[14]	Johnson's FOM[15]	Maximum operating temperature (°C)
Si	1300	11.4	1.1	1.0	1.0	300
GaAs	5000	13.1	1.4	9.6	3.5	300
SiC	260	9.7	2.9	3.1	60	600
GaN	1500	9.5	3.4	24.6	80	700

Through AlN, GaN, InN and related alloys a direct band gap range of 0.7 eV to 6.2 eV [2] is covered making the system highly adaptable and attractive for optical and electronic applications. Another unusual property is charge polarisation which results from the lack of inversion symmetry in the crystal lattice and uneven bond angles, providing the potential for bond polarisation to dominate electronic behaviour when materials are combined at heterojunctions.

Another advantage of III-nitride HEMTs (in fact HEMTs in general, including other material systems) with regard to space-based applications and compared to 'bulk' devices such as JFETs and MOSFETs is the 2-dimensional nature of the channel (see Section 2.3), and the reduced volume in which radiation damage can occur. While barrier layer thicknesses of the order of 20 nm have typically been deployed in III-nitride HEMTs, thinner barrier layers are possible with increased Al-content[16], as in the case for lattice-matched InAlN HEMTs[17]. Recently InAlN barrier layers grown lattice matched to GaN have demonstrated similar performance to more mature AlGaN/GaN

technologies while eliminating potential failure routes associated with strain relaxation in III-nitride HEMTs incorporating highly strained AlGaN barrier layers[18, 19]. Despite epitaxial challenges associated with the growth of InAlN (see Section 3), comparable 2DEG carrier sheet densities and channel mobilities have been achieved in lattice matched $In_{0.18}Al_{0.82}N$/GaN structures. The thinner barrier layers also allow for process innovations to improve RF and DC performance[20] but increases the influence of surface electrostatics and the need for effective surface passivation[21]. Defect states that exist at the barrier/air interface allow gate electrons to quantum-mechanically tunnel from the gate into surficial electronic surface states and form a virtual gate at the surface[22], limiting high frequency performance and degrading stability (see Section 2.6.2). Effective surface passivation of III-nitride HEMTs is therefore of considerable importance and it is reported to both neutralise surface trap effects and used to balance epitaxial strain[21].

The aim of this work is to identify critical factors affecting InAlN HEMT performance, reliability and production with comparison to AlGaN HEMTs manufactured in parallel. Exploration of relative robustness under space like conditions and testing throughout material and device process development stages facilitates understanding of fundamental mechanisms relevant to confirming the potential of InAlN HEMTs as a next generation candidate in space discovery.

2.2. III-nitride material crystal structure

III-nitride material may exist in either a thermodynamically preferred hexagonal ‘wurtzite’ structure or as cubic ‘zincblende’, with only the former being of serious interest for transistors due to its thermodynamic stability[23]. Wurtzite III-nitrides, shown schematically in Fig. 2.1, may be understood by considering two sublattices consisting of group III atoms and nitrogen, respectively, arranged in a hexagonal close packed configuration. A strong degree of electronegativity from the nitrogen atoms results in III-nitride bond ionicity expressed as local charge dipoles, incurring due to the non-centrosymmetric nature of the unit cell. Hence polarisation effects are strongly dependent on the crystal plane with which a device or structure is aligned with.

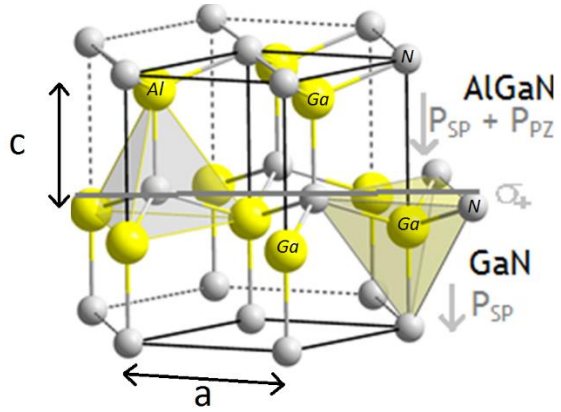

Fig. 2.1: The wurtzite crystal structure around an AlGaN/GaN heterojunction. The tetrahedral group-III and nitrogen sublattices are clearly visible and polarisation vectors are indicated.

Reference to crystallographic planes, direction and orientation in hexagonal-cylindrical wurtzite structures is aided by assigning Miller indices *(h,k,i,l)*, with *h, k* and *i* representing two of the vectors (Fig. 2.1) a_1, a_2 and a_3 and l representing *c*, with *i* included to maintain consistency within nomenclature when describing families of symmetrical planes.

At a ratio of $c_0/a_0 = 1.633$, where c_0 is the distance between hexagonal planes and a_0 is the unit hexagon length, the charge dipoles fully compensate and no net charge polarisation occurs[24]. However, real III-nitride materials display deviations from $c_0/a_0 = 1.633$ which result in macroscopic charge polarisation across the c-axis alone, and not in the a-plane. In fully relaxed materials this is known as spontaneous polarisation, $\underline{\mathbf{P}}_{SP}$, with each member of the III-nitride family exhibiting a different degree based on the corresponding ratio of c_0 and a_0 as shown in Table 2.2. Vegard's Law for calculating the lattice constants of alloyed materials is generally extended to polarisation and band gap with the correction of an experimentally determined bowing parameter[25]. However, InAlN has been found not to conform to this assumption through theoretical modelling[26] due to the differing responses of constituent atoms to internal strain and hydrostatic pressure[27, 28] producing nonlinear effects in resultant polarisation.

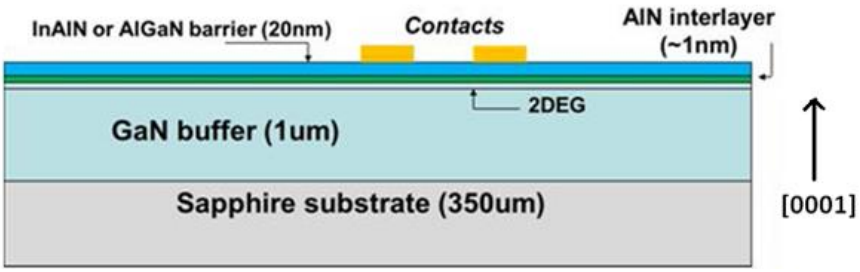

Fig. 2.2: Epilayer stack schematic for III-nitride HEMTs

In addition to spontaneous polarisation most systems include a piezoelectric component, $\underline{\mathbf{P}}_{PZ}$, arising due to strain and associated deviations from ideal crystal structure. III-nitride material containing heterojunctions prepared epitaxially typically includes both types of polarisation which must be accounted for and managed during device design. This is generally done through control over alloy composition and layer thickness.

Table 2.2: Lattice constants for the hexagonal binary III-nitrides, determined theoretically[29]

Material	c_0 (nm)	a_0 (nm)	c_0/a_0	$\mathbf{P_{sp}}$ (C/m^2)
AlN	0.4982	0.3112	1.601	-0.0898
GaN	0.5185	0.3189	1.626	-0.0339
InN	0.5705	0.354	1.612	-0.0413

It therefore follows that every heterointerface in c-plane III-nitride crystal structures exhibits polarisation. To maintain charge equilibrium loosely bound carriers may migrate through the system, affecting the valence and conduction band and carrier profiles. When designing devices it is therefore appropriate to consider epilayer alloy compositions based on band gaps, spontaneous polarisation and strain state. Through modelling of complex arrangements and advanced epitaxial techniques 'polarisation matching' has been demonstrated in multi-quantum well structures to align electron and hole wavefunctions and increase the internal efficiency by improving recombination[30]. The lack of c-plane inversion symmetry in the III-nitride wurtzite lattice results in different properties of group III- or N-face structures in terms of thermal stability and chemical behaviour. III-nitride on sapphire by MOVPE generally targets

III-face material, preferred for its smoother surfaces desired to minimize Coulombic scattering in the channel[31].

2.3 2DEG formation in GaN-based heterostructures for HEMTs

In 1993 Asif M. Khan [32, 33] demonstrated the first III-nitride HEMT. The AlGaN/GaN heterostructure (Fig. 2.2) has formed the basis of a large body of research looking to optimise the power handling, high frequency and reliability aspects of such devices. Generally, a thick epitaxial GaN pseudosubstrate is designated as the 'buffer' or 'channel' layer, with a higher bandgap alloy such as $Al_xGa_{1-x}N$ forming the thinner 'barrier' layer. The barrier layer is grown pseudomorphically on top of the GaN channel, resulting in a barrier layer strain that manifests electrically as piezoelectric polarisation. A combination of the spontaneous and piezoelectric polarisation components ($\underline{\mathbf{P}}_{tot} = \underline{\mathbf{P}}_{SP} + \underline{\mathbf{P}}_{PZ}$) results in a sheet of static charge at the barrier/channel interface. The amount of polarisation charge, $\sigma_{interface}$, is dependent on the difference between the barrier and channel total polarisation. Since the GaN channel layers is generally considered fully relaxed with the barrier layer grown pseudomorphically on top, the sheet polarisation charge at the barrier/channel heterointerface is given by Equation 2.1.

$$\sigma_{interface} = ((P_{SP-channel}) - (P_{SP-barrier} + P_{PZ-barrier})) \quad (2.1)$$

In III-face crystals a sheet of positive charge, $+\sigma_{interface}$, exists at the barrier/channel interface due to polarisation effects. This works in conjunction with the conduction band offset to form an electronic quantum well (Fig. 2.3), where the conduction band edge drops below the Fermi level encouraging surrounding electrons to congregate, forming a 2-dimensional electron gas (2DEG) (as opposed to N-face where a 2-dimensional hole gas (2DHG) would form). The 2DEG wavefunction is centred within the GaN channel layer, nominally isolated from the alloy scattering effect of the barrier resulting in good mobility. High saturation carrier saturation velocities in GaN combined with 2DEG densities (n_s) of order 10^{13} cm^{-2} being readily achievable results in an isolated channel

with low sheet resistance (R_{sh}) and high mobility (μ) close to the wafer surface (Equation 2.2).

$$R_{sh} = \frac{1}{Q_e . n_s \mu} \quad , \tag{2.2}$$

Q_e is the electron charge. It has been shown experimentally that the greatest contribution to 2DEG electrons in optimised devices are unbound electrons remaining at dangling bonds at the abrupt discontinuation of the barrier layer[34, 35]. Additional carriers are present due to the relatively high background doping concentration of order 10^{15} cm^{-3} found in III-nitride semiconductor material at the current state-of-the-art[36]. The lack of a requirement to dope epilayers allows the realisation of high electron mobility, limited by Coulombic scattering due to interfacial roughness, alloy scattering and intrinsic defects (see Section 2.3.1).

The electronic energy band profile experiences bending as a result of 2DEG formation. Band profiles are also determined by the influence of surface electrostatics, itself a function of the static charge polarisation and the energy and density of defect states at the upper boundary dangling bonds. Hence in equilibrium the extent to which the conduction band edge at the heterointerface drops below the Fermi level is dependent on the pinned surface potential at the barrier surface as well as the material electrical properties, with that influence directly proportional to the barrier layer thickness, $t_{barrier}$.

The theoretical 2DEG density may be calculated using Equation 2.3, in which the electric field is integrated along the c-plane with respect to position. By including correction terms accounting for quantum well sub-state offset and spin-orbit coupling, the carrier density can accurately reflect experimental studies using electrical characterization through

$$n_s = \frac{\sigma_{interface}}{Q_e} - \frac{\varepsilon_0 . \varepsilon_{r-barrier}}{t_{barrier} . {Q_e}^2} . (Q_e . \emptyset_{Barrier} - \Delta E_C + \Delta) - \frac{\varepsilon_0 . \varepsilon_{r-buffer}}{t_{buffer} . {Q_e}^2} . E_{C-buffer} \quad , \tag{2.3}$$

where Q_e is the electron charge, ε_0 and ε_r are absolute and relative dielectric constants, t is a layer thickness, Φ is work function of the gate metal, ΔE_c is the conduction band offset and Δ is the sub-band correction term[37-40]. The first term represents the effect of the interface polarisation charge $\sigma_{interface}$, and the second term the band offset

between barrier and channel. The third term may generally be neglected due to large thickness of the GaN buffer/channel layer compared to the barrier, except in the cases of growth innovations designed to increase 2DEG confinement. This equation may be solved computationally ([41, 42], see Appendix 2) to predict carrier concentrations induced by different barrier layer alloy compositions (Fig. 2.4(a)).

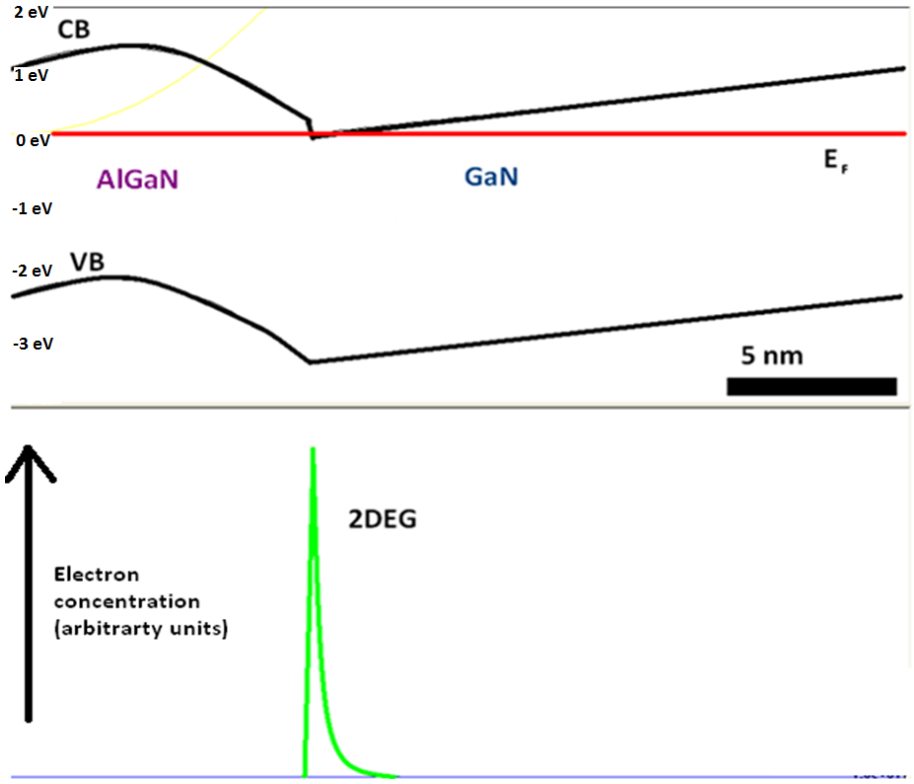

Fig. 2.3: Energy band profile and predicted 2DEG position from BandEng[41]. VB is valence band, CB is conduction band, E_F is the Fermi level

Barrier layer thickness is thus a critical parameter when considering the electrical behaviour of heterostructures. Thinner barrier layers are desirable in device design to maximize the control of the gate electrode over channel current and increase switching capability. However, below a minimum critical thickness carriers begin to recombine with empty surface donor states and the channel carrier concentration is depleted (Fig. 2.4(a)). Lattice matched InAlN barrier layers allow for sub-10 nm barrier layers while maintaining a high channel current[43] (Fig. 2.4(b)). Beyond a certain barrier layer

thickness (depending on the material and alloy composition) the carrier density plateaus to a maximum value, although positioning the 2DEG further away from the surface can be detrimental to performance, as will be discussed later in this chapter.

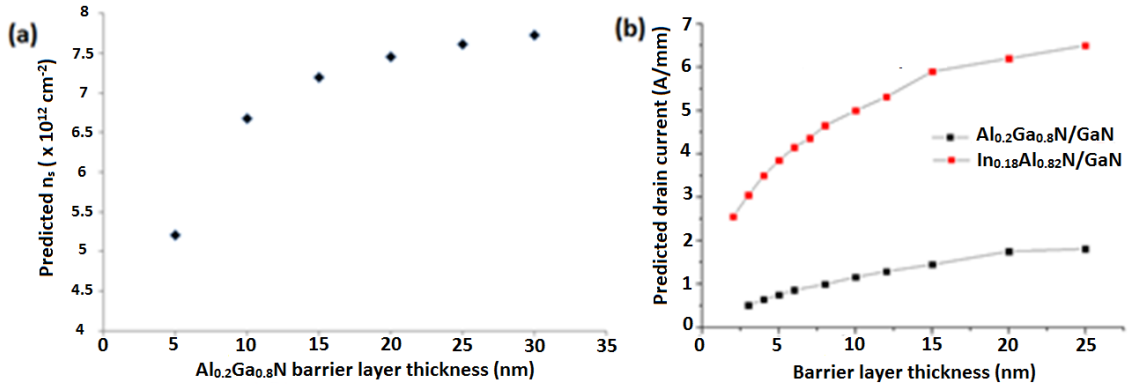

Fig. 2.4: Barrier layer thickness effect on (a) AlGaN predicted n_s from BandEng[41] and (b) InAlN and AlGaN HEMT drain current from Silvaco ATLAS finite element simulations (see Appendix 2)

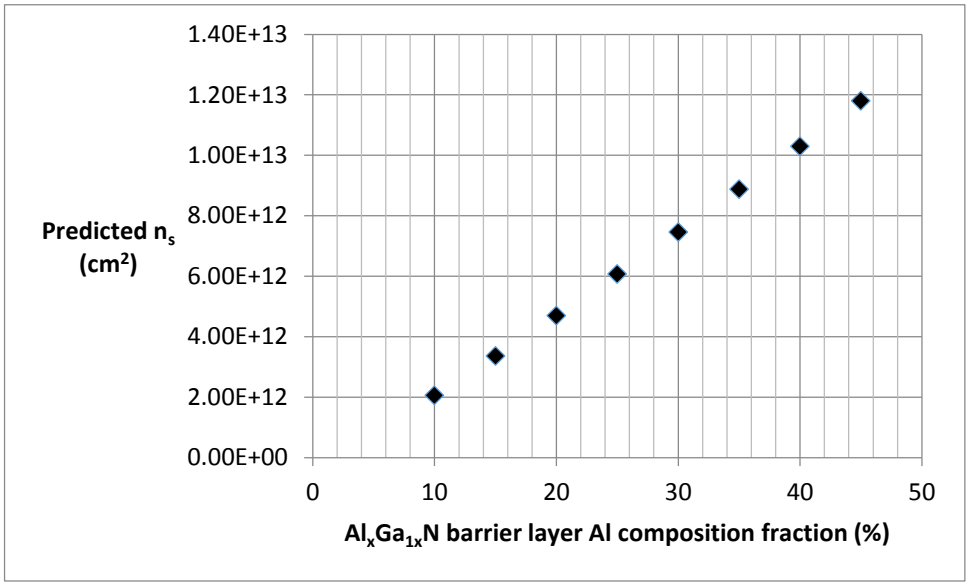

Fig. 2.5: Predicted sheet carrier density in $Al_xGa_{1-x}N$/GaN heterostructures for different values of x[41]

Fig. 2.5 shows the simulated effect on n_s in epistructures with AlGaN barrier layers with different Al content (see Appendix 2 for details of the simulation process). A large band gap and high degree of polarisation are preferable to maintain a high n_s at reduced barrier thicknesses. Recent research has highlighted the possibility of using ultra-thin

AlN barrier layers in which a depleted channel is used to create an enhancement-mode device, allowing for 'normally-off' operation[44]. This behaviour in which the channel current must be induced by applying a positive gate current rather than vice-verse is preferable to reduce system power consumption and prevent destructive power-surging – two factors critical for space-based applications.

In other applications a thicker barrier layer may be desirable, for example to minimize parasitic leakage in HEMT operation and maximise n_s for high power handling capabilities. In this case the thickness is limited by in-plane strain, with energy building with each additional layer and proportional to the different in a-plane lattice parameter. Strain relaxation reduces the piezoelectric component of polarisation and introduces defect centres, suppressing both n_s and channel mobility (μ) and potentially devastating the conducting ability of the transistor channel. Hence for thicker barrier layers a material with a high degree of spontaneous polarisation and a lattice parameter close to that of the buffer layer is appropriate.

2.3.1 Defects and scattering

In all semiconductor materials defects and dislocations are present that mark departures in behaviour from theoretical norms. During material growth, impurities or fluctuations in ambient conditions and reordering of thermomechanical strain lead to electronic states at classically forbidden levels accessible within the structure (i.e. traps) that act as scattering centres, reducing mobility. Traps may be in the semiconductor bulk or at a surface or interface. The amount by which shallow traps (i.e. those with energy levels close enough to the conduction band that thermal excitation is sufficient for carriers to escape at room temperature) deplete the amount of mobile carriers available for charge conduction shows a well-defined dependence on ambient temperature. Fig. 2.6 visualises this effect using experimental data[45].

In Fig. 2.6 the mobility of an organic semiconductor material with shallow electronic traps[45] is shown as a function of temperature when measured by the Hall technique

(solid blue circles see Section 3.2.2) and capacitance-conductance measurements (empty circles). In the Hall measurement only mobile carriers contribute to the result, and the mobility increases at low temperatures due to reduced carrier scatting from thermal lattice vibration (i.e. phonon scattering). The gate-channel capacitance technique uses a depletion effect such that the result accounts for shallow traps, which become dominant at low temperatures and cause scattering that reduces mobility compared to the intrinsic case in the Hall measurement.

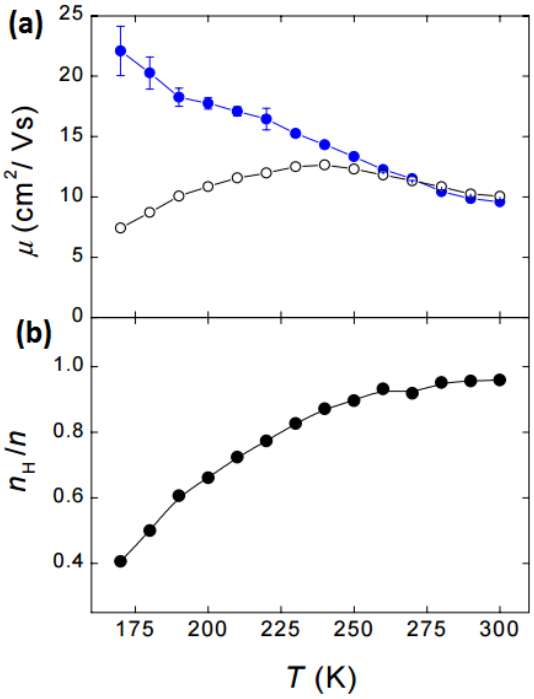

Fig. 2.6: (a) Mobility as a function of temperature as measured by Hall (solid blue circles) and gate-channel capacitance measurements (empty circles) and (b) Hall carrier density over ambient temperature for an organic semiconductor material with shallow electronic traps[45]

III-nitride material grown by current techniques at the state-of-the-art contains a high amount of intrinsic defects, such as oxygen and carbon incorporation; and edge-, screw- and mixed-type crystallographic dislocations[46, 47]. During device design the expected contribution to surface and bulk trap phenomena should be considered. In III-nitride HEMTs the high background donor concentration is commonly compensated by equivalent doping with Fe, Mg or C, [48]. Surface trap phenomena resulting in virtual

gate effects may be managed by passivating devices. Interfacial roughening can limit III-nitride HEMT mobility due to Coulombic scattering experienced by channel electrons, as can overflow of the 2DEG wavefunction into to the randomly alloyed barrier layer and advanced epitaxial techniques are implemented to limit such effects[20]. Each adjustment is accompanied by some trade-off in performance. Hence it is generally desirable during the epitaxy stages of transistor manufacture to optimise crystal quality and limit contamination as much as possible.

The mobility of carriers in the 2DEG is determined by the effective mass and momentum relaxation time associated with dominant scattering mechanisms. Modelling of the contribution of various scattering mechanisms combined with experimental data shows interfacial roughness scattering to be dominant at low temperatures with lattice vibrations (phonons) overtaking prior to room temperature[49]. In III-nitride HEMTs the large band gap and polarisation discontinuity makes scattering associated with interfacial roughness and alloy scattering particularly important[50]. Interfacial roughness is a dominant cause of scattering for InAlN HEMTs with sub-10 nm barrier layers [20, 51].

2.4 Metal-semiconductor junctions

Metal-semiconductor junctions may generally be categorised as one of two types – Ohmic or Schottky. Both are idealisations and depend on the energetic barriers relative to Fermi and vacuum levels in a system. Carriers approaching a metal-semiconductor junction under an externally applied field may experience conduction or rectification, depending on the local band structure and total energy. In III-nitride HEMTs, Ohmic contacts are used for source and drain access regions with a Schottky contact acting as the gate electrode to control channel flow using a field-effect, without the injection of charge.

Ohmic and Schottky contacts are characterised through well-established electrical techniques such as the transmission line model (TLM)[52], either gated or ungated, with the circular transmission line model (CTLM) popular for not requiring an isolation

fabrication stage[53] (see Section 3.6 for details). Optical and scanning electron microscopy (SEM) and surface profilometry are used to gauge contact morphology and cross section SEM or transmission electron microscopy (TEM) with elemental mapping through X-ray spectroscopy are used to image sub-surface activity (see Section 6.1).

2.4.2 Schottky contacts

Gate contacts in III-nitride HEMTs are generally Schottky contacts that act as capacitors when under bias, depleting the semiconductor region beneath the channel of free carriers and preventing the flow of charge between Ohmic contacts. The rectifying behaviour of a Schottky contact is due to the band properties of metal-semiconductor interfaces[54]. When a metal and semiconductor come into contact the metal work function (Φ_M) and the semiconductor electron affinity are arranged in accordance with Anderson's rule [55] which states the vacuum levels across a junction must be aligned. In addition Fermi-level pinning occurs in a practical metal-semiconductor junction, at an energy dependent on the metal and semiconductor species[56]. This causes band bending in the semiconductor and results in a built-in voltage (V_{bi}) and depletion region (extending to a width W), depicted in Fig. 2.7 where the effect of Fermi level pinning dominates the band bending at the metal/semiconductor interface.

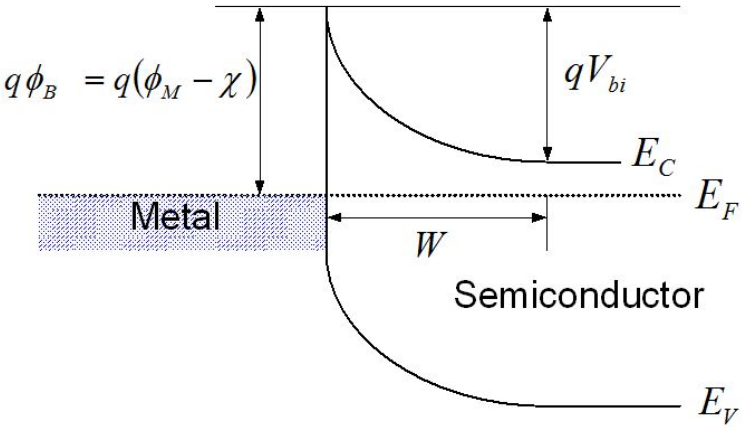

Fig. 2.7: Energy band diagram for a metal-semiconductor Schottky junction

This in turn results in a Schottky barrier of height Φ_B that prevents the conduction of carriers over the junction. Under reverse bias this situation is maintained and exaggerated, and a 'leakage' current is registered as some electrons have enough thermal energy to overcome the barrier. At critical reverse bias breakdown will occur in which leakage current increases sharply due to avalanche effects or more destructive processes[57-59].

Under forward bias a Schottky contact experiences diode behaviour, where enough carriers eventually have sufficient thermal energy to overcome the barrier and current rises rapidly, limited by the series resistance of the material. A sharp turn-on with low forward saturation current is desirable to maximize on/off current ratio in device design.

A Schottky 'gate' electrode in a HEMT is used to control channel current by means of a field-effect 'transconductance'. Theoretically transconductance and leakage properties are limited by device geometry, semiconductor relative permittivity and Schottky barrier height. In III-nitride HEMTs, Ni is a common choice for the gate metal in contact with the semiconductor surface due to its good adhesion and high work function, with pinning and band bending behaviour well established[60]. Au is used to lower lateral resistance in the contact and prevent oxidation, and a diffusion barrier such as Pt may be used to prevent electromigration of Au causing leakage increase over time[61]. Annealing at temperatures of around 500°C has been shown to reduce leakage currents without diminishing transconductance[62], although over-annealing can be damaging. For this reason Schottky contact formation is typically done after the annealing of Ohmic contacts at > 700°C.

2.4.1 Ohmic contacts

Low resistance Ohmic contacts are critical for device performance, and stability is necessary to limit dispersion and oscillations at high power. In a classical n-type semiconductor Ohmic contact, depicted in Fig. 2.8, the combination of the proximity of the Fermi level to the conduction band and band bending at the interface allows the low

resistance, linear voltage-current characteristic, proportional to the contact area. This is due to a combination of the low work function of the Ohmic contact metal, Fermi level pinning caused by electronic states at the metal/semiconductor interface and the doping level in the semiconductor.

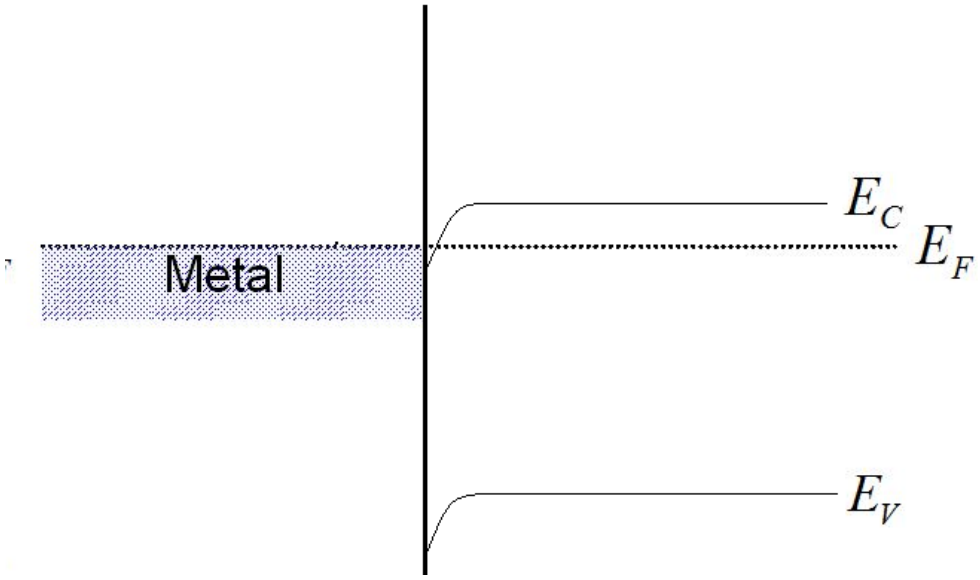

Fig. 2.8: Energy band diagram for a metal-semiconductor interface with high n-type doping

In most materials this is not practical, and deposited metal stacks used for Ohmic contact formation must be annealed to generate low resistance linear charge transfer, although non-alloyed Ohmic contacts to III-nitride HEMTs are possible by selective area doping of wafer material[63]. Generally Ohmic contacts are formed by annealing Ti/Al/Au based stacks[64-68], with Ni, Pt, Ti, Ta or Pd used as a diffusion barrier to prevent Au intermixing and the creation of high resistance compounds[69]. Au is necessary to reduce lateral contact resistivity and facilitate bridging with other devices. The use of Ti as a base layer is due to its good contact adhesion and relatively low work function[70], with Al providing contributing to lower resistances and preventing the oxidisation of the underlying Ti.

Experimental studies of the annealing process in Ohmic contacts to III-nitride HEMTs suggests linear low resistance electrical contact is facilitated by the formation of TiN or TiAlN compounds in direct contact with the 2DEG[71]. During annealing metal migrates

down into the epilayer, beyond the barrier and past the 2DEG. This process is non-uniform and may be aided by local variations in surface morphology and dislocations. Analysis of contact electrical behaviour over a range of temperatures suggests thermionic field-emission (TFE) to be the dominant mechanism, where carriers quantum mechanically tunnel through the energetically forbidden barrier according to the local electric field and assisted by the carrier's own thermal energy. An ultra-thin TiN_x barrier is penetrable due to the high electron concentration at the channel, and conduction through the barrier is then possible due to lattice nitrogen vacancies acting as shallow donor states.

Kim et al[71, 72] recognised a parallel network model as the Ohmic contact conduction process, where contact inclusions provide low resistance paths from contact 2DEG with adjacent areas through unaltered III-nitride barrier layer acting as high resistance paths. Annealing the contact generates such low resistance paths, their number increasing with incident energy (i.e. anneal time and temperature) and induces a corresponding reduction in contact resistivity. The parallel network model was found to apply to both InAlN and AlGaN HEMT epilayers.

Annealing of metal contacts at temperatures required for Ohmic contact formation (in excess of 700°C) results in adverse side-effects that may inhibit device performance[73, 74]. Despite epilayer material being commonly grown at similar temperatures, surface oxidisation from contaminants in thermal annealing apparatus or ambient gases can affect channel conductivity in uncontacted areas. A departure from unprocessed material sheet resistance can be expected underneath the contact, especially in areas affected by contact inclusions, and a reduction in current-voltage characteristics is expected to accompany excessive roughness at the metal-semiconductor junction due to over annealing.

Contact morphology may depart significantly from design tolerance parameters through lateral diffusion, causing short circuits, or the formation of 3-dimensional features due to variations in thermal stress coefficients upon alloy formation. Variation of metal stack thickness ratios and annealing conditions are methods employed to manage contact morphology and achieve low resistivity [73, 75], with for example Xin et al[76]

identifying the effect of Ni and Au thickness in Ti/Al/Ni/Au contacts to AlGaN HEMTs. Thinner barrier layers are presumed more convivial to low resistance Ohmic contact formation, and selective etching of epilayer material has been shown to effectively reduce contact resistivity through the introduction of an extra fabrication stage [279].

2.5 III-nitride HEMTs principles of operation

A HEMT is a type of field-effect transistor (FET), hence their alternate name, heterostructure field-effect transistors (HFETs). First invented in the 1930s, FETs did not become common until the invention of the metal-oxide field effect transistors in the 1960s[77]. The power MOSFET sector is worth US$ 6 billion as of 2014[6, 7], and shares domination of the power electronics market with insulated gate bipolar transistors (IGBTs), a separate technology with similar applications.

Because of this MOSFETs are well understood in terms of the principles governing device operation, and design and manufacturing procedures are well established. Traditionally in a MOSFET (Fig. 2.9) a gate contact (metal or polycrystalline Si) is deposited on top of an insulating dielectric layer (SiO_2) which itself is deposited on a lightly doped Si 'body' layer. Adjacent Si semiconductor regions of opposite doping types to the body (i.e. p-type if the body is n-type) define the source and drain regions of the semiconductor, on top of which the appropriate Ohmic contacts (metal) are positioned. In an enhancement mode device charge can flow freely between source and drain, with linear current-voltage characteristics, only when the gate bias is sufficient to generate an inversion layer in the semiconductor body. When the source-drain bias reaches a critical gate bias-dependent value the device is in saturation mode, and current no longer increases with voltage (see Fig. 2.9).

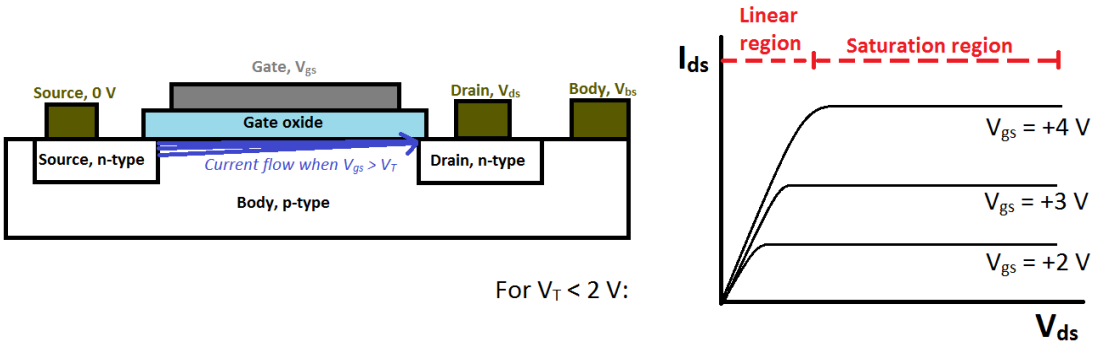

Fig. 2.9: Generic layout of MOSFET device in the common source configuration (V_{source} = 0 V), where the drain current increases with drain bias, +V_{ds}, and is depleted by the negative gate bias, -V_{gs}. A drain current-voltage is shown for different V_{gs} in the case where V_t < 2 V

III-nitride HEMTs also operate using source, drain and gate terminals, advantageous for integration into existing systems where circuit logic does not need to be adapted. FETs, i.e. HEMTs and MOSFETs are generally operated in the common source configuration, where the source terminal is grounded and the gate and drain voltages applied with reference to it, i.e. drain voltage becomes V_{ds} and gate voltage is V_{gs}. As a consequence, many of the improvements to MOSFET technologies made since their development over 50 years ago are directly transferrable to III-nitride HEMTs, discussed in Section 2.6.1. This is despite III-nitride HEMTs operating under different principles as discussed below.

AlGaN and InAlN HEMTs generally speaking comprise of similar semiconductor structures. A 2DEG, thin, mobile sheet of charge described in Section 2.3, exists near the surface at the AlGaN/GaN or InAlN/GaN heterointerface. Electrons travel from source to drain via the 2DEG, with the gate electrode controlling the flow of charge, similar to a MOSFET. However in a III-nitride HEMT the device is 'normally-on', i.e. the gate bias is used to deplete the already present channel rather than generate it. From a circuit design perspective this is detrimental, and a normally-off device is desirable for safety and a reduced power consumption. Innovations to produce normally-off (i.e. enhancement mode rather than depletion mode) HEMTs are reviewed in Section 7.

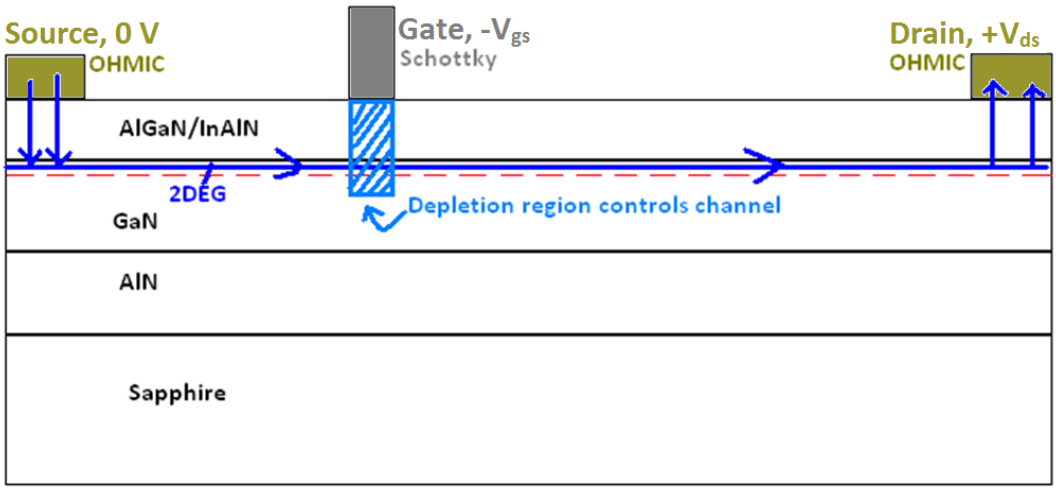

Fig. 2.10: Generic layout of a III-nitride based HEMT device in the common source configuration (V_{source} = 0 V), where the drain current increases with drain bias, $+V_{ds}$, and is depleted by the negative gate bias, $-V_{gs}$.

The layer structure for a III-nitride HEMT is shown in Fig. 2.10 and indicates the position of the 2DEG and contact terminals. In common-source configuration the source contact is grounded, and a source-drain channel is controlled by a positive drain bias, V_{ds}. A negative gate-source bias V_{gs} then controls the flow of current by depleting the channel, and under the correct bias conditions acts as a switch. A relatively small gate bias can control high power densities at frequencies of of beyond 300 GHz, with device geometry critical in maximizing performance.

A dielectric gate insulation layer may be used in III-nitride HEMTs rather than using a Schottky junction, in order to minimize gate leakage. This is not commonly implemented due to the introduction of parasitic capacitance that limits the frequency response of the device[78]. No biasing of the substrate is necessary for III-nitride HEMTs due to the semi-insulating nature of the buffer layer, and it is generally left floating. This simplifies HEMT operation such that only three terminals need be considered (source, drain and gate) rather than four as with MOSFETs, where the body must be biased due to it being a doped layer.

In an n-channel MOSFET the drain current I_{ds} is nominally zero when the gate bias is below the threshold voltage, i.e. $V_{gs} < V_t$. For $V_{gs} > V_t$, I_{ds} in terms of V_{gs} and V_{ds} is given

by Equation 2.4 for operation in linear mode ($V_{ds} < V_{gs} - V_t$) and Equation 2.5 for operation in saturation mode, when ($V_{ds} > V_{gs} - V_t$):

$$I_{ds-linear} = \mu \,.\, C_{oxide} \,.\, \frac{W}{L} \,.\, \left(\left(V_{gs} - V_t \right) . V_{ds} \; - \; \frac{{V_{ds}}^2}{2} \right) .\; (1 - \lambda V_{ds}) \quad , \qquad (2.4)$$

$$I_{ds-sat} = \frac{\mu}{2} \,.\, C_{oxide} \,.\, \frac{W}{L} \,.\, \left(V_{gs} - V_t \right)^2 .\; (1 - \lambda V_{ds}) \quad , \qquad (2.5)$$

μ is the electron mobility, C_{oxide} is the oxide capacitance, W is the device width and L is the gate length, i.e. the distance between the doped semiconductor regions corresponding to source and drain. λ is a channel length modulation term used to account for the reduction in output resistance as gate lengths decrease to maximise performance. For III-nitride HEMTs attempts have been made to produce similar equations [79-82] using various models accounting for the lattice polarisation effects, self-heating, electronic traps, resulting in formulae of limited practical use due to their complexity. Despite this III-nitride HEMTs show broadly qualitatively similar to MOSFETs when operated in the common source configuration, although because of their different but related operating principles they present a unique but familiar set of challenges with regard to performance optimisation, as detailed in the rest of this section.

In a normally-on depletion-mode HEMT care must be taken to ensure the gate area covers totally any conduction path between source and drain contact regions, to ensure the device can be fully switched off. In practice this is done by over-estimating the gate finger widths and etching a perimeter around the device to create mesa structures or by electrical isolation by ion-implantation.

The source-drain separation (d_{s-d} in Fig. 2.11(a)) sets the channel resistance, generally trading-off against reduced breakdown voltages as fields surpass the GaN critical breakdown field of 3 MV/cm at small distances[83, 84]. The device width, W in Fig. 2.11(a), determines the total current (and hence) power through the device, and values are usually quoted per mm as a reflection of the symmetry in that direction (i.e. A/mm, W/mm).

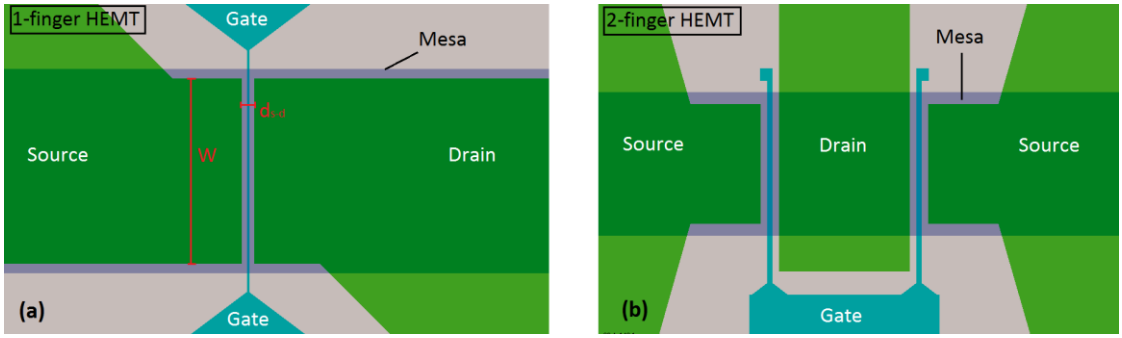

Fig. 2.11: Top view schematic of (a) 1-fingered HEMT and (b) 2-fingered HEMT

As with MOSFETs, the larger the contact area of the gate the higher the capacitance[85]. Thinner gates reduce the contact footprint although increase contact resistivity – another parasitic component that from a design perspective must be minimized to maximize the switching frequency. In MOSFET radio frequency integrated circuit design technologies it is a common technique where the gate RC constant is a limiting factor in the device switching speed to reduce the gate resistance by implementing different device design layouts to the standard rectangular drain-gate-source configuration in Fig. 2.11(a)[86]. Following this, many HEMT devices use multiple gate fingers controlled by the same voltage source. The gate resistance for a device of the usual layout of a given width may be reduced by replacing the wide device with several narrower devices connected in parallel. At high frequencies this technique also acts to limit the detrimental effects of the skin depth, and prevent an unnecessary increase in the gate resistance. The gate periphery is defined as the sum of the width of all the fingers. If two devices are compared, one with (for example) a single finger width W and another with N fingers each of width W/N, the gate length and contact area remain unchanged. Thus the majority of performance characteristics remain unchanged for a device, as does the total gate capacitance. The gate resistance per finger however will be a factor of N less than that of the wide single finger, and the fingers themselves will be in parallel with each other, giving another factor of N reduction. Hence the total gate resistance will be reduced by a factor of N^2 for N fingers. Similarly each gate finger may be contacted at both ends, effectively providing two fingers of equal width that happen to meet in the middle, for a further reduction of 4 in the gate resistance.

A key parameter in HEMT design is the aspect ratio, the ratio of the gate length to the barrier layer thickness (i.e., the gate-channel distance where no gate insulation is present)[87]. If the aspect ratio drops below a specified value for a particular material system (between 5[88] and 15[89, 90] for III-nitride HEMTs, compared with 2.5 - 6 for III-V HEMTs[89], the difference being due to the different dielectric properties of the two materials and hence the internal electric field distribution), short channel effects come into play, in particular the increase in magnitude of the pinch-off voltage of the device due to gate fringing effects (the field effect of the gate being more dominated by the edges of the gate than the centre region due to its small lateral size, resulting in the effective capacitor circuit departing from the parallel plate approximation, thus losing its homogenous gate-field profile beneath the gate), known as Drain Induced Barrier Lowering (DIBL) and gate leakage[90]. InAlN HEMTs can be produced with significantly thinner barrier layers than the AlGaN counterparts (Section 2.2). Consequently shorter gate lengths can be utilized for InAlN devices whilst maintaining the nitride aspect ratio, which would give significant short channel effects for AlGaN devices of the same dimensions[90]. This reduction in gate length, in conjunction with the back-barrier layer technology, has allowed record HEMT switching speeds to be realised[10], due to the reduction in channel length (and hence carrier transit time) and improved confinement of carriers to the channel layer. Thinner barrier layers also increase the influence of surface electrostatics on the channel current, with surface or passivation interface becoming critical.

2.6 III-nitride HEMT state-of-the-art performance

Performance in HEMT devices may be considered in terms of power handling capabilities and frequency limits in switching mode. Metrics such as the Johnson Figure of Merit (JFoM)[15] (Table 2.1) take into account device breakdown properties and electron velocity to rate overall transistor performance. Current- and power-gain cut-off frequencies (f_T and f_{max}, defined as the frequencies at which the current and power gain, respectively, fall to unity, and beyond which no signal gain is achieved) are quoted to refer to switching capability, and power added efficiency (PAE) is a measure of DC to RF

power gain accounting for the incident RF power. A system architect may select transistor components after consideration of the above and the characteristics relevant to the application. In space-based applications a large power handling capability is essential to minimize the number of devices required, and an increased power added efficiency at high frequencies allows for fast processing at low energy consumption.

Commercially available AlGaN/GaN HEMTs are available with PAE up to 65% at 13 W[91], small-signal gain up to 17 dB at X-band and cut-off frequencies in the 100s GHz regime[92]. HEMTs with current gain cut-off frequencies beyond 300 GHz have been reported in the literature[93, 94] and power performance records [95] are frequently broken through innovations in epitaxy[96-99] and reductions in gate length.

InAlN HEMTs have in their own right demonstrated record device performance on multiple occasions[100-102], and this study aims to contribute to the emerging interest in the technology by providing a systematic investigation into their manufacture, operation, performance scaling and suitability for space-based applications.

2.6.1 Factors governing performance

III-nitride HEMT DC electrical performance is represented in Fig. 2.12 by I_d-V_d (a) and I_d-V_g (b) plots. Referring to Fig. 2.12(a), at low drain bias the I-V relationship is linear and on-resistance (R_{on}) is defined, typically at V_{gs} = 0 V but generally applicable to all gate bias values prior to current saturation. Channel current saturates with increasing drain bias and a saturation current is defined (I_{dss} at V_{gs} = 0 V and I_{dss+} at V_{gs} = +1 V). In Fig. 2.12(b) the response of drain current to gate bias when the device is held in saturation (V_{ds} = 10 V) is shown with transconductance, g_m, i.e. the rate of change of I_{ds} with V_{gs}. The point at which the device begins to conduct is the threshold voltage, V_t, defined here as the gate voltage at which the drain current reaches 1 mA/mm for a V_{ds} value of 10 V. Gate and drain leakage currents measured during pinch-off are designated $I_{d\text{-}leak}$ (drain current at V_{ds} = 10 V and V_{gs} = -6 V) and $I_{g\text{-}leak}$ (gate current at V_{ds} = 10 V and V_{gs} = -6 V).

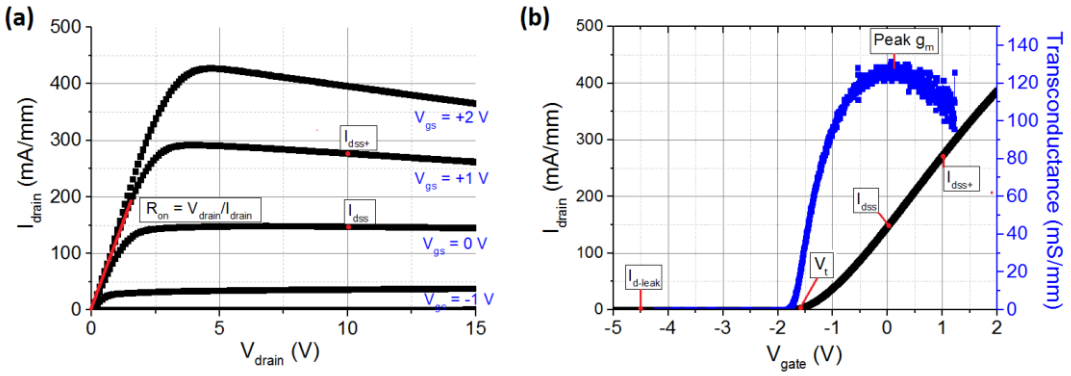

Fig. 2.12: DC electrical properties of a III-nitride HEMT in common-source configuration, (a) drain current against drain voltage at a range of gate bias point (I_d-V_d) and (b) drain current against gate bias when V_{ds} = 10 V (I_d-V_g)

The power handling capability of a device depends on the amount of controllable current available given a certain channel bias. Low R_{on} and high I_{dss} and g_m are desirable, as are low $I_{d\text{-}leak}$ and $I_{g\text{-}leak}$ to obtain large on/off ratios. Finite element simulations allow for the contribution of device geometry and material properties toward these parameters to be gauged (and therefore prioritised). A basic III-nitride HEMT device was simulated using the Silvaco software package, described in detail in Appendix 2. Saturation current is a function of GaN material properties such as electron saturation velocity, mobility and carrier concentration and limited by the overall system resistance, i.e. including contact resistance. Similarly on-resistance depends on material sheet resistance and source/drain contributions. Transconductance scales inversely both with barrier thickness and gate length (although at sub-100 nm gate lengths this relationship becomes more complex). Threshold voltage is a function of gate length (again down to a critical value) and barrier thickness as well as electronic surface pinning at the Schottky interface. Off-state leakage may be through paths in the bulk semiconductor or include a component along the surface, and is generally dependent on carrier confinement (i.e. good control over the 2DEG). Semiconductor background carrier concentration and Schottky barrier height are thus important factors in minimizing off-state leakage.

Equivalent circuit modelling can be used to show a predictable relationship between high frequency performance limits and DC electrical characteristics in a similar way to conventional III-V devices. The Angelov model[103] and varieties thereof [104](Fig. 2.13) confirm an approximate relationship for f_T as in Equation 2.6

$$f_T \cong \frac{g_m}{C_{gate}} \quad (2.6)$$

where C_{gate} is the total capacitance associated with the gate electrode ($C_{gate} = C_{gs} + C_{gd}$). This relationship can be derived by short-circuiting the input and output terminals such that gain is unity by definition and extracting the corresponding frequency [103]. f_{max} flows a similar trend with stronger dependencies on extrinsic parasitic impedance components such as contact resistance, R_{xy}. G_{M0} is a term used to represent transconductance.

Many of the practical routes to device optimisation are common when considering maximising power and frequency HEMT performance. Reduced contact resistivity, high channel mobility and suppression of parasitic leakage are fundamental ways to improve device rating and are as such the focus of much research.

T-shaped gates [88, 105, 106] are designed to minimize gate footprint without compromising contact resistivity, achieving high transconductance with low total capacitance. The maximum operating frequency of a device will scale approximately according to Equation 2.6, and T-shaped gates are an established tool in increasing high frequency performance at the cost of extra lithography stages during device fabrication. A T-shaped gate maintains the large cross-sectional area of the gate, keeping the lateral resistance within the contact to a minimum, but reduced the gate footprint hence maximizing g_m and minimizing C_{gate}, maximizing the maximum operating frequency in line with Equation 2.6. Gate recessing by selective area etching and selective area doping/etching of Ohmic contacts[93] have produced encouraging results at a similar expense to time and cost of the production process.

Regarding material growth, as well as varying the AlGaN barrier content or using InAlN or AlN (Section 2.3), extra layers may be included in the epistructure to improve performance. The inclusion of an optimised 1 nm AlN interlayer (IL) between the GaN and the barrier layer has been experimentally proven to increase channel mobility[18]. AlN has the highest bandgap in the III-nitride system, so the inclusion of a thin strained layer acts to further confine the carriers to the undoped GaN and minimize the electron wavefunction overlap with the barrier layer, reducing alloy-related scattering and hence improving mobility and overall device characteristics (it can also act as a growth barrier

in MOVPE preparation of InAlN/GaN heterostructures by protecting the underlying GaN from potential decomposition when the growth conditions are switched to those required for good quality InAlN growth, see Section 3.3). If the AlN IL is grown too thin, its effects are too weak, i.e., there is no measurable difference in 2DEG mobility[107]. However, if it is grown too thick, channel mobility is reduced undermining the inclusion of the IL, which is speculated to be due to roughening at the interface[108]. Another method of increasing carrier confinement is the inclusion of a thin (~2-8nm) InGaN[109, 110] or AlGaN[90] back-barrier, using a heterojunction beneath the 2DEG to stop it diffusing through the buffer layer as a result of short channel effects. A record breaking f_T = 300GHz $In_{0.17}Al_{0.83}N$ HEMT is reported by Lee et al. in Reference. [90], in which the back barrier suppresses short channel effects and allows for a gate length below 70nm.

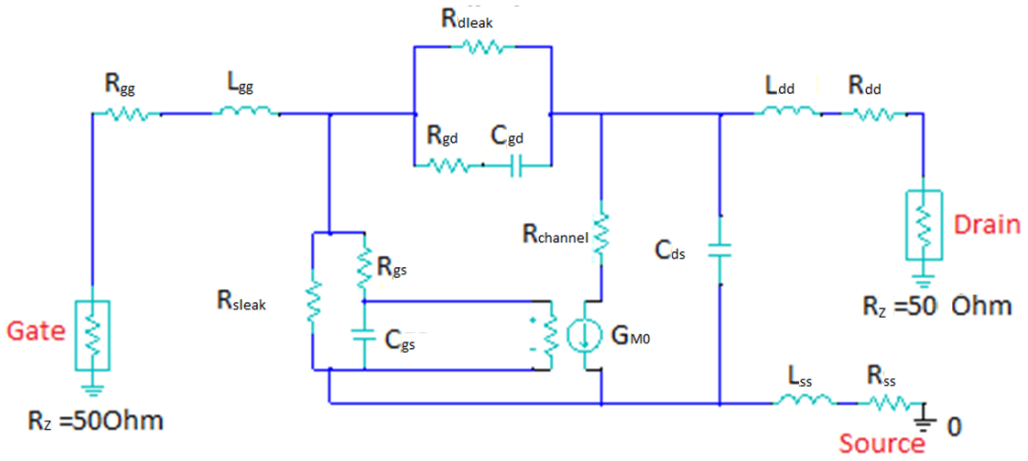

Fig. 2.13: The modified Angelov equivalent circuit model used in to confirm frequency response dependencies in this analysis[104]

2.6.2 RF-DC dispersion

III-nitride HEMTs commonly suffer from a phenomenon known as RF-DC dispersion (or current collapse), in which the measured current level at high frequencies is lower than at DC. The effect is known to be caused by carrier trapping in defects states that release on timescales dependent on their type (i.e. donor or acceptor) and energy level. The traps may originate in the bulk semiconductor material, at the barrier/buffer interface

or at the barrier surface. Pulsed I-V characterisation from different bias conditions can be used to gauge the contribution of bulk and surface trap effects[111], closely related to the parasitic leakage components [112]. The effects of bulk trapping are generally addressed during optimisation of III-nitride epitaxy, either by introducing p-type dopants to compensate for background n-type dopants or by improving crystal quality through modification of growth conditions to suppress intrinsic defect formation. Studies have shown traps associated with the background donor concentration contribute more to bulk effects than interfacial defects at the barrier/channel heterojunction[113]. Compensation p-type doping using C[114], Fe and Mg[115] are reported to suppress bulk leakage and current collapse to varying degrees.

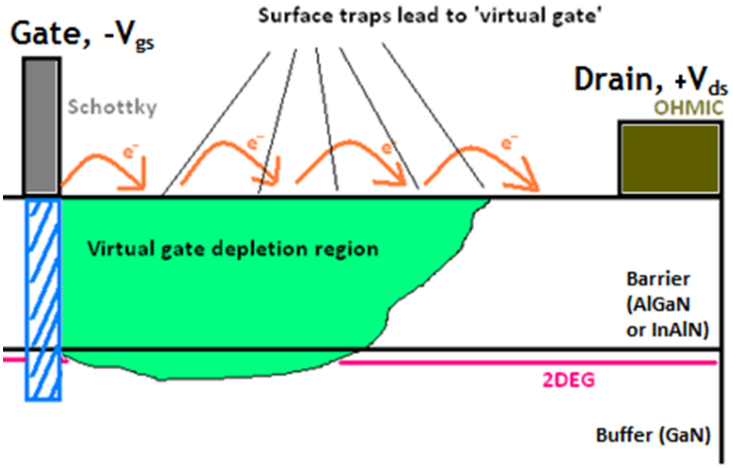

Fig. 2.14: Schematic visualising the virtual gate effect, in which gate electrons are captured by surface traps and cause an extension of the effective gate length with a reduced frequency response

The empty donor states that provide the 2DEG electrons (Section 2.3) may be accessible to gate electrons via trap-assisted tunnelling[116]. Capturing of electrons in surface traps can result in virtual gate effects, visualised in Fig. 2.14, where the effective gate footprint is extended. The frequency response of the device is then limited by the time constants associated with the surface traps[117], which is a function of the defect state energy level[118, 119]. The effective density of states at the upper barrier layer

boundary can be reduced by passivating the device surface[120] or managing the surface charge with in-situ GaN capping[121].

Effective surface passivation is reported to stabilise high frequency performance by improving output power and PAE[122], with performance generally a trade-off between the effect on DC characteristics and improvement on RF performance. SiN_x is frequently utilized as a passivation layer, deposited in-situ[123, 124], by sputtering[125] or by chemical vapour deposition[126], with the effectiveness reportedly governed by the strain-state of the SiN_x layer and contaminants incorporated at the interface during the deposition process. Alternate passivation materials are reported with similar results, and are thought to obey the same principles[120].

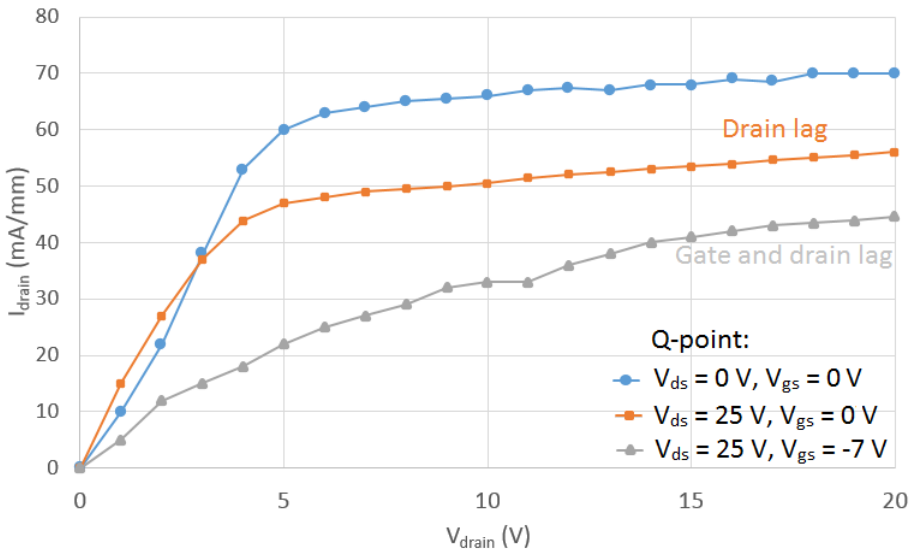

Fig. 2.15: Double-pulsed HEMT I_dV_d plot showing drain lag (orange squares) and the combined gate and drain lag (grey triangles) when pulsed from different Q-points for a pulse width of 500 ns and a duty cycle of 1%

The virtual gate effect manifests as a gate lag when transistors are characterized using pulsed IV measurements (Section 3.6). Fig. 2.15 shows an I_d-V_d profile for an III-nitride HEMT with the drain and gate voltages pulsed from some quiescent point (Q-point). Pulsing from V_{ds} = 0 V, V_{gs} = 0 V shows the highest saturation current. When the device is pulsed from V_{ds} = 25 V, V_{gs} = 0 V the saturation current is reduced due to carriers that

were previously mobile being localised in electronic traps located in the buffer layer, meaning they do not contribute to the measured current. The pulse duration and repetition period should be tuned close to the trap escape lifetime in order to measure this effect, typically around 500 ns for III-nitride HEMTs[127].

When pulsing from V_{ds} = 25 V, V_{gs} = -7 V (assuming the threshold voltage is more positive than -7 V and the device is turned off) the saturation current is further reduced in Fig. 2.15 and the on-resistance is also increased. In this case carriers are captured in traps located both in the buffer layer and close to the gate, i.e. the virtual gate effect. By comparing the saturation currents when pulsing from different Q-points, pulsed IV measurements can therefore be used to provide a quantitative analysis of trap effects in a device, and hence can measure the effectiveness of a passivation scheme (see Section 6.2) and buffer compensation doping in improving the high frequency response of a III-nitride HEMT.

Analysis of the pulsed IV characteristics is therefore a good indicator of RF performance – the trapping phenomena responsible for the degraded IV characteristics when pulsing from biased Q-points is the same that causes RF-DC dispersion, and so a device with reduced gate- and drain-lag can be accurately predicted to have improved RF performance, manifesting as greater cut-off frequencies, f_T and f_{max}.

2.6.3 Power management and breakdown

The practical usefulness of a power transistor is limited by the maximum operating conditions available. The physical processes governing such limits also depend on the operation mode being exploited, i.e is the device passing current or not. Switch-mode operation requires consideration of both on- and off-state breakdown modes.

When operated in the on-state, i.e. with a current passing between source and drain, power handling is principally set by the device width (*W* in Fig. 2.11) and saturation current. Referring to the I_d-V_d plot in Fig. 2.12(a) (Section 2.6.1), the saturation current is a function of the channel length, material properties and gate electrode bias

condition. At increased gate voltage in Fig. 2.12(a) the saturation current increases with gate bias – however, as the saturation current increases a negative differential resistance is noted, i.e. for V_{gs} = +1 and +2 V. Considering that power is the product of current and voltage, this phenomenon may be attributed to Joule heating effects at the channel where the 2DEG generates a large current density. An increased power dissipation with increasing drain current leads to greater thermal lattice vibrations, and therefore increased channel resistance as carriers are scattered by acoustic and optical phonons. Device self-heating is concentrated at the drain-edge of the gate, where the local electric field is maximum [128](Fig. 2.16).

Management of self-heating is critical to device optimisation. The high current/power density of III-nitride HEMTs is advantageous for cost and performance, so most studies focus on ways to efficiently extract heat from the active region via a heat sink typically thermally connected to the backside of the device via the substrate. Reducing the buffer thickness lowers the thermal resistance between channel and substrate (Fig. 2.16(d)). Sapphire substrates are a popular choice due to their low cost and are commonly use in light emitting devices, although III-nitride on sapphire suffers from the large lattice and thermal mismatch, and SiC is a more costly high performance alternative. The thermal conductivity of the GaN channel/buffer layer (2 W/(cm.K)) is high compared to other materials and allows good extraction of heat keeping the channel temperature manageable[57, 58]. AlN sub-buffer layers and the use of different substrates are methods commonly employed to improve backside heat extraction and improve device lifetime and output power[129]. Heat spreading layers on the device surface are another method of heat extraction, with diamond favourable for its high thermal conductivity[130]. In addition to degradation due to thermal build-up, 'hot electrons' can gain enough energy during on-state operation to activate deep acceptor trap states in high field (i.e gate-drain) regions and cause degradation via drain induced barrier lowering (DIBL)[59]. Electroluminescence[57, 58] and micro-raman thermography[131-133] are used to identify failure routes and associate structural features to device reliability. Field plates are used to smooth out internal electric fields[134] thus improving breakdown properties allowing for higher output power and efficiency, and are commonplace in state-of-the-art HEMTs, although they can introduce

additional parasitic capactiance that acts to limit the maximum operating frequency. Under extreme reverse bias conditions the inverse piezoelectric effect can cause strain relaxation in AlGaN and catastrophic degradation of channel conductivity[135]. InAlN HEMTs have exhibited improved robustness compared to AlGaN HEMTs under negative gate bias but are shown to suffer similarly from hot electron effects [9].

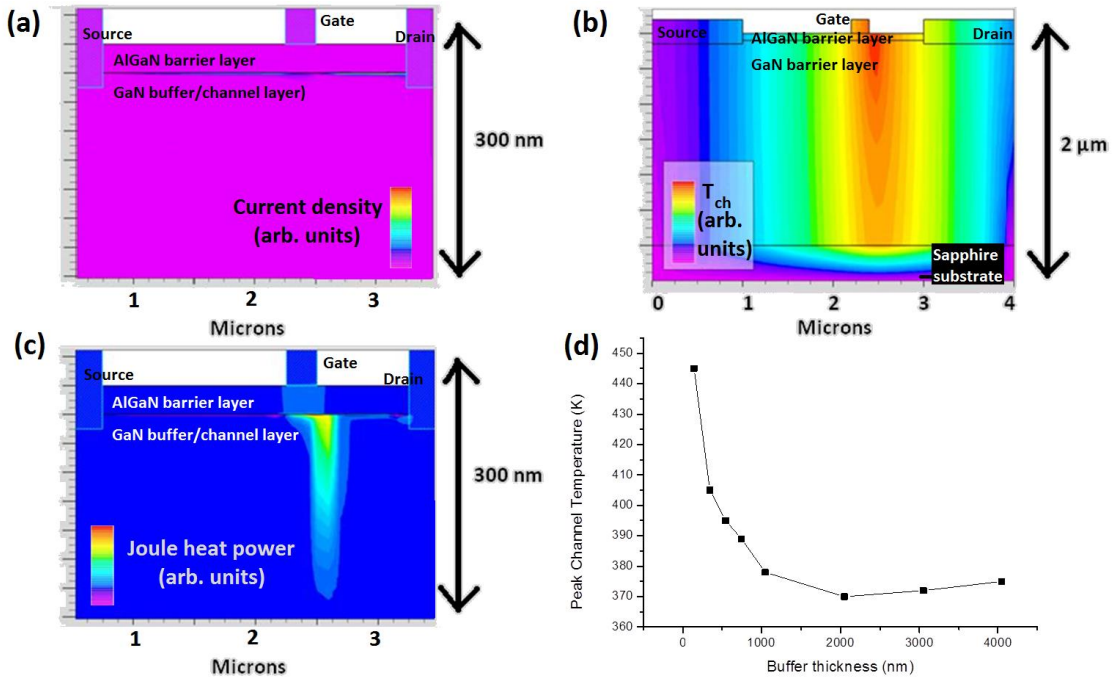

Fig. 2.16: Silvaco ATLAS and GIGA simulation of III-nitride HEMT structures showing (a) current density (b) lattice temperature (c) Joule heat power during on-state operation, and (d) shows peak channel temperature dependence on buffer layer thickness

The off-state power handling capabilities of a transistor are limited a parameter known as breakdown voltage, V_{bk}, defined as the drain bias at which the drain current reaches 1 mA/mm despite a gate voltage putting the device in the nominal off-state. The breakdown voltage influences the power handling capabilities (i.e. the maximum amount of power a device can handle, P_{MAX}) of a device according to Equation 2.7.

$$P_{MAX} = \frac{(V_{bk}-V_t)^2}{2.Z_0} \quad , \qquad (2.7)$$

where V_t is the threshold voltage, typically < 5 V in contrast to V_{BK} > 100 V), and Z_0 is the characteristic impedence of the system. All semiconductor material experiences

breakdown under high enough bias conditions, where valence electrons are provided enough energy by an external field to conduct and force avalanche effects. For field-effect transistors breakdown is defined at the bias condition where normal operation as described in Section 2.6.1 ceases and leakage currents $I_{d\text{-}leak}$ and $I_{g\text{-}leak}$ dominate electrical behaviour. This may be due to avalanche effects, lack of charge confinement or carriers gaining enough energy to penetrate Schottky junctions. In power MOSFETs the breakdown voltage is generally limited by the doping level and thickness of the channel layer. Off-state breakdown in III-nitride HEMTs and routes to optimisation are of keen interest to researches and the mechanisms are well described[57-59].

Source-drain breakdown occurs when the gate electrode field-effect is insufficient to prevent 'punch-through' effects, and conduction occurs via the GaN buffer. Poor confinement of charge to the 2DEG results in a strong dependence of V_t on the applied drain bias (DIBL), degrading performance stability at the system level. This 'short-channel' effect can be alleviated in the case of sub-100 nm gates, by increasing the contact footprint at the cost of transconductance and switching speed. Alternatively it may be managed by the introduction of deep-level traps through compensation doping similar to that discussed in Section 2.6.2[136] or through the use of back-barrier technologies[10, 137] to improve carrier confinement to the channel region.

Gate leakage facilitated by contact electrons quantum tunnelling between the surface defect states described in Section 2.6.2 offers an alternative breakdown route if punch-through conditions are not satisfied[138]. Under high electric fields a sharp increase in gate current is caused by reduced tunnel barriers, with increased power dissipation providing carriers sufficient thermal energy to cause a runaway effect in $I_{d\text{-}leak}$ and $I_{g\text{-}leak}$. As in Section 2.6.2 this effect is managed through effective surface passivation whereby gate electrons are denied access to surface states through the presence of an insulator. Substitution of gate metals to those less prone to diffusion under high electrical stress may also harden devices against gate-related breakdown [139, 140].

2.7 III-nitride HEMT thermal stability

Thermal stability is a crucial consideration when designing electronics for space-based applications. During a mission phase circuitry may be exposed to extreme temperatures due to incident solar radiation, often in cycles. Performance stability of transistor devices over a large range of ambient temperatures is therefore critical to ensure consistent operation where no maintenance can be performed.

The large band gap of GaN compared to Si and GaAs (Table 2.1) makes it a suitable choice for operation at high temperature. Carriers gaining sufficient thermal energy may transition from the valence to conduction band, increasing leakage currents and introducing noise into the system, decreasing the signal-to-noise ratio and limiting the signal processing ability of the device. AlGaN/GaN Schottky diodes have demonstrated function in ambient temperatures of 800°C[141, 142] and AlGaN HEMTs have been shown to perform predictably up to 500°C with moderate recoverable damage[143]. Theoretical work accounting for material and device thermal behaviour has advanced the understanding of AlGaN HEMT degradation[144].

The III-nitride epitaxial structure is considered stable up to temperatures commonly used during MOVPE growth. GaN has a Debye temperature of around 750°C and has been shown to be stable up to 800°C under atmospheric pressure[145]. Barrier layers with high Al alloy content are expected to show increased robustness against thermal decomposition due to the high thermo-chemical stability of AlN[43], and capping can play a similar role[146]. InAlN HEMTs have demonstrated performance at temperatures up to 1000°C, indicating the InAlN/GaN heterostructure is stable up to that point[11].

Thermal lattice vibrations in the form of acoustic and optical phonons incur scattering on 2DEG electrons, with mobility known to share a similar temperature coefficient to acoustic[144] and optical modes[49] depending on the temperature range. From a design perspective degradation of mobility may be managed by optimising heat extraction from the active regions as discussed in Section 2.6.3. Lattice-matched InAlN barrier layers are reported to reduce phonon lifetimes compared to strained AlGaN layers allowing for higher internal fields and carrier velocities[96, 147] and reduced scattering at elevated tempetatures.

Regarding Ohmic contacts, a reduced Al thickness in the Ti/Al/Ni/Au stack scheme described in Section 2.4.1 is reported to improve structural stability at elevated temperatures[11], with the ratio of Al to Ti also affecting thermal stability, with minimal degradation after long term use at 600°C being reported[73]. Electromigration of the Au overlay occurs at around 700°C when operated under electrical stress, causing device failure[11, 148], with Cu providing a more stable alternative with no major effect on contact resistivity[149]. Ohmic contact thermal stability does not appear to present a serious threat to prolonged device use at temperatures previously inaccessible to semiconductor technologies, although more extensive development and characterization is required to confirm this.

The Ni/Au Schottky contact scheme commonly used in III-nitride HEMT gate formation often includes an anneal stage to increase the measured Schottky barrier height, and as such are generally stable for extended periods up to 500°C[70]. Excessive annealing due to high temperature operation leads to the contact becoming Ohmic, with the energy required for collapse of the Schottky barrier due to metal diffusion into the epilayer depending on the exact metal stack used. Metals used in MOSFETs requiring reliable operation such as Ir, Ru and Pd [142, 150-152] are transferable to III-nitride HEMTs. They offer lower diffusivity than Ni due to their higher melting points while forming similar barrier heights [153] for improved contact stability without a trade-off in performance. Oxidation of such schemes at high temperatures can further bolster thermal stability over extended periods[154]. InAlN barrier layers are reported to show robustness against Schottky contact metal diffusion compared to AlGaN when operated at high temperatures[11], attributed to the high thermo-chemical stability of InAlN at 82% Al content.

The high temperature limit of the passivation scheme will similarly depend on the materials used, with SiN_x cracking at 900°C[11]. Structures without passivation schemes will be terminated by oxide formation at the barrier surface, with the species depending on the barrier layer alloy content[11] and high Al content barrier layers being advantageous. Passivation by oxidation of AlGaN HEMT surfaces has been reported to improve both performance and thermal stability compared to uncapped devices[155].

2.8 Radiation effects in III-nitride HEMTs

Devices being considered for space-based applications must demonstrate an ability to maintain performance under radiation conditions likely to be encountered during a mission. Increased radiation hardness minimizes the requirement for shielding and fail-safes, reducing the bulk and mission cost. Radiation hardness testing is often performed at higher doses than would be encountered in space to match the total lifetime dose within a shorter measurement period[156].

Radiation-induced performance degradation in semiconductor devices can be classified into two categories; displacement and ionization damage[157]. III-nitride materials have a large displacement energy making them more robust to incoming radiation removing lattice constituents compared to Si or III-Vs[158]. Furthermore the 2-dimensional nature of the HEMT channel reduces the volume susceptible to critical radiation damage, providing an additional advantage over bulkier MOSFET-type devices.

Heavy-ion or proton bombardment are reported to cause a reduction in drain current through the introduction of defects at radiation centres producing deep level traps that capture carriers from the 2DEG. Nitrogen is more susceptible to lattice displacement than group-III constituents due to its high atomic mobility evidenced by X-ray photoelectron spectroscopy (XPS) analysis of GaN surfaces after irradiation and the detection of increased numbers of Ga-Ga bonds relative to Ga-N bonds[159-161]. Performance recovery after annealing at 800°C (especially under nitrogen rich conditions[162, 163]) suggests the effect of displacement damage is minimal[164]. Schottky barriers are reported to be stable under proton irradiation[165], with low energy particles causing more damage due to the generation of defects close to the surface at the active heterojunction.

Ionization damage is a primary failure in III-nitride HEMTs exposed to radiation. Compton scattering from high energy photons can provide carriers enough energy to generate electron-hole pairs[166] introducing deep level traps in the semiconductor bulk and at interfaces with dielectrics. Low energy electrons are reported to incur similar effects[167, 168]. The traps act to deplete channel current and transconductance and

provide additional parasitic leakage routes. It has been suggested[169] that a photon radiation threshold exists, i.e. an energy or possibly intensity of incoming photons at which point vacancy creation becomes the dominant factor in performance reduction, likely applicable to other forms of radiation. AlGaN HEMTs irradiated with an identical source and analysed over a four month period revealed long term degradation can occur in the devices[170]. Electrical testing performed before, 1 month and finally 4 months after irradiation showed an increase in gate leakage current and low frequency noise over time. This was due not to an increased number of traps, but rather a spatial redistribution – vacancies in a wurtzite nitrogen lattice have an (effective) charge, and are thus subject to positional reorder under electric fields, both applied and intrinsic to crystal structure (i.e., spontaneous polarization)[46, 47].

2.9 Chapter summary

In this chapter the operation of III-nitrides HEMTs has been discussed within the context of existing (i.e. conventional) electronics, namely those using Si and III-V semiconductor materials. The individual physical components that comprise a III-nitride HEMT device have been introduced, such as the concept of a 2DEG and metal-semiconductor contacts. The similarities and differences to conventional field-effect transistor technologies has been discussed, with a focus on space application (meaning radiation hardness and thermal stability). Furthermore the state-of-the-art performance of III-nitride HEMTs has been discussed, with an emphasis on the production methods used to achieve such a status and the current limitations on power-handling and high frequency performance. The information provided in this chapter provides the context for the experimental results presented in subsequent chapters and may be referred to throughout to highlight the impact of the work being presented.

3. Overview of III-nitride HEMT production process

This chapter provides the necessary overview of the manufacturing process used in the production of devices described in the subsequent chapters, and acts as a reference for processes considered standard within the context of semiconductor device production. The first half of this chapter introduces metalorganic vapour phase epitaxy (MOVPE), the dominant technique used in III-nitride semiconductor crystal growth, and describes the primary methods used to characterise the structural and electrical characteristics of the resulting wafers. In the second half the device fabrication baseline process is outlined, from which modifications were implemented to produce the results presented in Chapter 6. The baseline device performance of InAlN and AlGaN HEMTs is presented, alongside a description of the characterization techniques utilized.

3.1 MOVPE crystal growth overview

As described in Chapter 2 the properties of semiconductor material are critical to device operation. Crystal quality and epistructures' adherence to design specification must be above tolerance levels to ensure devices perform reliably with intended performance levels. MOVPE is the most common method of III-nitride crystal growth, with molecular beam epitaxy (MBE) a popular alternative utilising a physical rather than chemical deposition process. MOVPE is capable of faster growth rates and has demonstrated material quality on a par with MBE, although less control over precursor switching is available[171].

In MOVPE of III-nitrides gas phase group-III and N precursors react on a substrate surface to form intermediate 'adatoms' that travel along the wafer surface with a characteristic diffusion length before becoming incorporated into the crystal lattice (Fig. 3.1). The surface is stepped owing to the miscut of the substrate surface relative to the c-plane growth direction, necessary for growth (see Section 4.2.1). The diffusion length, incorporation and desorption rates determine the composition and morphology of the resulting layer. For the N atom precursor NH_3 is used rather than N_2 principally due to

the strength of the triple bond in the N_2 molecule rendering it less reactive. NH_3 reacts with metal-organic precursors trimethylgallium (TMGa) for GaN, trimethylaluminium (TMAl) for AlN and Trimethylindium (TMIn) for InN. H_2 and N_2 are used for the main reactor flow and as carrier gases (not shown in Fig 3.1), flowing through metal-organic storage units and collecting a precise molar mass of precursor, with gas flux into the reactor chamber regulated by mass flow controllers for accuracy down to nmol/min.

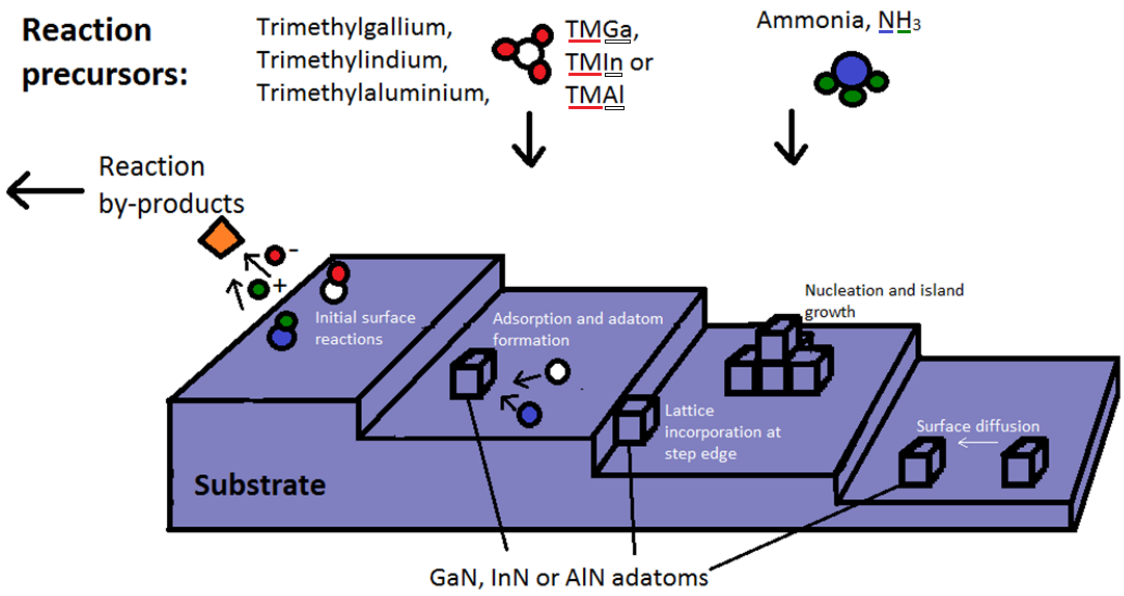

Fig. 3.1: Schematic of the processes involved during MOVPE of III-nitride semiconductors

Formation of the III-nitride wurtzite phase requires high temperatures, typically between 500°C and 1200°C, controlled by heating coils located beneath the substrate susceptor. High growth temperatures result in good thermodynamic stability of the lattice if decomposition does not occur during cooling to room temperature, and bow introduced by thermal stress is managed. Reactor pressure is also used to control growth[145, 172-175]. In addition to the precursor gas flux the ratio of NH_3 to metal-organic precursor is an important parameter, known as the V/III ratio. High V/III ratios are used to suppress nitrogen desorption at growth temperatures by providing high NH_3 partial pressures. The physics involved in MOVPE are complex and involve momentum, heat and mass transfer, all of which must be considered. Computational

models accounting for reactor geometry and process parameters are limited by physical understanding of the thermo-chemical processes involved[176].

3.2 III-nitride material characterisation techniques

3.2.1 Structural characterisation

During MOVPE the thickness and roughness of epilayers may be monitored in real time through the use of LED reflectometry. Monochromatic illumination of the wafer surface at normal incidence at a wavelength transparent to III-nitride material results in interference fringes characteristic of the layer thickness, with the damping factor proportional to surface roughness due to scattering effects[177]. For HEMT structures the active region is typically much less than the wavelength of light used (10 nm c.f. 400 nm) and as such reflectometry[178] is limited to use in analysing nucleation and buffer layers. Temperature is measured in-situ through the use of pyrometry, which assumes near black body emission from the wafer to infer a surface temperature, and a thermocouple placed beneath the susceptor.

Analysis of surface morphology is useful to infer interfacial roughening, especially for thin top layers, and provides information regarding growth processes. Differential interference contrast (also called Nomarski) microscopy[179] is an optical illumination method capable of enhancing material defects on scales larger than the optical diffraction limit. Large scale cracking, surface pits and surface roughness can be imaged easily across the whole wafer surface. Scanning electron micrscoopy (SEM), transmission electron microscopy (TEM), atomic force microscopy (AFM) and related methods provide more information at higher resolution compared to optical microscopy at the cost of a destructive testing process and extended sample preparation times.

AFM[180] allows for high resolution imaging of epilayer surfaces with atomic layer depth resolution and lateral resolution of order 1 nm. In tapping mode AFM a microscopic cantilever oscillates close to its resonant frequency with a laser reflecting off the top

surface. When the tip interacts with a sample surface the force generated modifies the tip frequency proportionally to the tip-sample distance. Raster scanning a small area allows for an image of the surface to be generated with high resolution imaging of morphology, dislocation pits, nano-scale surface cracking and evidence the growth mechanisms occurring in a given sample. In tapping mode AFM the force interaction between the tip and sample surface at the probing frequency (typically around 75 kHz) is such that phase is proportional to local elastic stiffness[181-183]. Hence in addition to surface morphology mapping, analysis of AFM tip phase can be used to generate a map of lattice strain distribution or composition variation[184, 185].

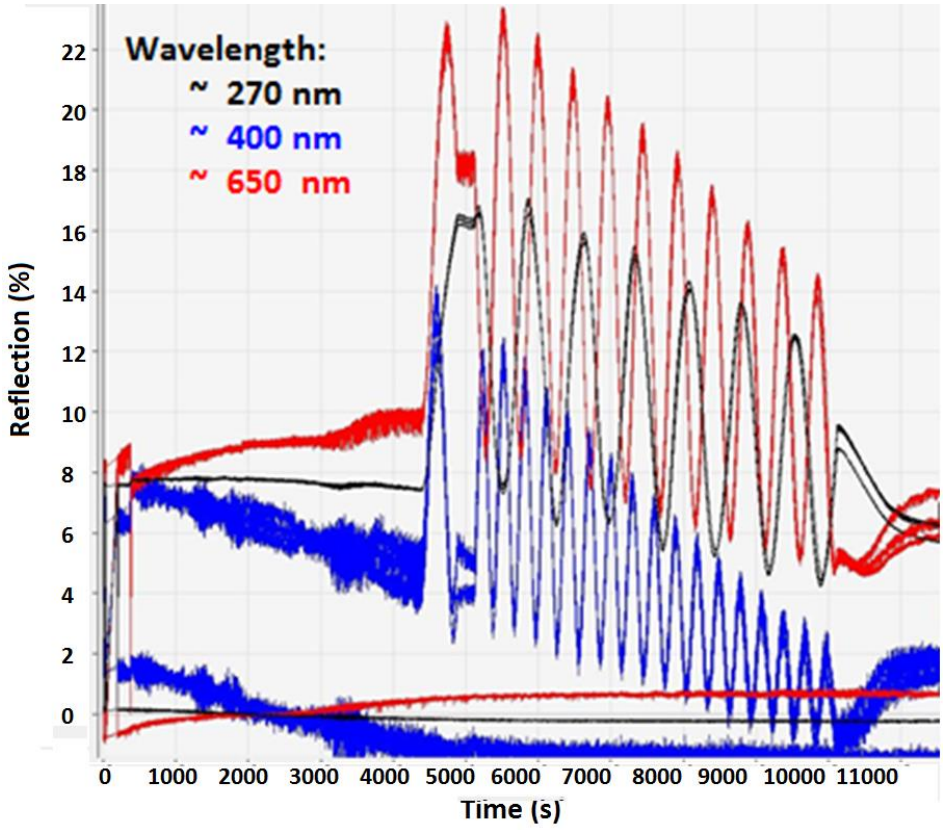

Fig. 3.2: Screenshot of the in-situ LED reflectrometry system, with the three wavelengths visible. The damping is due to epilayer roughening.

In SEM a focussed beam of electrons interacts with a sample with the detected signal used to image morphology with resolution much higher than optical methods, less than 5 nm[186] (Fig. 3.3(b)). A focussed ion beam (FIB) is often used to etch a cross section and image the vertical semiconductor stack. Wavelength Dispersive X-ray Spectroscopy

(WDX) is a SEM technique [187-190] that determines the atomic composition of a sample through X-ray fluorescence, produced by exciting the inner shell electrons of a constituent atom, using a focused high energy electron beam. WDX and the related energy dispersive X-ray spectroscopy (EDX) work by detection of X-rays generated from the transition of atomic electrons between orbitals that are characteristic of the host species. The main difference between WDX and EDX is the type of detectors used. Another SEM based technique is electron channelling contrast imaging (ECCI), where electrons are made to diffract along specific crystallographic planes in order to provide information on dislocations. This is described in more detail in Section 4.1.

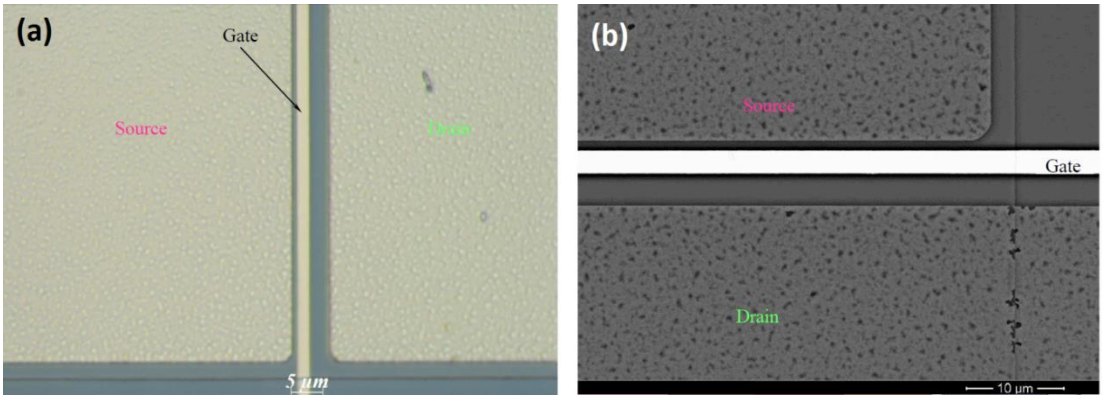

Fig. 3.3: (a) Optical microscope image of an InAlN HEMT close to the diffraction limit and (b) SEM image of InAlN HEMT with increased resolution.

In TEM[191] a FIB lamella with thickness of order 200 nm is subject to an electron beam that is redetected after passing through the sample. The transmission electrons interaction with the lattice allows for cross section imaging with higher magnification and greater resolution than SEM, and although restricted to 2-dimensions imaging of lattice dislocations and atomic level interfacial roughness is possible. Scanning transmission electron microscopy (STEM) combines elements of SEM and TEM through use of additional detectors, electron beam focussing and sample preparation. WDX and EDX can also be used in TEM measurements for elemental identification.

X-ray diffraction (XRD)[192] is the primary technique used to characterise epilayer thickness and composition post-growth. XRD is used to generate information on

thickness, alloy composition and strain state of individual layers in a crystal structure. X-rays with wavelength (λ) similar to the interplanar spacing (d) incident upon a crystal undergo scattering and are diffracted at angles (ϑ) specified by the Bragg formula

$$2d \sin\theta = n\lambda \quad , \tag{3.1}$$

where n is an integer representing the fringe order. By sweeping the X-ray incidence and detection angles and identifying intensity peaks representing constructive interference using dynamical diffraction fitting software, the lattice constant can be calculated for all layers within the penetration depth, typically beyond 1 µm.

The interplanar spacing of the (0002) plane, which relates directly to the c lattice parameter, is analysed in a symmetric ϑ-2ϑ scan in which the sample is fixed and the X-ray detector angle is swept. If the strain state of the structure is known, i.e. in the presumed case for a thin AlGaN or InAlN barrier layer on a relaxed GaN buffer, a ϑ-2ϑ scan in the (0002) plane is sufficient to provide a unique solution to the thickness and composition of the layers in a structure. At layer thicknesses below 10 nm this technique becomes more challenging and the thickness and compositon are calculated from analysis of Pendellösung fringes[193]

If the strain state of a system is ambiguous (as is the case for the high Al content AlGaN barrier layers in Section 4.1) then an asymmetric ω-2ϑ scan, typically focusing on the (10-12)[194] or (10-15)[195] planes, is necessary. Combined analysis of the (0002) ϑ-2ϑ and (10-15) ω-2ϑ scans allows for the calculation of the a and c lattice parameters, which in turn allows for calculation of the epilayer composition and strain state.

XRD can also be used for analysis of threading dislocations density and type (i.e. screw, edge or mixed) ascertained from the full width half maximum (FWHM) of measured peaks[196, 197]. Only screw and mixed type dislocations are detected in symmetric (0002) scans, while the FWHM of (10-15) scans represents the total discloation density, accounting for edge, screw and mixed types.

Reciprocal space mapping (RSM) (Fig 4.1, Section 4.1), is a useful tool for visualising a crystallographic system, where entire planes are represented as points on a map whose axis represent orthogonal lattice spacings. Reciprocal space maps therefore provide

information on the crystal quality, where the broadness of a point represents uniformity throughout the lattice, and the strain state, where the positioning of two points relative to one another shows the difference in the appropriate lattice spacing[198].

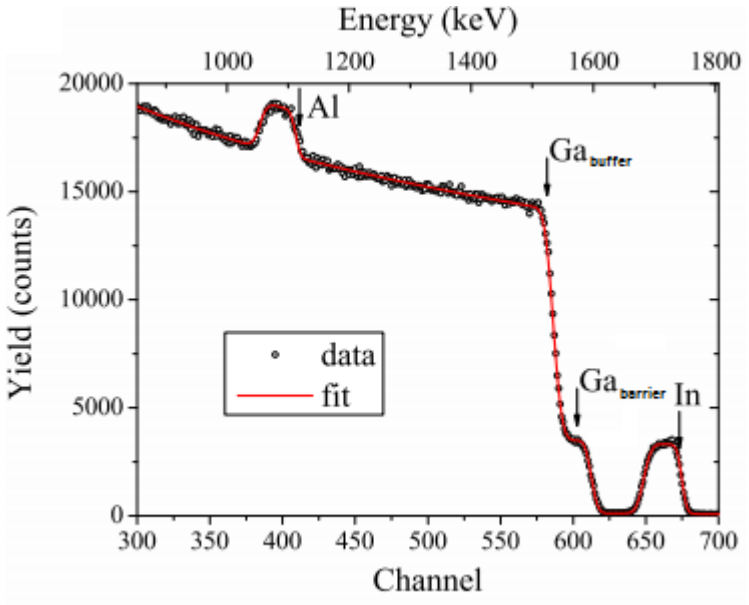

Fig. 3.4: Screenshot of the in-situ laser reflectrometry system, with the three wavelengths visible. The damping is due to epilayer roughening.

In Section 4.2.3 it is shown that XRD alone is insufficient for analysis of quaternary InAlGaN layers, where no unique solution exists to fit the measured lattice spacings. Other complimentary techniques are available that exploit different fundamental properties of the constituent atoms of a crystal, and can be considered independent to XRD. Rutherford Backscattering Spectrometry (RBS)[199-201] uses a positive ion beam scattering off the nuclei of a lattice's constituent atoms, and an analysis of the energy and angle of the redetected beam can generate a composition-depth profile. The technique is complex and requires the use of highly specialized modelling software not described in this work. An example spectrum is shown in Fig. 3.4, for the nominally InAlN barrier layers with Ga contamination (forming InAlGaN) on Ga buffer layers described in Section 4.2.3. The In and Al signals are clearly visible, and the Ga signal is split into the barrier ($Ga_{barrier}$) and buffer (Ga_{buffer}) contributions.

Techniques such as WDX and RBS require layers thicker than those practical for use as III-nitride HEMT barrier layers for valid measurements. In secondary ion mass spectrometry (SIMS) a sample surface is sputtered with a focussed ion beam and the resulting ejected secondary ions are detected, providing a composition-depth profile with sub-nm depth resolution very useful for HEMT barrier layers[202]. X-ray photoelectron spectroscopy (XPS) exploits the process of X-ray fluorescence to determine the composition just a few nanometres into the surface, although the depth resolution is not well defined[203, 204].

3.2.2 Electrical characterisation

For optimisation of devices it is useful to know the electrical properties of the raw wafer material prior to the potentially destructive processes encountered during device fabrication. Capacitance-voltage (C-V) profiling allows determination of carrier density-depth profiles, which in heterostructures for HEMTs generally applies to the position of the 2DEG relative to the wafer surface and the existence of parasitic conduction routes in the GaN buffer or at substrate interfaces. In the electrolytic capacitance-voltage (C-V) method employed in this work, an electrolyte forms a rectifying junction to the III-nitride surface, with an In-Ga eutectic scratched into the wafer surface for the required Ohmic contact. This creates a depletion region with the scaling relationship directly proportional to the carrier density.

The resistive properties of an epistructure are directly related to the power handling capabilities and frequency response of a device, as described in Section 2.6.1. Hall measurements are used universally usually employing the van der Pauw method[205] for its ability to accurately determine sheet resistance and 2-dimensional carrier concentration of any planar structure. In this work a sample is diced (see Section 3.4.2) to 1 cm x 1 cm squares and indium contacts around 0.5 mm in diameter are soldered at 350°C in each corner. Sheet resistance is calculated by driving current through two adjacent contacts along an edge and measuring the bias induced across the two other contacts and determining the corresponding resistance[205]. Under an external

magnetic field, applied perpendicular to the sample surface, free carriers within the sample accumulate in a region according to the Lorentz force. The resulting electric field is measureable as the Hall voltage, proportional to the sheet carrier density (n_s) and the magnetic field strength (fixed at 0.32 T in this work). The mobility may then be inferred from Equation 2.2.

The symmetry between results when the van der Pauw analysis is applied across the different contact configurations indicates the validity of the measurement. For a reliable result the contact resistance of the, in this case, In dots should be low enough such that it is negligible in the calculation. In HEMT heterostructures the ability to form contacts is related to the processes that govern sheet resistance and as such accurate measurement of low mobility samples may require the application of improved contact schemes that remain non-invasive. In this work Hall measurements were also conducted under liquid nitrogen at 77 K. Under this condition scattering due to phonons is reduced due the decreased vibration in the lattice, and other non-temperature related effects such as scattering due to interfacial roughening are highlighted. A drive current of ± 1 mA was used consistently in this work.

3.3 Overview of epilayers grown in this work

AIXTRON 3x2" vertical close-coupled showerhead (CCS) MOVPE reactors[206] were used in this work, both in-house and by NovaGaN[207] for additional InAlN HEMT epilayers (See Section 3.3.1). A graphite-coated susceptor was used (rotating to improve wafer composition and monitoring uniformity), with NH_3, TMGa, TMAl, and TMIn and precursor gases and N_2 and H_2 for the main reactor flow and as carrier gases. In the CCS reactor gas flows through a stainless steel pipes to a showerhead above and parallel to the rotating susceptor by a set distance. Flow though the reactor is well defined by the geometry and optimised for uniform growth. No intentional doping was used for any layers grown in this work, although reactor contaminants such as O and C are common in III-nitride MOVPE[208]. LayTec EpiCurve[178] in-situ laser reflectometry and an AIXTRON ARGUS pyrometry system[209] provided limited real-time information on

crystal quality, uniformity, thickness and surface roughness throughout growth and cool down. Insulating 2" sapphire substrates miscut by an angle between 0.1° and 0.4° relative to the (0001) plane were used primarily due to their low cost, with miscut angle and associated epilayer roughness shown to impact on wafer electrical properties. AlN sub-buffer nucleation layers[210] were implemented to mitigate the large lattice constant and thermal mismatch between sapphire and GaN, and achieve buffer layers with acceptable quality in terms of defect and dislocation density.

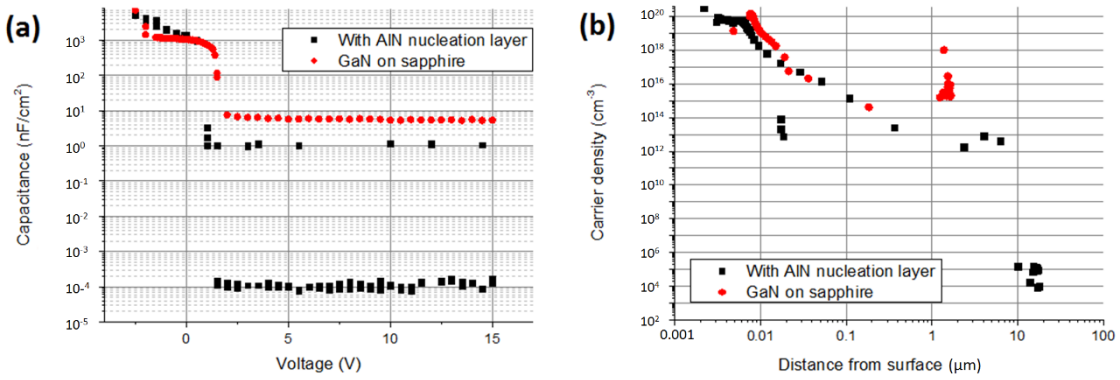

Fig. 3.5: (a) C-V and (b) calculated carrier density profile for InAlN HEMT epistructures with and without AlN nucleation layers

Initial structures consisted of 1 µm AlN nucleation/sub-buffer layers on 0.4° miscut sapphire substrates, with 1µm thick GaN buffer/channel leyers and 20 nm InAlN or AlGaN barrier layers. Due to the lack of compensation doping the buffer layer was required to be highly resistive to allow device pinch-off. GaN grown directly on sapphire results in island growth, with high oxygen incorporation on side-facets leading to unwanted carrier populations beneath the channel. AlN nucleation layers provide a resistive sub-buffer environment that acts to terminate dislocations that result from the high lattice mismatch to sapphire. Fig. 3.5 shows the C-V and carrier density profiles for layers with and without AlN nucleation layers, with the GaN on sapphire sample exhibiting a significant carrier population at 1 µm depth from the surface at the epilayer/substrate interface preventing full depletion beneath the rectifying contact. A potential drawback of AlN nucleation layers is the introduction of additional wafer bow

arising from the different thermal expansion coefficients of sapphire, AlN and GaN. Hence it is desirable to optimise the AlN nucleation layer growth conditions such that as thin a layer as possible performs the required function.

Because GaN may be readily grown 2-dimensionally on AlN, AlN templates are prepared to reduce time and cost. Further to work performed in-house ~ 100 nm AlN nucleation layers were grown by Kyma[210] by an unspecified method of physical deposition. It was necessary to deposit AlN connecting layers at least 100 nm thick prior to GaN buffer growth to avoid the existence of a conducting channel at the regrowth interface.

For GaN buffer layer growth, pressure was found to be a key growth parameter. When grown under low pressure (~ 20 mbar) buffer layers are smooth and insulating, ideal for HEMT epistructures, although the crystal quality was relatively poor, requiring at least 500 nm of GaN growth to ensure channel integrity. At higher pressure (~ 70 - 150 mbar) the crystal quality is improved at the expense of roughness that correlates with channels at the substrate interface detected by EC-V. For GaN channel layers used a standard recipe with growth at 1030°C with H_2 used as a carrier gas. Reduction of the GaN channel growth temperature to 1010°C in an attempt to improve crystal quality collapsed the channel mobility to < 100 $cm^2/V.s$.

AlGaN barrier layers are generally grown under the same carrier gas (H_2), temperature and pressure as the GaN channel through the introduction of TMAl, usually with the V/III ratio and NH_3 flow maintained and the TMGa/TMAl ratio used to control alloy composition. Growth of InAlN lattice-matched to GaN is more complicated due to the different optimal growth conditions of AlN and InN[145]. A compromise between the two extremes described in Table 3.1 must be made, depending on the required composition ratio.

Table 3.1: A comparison between the optimal MOCVD growth conditions for indium- and aluminium nitride.

Material	AlN	InN
Ideal carrier gas	H_2	N_2
V/III ratio	50:1	> 10000
Optimal growth temperature (°C)	>1100	<600

The low temperature and high V/III ratio requirement for In rich nitride material growth is attributed to the high equilibrium vapour pressure of nitrogen with respect to InN[174, 175, 211, 212].The relatively low temperature growth conditions necessary for a 17% indium composition fraction[213, 214] has been speculated to cause the hillock features that have been described on the surface of lattice matched InAlN structures; it is theorized by Yu et al[213] that these are caused by the poor surface mobility of aluminium under the low temperature growth conditions (AlN grows polycrystalline in low temperature conditions[215]). Similar features have been noted in layers grown with a much higher indium content[216]. This is in direct comparison with AlGaN at an aluminium composition of ~ 30%, where the step-bunching has developed to be in the direction of one consistent plane.

N_2 is used as the carrier gas for trimethylindium (TMIn) in growth of InAlN due to the occurance of pyrolysis when H_2 comes into contact with TMIn[217]. Intermediate V-III ratios (around 5000) and temperatures (700-800°C) must be accommodated for to grow InAlN lattice matched to GaN[218], typically with a moderate V-III ratio and, depending on the indium fraction required. To increase the indium fraction, the temperature and pressure may be reduced once the rough conditions for the lattice matched composition has been identified (at 13-24% In content)[219].

3.3.1 Externally procured InAlN HEMT wafer material

Despite significant improvement and identification of performance trends in heterostructures for InAlN HEMTs described in Section 4.2, sheet resistance and mobility results suggest full optimisation was not achieved compared to those reported in the literature. To properly asses the performance and reliability comparison of InAlN and AlGaN HEMTs, InAlN/AlN/GaN/AlN (5/1/1000/200 nm) heterostructures on sapphire substrates were acquired from a commercial source[207].

Surface morphology of externally procured material in Fig. 3.6 differs from the samples grown in-house (Fig. 4.10 and Fig. 4.11), possibly due to a reduced Ga incorporation in

the barrier (see Section 4.3) or alternative growth conditions. The 'cracking' may be evidence of strain relaxation, possibly indicating a departure from lattice-matched conditions, although this is unlikely given the layer is only around 5 nm. Another possibility is the overgrowth of areas with high local dislocation densities (as in Fig. 4.11(b)) originating from the method use to optimise epilayer conductivity. Despite this rms roughness was still 0.41 nm over a 1.5 µm range indicating a smooth layer. This is reflected in the electrical performance shown in Table 3.2, and with the high ratio of mobility at 77 K compared to room temperature indicates interfacial roughness scattering is minimized in the externally procured commercial wafer material.

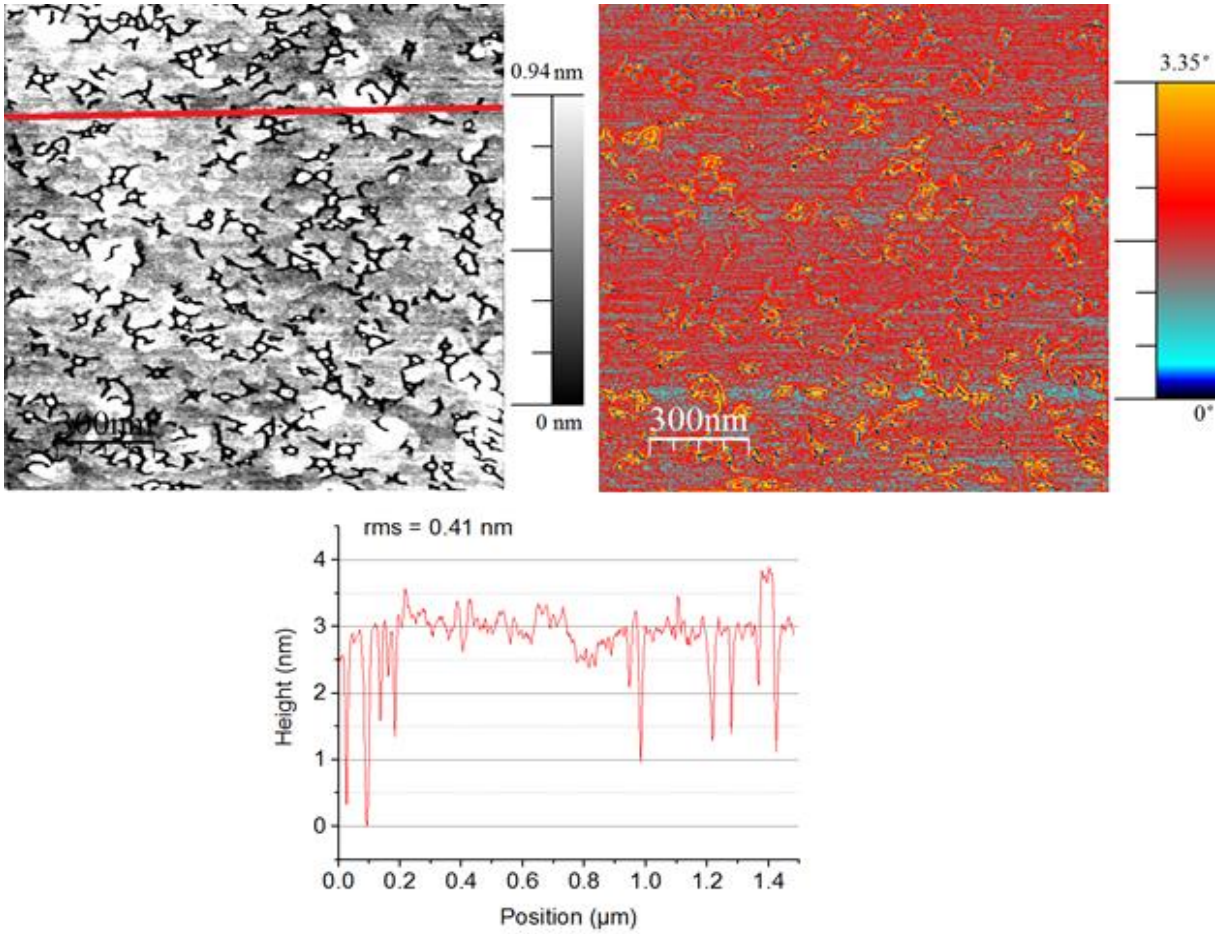

Fig. 3.6: 1.5 µm x 1.5 µm AFM scan of externally procured InAlN/AlN/GaN heterostructure surface with corresponding false-color phase map and morphology profile along the annotated line.

Table 3.2: Room temperature Hall measurement results for externally procured InAlN HEMT wafer material

	Sheet resistance (Ω/□)	Mobility ($cm^2/V.s$)	Carrier density (cm^{-2})
Externally procured InAlN/AlN/GaN heterostructures	258	1319	1.48×10^{13}

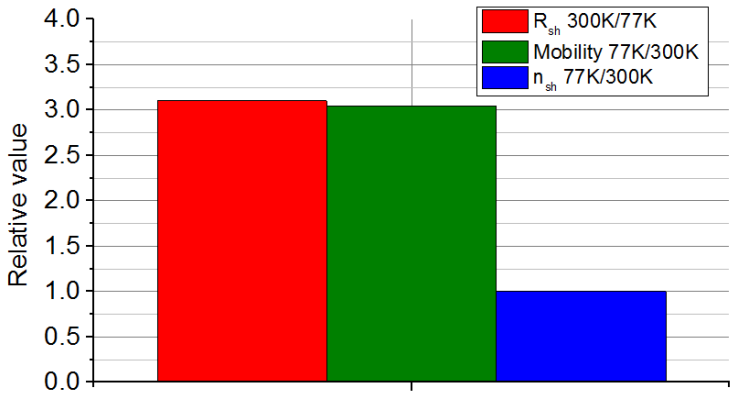

Fig. 3.7: Ratio of Hall measurement results at 300 K and 77 K for externally procured InAlN HEMT wafer material

The nanoscale surface fissures features (Fig. 3.6) interestingly did not lead to a change in Hall carrier density (Fig. 3.7), as was the case for AlGaN HEMTs (see Section 4.1). Their presence may however be related to the anomalous surface leakage properties identified in Section 6.2.3.

3.4 Device design and fabrication

3.4.1 Device simulation

A commercial finite-element simulation package[42] was used to explore the relationship between device geometry and output characteristics (see Appendix 2). This was done in order to achieve target dimensions use in for device design. Mask feature

design (see Section 3.4.2) therefore considers performance optimisation balanced with the practical limitations of the process, in this case the diffraction-limited critical dimension in the UV lithography process that operates in the 360 – 400 nm range.

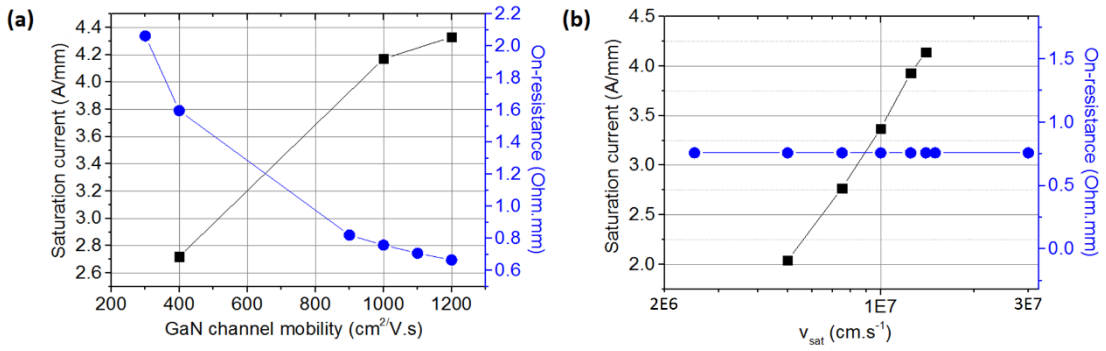

Fig. 3.8: Simulated effect of a varied GaN channel layer (a) mobility and (b) saturation velocity on InAlN HEMT saturation current and on-resistance

An ideal device was simulated using input parameter values obtained from the literature (mobility, saturation velocity, interface polarisation charge etc). The individual input parameters were varied to monitor their effect on saturation current and on-resistance. The resulting performance with respect to power handling and high frequency response may be extrapolated from their relationship to fundamental properties as outlined in Section 2.6.1.

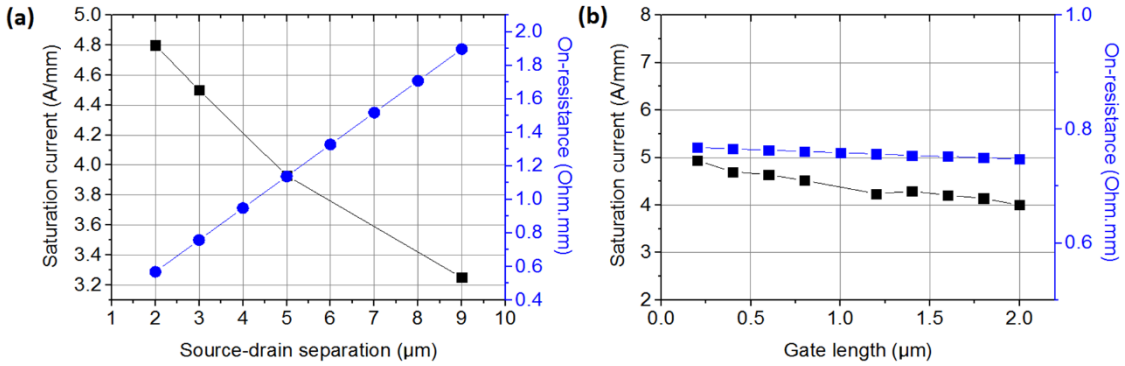

Fig. 3.9: Simulated effect of a varied (a) source-drain separation and (b) gate length on InAlN HEMT saturation current and on-resistance

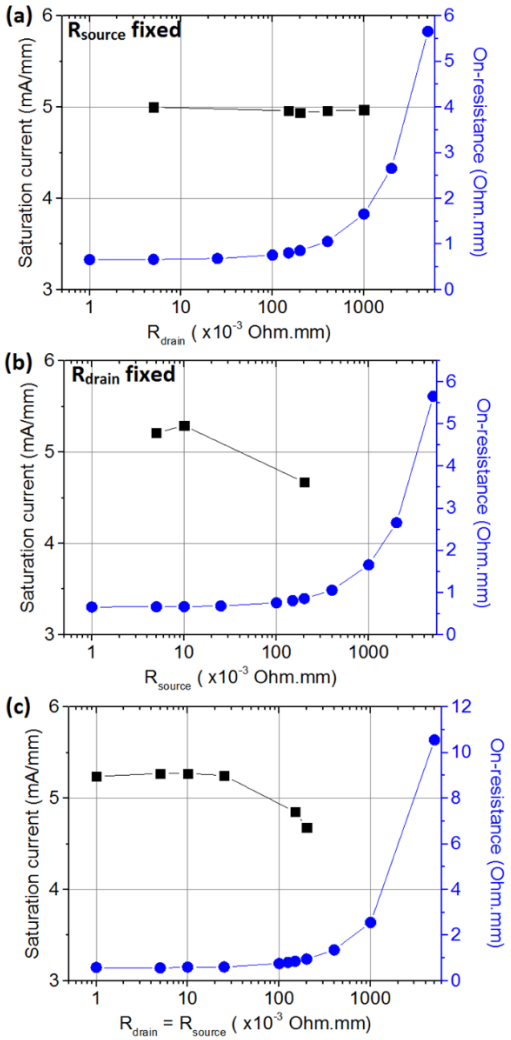

Fig. 3.10: Simulated effect of a varied (a) drain contact resistance (b) source contact resistance and (c) both source and drain resistance on InAlN HEMT DC output

Fig. 3.8 shows the simulated effect of channel mobility and saturation on output characteristics, for a device with a source-drain spacing of 3 µm and a gate length of 0.4 µm. Such material properties clearly exert tremendous influence over device performance, highlighting the importance of crystal growth as described earlier in this chapter.

On-resistance and saturation current scale with source-drain separation for a fixed gate length (Fig. 3.9(a), in which mobility and saturation velocity are fixed at 1000 $cm^2/V.s$ and 1 x 10^7 $cm.s^{-1}$, respectively) due to the contribution of ungated series resistance to the system. This well-defined effect may be used to extrapolate experimental device

performance within the limits of the long-channel approximation[220]. Gate length holds a minor influence over saturation current due to the field-effect immediately under the gate footprint, with the gate length affecting DC properties due to the contribution of series resistance along the channel (Fig. 3.9(b)). For a fixed source-drain distance (as is the case in Fig. 3.9(b)), this is also partially due to the variation of the effective source and drain access resistances. The effect of a varied source and/or drain contact resistance (Fig. 3.10, in which mobility and saturation velocity are fixed at 1000 $cm^2/V.s$ and 1 x 10^7 $cm.s^{-1}$, respectively, for a device with source-drain spacing of 3 µm and a gate length of 0.4 µm) on DC output characteristics was found to be similar to moving the position of the gate relative to those terminals.

3.4.2 Overview of device fabrication

A four layer UV lithographic mask was used to define transistor geometries and passive test structures for process control monitoring, with the layers being:

a) Mesa isolation
b) Ohmic contact formation
c) Schottky contact formation
d) Surface passivation

Two transistor designs were utilised based on the considerations in Fig. 3.8-3.10 and the critical lithography dimension of around 500 nm. A single finger design with 100 µm width and gate lengths of 1 and 2 µm was selected as well as a 2 x 50 µm design utlilising the same gate lengths. These are represent schematically in Fig. 2.11.

Passive test structures on the mask included linear and circular transmission line measurement (uTLM and CTLM, respectively), Schottky diodes, meandering gate line continuity structures and isolation test features. These were used to monitor individual aspects of system behaviour and link back to epitaxy and process development, and will be described in detail as appropriate in subsequent sections.

Prior to device fabrication, the epitaxial layers on 2” sapphire substrates were diced into smaller pieces to maximise experimental efficiency. Initially wafers were cut into ¼ x 2” pieces by mechanical dicing. This resulted in poor lithographic wafer uniformity, due to the effect of the edge-beading effect at corners producing thickness variations. Moving to laser dicing allowed for more control over dicing geometries (curved lines being a possibility) resulting in an increased lithographic yield, evident in Fig. 3.11 where the photoresist thickness fringes take up less area on the circular laser diced wafer.

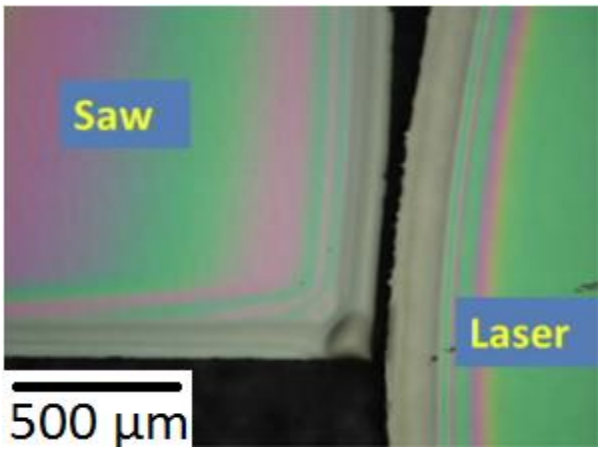

Fig. 3.11: Effect of laser dicing against mechanical saw dicing on thickness fringing of photoresists

The remained of this section provides an overview of the baseline device fabrication process, presented in the order of the associated mask layers and the chronology of the process. Modifications made to the fabrication process in order to optimise performance are detailed in Chapter 6.

a) Mesa isolation

For device isolation a mesa-style etch process was utilised using an inductively coupled plasma (ICP) dry etcher. Initial mesa isolation attempts used a Cl_2-based ICP reactive ion etch, using the recipes previously used for etching n-GaN at the facility in which this work was performed (Tyndall National Institute). Despite giving a reasonable etch rate and sidewall profile on the AlGaN/GaN samples it failed to penetrate InAlN. Increasing the ICP RF power was found to remove the photoresist (and hence mesa definition)

before InAlN began to etch even after moving from the standard definition resist S1813[221] to the thicker AZ-series[222], so was not a viable option.

A revised process based on a standard InGaN etch recipe was used in conjunction with a SiO_2 mask, as the inclusion of indium in a material to be etched in a Cl_2 plasma apparently yields $InCl_3$ formation at the interface under certain conditions[223]. The new recipe was found to etch InAlN at a rate of 440 nm/minute with sidewall profiles shown in Fig. 3.12 below. SiO_2 as an etch mask was in fact found to collapse channel conductivity (presumably though chemical interaction with surface states, see Section 6.2). The InGaN etch recipe was revised further and optimisation was achieved, with the final recipe providing reasonable sidewall profiles and etch rates (Fig. 3.12).

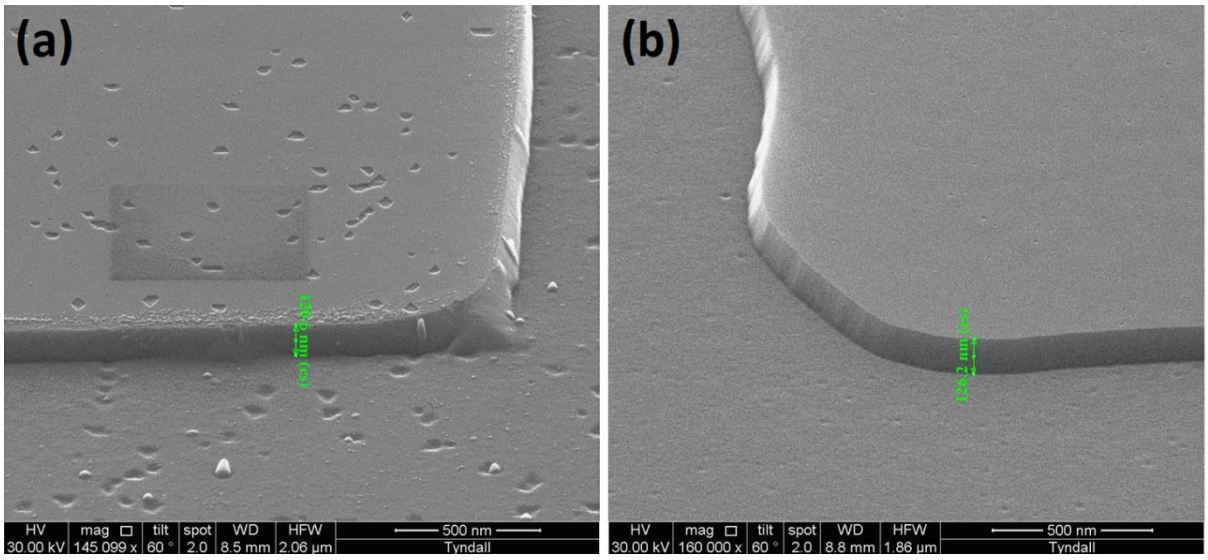

Fig. 3.12: SEM of InAlN mesa profiles with the (a) original and (b) optimised ICP etch recipes

b) Ohmic contacts

For Ohmic contact formation a Ti/Al/Ni/Au based scheme was used in accordance with literature reports (see Section 2.5) and previous internal optimisation of Ohmic contacts to n-GaN[224]. The results of an optimisation campaign are presented in Section 6.1. All metals were deposited under vacuum using a bell jar thermal metal evaporator. The initial production batch of devices (i.e. those used in Chapter 5) utilised a Ti/Al/Ni/Au

(3/50/50/50 nm) scheme annealed at 850°C under N_2 in a rapid thermal processor (RTP).

c) Schottky contacts

A Ni/Pt/Au scheme was used in the devices described in Chapter 5 and 6, annealed at 400°C under N_2 flow. Gate yield was maximised through optimisation of dicing profiles, exposure times and development conditions, in order to achieve 1 µm line resolution in yields approaching 100%, although the exposure time window under the conditions investigated was just 0.5 seconds.

d) Surface passivation

The SiN_x passivation scheme used in the devices described in Chapter 5 was implemented via plasma enhanced chemical vapour deposition (PECVD). The scheme was not optimised for use with InAlN HEMTs, and based on a dual-frequency deposition method explored in previous projects designed to minimize additional strain that would affect the piezoelectric polarisation contribution in AlGaN HEMTs[225]. Optimisation of passivation is explored comprehensively in Section 6.2, where it is shown that the SiN_x PECVD scheme used initially (MF-20/20, see Section 6.2) must be modified to prevent ion damage to the InAlN surface.

3.5 Device characterisation

Parameter and impedance analysers were used to evaluate the IV and CV profiles of test structures and monitor process development, in addition to the testing of active devices. HEMT DC performance was measured using the I_d-V_d and I_d-V_g plots shown in Fig. 2.12, from which important parameters like g_m, R_{on} and I_{dss} can be extracted, as well as gate and drain leakage components (described fully in Section 2.6.1). In this section the analysis of relevant test structures is discussed.

a) Isolation testing

Fig. 3.13 shows IV profiles of mesa isolation test features on InAlN/AlN/GaN heterostructures both with and without AlN nucleation layers, as described in Section 3.3. The isolation test feature measures the current that flows between two regions in which the 2DEG has been etched away (Fig. 3.12), thus providing the degree of parasitic conduction in the GaN buffer. The inclusion of the AlN nucleation layer suppresses buffer leakage by several orders of magnitude, corresponding to the lack of a carrier population at the substrate interface as shown in the C-V plots in Fig. 3.5. Isolation test features used in conjunction with $I_{d\text{-}leak}$ and $I_{g\text{-}leak}$ device parameters were used to identify the source of parasitic device leakage and focus process development accordingly. Extensive analysis of leakage associated with the surface (i.e. not the GaN buffer) in InAlN HEMTs both with and without surface passivation is presented in Section 6.2.3.

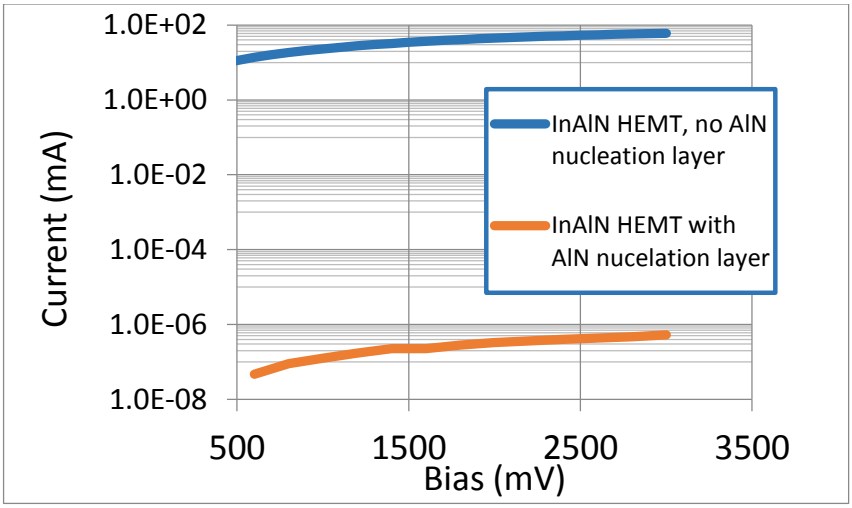

Fig. 3.13: IV profile of isolation test features for InAlN HEMT heterostructures with and without AlN growth nucleation layers

b) Evaluation of metal contacts

Fig. 3.10 illustrates the extent to which Ohmic contact resistance can influence device DC performance. Reduction of access resistance is critical to optimise I_{dss} and R_{on}, and by extension g_m and RF performance. TLM is an established[53, 64, 67, 226] technique

for measuring contact resistance, in which contacts are spaced at irregular intervals, and a plot of resistance against contact spacing is sued to calculate sheet and contact resistance. Sheet resistance may be compared to values obtained by Hall measurement, both as an independent verification and a measure of the effect of contact fabrication on channel conductivity.

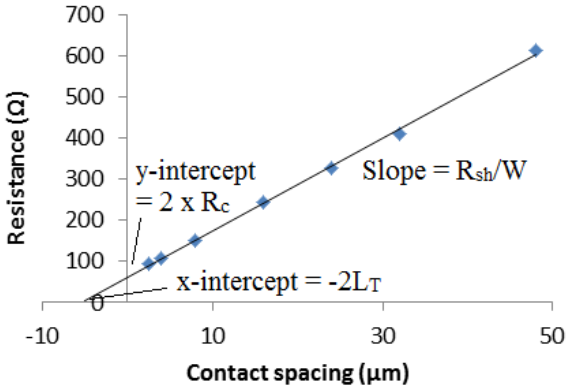

Fig. 3.14: uTLM resistance against contact spacing plot, showing sheet resistance (R_{sh}), contact resistance (R_c) and transfer length (L_T)

Fig. 3.14 shows how sheet resistance (R_{sh}), contact resistance (R_c) and transfer length (L_T) are determined from linear, ungated 'uTLM' test structures. W is the width of the test structure, equivalent to the device width and held at 100 µm throughout this work, and R_c scales with the inverse of W. L_T represents the average distance a carrier travels beneath a contact before entering it, i.e. the degree of current crowding at the edge of the contact. Specific contact resistivity, a more useful geometry-independent parameter, may be obtained by

$$\rho_c = R_c \,.\, L_T \,.\, W \quad , \tag{3.2}$$

The relationships shown in Fig. 3.14 are approximate and depend on certain assumptions. Lateral resistance in the contact itself should be negligible, which may not hold true if alloying and thermal stress causes significant deformation during annealing, and the contact current-voltage characteristic should be fully linear across all bias ranges. It has long been known that damage to semiconductor material as a result of aggressive contact fabrication methods can lead to increased sheet resistance in areas under the contact[227]. The anneal at temperatures of 700°C (see Section 2.5) and

expected degree of metal-semiconductor inter-diffusion in III-nitride Ohmic contacts makes this scenario likely, and end-resistance correction methods were attempted (i.e. measurement of the additional contribution to sheet resistance from regions beneath the contact, and resulting de-convolution from the uncapped regions). Unfortunately the uTLM test structure used here utilized geometries in which L_T approached the contact length (i.e. > 10 µm in some cases) due to higher than expected contact resistances, resulting in uncertainty values when separating sheet resistance in uncapped areas and those beneath a contact too large to obtain practical values. Full evaluation of end-resistance required redesign and manufacture of the uTLM test feature which was beyond the constraints of the project. In Section 6.1 the effect of contact inter-diffusion is explored and the metal stack/anneal conditions' effect on overall contact and sheet resistance is investigated, and a high degree of inter-dependence is observed between nominally independent R_{sh} and ρ_c. In addition to linear uTLM test features, CTLM features were used due to the lack of requirement of a mesa isolation stage making for an easier measurement.

Schottky contact process development was monitored by evaluation of gate-source and gate-drain IV profiles and testing of dedicated circular Schottky test features, with the central Schottky contact varied in size, and gated TLM structures with varying gate-length. Gate contact lateral resistance and gate-line continuity, especially over mesa islands, were monitored using meandering gate test structures.

c) High frequency analysis

Single- and double-pulsed IV measurements were used to evaluate the effect of carrier trapping in HEMT devices where the bias is held at some quiescent point (Q-point) and pulsed to the measurement value, sweeping to generate I_d-V_d and I_d-V_g plots as described in Section 2.6.2 wth a pulse width of 500 ns. The duty cycle is defined as the ratio of pulse duration to interval between pulses. By pulsing from Q-points representing open-channel, closed-channel and unbiased configurations and comparing the current levels the contribution of bulk and surface trapping phenomena is evaluated. This is implemented in Section 6.2.

Small-signal RF performance of HEMT devices was measured by analysis of scattering parameters (s-parameters), where the transmission and reflectance of a power signal is measured at the input (gate-source) and output (source-drain) ports. Measurements were calibrated before each iteration using a commercial standard test chip, where the s-parameters of known short circuit, open circuit and well-defined resistive structures are measured and used to compute a calibration factor. Power reflectance parameters (*S11* and *S22*) are plotted on Smith charts (Fig. 3.15(a)) and transmission parameters (*S12* and *S21*) on polar charts (Fig. 3.15(b)). Analysis of s-parameters allows for maximum current gain cut-off frequency (f_T) and maximum power gain cut-off frequency (f_{max}) to be extracted, by extracting the frequency value at which current or power gain falls to unity.

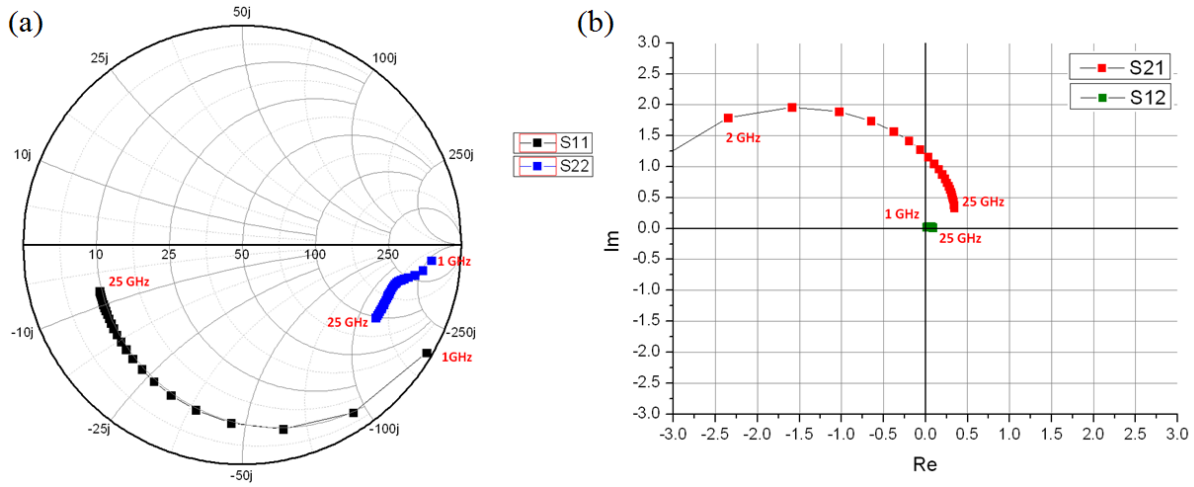

Fig. 3.15: (a) Smith chart showing simulated InAlN HEMT s-parameter power reflectance parameters and (b) polar chart showing power transmission parameters

d) Visual inspection

Nomarski microscopy and SEM were used to image fabricated devices and guide process development in parallel with electrical test features. Fig. 3.16 shows SEM of InAlN HEMTs with gate-source shorting due to lithographic misalignment and an incomplete gate line due to poor metal adhesion.

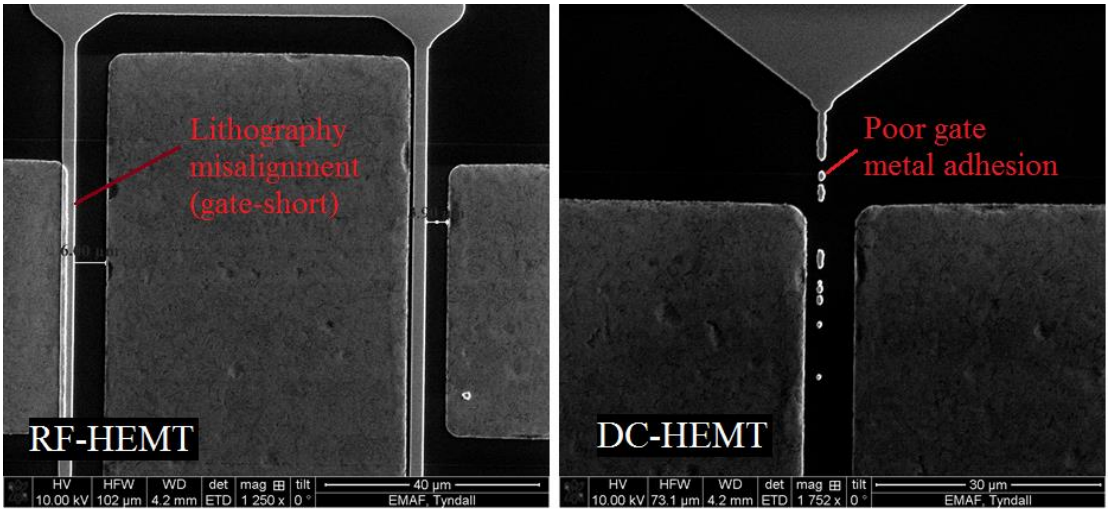

Fig. 3.16: SEM of AlGaN HEMT devices showing problems encountered during fabrication

3.6 InAlN and AlGaN HEMT performance

Selected DC parameters of HEMT devices are shown in Table 3.3, where uncertainty values represent the value spread. Both InAlN and AlGaN HEMTs were investigated, with InAlN/AlN/GaN (5/1/1000 nm) and AlGaN/GaN (10/1000 nm) layer structures, respectively. Furthermore the effect of SiN_x surface assivation was explored, with devices being designated '-uncapped' for the passivation-free cases and '-SiN_x' for the cases with surface passivation. In addition to the HEMTs fabricated in-house, well-optimised production level AlGaN HEMTs were included from a commercial supplier in certain tests. Production level devices show superior performance compared to the research level devices, partly due to the reduced source-drain spacing (4 µm c.f. 8 µm) and gate length (0.5 µm c.f. 1 µm) but highlighting the requirement for extensive optimisation of fabrication methods to fully exploit the performance potential offered by the III-nitride material system (see Section 2.2). In particular the MF-20/20 PECVD SiN_x capping scheme (see Section 6.2.1) used here based is clearly not optimised during fabrication and is seen to degrade research level HEMT transfer characteristics (saturated drain current, I_{dss}, and peak transconductance, g_{m_max}), affecting the InAlN devices more severely than AlGaN. Parasitic conduction routes in the bulk SiN_x or along barrier/SiN_x interfaces result in an increase in off-state drain and gate leakage ($I_{d\text{-}leak}$ and

$I_{g\text{-}leak}$), leading ultimately to difficulties in accurately defining the threshold voltage InAlN-SiN_x and AlGaN-SiN_x HEMTs.

Table 3.3: DC electrical characteristics of InAlN and AlGaN HEMTs without SiN_x capping (InAlN-uncapped and AlGaN-uncapped) and with SiN_x capping deposited by PECVD (InAlN-SiN_x and AlGaN-SiN_x) and production level AlGaN HEMTs

	InAlN-uncapped		**AlGaN-uncapped**		**InAlN-SiN_x**		**AlGaN-SiN_x**		**Production level AlGaN HEMTs**	
	Average	±	Average	±	Average	±	Average	±	Average	±
I_{dss} (mA/mm)	146.7	*44.9*	58.3	*6.1*	24.8	*10.3*	47.6	*6.4*	726.6	*20.5*
g_{m_max} (mS/mm)	83.1	*7.8*	61.1	*8.5*	43.0	*4.9*	46.6	*4.7*	304.0	*6.9*
V_t (V)	-2.5	*0.9*	-1.3	*0.0*	-	-	-	-	-3.3	*0.1*
R_{on} (Ohm.mm)	26.1	*11.1*	179.6	*124.2*	92.7	*18.9*	40.4	*1.4*	2.0	*0.0*
$I_{d\text{-}leak}$ (A/mm)	7.E-05	*1.E-04*	6.E-09	*4.E-09*	7.E-04	*2.E-04*	3.E-04	*1.E-04*	6E-05	*5E-05*
$I_{g\text{-}leak}$ (A/mm)	-1.E-04	*2.E-04*	-9.E-09	*5.E-09*	-3.E-03	*2.E-03*	-2.E-03	*7.E-04*	6E-05	*5E-05*

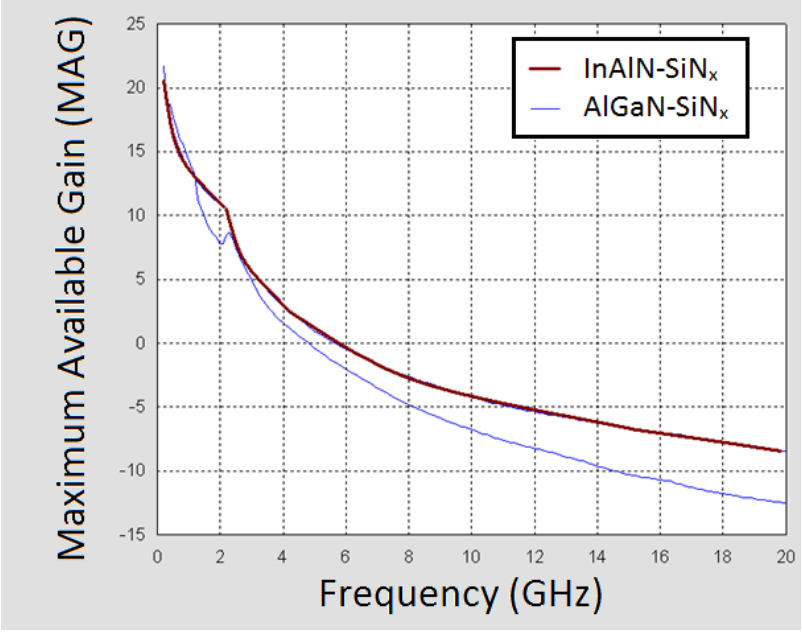

Fig. 3.17: Demonstration of power gain at frequencies up to 4 GHz for InAlN and AlGaN HEMTs with SiN_x passivation

The research-level InAlN-SiN_x and AlGaN-SiN_x HEMTs show similar responses to RF stimulus, with both giving f_T values of 3.6 GHz. Fig. 3.17 shows $f_{MAG10dB}$ of 1.2 GHz for AlGaN and 1.4 GHz for InAlN. Production level AlGaN devices had f_T = 17.8 GHz and

$f_{MAG10dB}$ > 20 GHz. f_T and $f_{MAG10dB}$ were limited by gate capacitance in research level InAlN and AlGaN HEMTs, as evidenced by the scaling of cut-off frequency with gate-source separation in structures with inconsistent contact pattern definition. The high values recorded in the production level devices reflects the increased transconductance and lower gate capacitance (measured but not shown here) due to the larger and better confined channel current and shorter gate length, respectively. Both systems showed no evidence of oscillation with stability factors greater than unity above the 1 GHz range.

Pulsed-IV measurements of InAlN-SiN_x and AlGaN-SiN_x HEMTs were taken to assess the effect of gate- and drain-lag on device performance. I_d-V_d profiles with V_{gs} = 0 V were taken by pulsing from Q-points (V_{gs}, V_{ds}) of Q_{ref} = (0 V, 0 V), Q_{GL} = (-6 V, 0 V) and Q_{DL} = (-7 V, 25 V), using pulses of width 500 ns and with a duty cycle of 1%. The drain-lag current slump is defined as percentage decrease in I_{dss} when pulsed from Q_{ref} and Q_{DL} (Equation 3.3) and includes the contribution from trapping in both the HEMT barrier layer (including the barrier-SiN_x interface) and the bulk GaN, whereas the gate-lag current slump (Equation 3.4) discounts the latter channel component. Table 3.4 and Fig. 3.18 show the gate- and drain- lag current slump for InAlN-SiN_x and AlGaN-SiN_x HEMTs, defined by

$$\text{Drain lag current slump (\%)} = 100 \times [I_{dss}(Q_{ref})-I_{dss}(Q_{DL})]/I_{dss}(Q_{ref}) \quad (3.3)$$

$$\text{Gate lag current slump (\%)} = 100 \times [I_{dss}(Q_{ref})-I_{dss}(Q_{GL})]/I_{dss}(Q_{ref}) \quad (3.4)$$

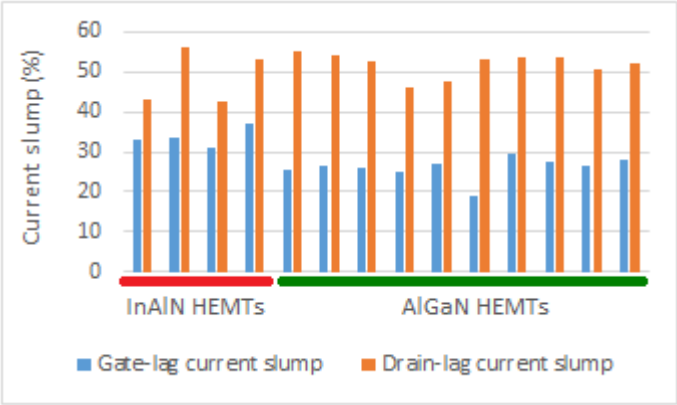

Fig. 3.18: Gate- and drain-lag current slump values for the InAlN-SiN_x and AlGaN-SiN_x HEMTs measured in this work

Table 3.4: Pulsed-IV measurement results

	Drain-lag current slump (%)	Gate-lag current slump (%)
InAlN-SiN_x	48.6 ± 7.1	33.8 ± 2.5
AlGaN-SiN_x	51.9 ± 2.9	26.1 ± 2.7

Both InAlN-SiN_x and AlGaN-SiN_x HEMTs measure an average drain-lag current slump of 50%, symptomatic of wide scale trapping in the bulk and barrier regions of the devices. The GaN buffers used here were unintentionally doped, and despite the elimination of the conducting channel at the substrate/buffer interface (Section 3.3) significant trapping behaviour is still apparent from the ratio of drain-lag to gate-lag current slump. Section 2.6.2 describes some of the techniques used to manage RF dispersion due to bulk GaN trapping via compensation doping.

The higher gate-lag current slump for InAlN-SiN_x compared to AlGaN-SiN_x correlates with the increased suppression of channel current when SiN_x capping is included in InAlN HEMTs compared to AlGaN, as seen in Table 3.3. This is evidence for carrier trapping within the barrier layer or at the barrier/SiN_x interface being primarily responsible for current collapse, with compression at high frequencies due to the non-negligible release times and resulting virtual gate effects. InAlN-SiN_x HEMTs are more susceptible than AlGaN-SiN_x, partly due to the decreased channel-surface separation in the former and electronic band properties as discussed in Section 6.2.

3.7 Chapter summary

In this chapter the III-nitride HEMT production methods and characterization techniques used in the remaining chapters of this thesis have been introduced. The physics behind III-nitride crystal growth by MOVPE was explained, and the usefulness and limitations of the process were explained; this provides context for the results presented in Chapter 4. III-nitride HEMTs were confirmed to be capable of RF gain, and the DC performance that is referenced throughout Chapter 5 within the context of device reliability is presented.

The baseline device fabrication process has been introduced, which is modified in Chapter 6 in order to optimise InAlN and AlGaN HEMT performance.

4. Optimisation of MOVPE of InAlN/GaN and AlGaN/GaN heterostructures

This chapter explores the use of MOVPE to produce InAlN/GaN and AlGaN/GaN heterostructures for use in HEMTs, as described in Chapter 3. The two material systems require a different approach due to the contrasting growth conditions necessary to produce high quality epilayers. The importance of an optimised crystal growth process cannot be overstated if maximum device performance and reliability is to be achieved, as will become evident in Chapters 5 and 6.

4.1 AlGaN HEMT heterostructures

In order to fully appreciate the challenges associated with MOVPE of epistructures for InAlN HEMTs within the broader context of III-nitride growth, a study of AlGaN/GaN heterostructures was undertaken. In AlGaN/GaN heterostructures, unlike lattice matched $In_{0.18}Al_{0.82}N$/GaN heterostructures In-plane strain across the heterojunction results in a critical thickness depending on $Al_xGa_{1-x}N$ barrier layer alloy content[228-230]. Beyond the critical thickness strain relaxation diminishes the piezoelectric polarisation component reducing the 2DEG carrier density[231], and suppresses mobility through the introduction of scattering from defect centres[232], degrading device performance and stability[233]. Redistribution of strain has been reported to manifest as surface features on the wafer surface on the micro- and nanoscale[234, 235]. Microscale cracking is well established to be highly detrimental to HEMT channel sheet resistance, and is reported to occur during initial MOVPE stages if strain resulting from the lattice mismatch to the substrate is not properly managed[236]. Nanoscale fissures may occur during MOVPE, particularly during cooling to room temperature from growth temperatures of greater than 1000°C.

Cooling of MOVPE reactors after AlGaN/GaN growth conventionally takes place under NH_3 and H_2 flows identical to those used during deposition, where it acts as a carrier gas

to deliver reaction precursors to the chamber. However, it has been reported that the appearance of nanoscale fissures is influenced by barrier layer carrier gas and growth temperature[237, 238], with hydrogen etching during cooldown playing a critical role. GaN-based materials can experience desorption under certain conditions[173], which is compatible with fissure formation emanating from dislocation cores. GaN capping is reported to prevent nanoscale fissure nucleation[239], presumably through redistribution of epitaxial strain[240], although adding a capping layer potentially adds complexity to the device fabrication process through the need to make electrical contact.

Nanoscale fissures formed after MOVPE cooling result in minor changes to 2DEG density and mobility, attributed to partial lattice relaxation and the associated alleviation of interfacial roughness scattering in previous works[238]. However, a strong relationship between abrupt device failure and nanoscale formation is reported[241] in devices subject to intense or long term stress due to the inverse piezoelectric effect[242], appearing independently to pits that cause gradual performance degradation[243]. The mechanisms linking AlGaN/GaN heterostructure surface features and 2DEG electrical characteristics require further investigation to better understand AlGaN HEMTs and further improve performance and reliability.

AlGaN/GaN surfaces can be imaged in a number of ways. Differential interference contrast optical (also called Nomarski) microscopy can detect large scale cracking and surface morphology features down to the diffraction limit. Atomic force microscopy (AFM) can achieve nanoscale lateral resolution and resolve local height differences at the atomic level. Electron channelling contrast imaging (ECCI) is an electron microscopy diffraction technique used to enhance contrast, used to analyse nano- and micro-scale features as well as dislocation types and position. ECCI measurements indicate the nanoscale fissure formation during the MOVPE cooling stage is related to threading dislocations[239], which are known to act as stress centres[234]. The effect of surface fissures on Ti/Al/Ni/Au Ohmic contact formation is explored in Section 6.1.2.

$Al_xGa_{1-x}N$/GaN epitaxial heterostructures described in this study were grown by MOVPE using an AIXTRON 3x2” close-coupled showerhead reactor. Sapphire substrates with AlN

layer templates were used. The group-III precursors were trimethylgallium (TMGa) and trimethylaluminium (TMAl) and the combined flow was kept constant at 60 µmol/min (based on previous internal optimization of generic AlGaN epilayers), with relative TMGa and TMAl flows varied to modify $Al_xGa_{1-x}N$ alloy composition. The V/III ratio was kept constant at 781, with an ammonia precursor flow of 46.9 mmol/min. All samples were grown under H_2 carrier gas, and the growth pressure and temperature were constant at 150 mbar and 1025°C, respectively, with in-situ reflectometry used to provide real-time monitoring of growth conditions. Following a GaN buffer layer growth of 1 µm, AlGaN barrier layers were deposited with a target thickness of 15 nm, chosen to achieve low contact resistance while maintaining a reasonable 2DEG density against surface recombination. Upon completion of wafer growth samples were cooled under NH_3 gas flow with either H_2 or N_2 forming the remainder of the total reactor flow.

Table 4.1. Barrier layer Al content for $Al_xGa_{1-x}N/GaN$ heterostructures cooled in NH_3 and either H_2 or N_2

	Cooled under NH_3 +	Barrier thickness (nm)	Barrier layer Al content
Sample-HA	H_2	9	18%
Sample-HB	H_2	17	24%
Sample-HC	H_2	13	32%
Sample-HD	H_2	12	35%
Sample-NA	N_2	15	20%
Sample-NB	N_2	16	28%
Sample-NC	N_2	15	35%
Sample-ND	N_2	12	37%

Epilayer alloy composition and thickness was determined from analysis of (0002) ω-2θ X-ray diffraction (XRD) scans. AlGaN epilayer strain relative to the underlying GaN was measured using reciprocal space mapping (RSM, see Section 3.2.1) from (10-15) 2θ scans. Nanoscale surface was imaged using tapping-mode AFM[180], in which the force interaction between the tip and sample surface at the probing frequency (typically

around 75 kHz) is such that phase is proportional to local elastic stiffness[181-183]. Hence in addition to surface morphology mapping, including features such as pits due to threading dislocations, analysis of AFM tip phase can potentially be used to generate a map of lattice strain distribution or composition variation[184, 185]. ECCI exploits the diffraction properties of electrons that causes them to channel through the lattice, depending on the crystallographic orientation. Electrons can be made to channel with respect to a single orientation, resulting in dislocations of different types being visible and identifiable due to their specific contrast variations[244]. Nanoscale fissures may be identified using the same principle, and the location and density of dislocations and nanoscale fissures are compared in layers grown under different conditions.

Hall/van der Pauw measurements were used to determine sheet resistance (R_{sh}), sheet carrier density (n_{sh}) and mobility (μ) (see Section 3.2.2). Circular TLM (CTLM) features[245] were evaluated to determine contact resistance and confirm sheet resistance as determined from Hall measurement. CTLM electrical contacts were fabricated through evaporation of annealed Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) stacks where the fabrication process was required to be optimised depending on the epilayer under investigation as discussed in Section 6.1.2.

The samples examined in this work are listed in Table 4.1. Compositions were determined from XRD (0002) ω-2ϑ scans, with Pendollösung fringes used to confirm barrier thickness, and RSM analysis showing no evidence of measurable strain relaxation (Fig. 4.1, see Section 3.2.1). Nomarski microscopy inspection of all AlGaN/GaN wafers revealed generally smooth layers irrespective of cooling, with no evidence of cracking in the epitaxy even for the highest Al compositions studied, indicating that ~ 15 nm was below the critical thickness for large scale (micro) crack formation throughout this study.

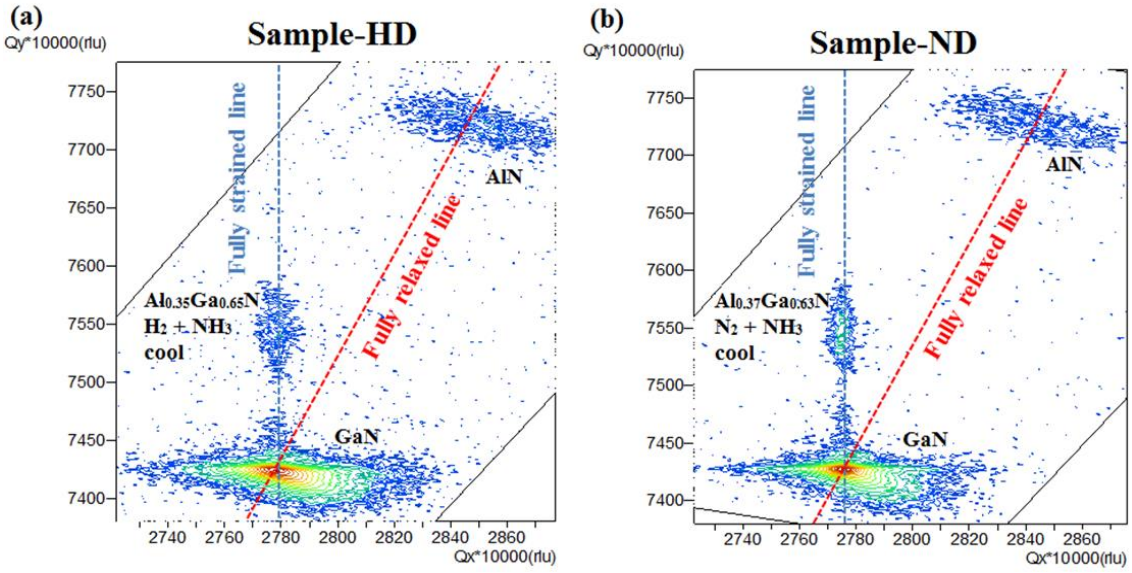

Fig. 4.1: Reciprocal space map of (a) Sample-HD and (b) Sample-ND, AlGaN/GaN heterostructure grown by MOVPE with the relaxed AlN nucleation layer for reference, with the AlGaN mostly strained to the GaN channel in both cases

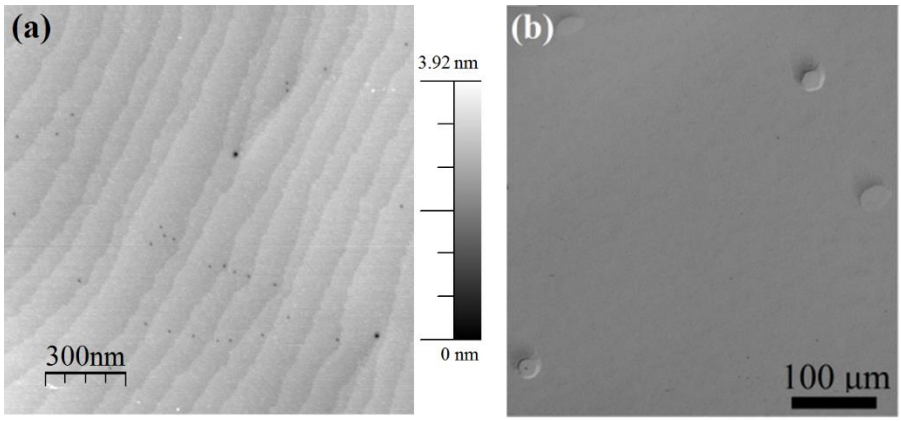

Fig. 4.2: (a) AFM surface of GaN buffer layer and (b) Nomarksi microscopy image of AlGaN/GaN Sample-HD

Fig. 4.3 shows 1.5 x 1.5 μm^2 AFM surface morphology scans of the $Al_xGa_{1-x}N$/GaN heterostructures. A GaN surface is shown in Fig.4.2(a) for comparison, and a Nomarski microscopy surface image of AlGaN/GaN Sample-HD is shown in Fig 4.2(b). There are clear differences in the AlGaN surface morphologies observed as a result of sample cooling in NH_3 and either H_2 or N_2 atmospheres, with the exception of the highest Al

content layer (Sample-ND, Fig. 4.3(h)). A step like morphology is observed for cooling under nitrogen with screw dislocations clearly visible at step edge terminations, most clearly observed for Sample-NA in Fig. 4.3(b). In contrast, a rapid development of very small fissure-like features (Fig. 4.3(a)) to a high density of elongated nanoscale fissures is found as the barrier layer Al content increases for those cooled under hydrogen. This suggests that cooling in a hydrogen atmosphere leads to preferential etching with the initial desorption sites being linked to threading dislocation sites, as observed elsewhere[235]. The behaviour of the high Al content sample in cooled under nitrogen (Fig. 4.3(h)) is clearly a departure from the lower Al content samples in terms of surface morphology. Given the dramatic change a repeat growth was performed on this sample, leading to the same result. It is unclear if this relates to rapid material redistribution during cooling, or the exceeding of some critical threshold for roughening during growth. It was noted in this sample that “pits” were located close to the boundary of steps, which may be associated with edge dislocations.

AFM-tip phase maps of the samples depicted in Fig 4.3 are shown in Fig 4.4. Relating the tip phase to elastic rigidity we can infer a local distribution of stiffness arising from lattice distortion. In samples cooled under nitrogen moderate build-up is observed, confined to step edges (Fig. 4.4(b)) increasing sharply in areas with advanced proliferation of step-bunching (Fig. 4.4(h)). In samples cooled under hydrogen a local stiffness distribution emanates from boundaries between smooth regions and extended pit/fissure boundaries, possibly suggesting the material adjacent to fissures is highly defective, has undergone partial strain relaxation or has a different alloy composition to areas not influenced by fissures. The latter case is ruled out by Fig. 4.1 in which Sample-HD and Sample-ND share the same average Qx and Qy value (i.e. a-plane and c-plane lattice parameter, respectively) in RSM, although the slightly broader Qx signal of Sample-HD compared Sample-ND is evidence for a less coherent crystal at the surface.

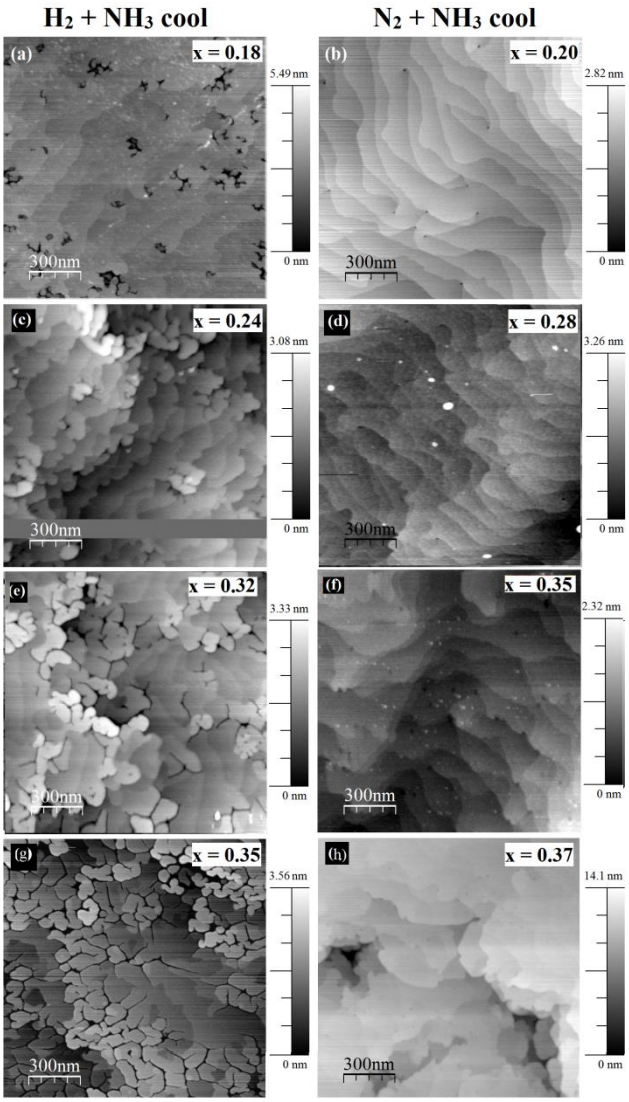

Fig. 4.3: 1.5 x 1.5 µm² AFM surface scans of $Al_xGa_{1-x}N$ epilayers (a) Sample-HA, x = 0.18, H_2 cool, (b) Sample NA, x = 0.2, N_2 cool, (c) Sample-HB, x = 0.24, H_2 cool (d) Sample-NB x = 0.28, N_2 cool (e) Sample HC, x = 0.32, H_2 cool (f) Sample-NC, x = 0.35, N_2 cool (g) Sample HD, x = 0.35, H_2 cool (h) Sample-ND, x = 0.37, N_2 cool

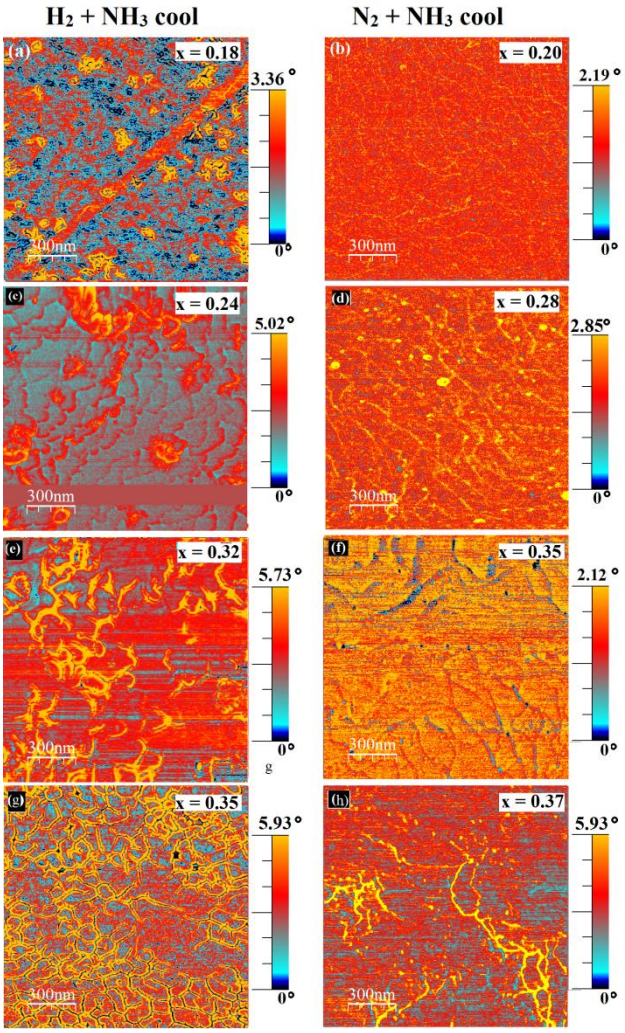

Fig. 4.4: 1.5 x 1.5 µm² AFM tip phase maps of ~ 15 nm $Al_xGa_{1-x}N$ epilayers (a) Sample-HA, x = 0.18, H_2 cool, (b) Sample NA, x = 0.2, N_2 cool, (c) Sample-HB, x = 0.24, H_2 cool (d) Sample-NB x = 0.28, N_2 cool (e) Sample HC, x = 0.32, H_2 cool (f) Sample-NC, x = 0.35, N_2 cool (g) Sample HD, x = 0.35, H_2 cool (h) Sample-ND, x = 0.37, N_2 cool

It should be noted that the phase contrast in Fig. 4.4 is low and the methods linking AFM phase to stiffness and stiffness to small-scale lattice relaxation are not well established. It is conjectured that in this case the AFM phase mapping cannot be used to confidently state there is a difference in the material composition, strain or defect density. The technique is however promising and holds potential for future use in increasing the AFM image contrast, and in the future may be used with confidence for the reasons outlined in this work once calibration has been achieved using surfaces with deep, nanometer-scale width features with known strain and composition.

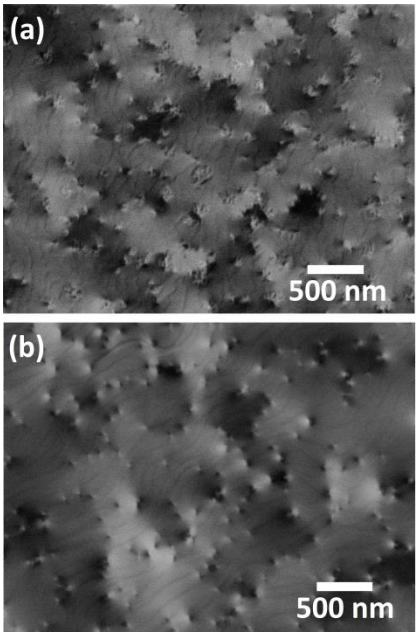

Fig. 4.5: ECCI of $Al_xGa_{1-x}N$ epilayers (a) Sample-HA, x = 0.18, H_2 cool (b) Sample NA, x = 0.2, N_2 cool

Fig. 4.5 shows ECC images for AlGaN barrier layers with x ~ 0.2 cooled under NH_3 and either H_2 or N_2. The majority of fissures in Sample-HA (Fig. 4.5(a)) are located on sub-grain boundaries and are assumed to be associated with dislocations. The density of fissures is of order 3 $x10^9$ cm^{-2}, in broad agreement with the AFM scan in Fig. 4.4(a). For Sample-NA no cracks are observed and dislocations are revealed with the characteristic black-white contrast (Fig 4.5(b)). The dislocation density is of order 2 $x10^9$ cm^{-2} with a ratio of pure edge dislocations to dislocations with a screw component (i.e. screw or mixed type dislocations) of around 2:1. This correlates with the screw type dislocation density in Fig. 4.3(b), identified by their position at double step terminations, with edge type dislocations not visible in AFM for $Al_xGa_{1-x}N$ barrier layer Al content until x ~ 0.37 (Fig. 4.3(f)) but clearly detectable in ECCI.

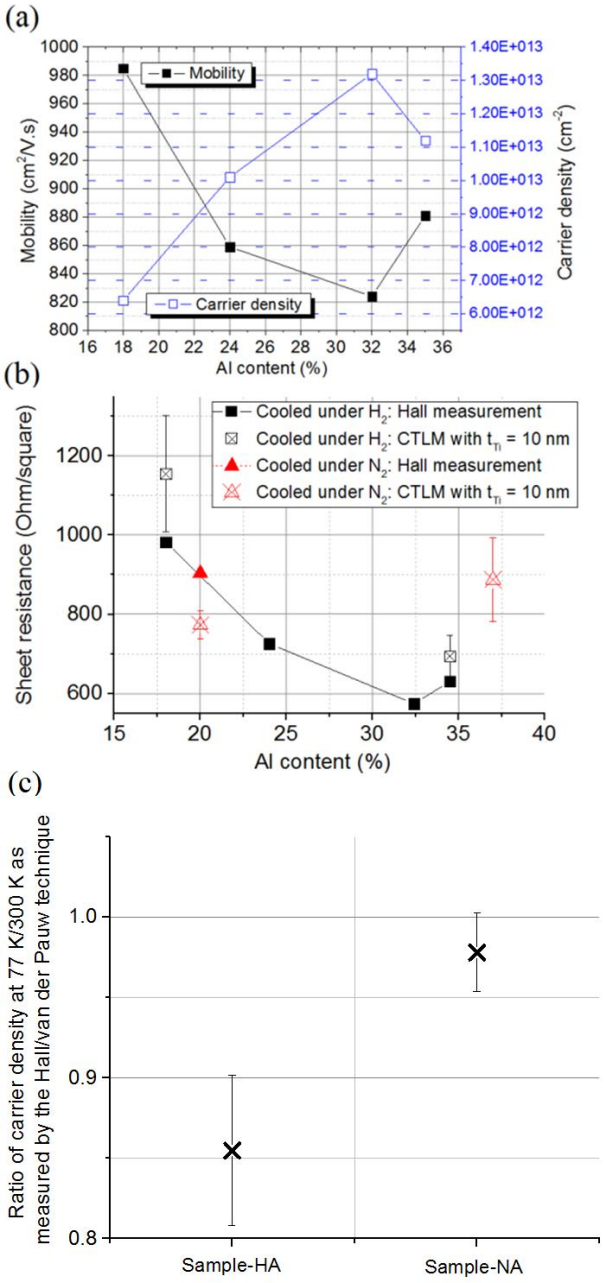

FIG 4.6: (a) Hall measurement data from $Al_xGa_{1-x}N$/GaN heterostructures grown by MOVPE and cooled under H_2 and NH_3 (b) sheet resistance as measured by Hall and CTLM for cooling after growth under NH_3 and N_2 or H_2 (c) ratio of Hall carrier density at 77 K to when at room temperature

Electrical properties from Hall measurement of the $Al_xGa_{1-x}N$/GaN heterostructures cooled under H_2 are shown in Fig. 4.6(a). An increase in carrier density with barrier layer Al content up to $x = 0.32$ is consistent with the expected increase piezoelectric polarisation charge at the heterojunction due to increased strain. The reduction at

x = 0.35 (Sample-HD) is more than can be accounted for by barrier layer thickness variation (only 1 nm, see Table 4.1), and correlates with a break in the trend of mobility reducing with Al content. This increase in mobility at x = 0.35 (Sample-HD) correlates with a reduction in rms roughness compared to at x = 0.32 (Sample-HC), with regions between fissures becoming smoother with increased fissure development. This is consistent with a general decrease in mobility with surface roughness as is the case in Fig. 4.6(a). The structural reordering evidently does not involve measurable lattice relaxation as evidenced by the RSM in Fig. 4.1(b) suggesting reduction of the piezoelectric polarisation component is not the main cause of the drop in carrier density, and rather the existence of shallow traps presumably associated with the nanoscale fissures. A Hall measurement of the samples cooled under N_2 was not possible due to difficulty in forming Ohmic contacts via the In dot method, with only the low Al content Sample-NA measureable. Mobility and carrier concentrations for Sample-NA were similar to those measured for Sample-HA, with similar barrier layer Al concentration.

Sheet resistance as measured by the Hall technique was confirmed by CTLM evaluation with Ti/Al/Ni/Au (10/50/50/50 nm) contacts as shown in Fig. 4.6(b). A slight systematic increase may be attributed to end-resistance effects in CTLM[246] and possible structural damage to the epilayer during contact annealing, although this was not observed for Sample-NA. Samples cooled under H_2 and NH_3 generally show a decrease in sheet resistance with increasing barrier layer Al content, consistent with the rise in Hall sheet carrier concentration. Sample-NA, cooled under N_2 and NH_3 with 20% barrier Al content, exhibited low contact resistivity and sheet resistance. The sheet resistance for Sample-ND at x = 0.37 was somewhat higher than for Sample-HD, which is likely an effect of the roughening identified in Fig. 4.3(h). The greater reduction in carrier density at 77 K for Sample-HA compared to Sample-NA in Fig. 4.6(c) is further evidence for the existence of shallow traps associated with the nanoscale fissures (see Section 2.3.1), which will be shown to have an effect on fabricated device contact formation and thermal stability in Section 6.1.2.

In conclusion, structural and electrical properties of $Al_xGa_{1-x}N$/GaN heterostructures grown by MOVPE and cooled under NH_3 and either N_2 or H_2 were evaluated. No

measureable strain relaxation was detected up to x = 0.37 under either cool down condition, and nanoscale crack formation was observed only in epilayers cooled under H_2. Fissure density increased with barrier layer Al content and they were linked to structural reordering in response to 3-dimensional growth and etching from dislocation centres. Compared to fissure-free samples, those with nanoscale fissures showed instability with regard to carrier density, associated with shallow trap formation in defect-rich areas around fissure boundaries[45]. The effect of nanoscale surface fissures on Ohmic contact formation is explored in Section 6.1.2.

4.2 InAlN HEMT heterostructures

As described in Chapter 2, lattice matched InAlN/GaN heterostructures offer performance and reliability advantages over AlGaN/GaN. Table 3.1 highlights the additional challenges associated with MOVPE of InAlN barrier layers, and remained of this chapter aims to provide an overview of the practical steps taken to identify and implement routes to optimisation.

4.2.1 AlN interlayers in InAlN HEMT heterostructures

As described in Section 2.6.1 an AlN interlayer (IL) between the GaN buffer and AlGaN (or InAlN) barrier layer can improve HEMT performance. Table 4.2 shows the increase in fissure-free AlGaN/GaN heterostructure DC conduction properties at room temperature upon the inclusion of a 1 nm AlN IL. A clear improvement is noted, and optimization of the AlN IL is therefore a critical growth parameter for minimizing channel resistance.

It is reported that AlN ILs can also act as a growth barrier in MOVPE preparation of InAlN/GaN heterostructures, by protecting the underlying GaN from potential decomposition when the growth conditions are switched to those required for good quality InAlN growth[247]. With the effect of 1 nm AlN IL on improving AlGaN HEMT heterostructure channel conduction characteristics as demonstrated in Table 4.2, AlN IL

growth conditions were varied in InAlN HEMT heterostructures. Interlayers were imaged as they would appear prior to InAlN barrier layer deposition using AFM scans undertaken immediately after growth. Surface morphologies and subsequent heterostructure conductivity suggested minimum on-resistance can be achieved by balancing the underlying GaN channel decomposition and interfacial roughening when deciding AlN interlayer growth parameters on a sapphire substrate of a given miscut.

Table 4.2: Hall measurement results for AlGaN/GaN heterostructures showing the effect of a 1 nm AlN IL with layer thicknesses measured by XRD

Sample	**2DEG density (x 10^{13} cm^{-2})**	**Mobility (cm^2/V.s)**	**Sheet resistance (Ω/□)**
$Al_{0.2}Ga_{0.8}N$/GaN (20/1000 nm)	1.4	1121	386
$Al_{0.2}Ga_{0.8}N$/AlN/GaN (20/1/1000 nm)	1.6	1258	308

The literature suggests the optimal thickness of a single AlN layer to be ~ 1 nm[18, 107, 108] which was the nominal thickness used in this assessment, assuming a linear growth rate based on bulk (~ 1 µm) AlN calibration layers. A nominal 1 nm AlN/10nm GaN superlattice grown under similar conditions was analysed using XRD, indicating the AlN thickness may be slightly thinner than that estimated from growth rates, at around 0.7 nm. A slightly thinner AlN layer will act to enhance the decomposition mechanisms discussed later in this chapter. The temperature during the AlN deposition is fixed to be the same as that of GaN (1060°C); higher temperature is preferable for good quality AlN, but increasing the temperature whilst the GaN surface remains exposed risks channel decomposition[108], increasing the sheet resistance uncontrollably.

Two remaining growth parameters are the V/III ratio and the substrate miscut, i.e., the angle between the surface of the sapphire substrate and the (0001) growth plane. 1 nm AlN /2 µm GaN layers were grown, with V/III ratios 100, 500, and 25,000 utilized during AlN deposition. c-plane sapphire substrates were used, miscut by either 0.1° or 0.4° toward the m-plane. GaN samples were prepared on sapphire substrates of each miscut and used as templates for subsequent growth of the GaN channel, AlN interlayers, and

InAlN barrier layers. Assuming no major electrical degradation from incorporated regrowth impurities at the buried interface (as indicated by evaluation of C-V characteristics), the GaN template surfaces may be regarded as exposed channel layers in a nitride HEMT.

Fig. 4.7(a) shows a 1 x 1 μm^2 AFM scan of a GaN template grown on sapphire with a miscut of 0.4°. It is typical of a MOVPE GaN-on-sapphire surface[168] —step flow growth is observed, characteristic of the moderate surface diffusion length of GaN and the initial stepping on the sapphire. Screw and mixed type dislocations terminate steps and manifest as nm-scale pits at a density of around 10^9 cm^{-2}, estimated from XRD ω-2ϑ scans (see Section 3.2.1). The GaN surface rms surface roughness from AFM is around 0.8 ± 0.3 nm.

After the AlN layers were deposited, the wafers were brought back to room temperature in a N_2 ambient atmosphere with an ammonia flow mimicking that of InAlN barrier layer deposition. Fig. 4.7(b)–4.7(d) show AlN interlayer AFM scans for various V/III ratio and substrate miscut configurations. AlN is known to exhibit “step-bunching” when grown via MOVPE on GaN (i.e. growth instabilities linked to the accumulation of AlN adatoms at step eges due to their low surface diffusion length and non-uniform adatom incorporation), exaggerating the step flow pattern on the underlying GaN, evident in Fig. 4.7.

Fig. 4.7(b) and 4.7(d) provide some insight into the genesis of this process as a function of growth parameters—increasing the V/III ratio from 500 to 25,000 on samples on substrates with the same miscut appears to encourage the step-bunching, evidenced by the loss of regularity in step spacing and direction and resulting in bunches of step edges occurring more frequently in Fig. 4.7(d) than 4.7(b). This is due to the reduction of the surface diffusion length with increasing ammonia concentration, where AlN adatoms accumulate at step edges, thus departing from the underlying morphology of the GaN channel layer.

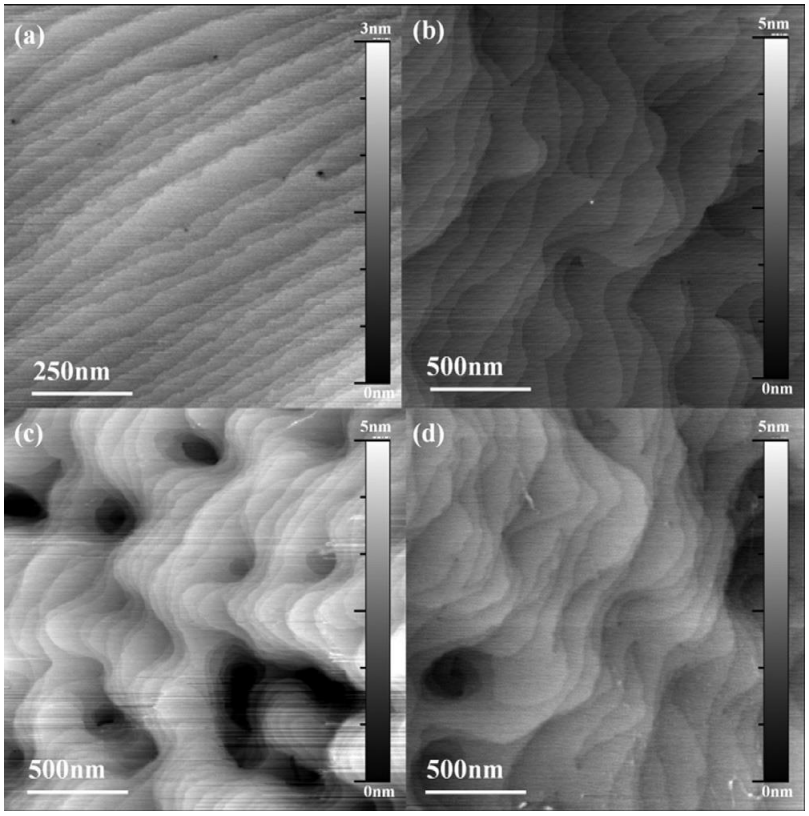

Fig. 4.7. AFM surface images of (a) a bulk GaN surface, (b) 1 nm AlN on GaN at V/III ratio = 500 on 0.4° miscut sapphire (c) 1 nm AlN V/III ratio = 500 on 0.1° miscut sapphire, and (d) 1 nm AlN V/III ratio = 25 000 on 0.4° miscut sapphire.

Samples grown on 0.4° miscut sapphire are expected to show more step-bunching behaviour than those on the 0.1° miscut substrates due to the geometry dictating an increased number of initial steps on the former; Fig. 4.7(b) and 4.7(c) demonstrate this. Roughness measurements across the AlN surfaces were made in areas excluding the large pits (see next paragraph), and did not show any variation in step height with increased V/III ratio (with atomic steps in all cases and rms surface roughnesses of between 0.6 and 1.4 nm).

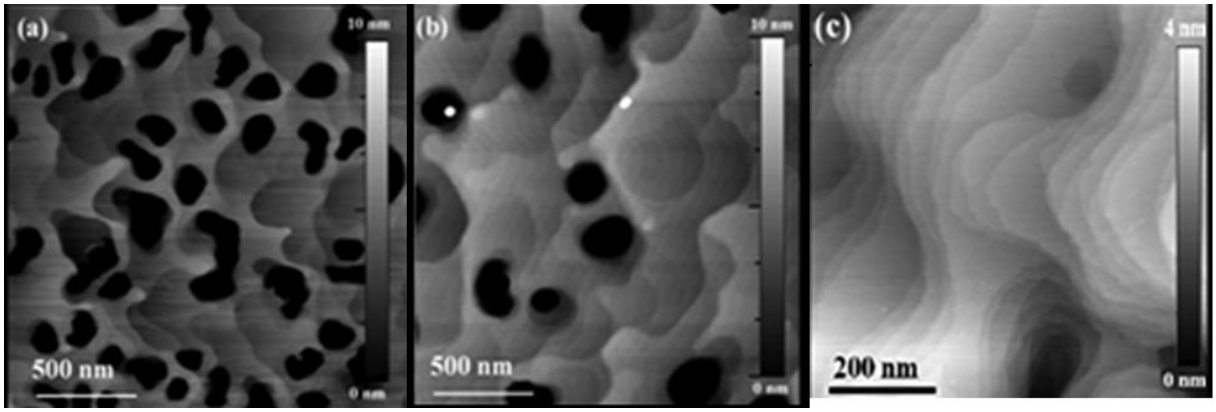

Fig. 4.8. AlN IL on GaN with (a) V/III ratio = 500, (b) V/III ratio = 2,500, and (c) V/III ratio = 25 000, deposited at 1060°C with AlN IL N_2 and ammonia flows maintained during the cool down stage.

The ammonia flow during the post-growth cooldown is a crucial parameter; without this stage, large pits are observed upon AFM surface analysis (~200 nm across and at least 20 nm deep). Fig. 4.8 displays such surfaces on 0.4° miscut sapphire substrates with different AlN V/III ratios utilized during growth—the pits extend well into the GaN through the partially deposited AlN layer. Their depth suggests they are the result of the GaN decomposition in an ammonia-poor environment, as does their decrease in number from ~12 μm^{-2} to~ 3 μm^{-2} for V/III = 500 and 2,500 in Fig. 4.8(a) and 4.8(b), respectively. The corresponding sample with V/III = 25,000 (Fig. 4.8(c)) had fewer pits at around 1 μm^{-2}, and had a roughness comparable to the surface in Fig. 4.7(d), which was grown identically except for the inclusion of the ammonia cool down phase. This supports the hypothesis that the pits may be suppressed by ensuring there is sufficient ammonia present during the cool down. We may attribute the large pit features in Fig. 4.7(b) and 4.7(c) to the same effect, i.e., decomposition of exposed GaN during the cool down phase prior to wafer extraction. Such roughness would be detrimental to HFET performance, and GaN decomposition must be considered when speculating on the quality of a heterojunction channel.

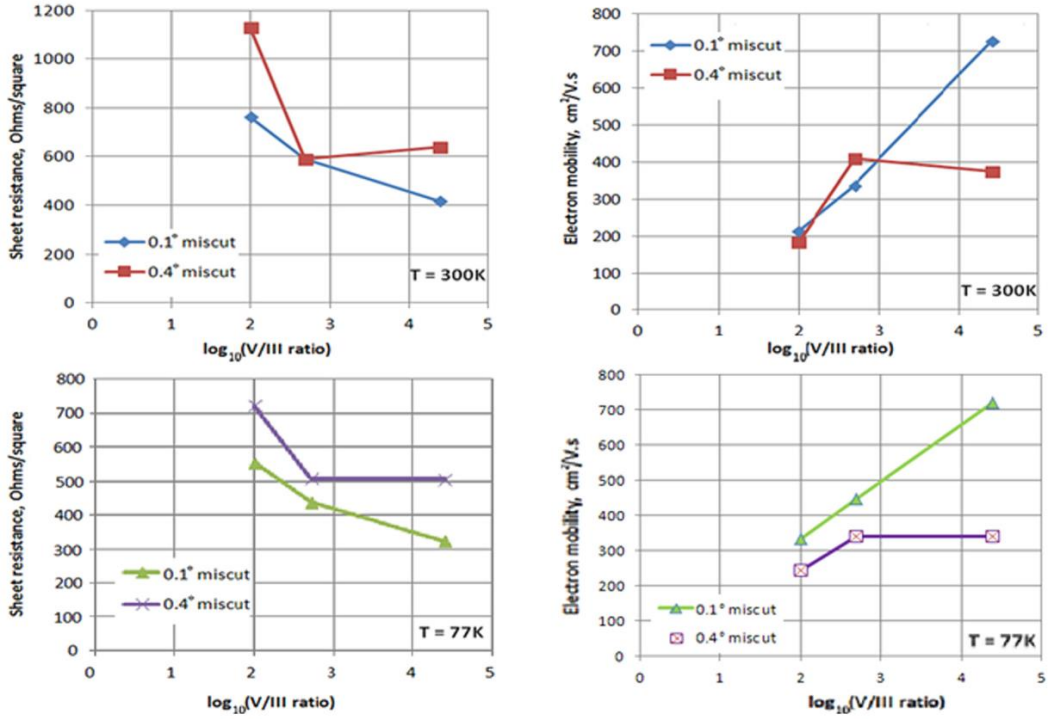

Fig. 4.9: Sheet resistance and electron mobility of InAlN/AlN/GaN heterostructures at 300K and 77 K as a function of AlN interlayer growth conditions.

Heterostructure DC performance obtained from Hall measurements across the series is displayed in Fig. 4.9. The growth process is identical to that of the exposed AlN IL samples with the inclusion of 10 nm of nominally lattice matched InAlN capping the structure acting as a barrier layer, with growth temperature/composition calibration performed on bulk layers immediately prior. The samples grown on 0.1° miscut sapphire show a clear increase in channel mobility, and consequential reduction in sheet resistance, at room temperature with increased V/III ratio, attributed to a higher quality GaN channel and uniform AlN interlayer which itself stems from the original surface morphology (i.e. that of the substrate) being smoother. Structures grown on the 0.4° sapphire show a room temperature sheet resistance of ~ 590 Ω/□ at V/III = 500 (roughly the same as on the 0.1° miscut substrate) but an increase up to ~ 640 Ω/□ at V/III = 25,000; in this configuration interfacial scattering caused by AlN step-bunching inhibits the channel mobility, overcoming the benefits of the high quality underlying GaN and representing the importance of considering the multiple physical mechanisms

active in AlN interlayer deposition. Notably, there is a clear reduction in sheet resistance with V/III ratio for the samples on the 0.1° miscut sapphire without any significant variation in the surface rms roughness, but with a clearly visible change in step spacing and direction. This result was confirmed with 77 K Hall measurements, also displayed in Fig. 4.9, where phonon scattering is suppressed and the roughness scattering mechanisms are more dominant. The 2DEG concentration was found not to vary significantly across either series. The similarity of the 77 K and room temperature mobility measurements confirms the channel resistances are dominated by interfacial roughness and not thermal phonon scattering, which suggests further optimisation is still required.

In conclusion, AlN interlayers for InAlN/GaN HEMT heterostructures were grown on sapphire substrates of different miscuts and with different V/III ratios and directly imaged AFM. Subsequent heterostructure conductivity suggests reduced on-resistance may be achieved by balancing GaN channel decomposition and interfacial roughening when considering AlN interlayer growth conditions on a sapphire substrate of a given miscut. AlN surfaces that most closely resemble the underlying GaN reference sample produce samples with the lowest sheet resistance, as these layers have the most uniform thickness and hence the least amount of roughness scattering. Further improvements to optimise the narrow AlN growth window look to be required.

4.2.2 Reducing the InAlN barrier layer thickness

As mentioned in Section 2.2, an advantage of the InAlN system as a barrier layer is the ability to reduce the thickness and improve DC and RF performance without depleting the 2DEG of carriers, to a greater degree than in AlGaN. State-of-the-art InAlN HEMTs typically utilize barrier layers of thicknesses around 5 nm in order to take advantage of the improved gate-control over the channel[17,18,101]. Reducing the nominal InAlN barrier thickness from 10 nm to 5 nm, keeping the AlN IL thickness at 1 nm, acted to degrade channel conductivity as described in Table 4.3.

Table 4.3. Hall measurement results for InAlN/AlN/GaN heterostructures showing the effect of a reduced InAlN barrier thickness, with barrier layer thicknesses measured by XRD

Sample	**2DEG density ($x10^{13}$ cm^{-2})**	**Mobility ($cm^2/V.s$)**	**Sheet resistance (Ω/□)**
$In_{0.18}Al_{0.82}N$/AlN/GaN (9/1/1000 nm)	1.4	858	519
$In_{0.18}Al_{0.82}N$/AlN/GaN (5/1/1000 nm)	0.6	455	2206

Analysis of surface features by AFM of the samples described in Table 4.3 are shown in Fig. 4.10. The hillock features observed in both samples are characteristic of InAlN surfaces, caused by the different surface diffusion lengths and incorporation rates of InN and AlN adatoms. A reduced threading dislocation pit density in Fig. 4.10(c) compared to Fig. 4.10(d) (t_{InAlN} = 9 nm c.f. 5 nm) did not appear to significantly degrade channel conduction properties. For the 5 nm barrier InAlN layer a surface morphology feature on a scale of approximately 1 µm is evident on the surface, not present for the 9 nm layer, observable in both the 1.5 x 1.5 μm^2 AFM scans in Fig. 4.10(c) and (d) and the 10 x 10 μm^2 AFM scans in Fig. 4.10(a) and (b). Despite a reduced average individual hillock height (of order 1 nm at t_{InAlN} = 9 nm c.f. 0.5 nm at t_{InAlN} = 5 nm) the µm-scale roughness acted to increase the rms roughness (Fig. 4.10(e) and 4.10(f)). Assuming the GaN buffer/channel layer morphology is the same in both samples (reasonable as growth conditions were the same), the degradation of mobility may then be attributed to increased Coulombic scattering resulting from variation in the effective 2DEG-surface separation. A reduced 2DEG density is expected with decreasing InAlN barrier thickness, although not to the extent as described in Table 4.3 for such a moderate decrease in nominal thickness. Rather it is proposed that the conduction characteristics obtained via Hall measurement are dominated by the regions with the smallest 2DEG-surface separation, i.e. the lowest 2-dimensional carrier density. Ref[248] shows how interfacial roughness modelled as 'islands' of potential energy mounds can give good agreement with mobility at room temperature, consistent with this model as the measured sheet resistance is the product of carrier density and mobility, as in Equation 2.2 in Section 2.3.

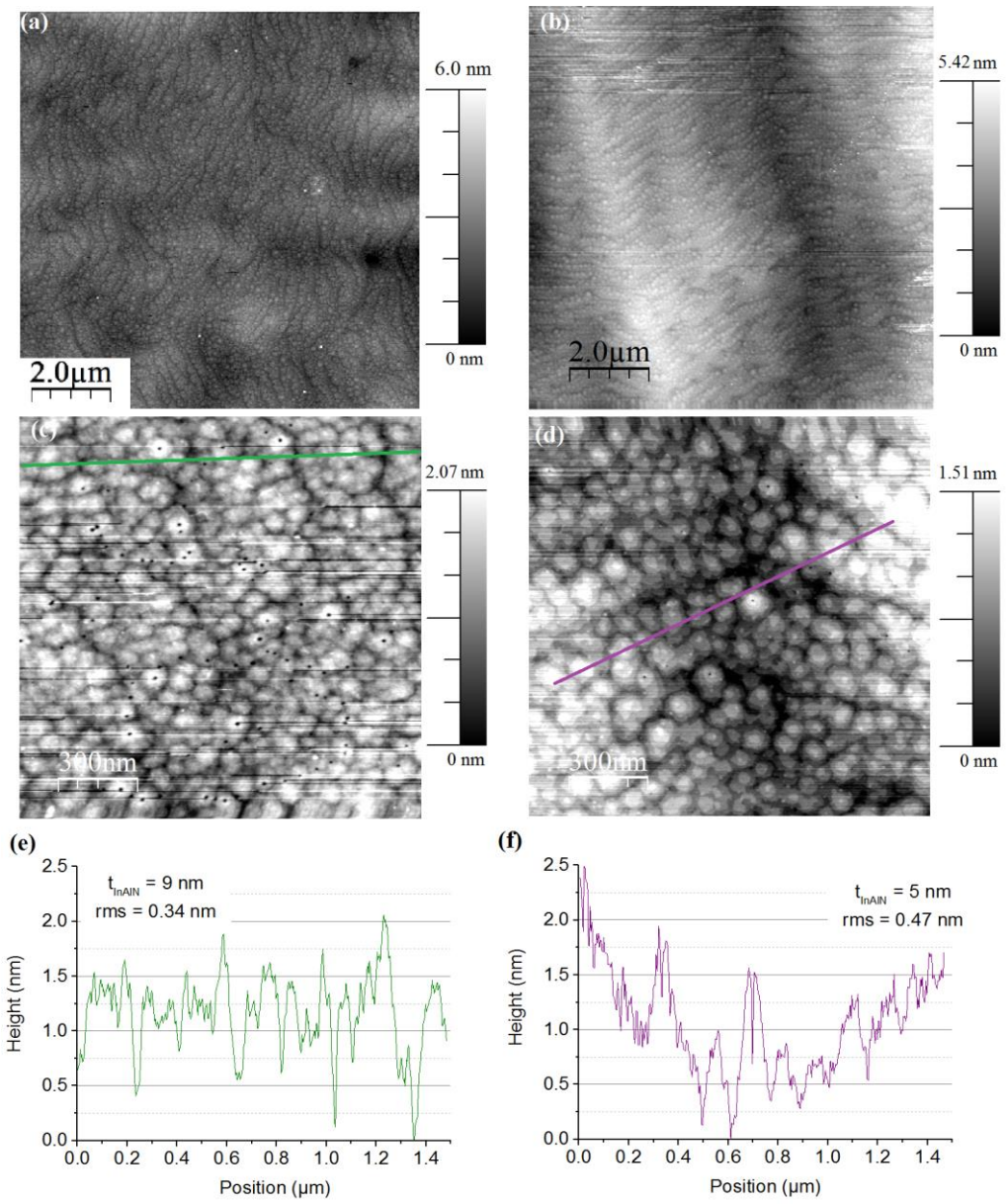

Fig. 4.10: AFM surface scans of InAlN/AlN/GaN heterostructures with (a) t_{InAlN} = 9 nm, 10 x 10 µm² scan and (b) t_{InAlN} = 5 nm, 10 x 10 µm² scan, (c) t_{InAlN} = 9 nm, 1.5 x 1.5 µm² scan and (d) t_{InAlN} = 5 nm, 1.5 x 1.5 µm² scan with corresponding surface profile plots in (c) and (d), respectively

It is speculated that the roughening on the 5 nm InAlN barrier layer surface is due to structural reorganisation in accordance with stress differentials across the barrier/buffer boundary arising due to the different thermal expansion coefficients of AlN, GaN, InN and the associated alloys. Further to this it is thought an increased InAlN barrier

thickness stabilises the system against deformation due to a smoothing out of the stress field into the additional barrier layer material.

To test this hypothesis the AlN IL was grown at different stages relative to the temperature ramp from GaN buffer conditions (T_{GaN} = 1060°C) to those required for InAlN barrier layers with compositions fulfilling the lattice matched condition (T_{InAlN} = ~ 780°C). Depositing the AlN IL after the ramp to T_{InAlN} risks exposing the GaN channel to conditions that encourage desorption and decreasing the crystalline quality of the AlN itself although it eliminates the possibility of structural reorganisation due to the temperature reduction to values required for InAlN.

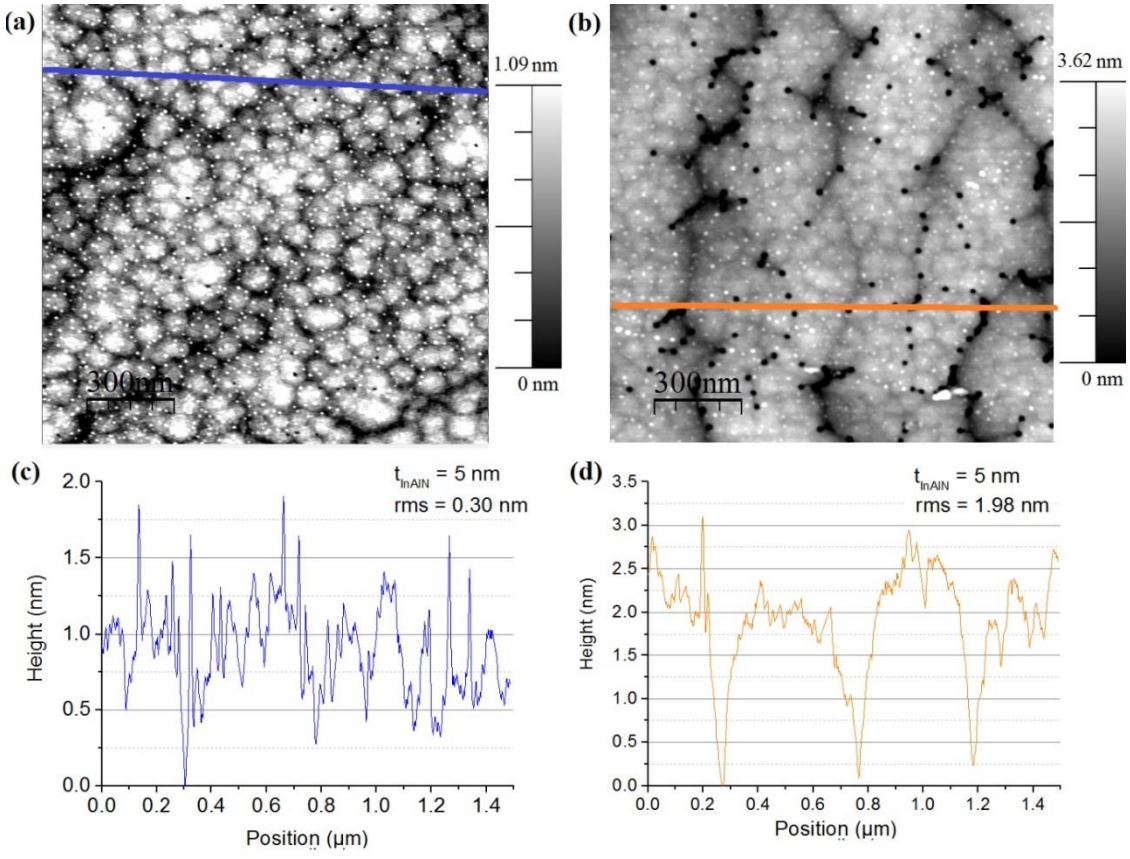

Fig. 4.11: 1.5 x 1.5 µm² AFM surface scans of InAlN/AlN/GaN heterostructures with (a) ramp to T_{InAlN} immediately upon completion of the GaN channel and prior to AlN IL depositon and (b) ramp to T_{InAlN} during GaN channel growth, with corresponding surface profile plots in (c) and (d), respectively

Fig. 4.11 shows AFM surface images of InAlN HEMTs identical to that shown in Fig. 4.10(b) and (d), with the exception of the AlN IL being grown immediately prior to

InAlN deposition at T_{InAlN}. In Fig. 4.11(a) the ramp to T_{InAlN} occurs after the completion of GaN channel growth, i.e. after TMGa precursor flow is ceased. In Fig. 4.11(b) the temperature is ramped from T_{GaN} to T_{InAlN} during the final 100 nm of GaN channel growth, with the switch to N_2 carrier gas immediately prior to the temperature ramp to allow for continuous growth of the AlN IL and InAlN barrier upon completion of the ramp to T_{InAlN}.

In Fig. 4.11(a), with the ramp to T_{InAlN} immediately upon completion of the GaN channel and prior to AlN IL deposition the µm-scale roughness is not present, with the layer benefitting from the reduced hillock height associated with thinner layers in terms of rms roughness (Fig. 4.11(c)). In Fig. 4.11(b), where the ramp to T_{InAlN} takes place during GaN growth, a significantly increased pit density is observed. The µm-scale roughness features are not present although hillocks appear to line up with areas with high dislocation densities forming ~ 2 nm trenches that span the several tens of µm across the wafer.

A comparison of the electrical properties of InAlN/AlN/GaN (5/1/1000 nm) with AlN interlayers deposited at different stages is shown in Fig. 4.12. Clearly GaN channel growth during the ramp to T_{InAlN} acts to collapse mobility, presumably due to extensive scattering from the defect centres associated with the high pit density seen in Fig. 4.11(b). Similarly the greater reduction in carrier density at 77K compared to room temperature (Fig. 4.12(d)) is attributed to a proliferation of shallow traps associated with the same defect centres[45] (see Section 2.3.1).

Samples with the ramp to T_{InAlN} immediately prior to AlN IL growth (with the smooth surface as in Fig. 4.11(a)) exhibit the highest mobility (Fig. 4.12(f)), strengthening the link between surface roughness and channel resistance. Furthermore the ratio of mobility at 77 K to that at room temperature scales with the absolute value of mobility itself, confirming scattering via interfacial roughening is the dominant factor limiting mobility in this sample set which is consistent with previous reports[20]. In addition the carrier density in these samples exceeded 1.0×10^{13} cm^{-2}, an improvement on the heterostructures in which the AlN IL was subject to the T_{InAlN} temperature ramp and

again attributed to the more uniform thickness of the InAlN barrier layer and hence consistent 2DEG-surface separation.

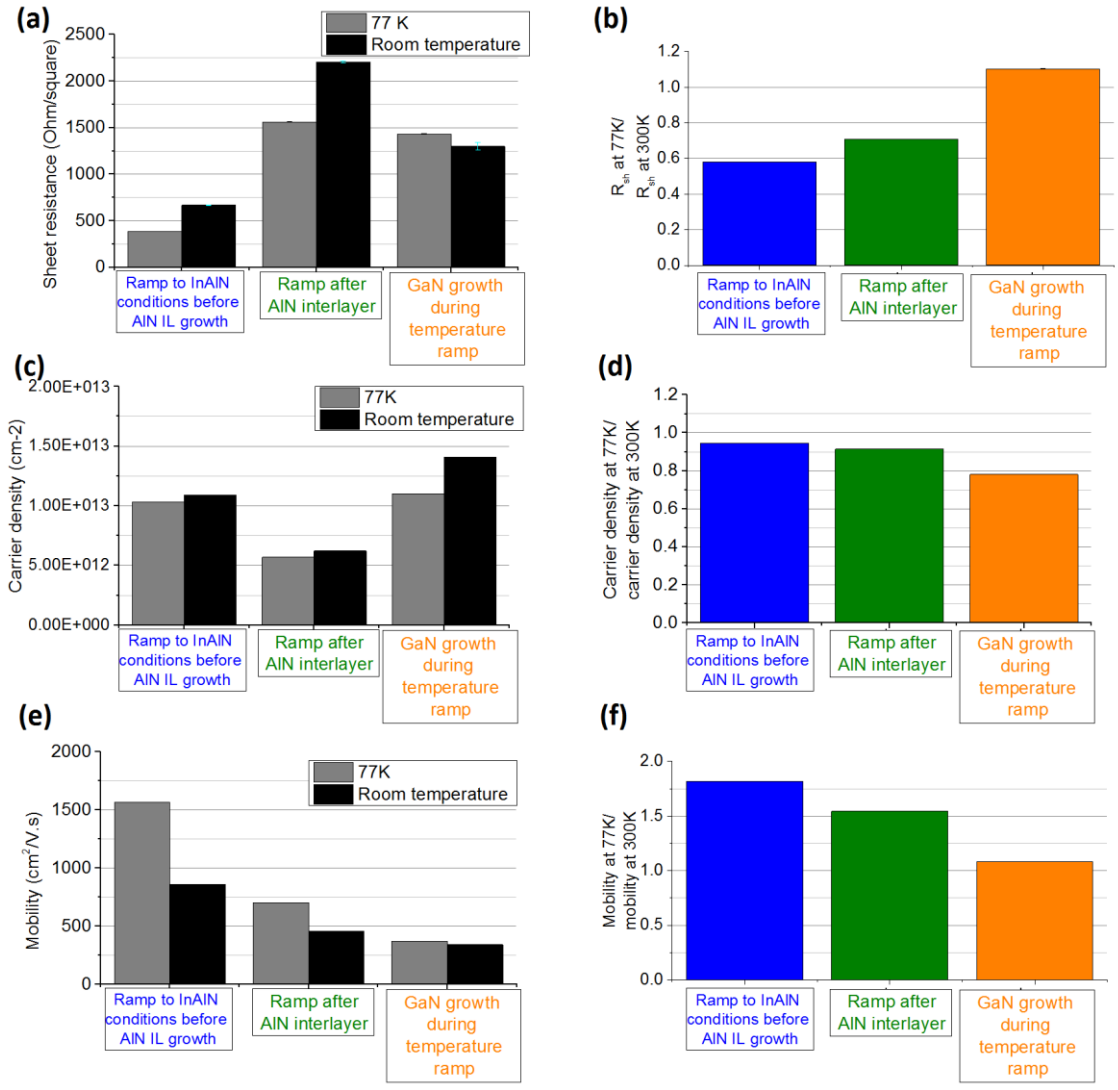

Fig. 4.12: Electrical properties of InAlN/AlN/GaN (5/1/1000 nm) with AlN interlayers deposited at different stages from Hall measurement at room temperature and at 77 K, and the ratio of the two

TEM cross sections of InAlN/AlN/GaN (5/1/1000 nm) heterostructure lamellas with the AlN interlayer grown immediately subsequent and prior to the ramp to T_{InAlN} are shown in Fig. 4.13(a) and (b), respectively. Fig. 4.13(c) and (d) show the same samples at lower levels of zoom. The TEM scans were taken in order to directly image the 2DEG interface and attempt to identify interfacial roughening inferred from the AFM scans in Fig. 4.10

and Fig. 4.11. However, the samples were indistinguishable by TEM, with even the surface roughening clearly visible in Fig. 4.10 and Fig. 4.11 not being readily observable.

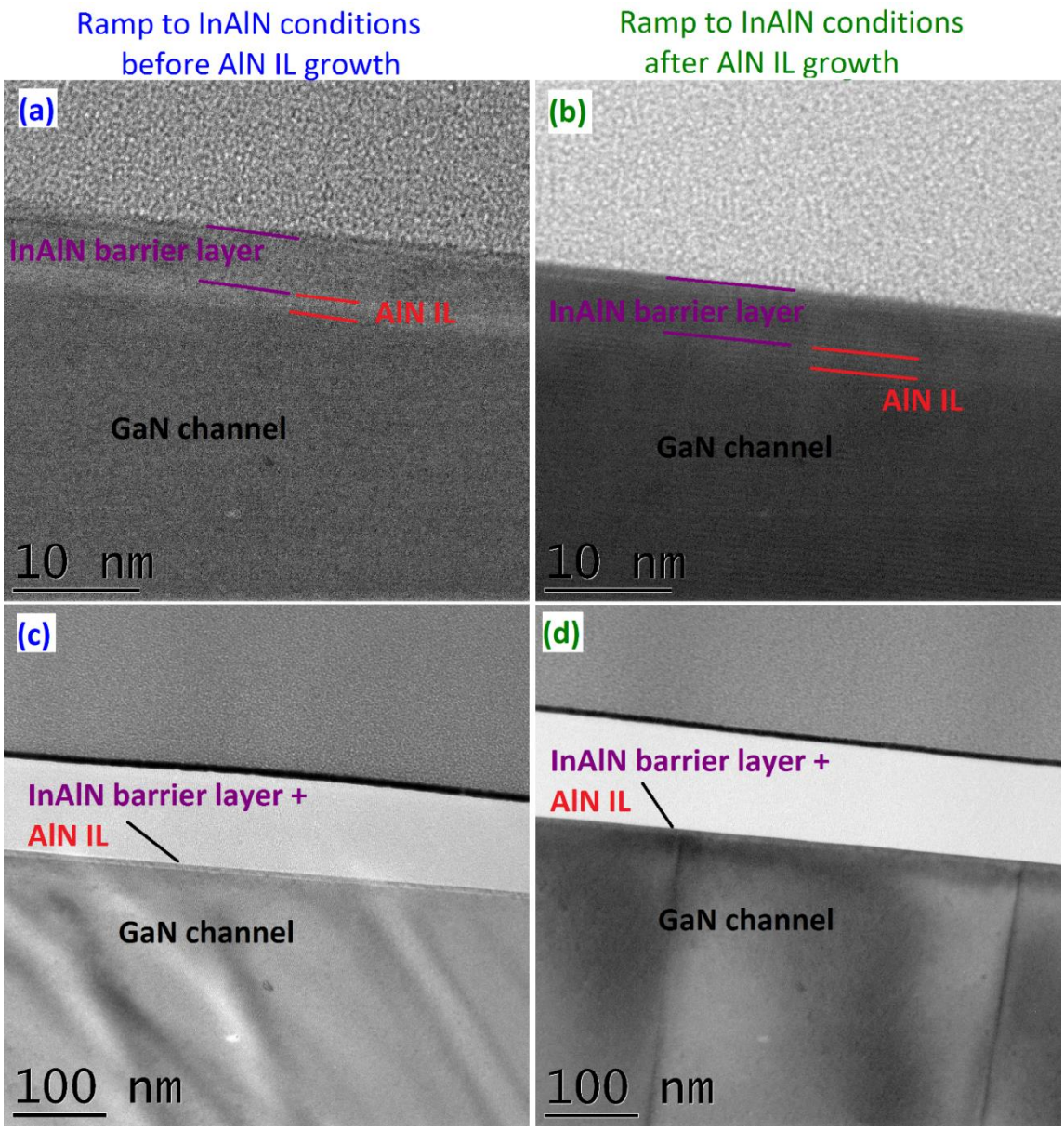

Fig. 4.13: TEM cross sections of InAlN/AlN/GaN (5/1/1000 nm) heterostructures with the AlN IL grown (a) immediately after the temperature ramp from T_{GaN} to T_{InAlN} and (b) immediately subsequent to the temperature ramp. (c) and (d) show the same samples at different zoom levels.

The data presented in this section and Section 4.2.1 demonstrate the range of factors that influence the conductive properties of InAlN/AlN/GaN heterostructures. GaN decomposition under the relatively low temperatures required for InAlN growth at lattice-matched compositions must be managed to ensure high channel mobilities,

although the data in Fig. 4.11 and Fig. 4.12 confirms that conditions exist where GaN surfaces can be exposed to such temperatures and not decompose in a way that introduced significant scattering. A layer-by-layer desorption process, rather than one initiated at around dislocation pit centres (as is the case in Fig. 4.8(a) and 4.8(b)) fulfils that criteria as appears to be the case for the sample imaged in Fig. 4.13(a). While ramping to T_{InAlN} during GaN growth acted to cause severe degradation of the channel layer in this work, discussion with industry contacts suggests this may be managed by optimisation of the ramp time and growth conditions. Indeed, variation of the AlN IL thickness in samples with the ramp to T_{InAlN} during GaN growth showed trends in electrical performance similar to better optimised structures found in the literature[18, 107, 108] albeit with much optimisiation still required.

4.2.3 Ga auto-incorporation in nominally InAlN barrier layers

This section is regarding the measurement of unintended Ga incorporation in nominal InAlN layers using various complimentary techniques, underpinned by X-ray diffraction. Nominal InAlN layers with similar growth conditions were prepared and a Ga signal was detected, with the amount depending on the total reactor flow rate. Ultra-thin InAlN/GaN HEMT layers were grown in a clean reactor to minimize Ga auto-incorporation, confirmed by using X-ray photoelectron spectroscopy and secondary ion mass spectrometry. The implications of Ga incorporation in InAlN layers within optoelectronic and power devices is discussed.

It was been reported that unintentional Ga incorporation in InAlN layers can occur during MOVPE, attributed to both left-over Ga-containing residue from previous growth on the reactor walls/susceptor[172, 249-251] or the decomposition of preceding Ga-containing layers[252]. Each proposed reason has convincing arguments, particularly when the geometry of the reactor and the use of Ga in the preparation of buffer or device layers prior to the InAlN growth are considered. Unwanted Ga has implications for both the structural and electrical properties of InAl(Ga)N epilayers. The band gap and

polarisation of the layer both depend on the composition fraction, and are critical parameters in determining the wavelength and efficiency of light emitted by an optoelectronic device and also the current handling capabilities of a power transistor. Structurally the growth mechanism of a quaternary epilayer may differ from that of a ternary, and as such the morphology of as-grown layers may not be the same. This is particularly important for heterostructures where interfacial roughness is a limiting factor, as for InAlN HEMTs (Section 4.2.1). MOVPE growth of InAlN/GaN heterostructures is a fundamental stage in achieving the desired electrical performance in InAlN HEMTs, and modifications to optimise growth and processing may not have the desired effect if implemented on InAlGaN layers.

Table 4.4: Selected growth parameters for the nominally InAlN epilayers grown in this series (sccm is standard cubic centimetres per minute). Also shown are composition fraction results from WDX and RBS measurements, checked for consistency by XRD, and fitting parameters for XRD analysis. The linear fitting refers to the lines in Fig. 4.16, assuming fully strained InAlGaN on relaxed GaN

	Sample A	Sample B	Sample C
NH_3 (mmol min^{-1})	56	168	56
TMIn (μmol min^{-1})	5	16	5
TMAl (μmol min^{-1})	5	16	5
Growth time (s)	1330	1300	2520
Reactor total flow (sccm)	8000	24000	24000
WDX Al%	69.0	73.0	79.0
WDX In%	7.0	15.0	7.0
WDX Ga%	24.0	12.0	14.0
RBS Al%	72.2	74.9	79.7
RBS In%	7.9	14.4	8.0
RBS Ga%	19.9	10.7	12.3
XRD thickness (nm)	87.5	82.0	88.0
RBS thickness (nm)	80	79	81
Linear fitting:			
'm' gradient value	4.00	4.05	3.99
'c' intercept value	0.56	0.72	0.49
If layers were Ga-free: XRD composition estimate	Al: 86.0% In: 14.0%	Al: 82.2% In: 17.8%	Al: 87.8% In: 12.3%

Initially, three nominally InAlN (80 nm) layers were grown on 1 μm GaN buffers on 0.4° miscut sapphire substrates. All layers were undoped and were grown continuously.

Before each wafer was grown the showerhead through which precursor gases enter the reactor was cleaned and the reactor baked in an attempt to minimise contamination of epilayers. The InAlN epilayer growth for samples designated A, B and C are presented in Table 4.4. The temperature, pressure and V/III ratio used were 790°C, 70 mbar, and 5481, respectively in all cases. Structures were analysed succeeding growth from XRD (0002) ω-2ϑ scans, with the layer thickness calculated from Pendellosung fringes, sensitive to around 1 nm.

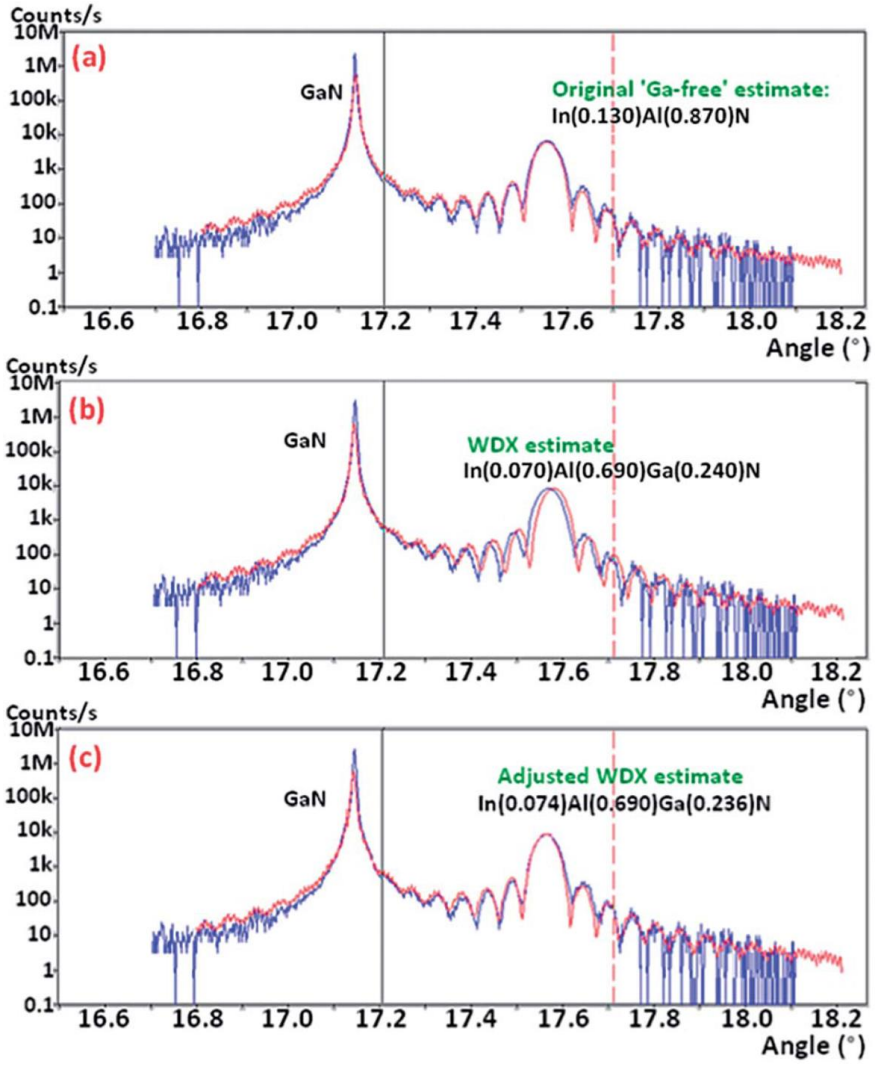

Fig. 4.14: (0002) ω-2ϑ XRD scans of sample A using a Ga-free InAlN layer (a), WDX composition values (b) and WDX values adjusted visually (c). This method is sensitive to changes in composition down to 0.1%

Assuming the layer to be both fully strained and Ga free, an initial estimate of the InAlN composition was made, as shown in Fig. 4.14. A (10-15) reciprocal space map confirmed the InAlN layers to be fully strained to the GaN buffer, to within a relatively large experimental error of 30%. However, the fact that the InAl(Ga)N composition is close to that which is lattice matched with GaN means the layers are likely to be fully strained.

While the c-plane lattice parameter and knowledge of the strain state of a layer can give an accurate estimate of the composition of ternary compound such as InAlN, it cannot unequivocally estimate the composition of a quaternary like InAlGaN as for fully strained layers a range of compositions will allow fitting. WDX and RBS were used to independently measure the level of Ga auto-incorporation in Samples A, B and C. To measure the same in HEMT barrier layers (too thin for analysis by WDX or RBS) SIMS and XPS were utilised. Three HEMT wafers were prepared, as shown in Fig. 4.15. HEMT-1 and HEMT-2 were grown with InAl(Ga)N barrier layer flow conditions identical to that of sample A described in Table 1. HEMT-1 and HEMT-2 have thicknesses of 9 nm and 14 nm, respectively, on top of GaN buffer layers with 1 nm AlN interlayers as described in Section 4.2.1. These samples were grown 'continuously', i.e. in a single growth run.

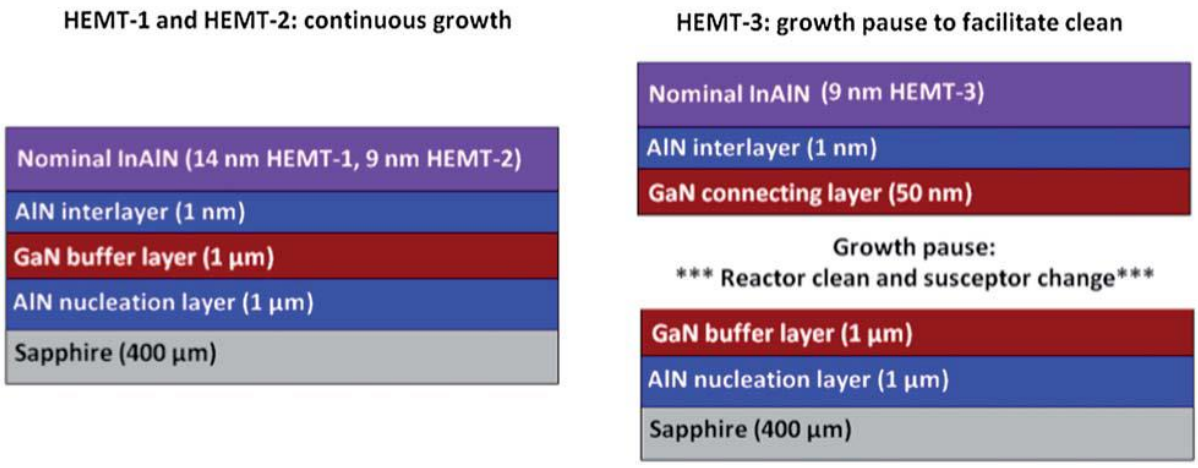

Fig. 4.15: Schematic of the HEMT layers grown in this series. HEMT-1 and HEMT-2 were grown continuously while HEMT-3 included a growth pause so the reactor could be cleaned and susceptor changed.

For HEMT-3, a revised growth procedure was developed with the aim of eliminating Ga auto-incorporation in the ultra-thin barrier layer. A growth pause after GaN buffer layer deposition was included during which time the reactor and showerhead were cleaned and the susceptor changed to one not previously exposed to MOVPE of Ga-containing layers. Growth of the 9 nm InAlN barrier layer and AlN interlayer then commenced after deposition of a 50 nm GaN connecting layer, thought to be sufficiently thin to not influence the composition of the subsequent layer.

The compositional estimates for the samples A, B and C analysed are shown in Table 4.4. XRD indicated InAlN compositions in the range of 12–18% InN assuming the absence of Ga. As a test of the consistency of the measurement the WDX composition fraction estimates can be fed back into the XRD fitting software and the legitimacy of the measurement scrutinized. Fig. 4.14(b) exhibits the fit to the experimental curve data based on the WDX derived values, showing a close match. In this case, fixing the Al and modifying the In and Ga concentrations by less than 0.5% can lead to a fit (Fig. 4.14(c)) that is as good as the original, assuming pure InAlN (Fig. 4.16(a)). Such a small change is well within the error limits of the WDX compositional measurement. Similarly, feeding the RBS composition fraction estimates back into the XRD simulation confirms a match that is self-consistent given the uncertainties in the measurement (detailed in Ref. [253]). While the RBS data is consistent with films uniform in composition, this cannot be assumed the case given the source of the Ga in the “InAlN” films has not been unequivocally determined. It may be possible that the Ga content may have a graded profile, and indeed SIMS data suggests graded Al and Ga composition–depth profiles down the heterointerface (with In appearing to mediate the process by maintaining a constant composition fraction), with profiles becoming flat after ~ 4 nm. Further work is required to analyse this effect and further probe the origins of the phenomenon.

Fig. 4.16 exhibits the range of composition fractions that are compatible with the XRD (0002) scan for two samples (A and B). The lines produced were based on multiple simulations using the X'Pert X-ray fitting software to confirm the linear nature of the compositional XRD isolines. The range of compositions allowed by XRD assuming fully strained InAlGaN on relaxed GaN can be fitted by a line using the values in Table 4.4. It should be noted that the RBS and WDX data for Sample A do not lie on the line

representing a fully strained InAlGaN layer, and might suggest some limited InAlGaN relaxation (relative to the underlying GaN layer). With the exception of the WDX measurement of sample B, all the compositional analyses of the three samples indicated fell into this regime. Given the width of the peaks in Qx in reciprocal space it is possible that there is some limited relaxation, or development of relaxation across the 80 nm film towards the surface, though a relaxation as high as 30% seems unlikely due to the composition being close to the lattice matched condition. It is believed the variances observed are related to the respective errors in the different techniques, and the layer is assumed to be close to fully strained whilst acknowledging a degree of uncertainty in this regard. In this analysis it is also assumed the > 1 µm GaN layers grown on sapphire to have 100% relaxation, and any residual strain in the GaN to have would be expected to have negligible second order effects on the data.

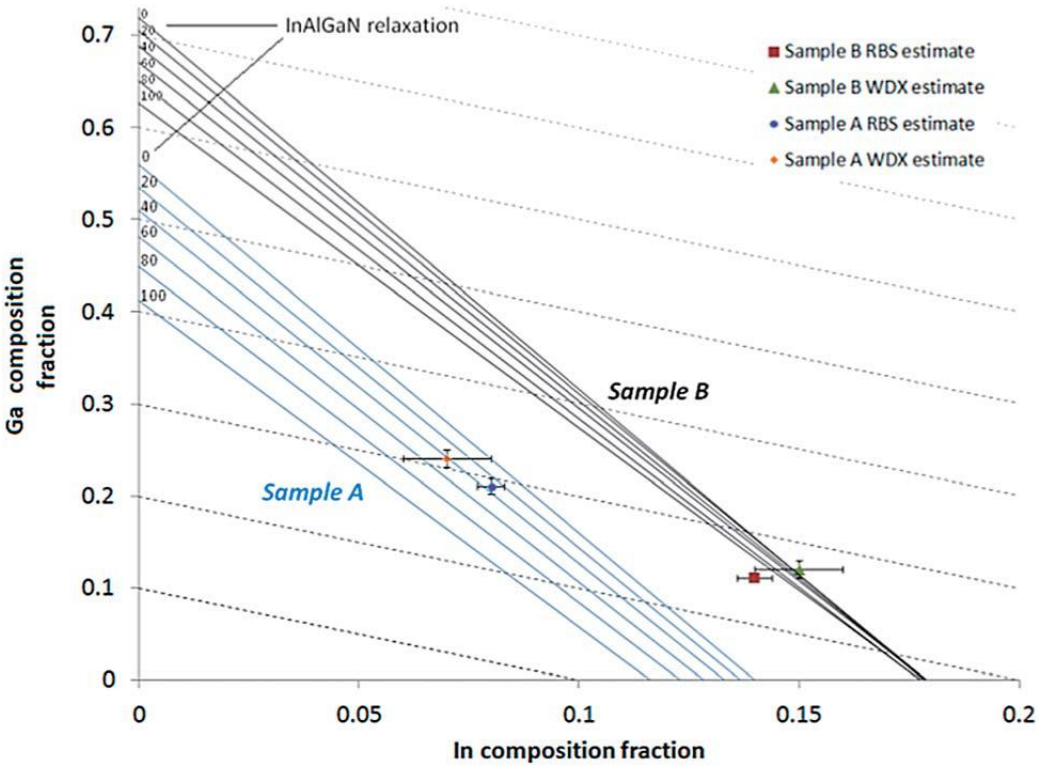

Fig. 4.16: [0002] ω-2ϑ XRD fitting parameters that give compatible results for Sample A (solid blue lines) and Sample B (solid black lines), with different InAl(Ga)N relaxation values considered. Constant Al content contour lines are also shown (dashed lines)

A significant proportion of gallium is found in all three samples, ranging from 11% (RBS estimate, Sample B) to 24% (WDX estimate, Sample A), clearly showing a consistent presence in all nominally Ga-free layers. This could be easily overlooked if a layer was grown and immediately characterised via XRD for a composition fraction estimate, as a pure InAlN layer might have the same c-plane lattice parameter as an InAlGaN layer. The subtle structural and electrical effect of Ga contamination may provide substantial problems when processing and characterizing a semiconductor device if a pure InAlN layer is assumed, for example when trying to optimise a contact to a HEMT, polarisation-match a quantum well or optimise the reflectivity of a distributed Bragg reflector.

Referring to Table 4.4 we can analyse the growth conditions used for the InAl(Ga)N layers of Samples A, B and C and compare composition estimates to probe the origins of the Ga contamination. A reduced gallium content is seen for Samples B and C compared with A. Referring again to Table 4.4 we see that an increase in the total gas flow into the reactor, that is the combined flow of the N_2 carrier gases and TMAl and TMIn (but not TMGa), appears to suppress gallium incorporation in the upper layer. Sample B has three times the group III and V precursor flows of sample A, and the carrier flows are scaled up accordingly to give a total flow of 24,000 sccm compared to 8,000 sccm for A. Sample C uses the same group III and V precursor flow rates as A but has the high 24,000 sccm total flow rate as used for Sample B. The InAl(Ga)N thickness was maintained by extending the growth time. It is clear that increasing the total flow rate from 8,000 sccm to 24,000 sccm acts to suppress Ga incorporation in the InAl(Ga)N layers by 50%. This suggests a higher gas flow prevents lingering contaminants from reacting on the surface of the wafer, supporting an argument[172, 249-251] that unwanted Ga in the group III sublattice originates from Ga-containing material sticking to the reactor walls, susceptor and/or gas delivery pipes and partially redepositing on a wafer surface during subsequent growth runs. The small measured difference in Ga fraction between layers B and C (with proportions spanning 11–14%) is much less than the higher values of 25% Ga content obtained for Sample A. Furthermore Sample B contains roughly twice as much indium as Sample C. This suggests the higher growth rate in sample B relative to sample C (arising due to the larger ratio of precursor gas flow to total gas flow) acts to

reduce indium desorption, encouraging a more indium rich lattice than when the growth rate is lower as in Sample C. This may give further clues as to the mechanisms at work during pure InAlN growth, although further analysis is required before a conclusion can be made.

To fully suppress Ga incorporation into InAlN-on-GaN layers the susceptor and glassware through which precursor gases are delivered may have to be cleaned, along with the reactor and showerhead itself, between GaN and InAlN growth. Over many growth runs matter builds up on the walls of the reactor over which it passes and there may be no way to prevent it redepositing by modulation of the gas flow and growth conditions alone. The geometry and design of the AIXTRON CCS[206] system makes a full clean a long and cumbersome task, which may prevent it from being a practical solution. Instead it may be more useful to consider embracing a small, controllable amount of Ga and modifying MOVPE growth conditions and device processing accordingly.

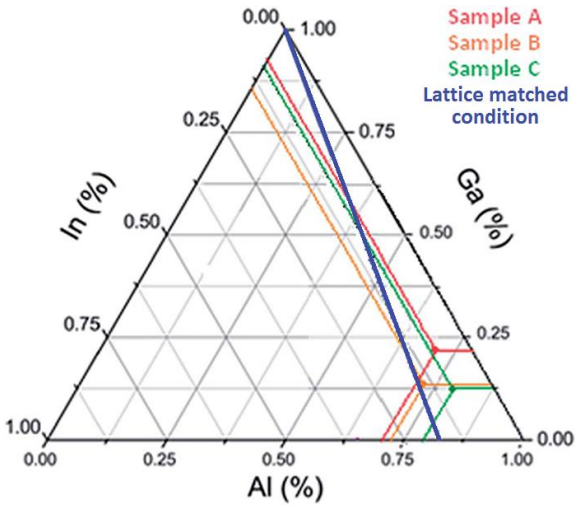

Fig. 4.17: Quaternary map of samples A, B and C, showing the compositions of InAlGaN lattice matched to GaN.

Ga incorporation in nominal InAlN layers has implications for all InAlN-based devices; although InAlGaN/AlN/GaN HEMTs have been reported with power handling capabilities and high frequency operation comparable with state-of-the-art InAlN and AlGaN based

devices[101], both growth and processing must be adjusted to facilitate the difference in structural and electrical properties and the composition fraction must be tightly controlled for performance to be optimised. From a HEMT reliability perspective InAlGaN layers can be grown lattice matched to GaN, both reducing interfacial roughness scattering[101] and eliminating interfacial strain, a potential HEMT failure as detailed in Chapter 2. For optoelectronic devices InAlN can be used for bandgap engineering and polarisation matching in quantum well structures to optimise light output efficiency and a desired wavelength[254]. The graphic displayed in Fig. 4.17 is a quaternary map representing the composition of the InAlGaN layers grown in this work in comparison to that required to be lattice matched to GaN. Sample B lies close to the solid blue line, suggesting it has an in-plane lattice parameter identical to that of the underlying GaN layer and is thus fully relaxed/free of strain.

Table 4.5: Comparison of samples grown conventionally and using a revised growth procedure to suppress Ga auto-incorporation

Sample	In%	Ga%	Al%	Comment
HEMT-1	8	13	79	No reactor conditioning
HEMT-3	18	1	81	Reactor cleaned & susceptor changed before InAlN growth

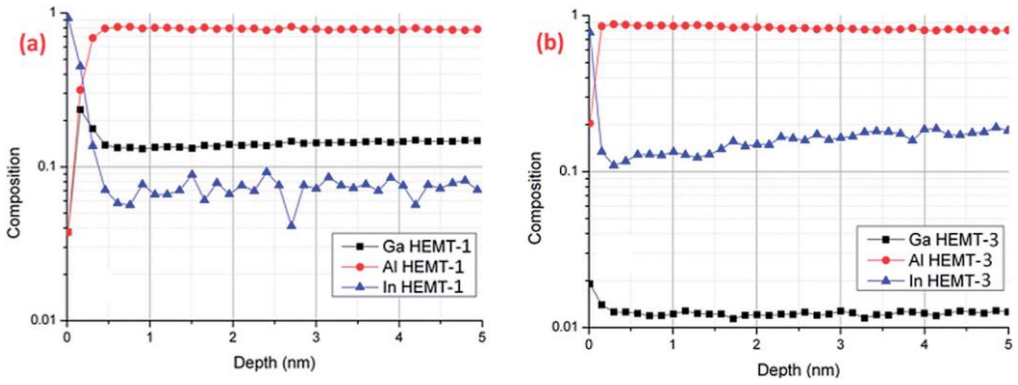

Fig. 4.18: SIMS profiling of InAlN HEMT barrier layers without (a) and with (b) the MOVPE reactor undergoing a clean and change in susceptor to one not previously exposed to Ga-containing layers (HEMT-1 and HEMT-3, respectively)

The results of SIMS analysis on heterostructures HEMT-1, grown in the conventional manner without a growth pause and HEMT-3, grown with a pause during which the reactor was cleaned and susceptor changed, are displayed in Fig. 4.18 and summarised in Table 4.5. Removing the samples from the reactor before InAlN growth for InAlN-on-GaN heterojunction transistors and taking measures to minimise unintended Ga incorporation is found to suppress contamination by at least an order of magnitude, confirming the source to be residual matter inside the growth chamber and not inter-diffusion from the underlying buffer layer[172, 249-251].

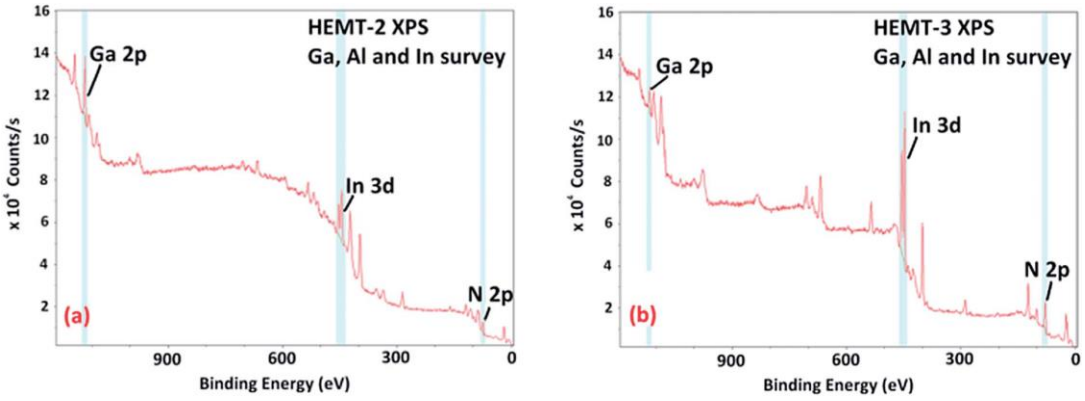

Fig. 4.19: XPS profiling of InAlN HEMT barrier layers without (a) and with (b) the MOVPE reactor undergoing a clean and change in susceptor to one not previously exposed to Ga-containing layers (HEMT-2 and HEMT-3, respectively).

Despite HEMT-1 and HEMT-2 being grown with nominally identical conditions as sample A (except for growth time), different composition values were measured. This is partly due to grading in the Al and Ga compositions at the heterointerface, which will contribute proportionally depending on the InAlGaN layer thickness, but may be chiefly attributed to the different, undefined measurement resolutions of the various techniques in the depth direction. XPS is a cheaper, faster alternative to SIMS, which can be costly and time consuming. Results are shown in Fig. 4.19 and Table 4.6, where the binding energy position represents the species of atom detected (assuming certain information about the bonding state, which is valid here) and the area of the peak

describes the abundance, once the X-ray sensitivity factors are accounted for. Table 4.6 indicates that HEMT-3, grown using the revised procedure aiming to suppress unwanted Ga incorporation in the nominally InAlN barrier layer, has 6 times less Ga in the region of crystal nearest the surface than the reference sample HEMT-2, grown under conditions favourable to Ga contamination to ensure it is detectable by the non-optimised XPS measurement. This qualitatively supports the SIMS data and the hypothesis that unwanted Ga in InAlN layers arrives from lingering precursors in the reactor during InAlN growth, especially given the fact that HEMT-3 shows only 1% Ga contamination in both cases. Further development and validation of the XPS cross referenced with SIMS measurements will allow XPS to be used as a rapid robust feedback technique for ultra-thin InAlGaN HEMT layers, although more work is required to this end; InAlGaN layers should be grown with a wide range of alloy compositions, characterized by independent and more established techniques such as RBS and WDX and cross-referenced with XPS to generate confidence in the latter.

Table 4.6: XPS results table corresponding to HEMT-2 and HEMT-3 as in Fig. 4.19

Name	Position (eV)	FWHM (eV)	Composition (%)
HEMT-2 Al – 2p	73.4	3.7	77
HEMT-2 Ga – 2p	1118.4	3.6	7
HEMT-2 In – 3d	444.8	8 4	16
HEMT-3 Al – 2p	73.6	3.3	80
HEMT-3 Ga – 2p	1118.6	3.4	1
HEMT-3 In – 3d	445.0	3.5	19

To suppress Ga auto-incorporation in InAlN HEMTs an attempt was made to encourage Ga-containing residue from the reactor walls to incorporate earlier in the growth process in the GaN buffer, rather than the InAlN barrier. It was posited that the presence of the In precursor TMIn may be the catalyst that instigates the desorption process. TMIn was introduced during GaN buffer growth, and no change in surface morphology was observed. Due to the well described low incorporation rate of In to into III-nitride wurtzite lattice structures at high temperatures the inclusion was not expected to significantly affect the channel crystallinity. However, mobility was reduced to less than

50 cm^2/V.s, indicating some In incorporation may have taken place or elsewise affected the channel integrity.

In conclusion nominal InAlN layers were found to contain gallium at high group III sub-lattice fractions in the 12–24% range, depending on the growth conditions. RBS and WDX were used to measure composition fractions, supported by ω–2θ (0002) XRD scans, also used to confirm and refine the WDX and RBS data. The results suggest Ga incorporation may be suppressed by increasing the total gas flow into the reactor, indicating the origin of unwanted Ga is the susceptor and the walls of the reactor. Ultra-thin InAlN HEMT epilayers were analyzed using SIMS and XPS, and a revised InAlN HEMT growth procedure aimed at reducing Ga auto-incorporation was shown to be successful.

4.3 Chapter Summary

In this chapter the MOVPE of InAlN/GaN and AlGaN/GaN heterostrutures for use in HEMT structures has been explored. InAlN and AlGaN have distinct properties in terms of their growth mechanics and material properties, despite providing similar functions as HEMT barrier layers. This principally stems from the different atomic properties of Al, Ga and In. The challenges faced by (less established) InAlN growth must be approached uniquely, without assuming optimisation techniques proven to work for AlGaN are applicable. The effect of MOVPE on device fabrication, performance and reliability are discussed in Chapters 5 and 6.

5. Reliability and failure analysis

In this chapter the performance of InAlN and AlGaN HEMTs detailed in Section 3.6 is explored when devices are subject to incident gamma radiation, high ambient temperatures and extended off-state bias stress. Overall, the results show III-nitride HEMTs to be a robust technology well suited for applications such as those in space, where the maintaining of electrical performance under extreme conditions is critical. This chapter focusses on the identification of mechanisms that limit the overall good stability, principally the capture of charge carriers in electrically active defect trap states. The inclusion of well optimised AlGaN HEMTs from a commercial source highlights the link between optimisation of device performance and reliability. The results of the reliability characterization were instrumental in optimisation of the InAlN HEMT surface passivation detailed in Section 6.2.

5.1 Gamma radiation hardness

The radiation stability of III-nitride HEMTs reported in the literature was outlined in Section 2.8. In this study we aim to directly compare the radiation stability of InAlN/AlN/GaN and AlGaN/GaN HEMTs fabricated by the author, both with and without SiN_x capping layers deposited by PECVD. Results across the sample set are contrasted with optimised production level AlGaN HEMTs. A direct comparison of gamma radiation hardness was measured for up to a total dose of 9.14 Mrad at 6.6 krad/hour, followed by monitoring the performance recovery during post-irradiation annealing. A direct systematic comparison highlights the comparative susceptibility of InAlN and AlGaN HEMTs, as well as the role of SiN_x capping in III-nitride HEMT radiation hardness, and it is further shown by comparison with production level devices that incomplete device optimisation can act to increase sensitivity to radiation induced trap-related performance degradation.

The research level devices described here were the products of first experimental trials, and share similar geometries to the production level AlGaN HEMTs also evaluated. Little is known about the manufacturing process in the latter case. The research level InAlN/AlN/GaN and AlGaN/GaN heterostructures were grown by metal-organic vapour phase epitaxy (MOVPE) using an AIXTRON 3x2" close-coupled showerhead reactor (Section 3.1). The barrier layer thicknesses were 12 nm and 6-8 nm for AlGaN and InAlN, respectively. An AlGaN barrier layer composition of 20% Al was obtained by X-ray diffraction. The low thickness of InAlN barriers prevented a similar analysis but the lattice matched $In_{0.18}Al_{0.82}N$ condition is assumed fulfilled from bulk growth estimates. A 1 nm AlN interlayer was included in the InAlN HEMT heterostructures to increase channel conductivity and prevent GaN decomposition during the transition of growth conditions between GaN and InAlN (Section 4.2.1). InAlN/AlN/GaN wafers measured R_{sh} = 350 Ω/□, n_s = 1.3 x 10^{13} cm^{-2} and μ = 1000 cm^2/V.s, and AlGaN/GaN structures show R_{sh} = 850 Ω/□, n_s = 6.6 x 10^{12} cm^{-2} and μ = 1100 cm^2/V.s, with AlGaN/GaN showing a superior wafer uniformity. These values are broadly in line with what is to be expected given the barrier layer thicknesses and alloy compositions according to finite-element simulations.

A Cl_2-based ICP MESA etch to a depth of 100 nm into the buffer was used to isolate devices during transistor fabrication. This was followed by the deposition of the source and drain Ti/Al/Ni/Au (3/50/50/50 nm) Ohmic contacts that were annealed under N_2, at 850°C for InAlN and 750°C for AlGaN HEMTs (the different temperature is explored in Section 6.1). Schottky gate contacts comprising of Ni/Pt/Au (30/50/250 nm) stacks were then deposited and annealed at 400°C for 60 seconds under N_2. A selection of wafer material was then surface capped with 100 nm SiN_x by PECVD subsequent to a 60 seconds dilute (1:1) NH_4OH:H_2O surface clean. The PECVD process was based on a technique developed for AlGaN HEMTs, with no modification made to account for the potentially different behaviour when applied to InAlN surfaces. It involved a mixed-frequency deposition technique to minimise strain build up in the SiN_x layer which could lead to additional strain at the HEMT surface and thus modification the piezoelectric polarisation charge component at the barrier/GaN interface (see Section 6.2 for further details). The SiN_x cap was selectively wet etched using a HF-based solution

to contact the metal pads, with devices then categorised as (i) InAlN-uncapped (ii) AlGaN-uncapped, (iii) InAlN-SiN_x and (iv) AlGaN-SiN_x. Production level devices are presumed to share a similar manufacture flow based on optical inspection and the prevalence of the afore-mentioned techniques in the scientific literature, and a passivation layer was identified from the openings to bond pads.

A test plan was concocted based on the equipment available at the European Space Research and Technology Centre (ESTEC) and the time available for experiment, in accordance with European Space Agency standards. Devices were subjected to ^{60}Co gamma radiation at energies of 1.173 MeV and 1.332 MeV and at a dose rate of 6.6 krad/hour for 59 days. These gamma energies are commonly used for radiation qualification due to the relative abundance of ^{60}Co sources. The total ionizing dose was 9.16 Mrad and devices were unbiased during exposure and maintained under standard ambient temperature and pressure conditions. Intermediate DC characterization was performed on all devices every 12 days approximately and upon completion of the final dose. This was followed by storage at room temperature for 24 hours and then at 100°C for 168 hours, with DC parameter evolution monitored for all devices at the end of each stage. InAlN-SiN_x and AlGaN-SiN_x reference devices stored in a desiccator chamber and not subject to irradiation or annealing were measured in parallel to isolate the effects of gamma radiation and time-varying instability introduced by SiN_x passivation.

The evolution of parameters listed in Table 3.3 when subjected to ^{60}Co gamma radiation exposure and voltage stress are generally discussed with reference to values normalised to those for unstressed devices, in order to compare relative variation of DC characteristics. Standard deviation is represented by error bars to indicate the range of parameter drift from pre-stressed values, and is necessarily broad due to the small sample size needed to complete device characterization within the allowed timeframe between irradiation stages. Results not included in averaging are presented as unfilled larger shapes, and are characterised by corresponding anomalous surges in leakage current and certain dramatic changes in DC parameters likely caused by the release of trapped charge[255]. Better statistics from larger sample sets are required to draw valid conclusions as to their relationship with incident radiation in comparison with

unstressed reference devices due to their low rate of occurrence, and only general trends in parameter variation are discussed here. Ohmic contact metallisation is reported to be stable under radiation exposure[156, 166, 256] in AlGaN HEMTs, with a similar conduction mechanism identified in InAlN HEMTs[71, 72], so performance variations are attributed to defect generation in the bulk nitride material and at semiconductor/dielectric interfaces. While there is no standard 'acceptable' level of radiation stability, the exceedingly high dose rate (6.6 krad/hour) and total ionizing dose (9.16 Mrad) used here is sufficient to qualify the devices as 'radiation-hard' should they maintain operation after exposure, based on the expected radiation exposure during the JUICE mission lifetime [1,258].

5.1.1 Uncapped InAlN and AlGaN HEMT stability under gamma radiation

Fig. 5.1 shows the evolution of InAlN-uncapped and AlGaN-uncapped HEMT saturated drain currents (I_{dss}, defined as I_{drain} when V_{ds} = 10 V and V_{gs} = 0 V) and on-resistance (R_{on}, defined as $2/I_{drain}$ when V_{ds} = 2 V and V_{gs} = 0 V) under gamma radiation at 6.6 krad/hour (up to day 59) followed by consecutive ex-situ anneal stages (shaded region with dashed lines) of 24 hours at 23°C and 168 hours at 100°C. Production level AlGaN HEMTs are included for comparison. InAlN-uncapped HEMTs on average show a steady degradation of I_{dss} (Fig. 5.1(a)) with increasing total dose, exhibiting a general recovery during the anneal stages. AlGaN-uncapped devices degrade more rapidly until ~ 3.8 Mrad, where damage appears to stabilise before showing limited recovery. Fig. 5.1(b) shows on-resistance (R_{on}) evolution throughout the experiment, both during the radiation exposure and thermal storage periods. InAlN-uncapped HEMTs show good stability throughout all stages deviating by less than 20% from the initial value, a broad standard used by the European Space Agency to indicate good radiation stability. AlGaN-uncapped HEMTs show a cumulative increase in R_{on} up to ~7.2 Mrad, with moderate recovery during annealing. The production level AlGaN HEMTs exhibit superior stability and inter-device uniformity compared to both research level InAlN-uncapped and AlGaN-uncapped with respect to saturated drain current

(Fig. 5.1(a)) throughout all stages. In terms of on-resistance only a moderate reduction during radiation exposure to around 10% from pre-stressed values is noted at 9.16 Mrad total dose, stabilising during the anneal (Fig. 5.1(b)) and consistent across the sample set.

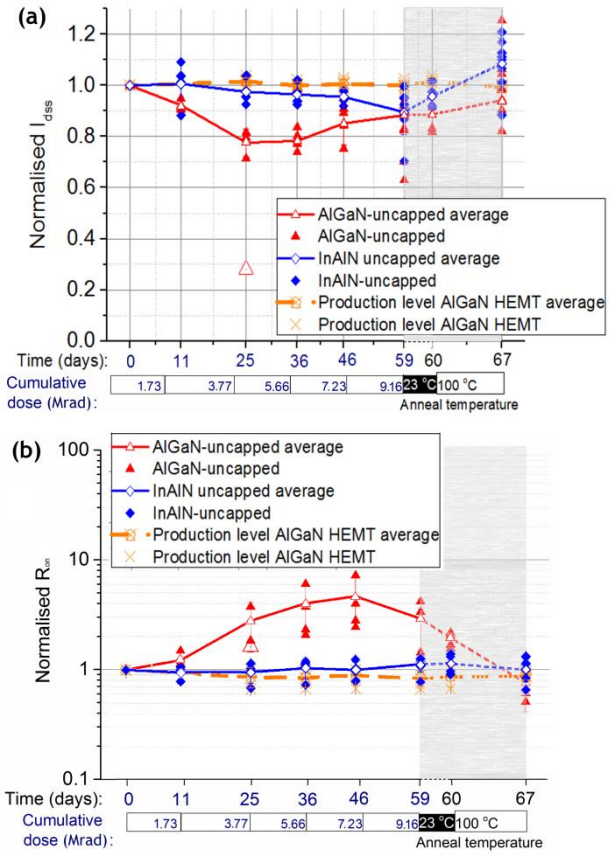

Fig. 5.1: Uncapped InAlN and AlGaN HEMT (including production level devices) saturated drain current I_{dss} (a) and on-resistance R_{on} (b) over the duration of gamma radiation exposure (up to day 59) and post-irradiation anneal

Fig. 5.2 shows absolute changes in threshold voltage (V_t) over the same timescale. A large range of threshold voltage values is noted for InAlN HEMTs in Fig. 5.2 (a), indicative of poor uniformity across the device sample set possibly arising from nm-scale roughness of the InAlN barrier layer, and as a result different effective gate-channel thicknesses. Negligible drift in V_t is recorded throughout the radiation exposure stages for both InAlN-uncapped and AlGaN-uncapped (Fig. 5.2(b)). Production level AlGaN

HEMTs showed no change in V_t values, except for a single device that showed a drift of -0.2 V after the first intermediate characterisation stage before stabilising.

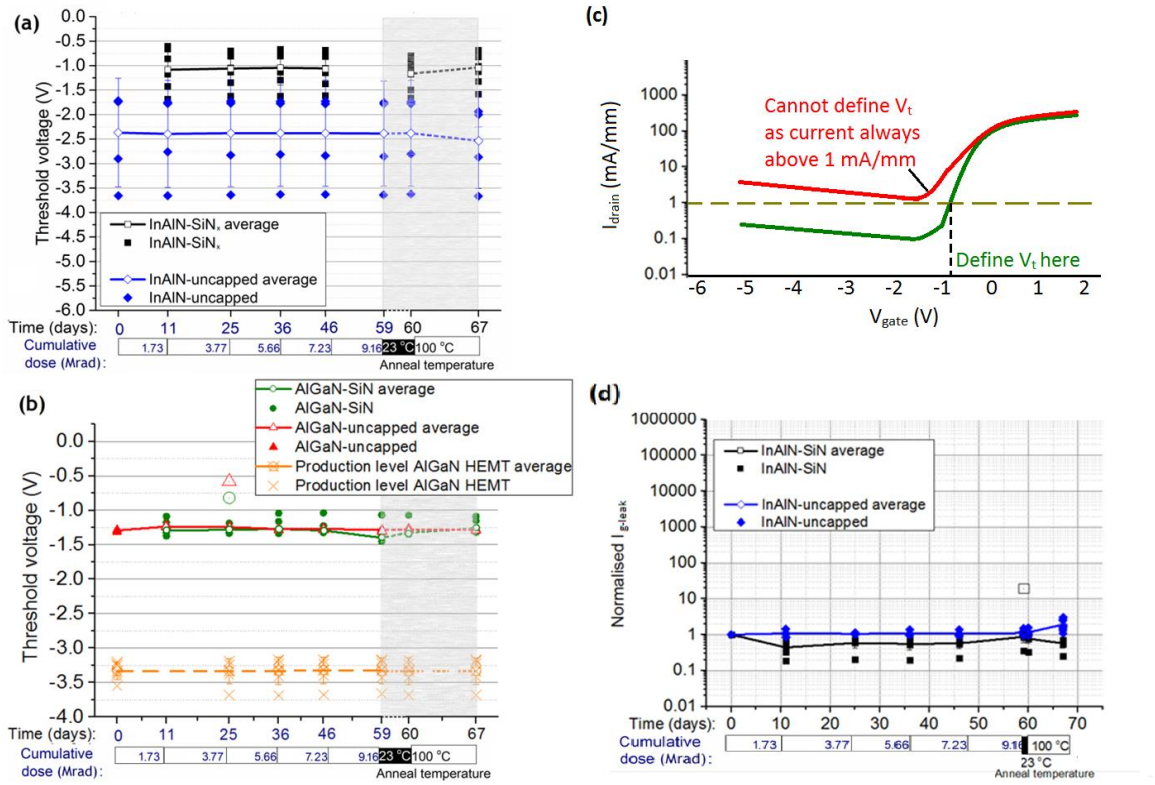

Fig. 5.2: Threshold voltage response of (a) InAlN and (b) AlGaN (including production level) HEMTs with and without SiN_x capping to gamma radiation exposure (up to day 59) and post-irradiation annealing. (c) shows a schematic of I_d-V_g plots inn which V_t can and cannot be defined, and (d) shows the evolution of InAlN HEMT leakage current

The degradation of I_{dss}, and R_{on} for the AlGaN-uncapped HEMTs correlates with an increase in $I_{d\text{-}leak}$ on a similar timescale. No similar rise is seen in the gate leakage current. This is consistent with traps induced by high energy radiation in the AlGaN barrier layer capturing charge carriers (although presumably not directly under the gate[257], further evidenced by the good stability of V_t), which release upon annealing. A negative shift in V_t in the InAlN-uncapped devices during the 100°C anneal is consistent with an increase in carrier density beneath the gate, correlating with the increase in I_{dss} (Fig. 5.1(a)) and $I_{d\text{-}leak}$ with the shift being greater for devices with less negative initial values of V_t. In comparison the high stability of the production level AlGaN HEMTs indicates

considerably less trap-related degradation, likely due to the maturity of the optimised surface passivation process.

5.1.2 SiN_x capping effects on HEMT stability under gamma radiation

The effect of PECVD SiN_x capping on threshold voltage stability under gamma irradiation is shown in Fig. 5.2(a) and (b). In pre-stressed research level InAlN-SiN_x and AlGaN-SiN_x devices threshold voltage is not definable for the majority of samples due to high off-state leakage currents preventing adequate channel pinch-off (i.e. the red curve in Fig. 5.2(c), see Section 2.6.1 for more details). Off-state leakage in InAlN-SiN_x and AlGaN-SiN_x HEMTs is generally suppressed upon initial gamma radiation exposure by a factor of 2 (Fig. 5.2(d), see Appendix 1 for full details), although the high initial values should be noted from Table 3.3. When compared to unstressed reference devices the suppression of leakage under irradiation is more pronounced for InAlN-SiN_x HEMTs (Appendix 1), attributed to the greater contribution of interfacial leakage at the InAlN/SiN_x boundary, suggesting InAlN surfaces are more sensitive to trap-related degradation than AlGaN at the alloy compositions studied here. Leakage currents in InAlN-SiN_x HEMTs are suppressed during initial radiation exposure periods allowing for a stable threshold voltage to be defined (Fig. 5.2(a)); the mechanism for this is not clear, although it is presumed to be due to electronic trap generation and the resulting capture of carriers and elimination of leakage routes. At 9.16 Mrad total dose leakage is again increased and V_t is not definable. The leakage is again suppressed after the post irradiation 24 hour room temperature storage with a shift of approximately -0.2 V in V_t compared to values recorded during the first intermediate characterization stage at 1.73 Mrad followed by a complete return after the 168 hour anneal at 100°C. These variations in V_t are small but consistent across the sample set, and are contrasted with a negative shift during the 100°C anneal stage in InAlN-uncapped devices, suggesting interaction at the InAlN/SiN_x interface dominates InAlN-SiN_x HEMT behaviour and confirming the mechanism by which additional charge is introduced into the system under thermal stress is somewhat suppressed by SiN_x capping[146]. Similarly the V_t variations in AlGaN-SiN_x HEMTs broadly correlate with an increased range of off-state

leakage currents induced by radiation, suggesting the mechanism is the same. This behaviour is consistent with carrier accumulation under the gate facilitated by leakage paths, suggested to be parasitic conduction along the barrier/SiN_x interfaces[255]. It is in contrast to the production level AlGaN HEMTs (passivated with an unknown material), which show consistent values of V_t throughout all stages, again attributed to a more mature passivation technique.

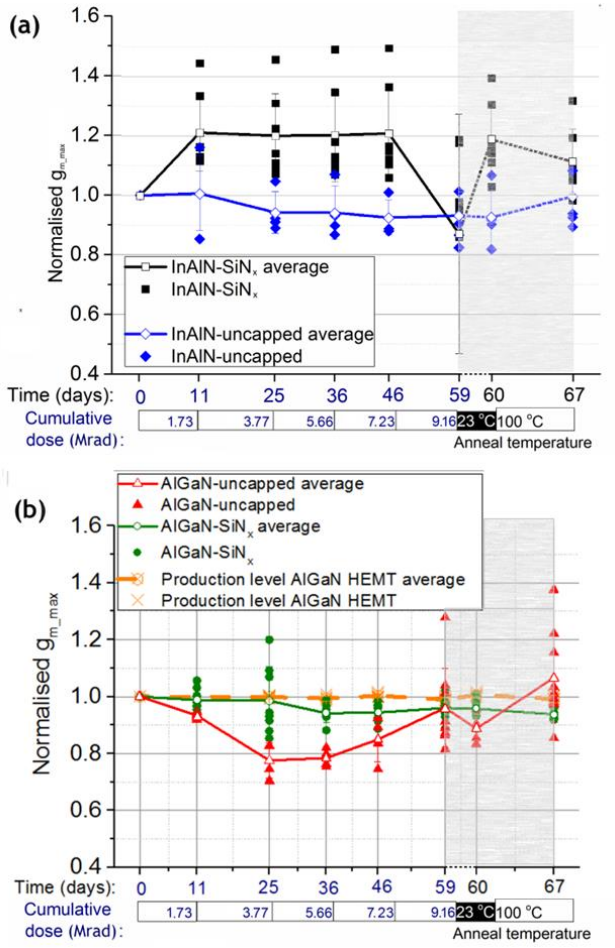

Fig. 5.3: The effect of SiN_x capping on (a) InAlN/AlN/GaN and (b) AlGaN/GaN HEMT (including production level devices) peak transconductance in response to gamma radiation exposure (up to day 59) and post-irradiation annealing

Fig. 5.3 shows the normalised variation of peak transconductance, g_{m_max}, throughout the experiment. Production level AlGaN devices show deviations of less than 2% from pre-stressed values throughout all stages. For the research level devices, I_{dss} and g_{m_max} follow similar trends in all sets. The lower InAlN-SiN_x values of g_{m_max} prior to irradiation and after 9.16 Mrad correlate with high leakage currents that prevent channel pinch-off,

as is to be expected. InAlN-SiN_x devices show a large range in variation of normalised I_{dss} and g_{m_max} values during irradiation beyond that accounted for by the suppression of leakage paths, failing to recover during the post-irradiation anneal. Moderate divergence of g_{m_max} values in InAlN-SiN_x reference samples not subjected to irradiation confirm instability is present already in the SiN_x capped devices, and is further aggravated by gamma radiation exposure. The significant reduction in g_{m_max} at 9.16 Mrad total dose coincides with the lack of definable V_t in Fig. 5.2(a) and is similarly caused by a (roughly 2x) increase in leakage current (Fig. 5.2(d)) diminishing the gate's control over the channel.

For research level AlGaN/GaN devices a stabilisation of parameter degradation throughout irradiation and anneal stages is noted with SiN_x capping. This suggests the passivation scheme employed here acts to suppress the negative effects of trapping at the upper AlGaN boundary through the introduction of additional leakage paths[166], consistent with the variation of V_t in Fig. 5.2(b). Similarly the steep increase of the on-resistance associated with AlGaN-uncapped HEMTs featured in Fig. 5.1(b) is stabilised in AlGaN-SiN_x devices (not shown) at 3.8 Mrad, probably by allowing a gradual release of trapped charge along the AlGaN/SiN_x interface through the introduction of states at that boundary[166], with the normalised value remaining close to unity throughout the anneal stages. This data, combined with the high performance and stability of the (passivated) production level AlGaN devices, is further evidence that optimisation of the surface capping layer/barrier interface is critical to exploit the robustness to radiation and thermal stress offered by III-nitride HEMTs.

In addition to the experiments above with a ~ 1 MeV gamma ray dose rate of 6.6 krad/hour, separate InAlN-SiN_x devices were irradiated at dose rates of 402 krad/hour for a total dose of 1 Mrad. Fig. 5.4 shows I_d-V_g profiles of reference devices not subject to irradiation compared to those that have, after being allowed to recover, unbiased, for several days after exposure. No significant change in V_t, g_{m_max}, I_{dss} and leakage properties is apparent, and indicates InAlN HEMTs are robust against gamma irradiation up to 1 MeV for short periods at dose rates beyond what would be expected in a space-based application.

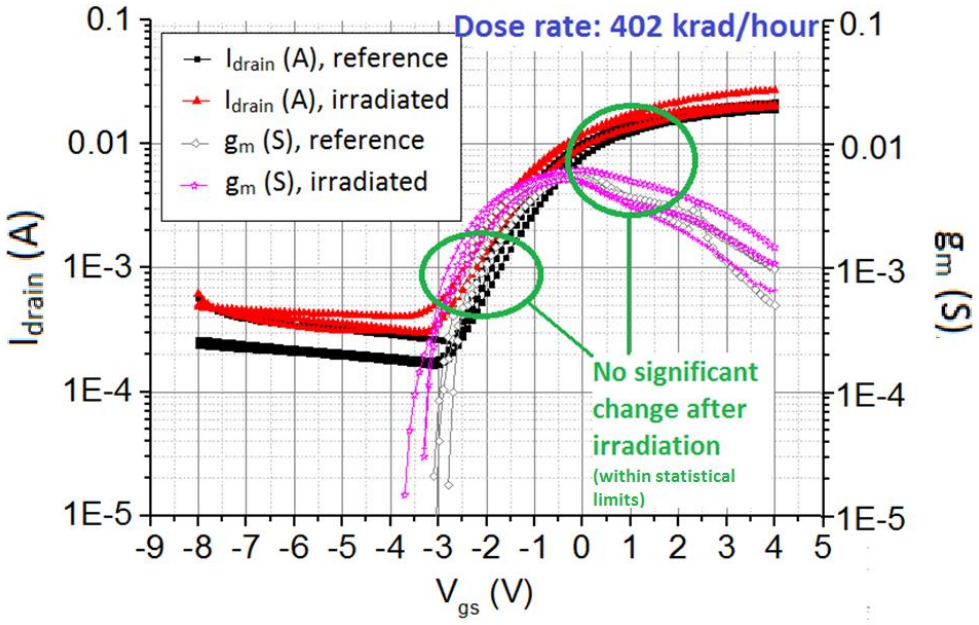

Fig. 5.4: I_d-V_g profile of InAlN HEMTs with SiN_x passivation, reference samples and those subject to 1 Mrad of 1 MeV gamma radiation at 402 krad/hour

The expected total ionizing dose for the ESA JUICE mission [1] is less than 1 Mrad over the entire mission lifetime assuming a 1 cm Al radiation shield is in place[258]. Clearly both InAlN and AlGaN HEMTs technologies are well suited for such an application, and may allow for a reduction of the radiation shielding to reduce the overall system weight. This may be stated due to the relative stability of the electrical characteristics under radiation exposure, especially for the production level AlGaN HEMTs where the change in performance compared to pre-exposed values was less than 5%. The robustness of III-nitride HEMTs against incident radiation may also open up previously prohibited applications such as in-situ monitoring of nuclear radiation environments, where dose rates are significantly higher than space applications but exposure times are typically much lower[259].

5.2 Off-state bias stressing and breakdown

Separate voltage step-stress experiments on equivalent devices were performed in parallel with gamma radiation hardness experiments, with bias maintained in the off-state (V_{gs} = -6 V) and at a source-drain bias of V_{ds} = 20 V for 5 minutes. This test plan

is in line with similar experiments reported in the literature [57,58] and was approved by the European Space Agency. Stress was applied under dark conditions, and a 15 minute relaxation time was allowed for trap release followed by execution of a DC characterization script. This test cycle was repeated with V_{ds} increasing by 10 V increments until breakdown, defined when drain leakage current reached 1 mA/mm. Fig. 5.5 is presented purely to highlight the necessity to conduct step-stress experiments under dark conditions, as ambient light may not be consistent and clearly facilitates the release of trapped charge that contributes to device conduction. The 15 minute relaxation time was chosen as being sufficiently long to allow trap release between consecutive step-stress/characterization stages and obtain enough measurements for valid statistics. Broader representations of parameter drift and breakdown voltages may show a dependence on stress/relaxation times[48, 59, 260], but are consistent here and should accurately reflect the comparative robustness of InAlN and AlGaN HEMTs.

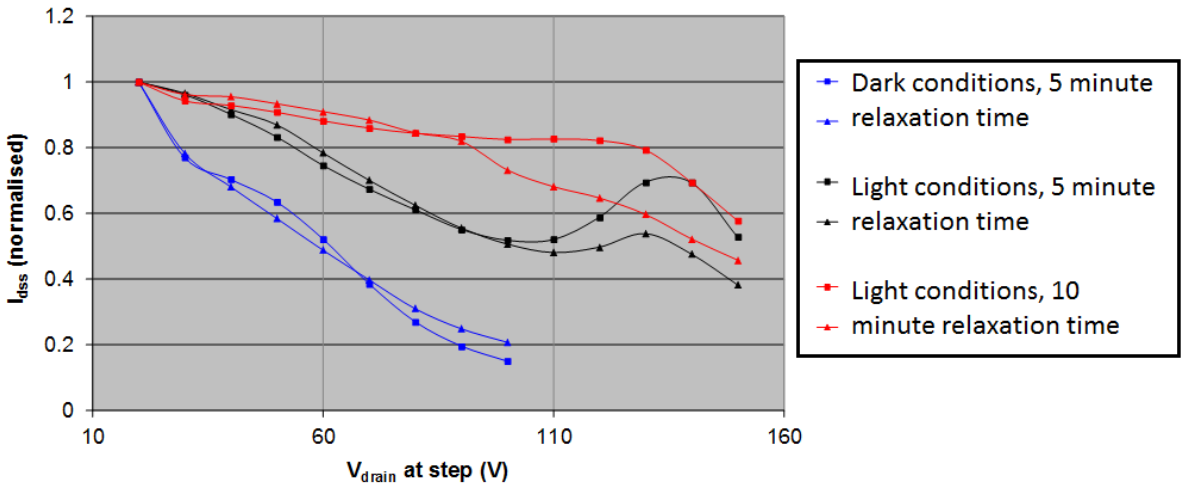

Fig. 5.5: The effect of a varied relaxation time and light/dark conditions on InAlN-SiN_x step-stress measurements, with two devices shown for each condition to indicate the inter-device variation.

Off-state voltage step-stress experiments are presented in Fig. 5.6, with breakdown voltages stated in Table 5.1. Production level AlGaN HEMTs show the highest degree of parameter stability under bias stressing showing virtually no parameter drift from pre-stressed values, confirming the lack of significant trapping behaviour present in the system. No breakdown occurred during off-state stress up to a drain bias of 150 V, with

leakage currents remaining stable at less than 0.1 mA/mm throughout. Of the research level devices, InAlN-uncapped HEMTs showed generally superior DC parameter stability during off-state bias step stress compared to AlGaN-uncapped devices. AlGaN HEMTs show generally the same trends regardless of surface capping, with AlGaN-SiN_x devices showing a marginal improvement in terms of I_{dss} and $I_{d\text{-}leak}$. AlGaN-SiN_x HEMTs showed gradually increased on-resistance (Fig. 5.6(b)) more-so than AlGaN-uncapped (without the spiking behaviour noted in one of the three AlGaN devices at V_{ds} = 30 and 50 V) while maintaining a larger proportion of I_{dss} (Fig. 5.6(a)), consistent with the capturing of an increased number of carriers at the source-gate access region of the AlGaN-SiN_x interface.

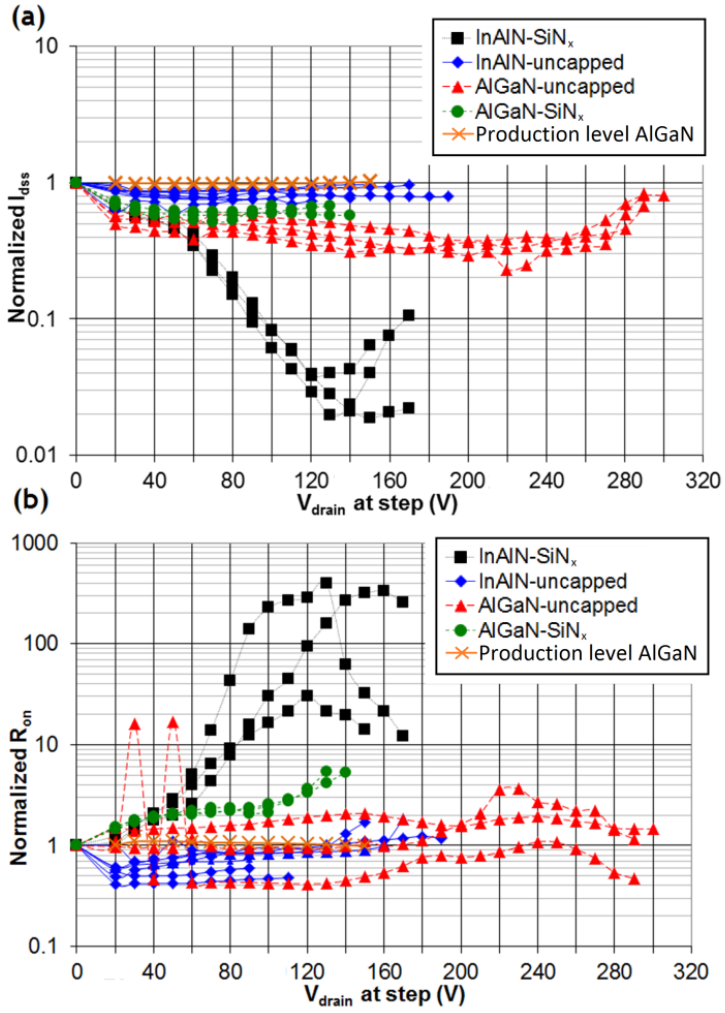

Fig. 5.6: (a) Saturated drain current and (b) on-resistance parameter evolution with off-state voltage step-stressing of uncapped and SiN_x capped InAlN and AlGaN HEMTs (including production level devices)

As well as having a more severe effect on channel current suppression for InAlN HEMTs than AlGaN (Table 4.1), the SiN_x cap here encourages further loss of remaining channel current (Fig. 5.6(a)) and transconductance during step-stressing. In Fig. 5.6(b) the normalised on-resistance of InAlN-uncapped HEMTs remains stable until breakdown, whereas for InAlN-SiN_x devices it continued to rise to greater than 100 times pre-stressed values, a significantly more severe effect than observed for AlGaN-SiN_x HEMTs. The depletion of both channel current and on-resistance implies SiN_x capping of InAlN HEMTs has generated ubiquitous SiN_x/barrier interface states that are accessible regardless of position relative to the gate.

Table 5.1: Breakdown voltages of InAlN and AlGaN HEMTs with and without SiN_x capping, including production level devices

	Step-stress breakdown voltage (V)	**Standard dev. (±)**	**Breakdown mechanism: gate or source?**
InAlN-uncapped	135	39	Depends on initial leakage values
InAlN-SiN_x	192	35	Gate
AlGaN-uncapped	> 300	NA	NA
AlGaN-SiN_x	130	20	Depends on initial leakage values
Production-level AlGaN	>150	NA	NA

Research level AlGaN-uncapped HEMTs exhibited the highest breakdown voltages of greater than 300 V, the upper bias limit of the experiment (discussed in Section 5.4), with AlGaN-SiN_x devices breakdown at drain voltages of 130 ± 20 V. Breakdown was defined as when $I_{d\text{-}leak}$ reached 1 mA/mm (see Section 2.6.3), and AlGaN-SiN_x breakdown channels were a mixture of gate-drain and source-drain (i.e. with $I_{s\text{-}leak}$ or $I_{g\text{-}leak}$ also reaching 1 mA/mm, respectively). The mechanism depended on the leakage currents of the virgin devices, with high initial off-state leakage encouraging gate-related collapse (Fig. 5.7(b)). AlGaN-SiN_x HEMTs with low initial leakage currents experienced source-drain breakdown via punch-through effects[59] (Fig. 5.7(a)) under significantly reduced bias conditions compared to AlGaN-uncapped devices, meaning SiN_x capping of AlGaN/GaN HEMTs acts to degrade channel robustness against bias stressing. This consistent with increased trap-related phenomena and is possibly helped by the

introduction of further epitaxial strain. The lack of a similar phenomenon in the (passivated) production level AlGaN HEMTs again highlights the critical importance of the capping layer/barrier interface with respect to robustness against radiation, thermal and off-state bias stress.

The routes to breakdown of InAlN-uncapped HEMTs, at 135 ± 39 V, similarly depended on the unstressed device leakage properties with gate-drain breakdown recorded for all devices registering initial leakage above a threshold of around 0.1 mA/mm (Fig. 5.7, where the measurement approach is discussed at the beginning of this section). The reduced breakdown voltages in InAlN-uncapped compared to AlGaN-uncapped devices are likely due to the higher initial leakage currents in InAlN layers.

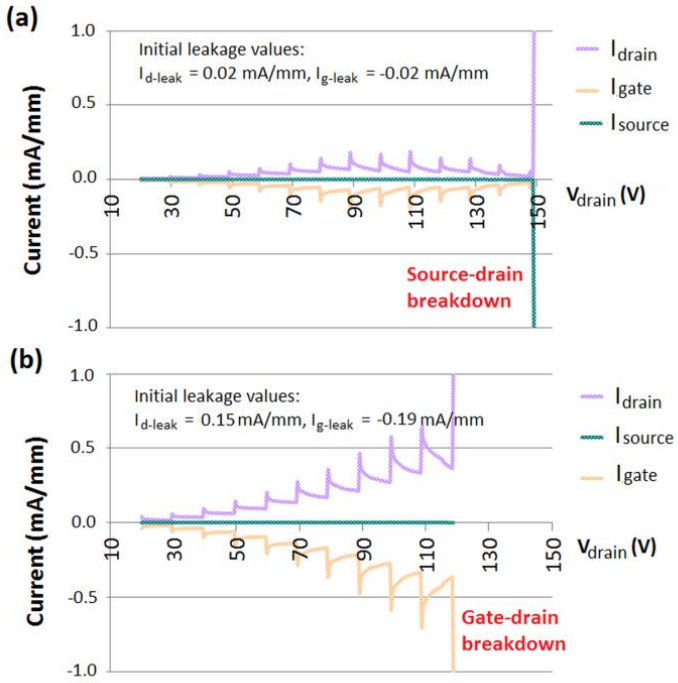

Fig. 5.7: Leakage currents during off-state bias step stressing of InAlN-uncapped HEMTs with (a) low initial leakage currents and source-drain breakdown and (b) initial leakage currents greater than 0.1 mA/mm and subsequent gate-drain breakdown

InAlN-SiN_x HEMTs showed improved breakdown voltages compared to the InAlN-uncapped case by around 60 V at 192 ± 35 V. This is likely due to surface leakage routes present only in the InAlN-uncapped case, elaborated on in Section 6.2.3, with the

tunnelling processes responsible highly sensitive to local electric fields and thus unsurprisingly manifesting as a reduction in off-state breakdown voltage. Another factor may be the larger currents passing through InAlN-uncapped HEMT channels during periodic step-stress characterization stages (see Table 5.1 and Fig. 5.6) and the resulting thermal build-up, rather than it being the case of the SiN_x cap acting to empower InAlN HEMT against off-state bias stressing, where we would expect a corresponding improvement in trap-related degradation[12].

5.3 Thermal stability of InAlN and AlGaN HEMTs

The thermal stability of III-nitride HEMTs reported in the literature is outlined in Section 2.7. In this section thermal stability is gauged from high temperature storage experiments with uncapped and PECVD SIN_x capped InAlN and AlGaN HEMTs and in-situ high temperature RF and DC characterization of SiN_x capped InAlN and AlGaN HEMTs. The SiN_x capping layer is shown to influence the thermal stability of electrical characteristics, although all devices showed a generally high degree of stability.

In the high temperature storage experiments, HEMTs were kept in dark conditions under vacuum at 250°C for four weeks, with I_d-V_d and I_d-V_g measurements taken after samples cooled to room temperature, intervals of one week. Subsequent recovery in the subsequent period during room temperature storage was also investigated. No immediate catastrophic damage was expected during storage at 250°C, as the process temperatures encountered during the final fabrication stages are 300°C for PECVD capped devices and 400°C (from the Schottky anneal) for the uncapped devices. Hot electron effects are not accounted for, as devices remained unbiased during thermal storage.

Fig. 5.8 shows the change in I_d-V_g (with V_{ds} = 10 V) characteristics after storage at 250°C. For the InAlN-uncapped HEMTs in Fig. 5.8(a) a shift in V_t of around -0.5 V occurs mostly after the first week, stabilising after three weeks. Maximum saturation current is unaffected here, although around 50% of InAlN-uncapped HEMTs showed a rise in leakage current of several orders of magnitude that stabilised after the initial increase

after one week. The increase in leakage was recorded at both gate and drain terminals, confirming it is associated with degradation of the InAlN barrier rather than the GaN channel layer due to the physical layout of the device layers and the fact that both the InAlN and AlGaN HEMTs utilized the same GaN buffer. For InAlN-SiN_x (Fig. 5.8(b)), V_t and leakage currents are stable throughout the thermal storage period. Saturation current rises significantly after the first week, stabilising to the values recorded in InAlN-uncapped HEMTs after three weeks. After the fourth week of storage at 250°C a significant change in the IV profile is noted, also occurring in AlGaN-SiN_x devices (Fig. 5.8(d)), suggesting it is associated with degradation of the SiN_x passivation layer (this behaviour is currently not fully understood). A further examination of the drift in DC parameters of InAiN-SiN_x and InAlN-uncapped HEMTs is given in Section 6.2.1 (Fig. 6.12) with reference to optimisation of the SiN_x PECVD process and leakage current mechanisms.

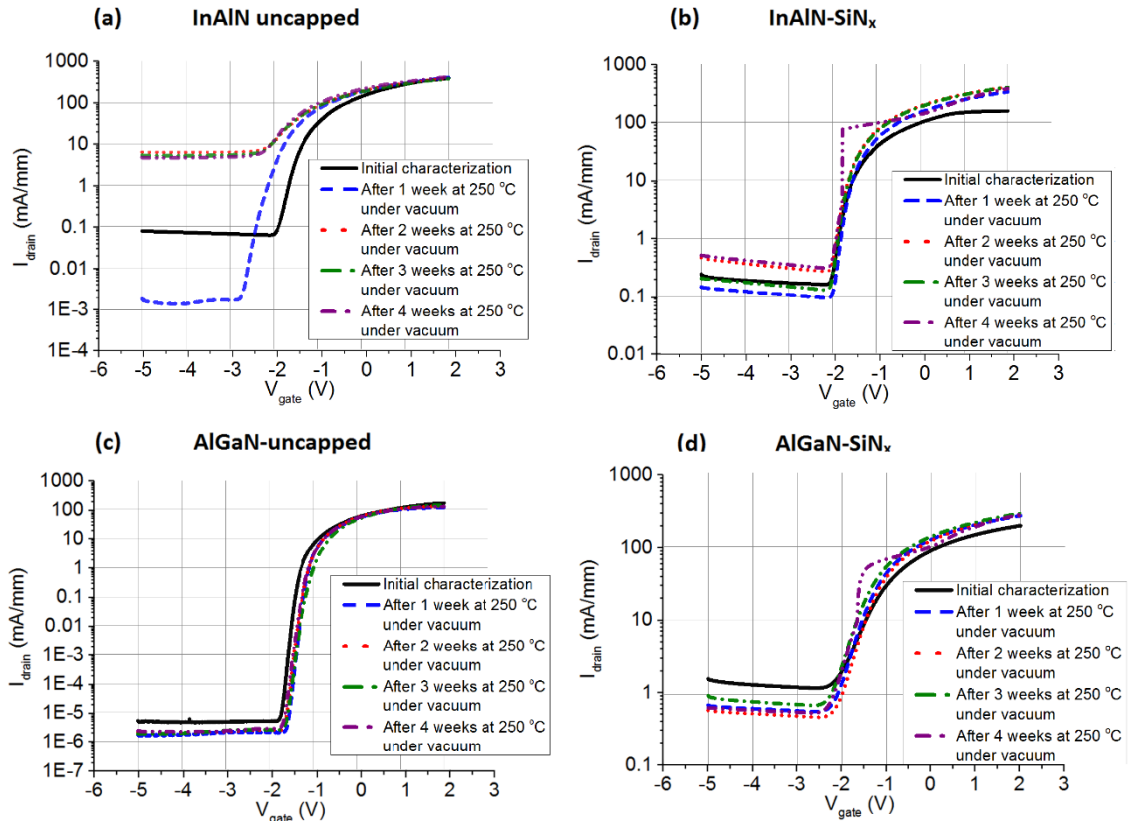

Fig. 5.8: I_d-V_g (with V_{ds} = 10 V) plots for (a) InAlN-uncapped (b) InAlN-SiN_x (c) AlGaN-uncapped and (d) AlGaN-SIN_x after storage at 250°C for four weeks

AlGaN-uncapped HEMTs (Fig. 5.8(c)) show a shift in V_t of +0.25 V after the first week, before showing a slight (~ 0.1 V) drift in either direction across the sample set in the following weeks. Saturation current is mostly stable, although two devices with initially low I_{dss_max} apparently recovered after 1 week thermal storage. Leakage current remains low allowing for a high on-off ratio to be maintained throughout the thermal storage period. The different turn-on characteristics of the AlGaN-uncapped and AlGaN-SiN_x HEMTs in Fig. 5.8(c) and (d) are due to the larger barrier layer thickness of the AlGaN-SiN_x samples in this case (20 nm c.f. 15 nm for AlGaN-uncapped).

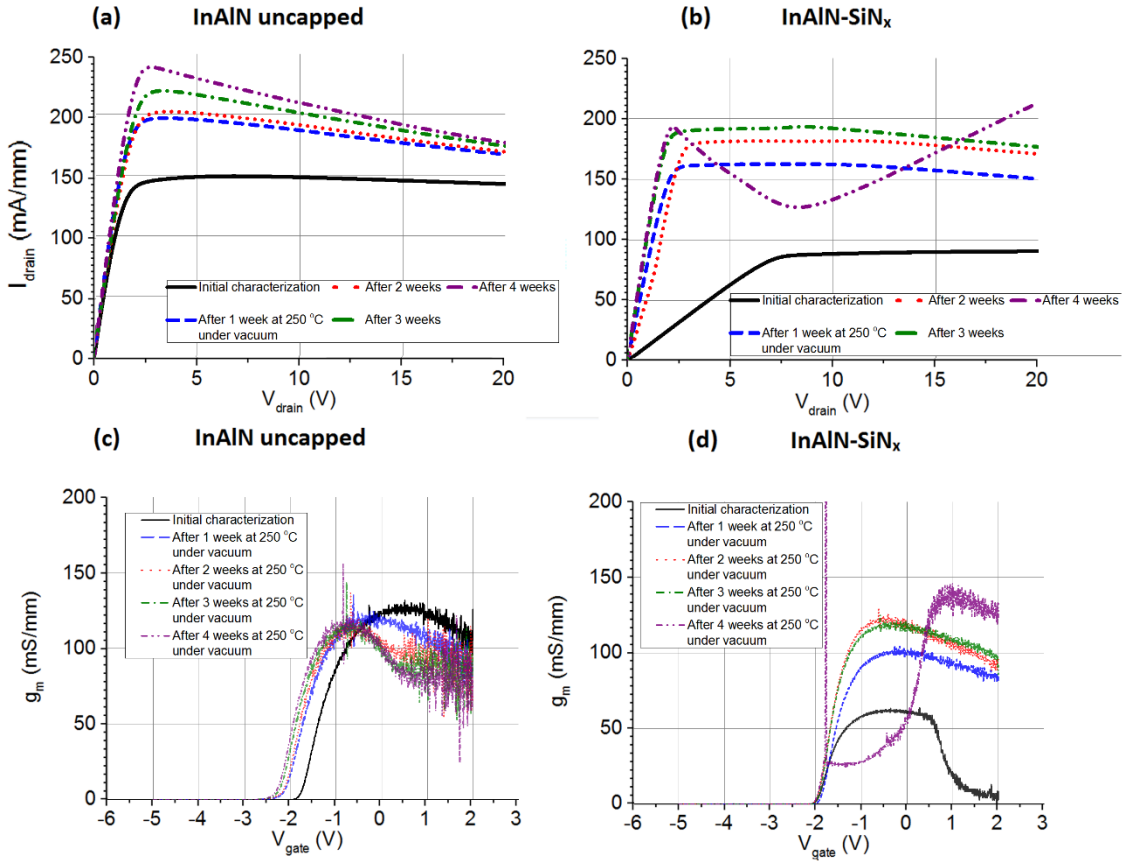

Fig. 5.9: I_d-V_d (with V_{gs} = 0 V) plots for (a) InAlN-uncapped (b) InAlN-SiN_x and transconductance from I_d-V_g (with V_{ds} = 10 V) plots for (c) InAlN-uncapped and (d) InAlN-SiN_x after storage at 250°C for four weeks

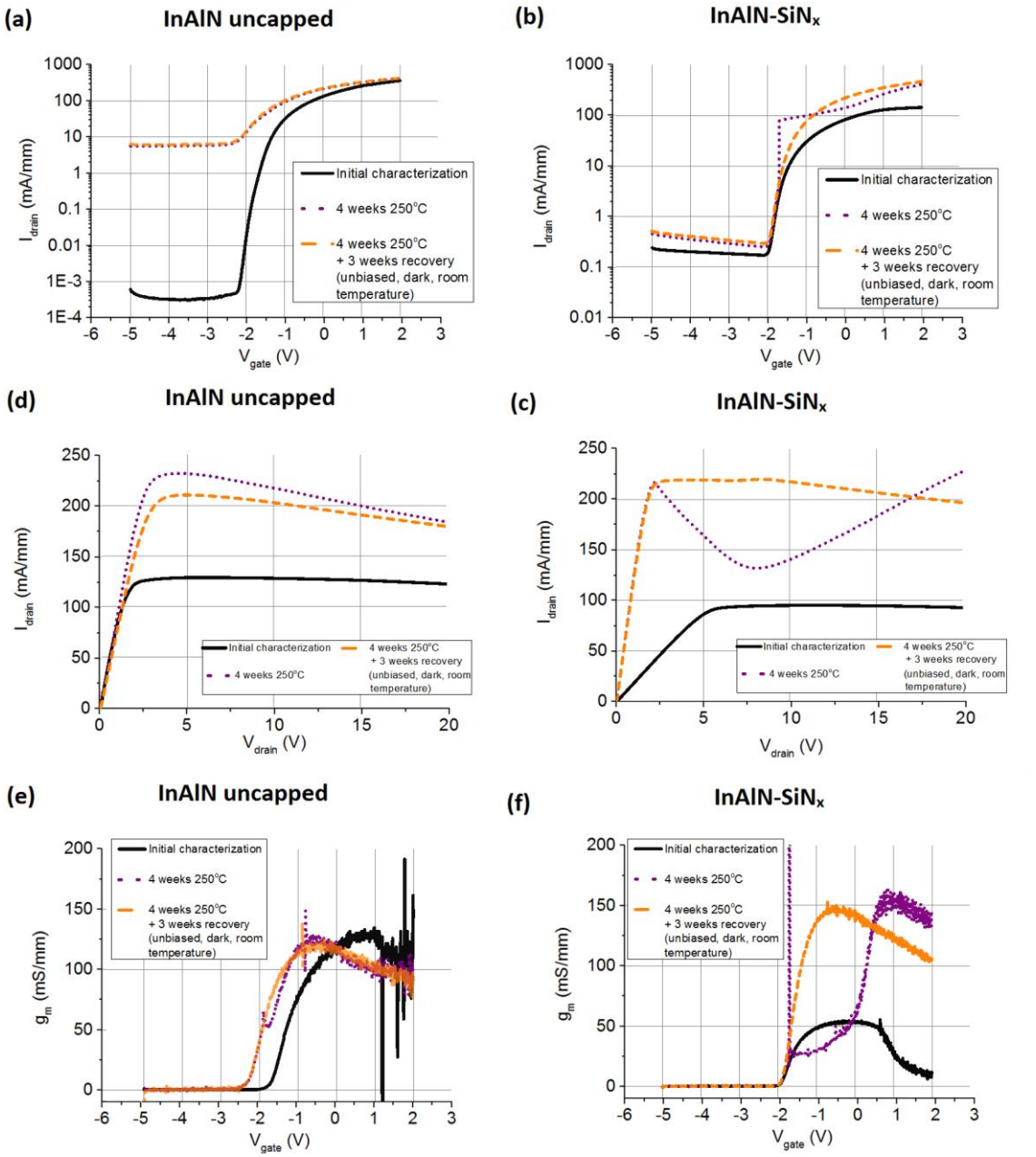

Fig. 5.10: I_d-V_g (with V_{ds} = 0 V) plots for (a) InAlN-uncapped (b) InAlN-SiN_x I_d-V_d (with V_{gs} = 0 V) plots for (c) InAlN-uncapped (d) InAlN-SiN_x and transconductance from I_d-V_g (with V_{ds} = 10 V) plots for (e) InAlN-uncapped and (f) InAlN-SiN_x after storage at 250°C for four weeks and recovery at room temperature for three weeks

R_{on} was stable for InAlN-uncapped devices (Fig. 5.9(a)). For InAlN-SiN_x HEMTs, R_{on} decreased stabilising to values seen for InAlN-uncapped devices, in a similar way to saturation current. After four weeks the unusual behaviour is again attributed to degradation of the SiN_x cap, being present in AlGaN-SiN_x devices also. For transconductance of InAlN HEMTs in Fig. 5.9(c) and (d), the noise behaviour in the

uncapped devices (present also in pre-stressed samples) is absent for HEMTs with SiN_x capping, also the case for AlGaN HEMTs. InAlN-SiN_x devices show a recovery of transconductance to uncapped values in line with saturation current and on-resistance, before showing the similar breakdown properties after the fourth week in which the noise phenomena is present.

After the characterization at four weeks the devices were left unbiased at room temperature in dark conditions for three weeks before being characterized again (Fig. 5.10). Both InAlN and AlGaN HEMTs with and without SiN_x capping showed performance recovery to the best values seen throughout the experiment. In particular the anomalous behaviour of InAlN-SiN_x and AlGaN-SiN_x devices after four weeks at 250°C, in terms of the I_d-V_d and I_d-V_g profiles, is not present after the recovery phase. This suggests the change is electronic rather than structural, where a permanent change would be expected.

In-situ DC and RF thermal stability of InAlN-SiN_x and AlGaN-SiN_x HEMTs over the range -25°C to +125°C is shown in Fig. 5.11. With respect to DC parameters (I_{dss}, g_{m_max}, R_{on}, V_t, Fig. 5.11(a) – (d)) InAlN-SiN_x show superior thermal stability in all categories compared to AlGaN-SiN_x devices. The RF cut-off frequencies (f_T and $f_{MAG10dB}$) show a less clear distinction. RF characteristics were dominated here by capacitance (Section 4.4), which remained mostly stable for both InAlN-SiN_x and AlGaN-SiN_x devices. Gate and drain leakage showed a positive correlation with temperature (Fig. 5.12), with InAlN-SiN_x HEMTs showing superior thermal stability, although with a less clear trend due to the poor inter-device uniformity.

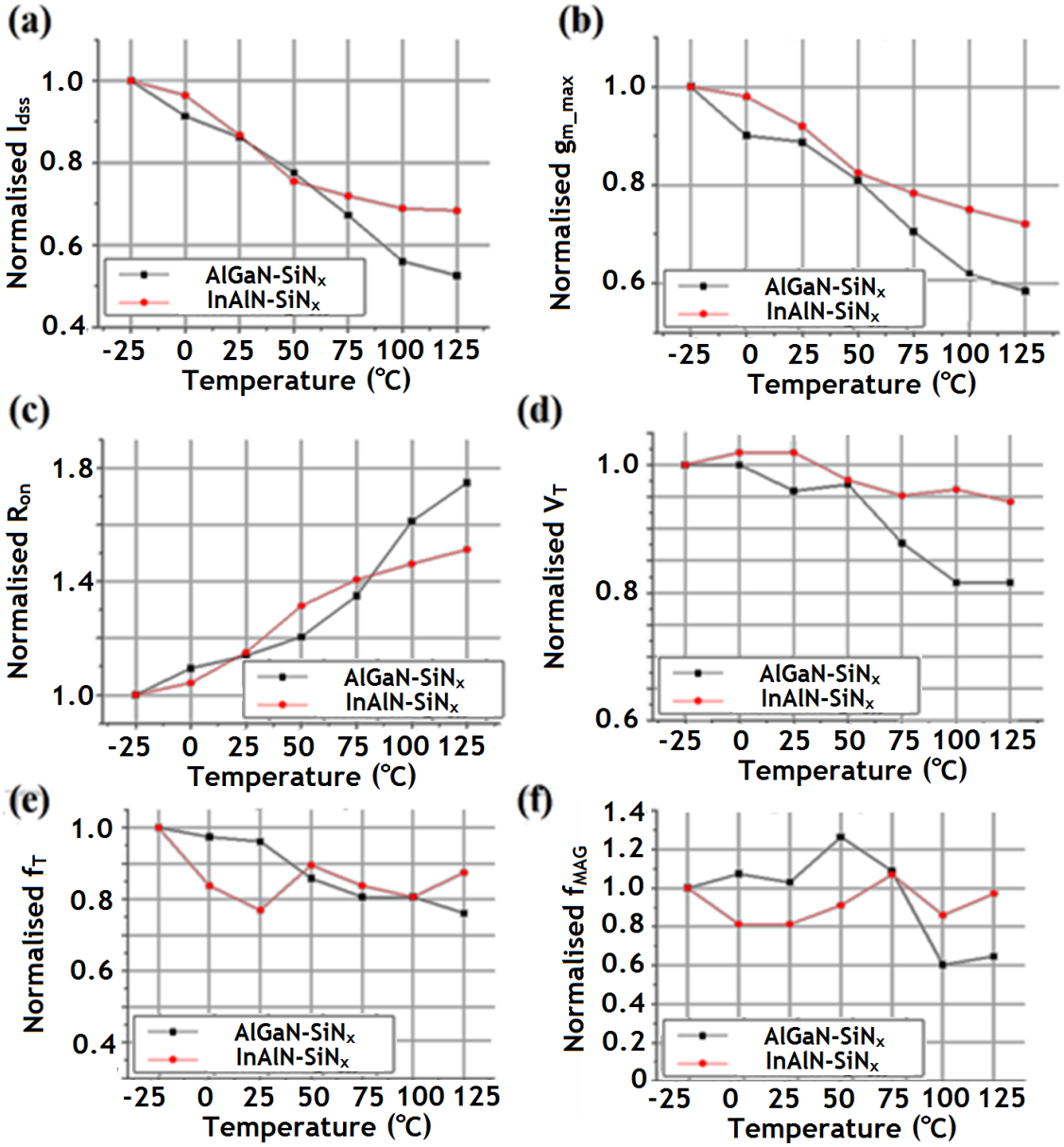

Fig. 5.11: In-situ DC and RF thermal stability measurements for InAlN-SiN_x and AlGaN-SiN_x HEMTs

All SiN_x capped devices tested in-situ at -25°C to +125°C showed recovery to with 2% of pre-stressed values in all cases for all DC and RF parameters after being stored at room temperature for 24 hours.

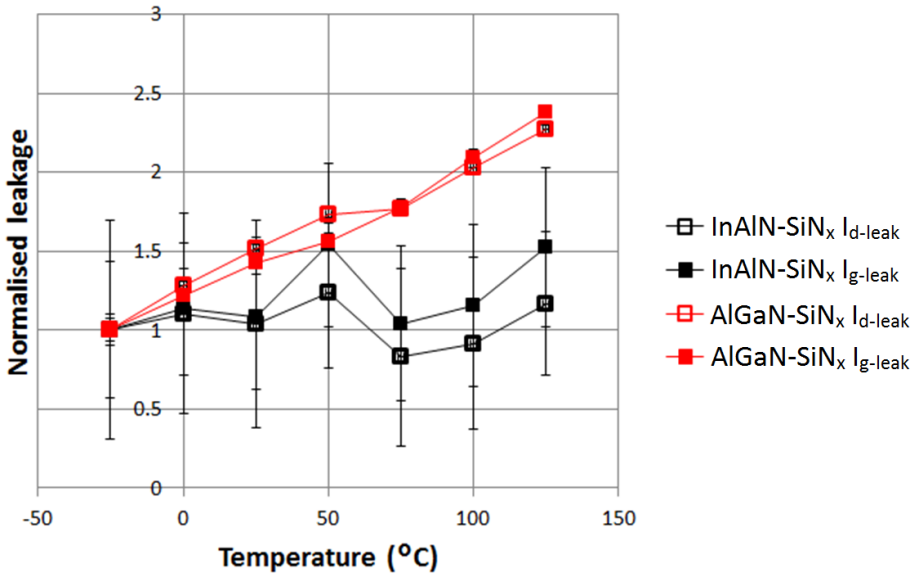

Fig. 5.12: In-situ off-state leakage thermal stability measurements for InAlN-SiN_x and AlGaN-SiN_x HEMTs

5.4 Discussion of reliability and failure analysis

The general properties of III-nitride HEMTs shown in this chapter highlight their overall stability. The total ionizing doses used here (1 – 10 Mrad) on unshielded III-nitride devices resulted in no significant degradation except in the case of samples with non-optimised surface passivation, and are similar to those quoted as the failure limits for conventional Si and III-V based technologies [157, 261], i.e. the III-nitride HEMTs tested here generally did not undergo failure. The commercially available performance-optimised AlGaN HEMTs included in the experiments in Section 5.1 showed superior DC transport properties and reduced leakage despite similar device geometries to the research level counterparts. Improved performance correlated with strong stability in terms of both radiation hardness and bias step-stressing, with breakdown voltages of > 150 V, suggesting a link between the manufacturing routes to performance and stability optimisation. The stability of the production level AlGaN HEMTs confirms III-nitride transistor technology is a suitable candidate for space-based applications, being robust against total ionizing dose radiation.

For the uncapped research level devices described here, InAlN HEMTs generally showed superior stability of DC properties throughout the duration of ^{60}Co gamma radiation exposure. Uncapped AlGaN HEMTs and to a lesser extent InAlN HEMTs show parameter degradation consistent with cumulative charge build up around the active region influencing local electric fields and conduction paths, likely caused by the introduction of trap states induced by incident radiation. The increased resistance of InAlN to such effects is likely due to its large bandgap and associated defect state energy levels[166, 262, 263] and despite the weaker average bond strength compared to AlGaN[264].

Charge trapping at the capping layer/barrier interface dominated the radiation hardness and breakdown behaviour of SiN_x capped research level devices, which may be attributed to the immaturity of the PECVD processing methods implemented here. InAlN-SiN_x HEMT device performance suffered more severely than that of AlGaN-SiN_x HEMTs (see DC characteristics shown in Table 3.3), as well as showing increased reductions in radiation hardness and robustness under bias stressing. The PECVD SiN_x cap used here introduces inherent parameter trap-related instability in InAlN HEMTs, prone to aggravation by electrical stress and radiation exposure as evidenced by the data shown in Figs. 5.2, 5.3 and 5.6. PECVD SiN_x capping stabilised AlGaN HEMTs against parameter degradation under off-state stress and radiation exposure (Figs. 5.3 and 5.6) but acted to increase leakage and reduce breakdown voltage to 130 ± 20 V from greater than 300 V, consistent with the introduction of localised channels allowing the slow release of trapped charge, probably at the AlGaN-SiN_x interface, with reduced breakdown fields[255, 265]. The severity of performance and reliability degradation when SiN_x capping is included in InAlN HEMTs compared to AlGaN HEMT devices is believed to stem from the differing surface electronic trap energy and behaviour associated with the barrier layer materials[262, 263]. Effective surface passivation to limit virtual gate effects is critical to fully exploit high AlN barrier content, reduced gate-channel separation and favourable band structure[12] in lattice matched $In_{0.18}Al_{0.82}N$/GaN structures.

The changes in electrical behaviour after thermal storage for uncapped devices compared to those with SiN_x capping provides further evidence that carrier trapping at the barrier/SiN_x interface is the dominant controlling mechanism, especially in the case

of InAlN. This behaviour is elaborated on and referenced in Section 6.2, where the change in electrical characteristics with temperature is used to identify leakage pathways in uncapped and SiN_x passivated InAlN and AlGaN HEMTs. The negative shift in threshold voltage for InAlN-uncapped after storage at 250°C is symptomatic of positive charge accumulation under the gate, possibly caused by the activation of donor traps, while stable on-resistance and saturation current suggest the InAlN surface is unaffected. In contrast the transformation of InAlN-SiN_x on-resistance and saturation current to uncapped values and stable threshold voltage indicate a migration of trapped carriers from the gate-drain and gate-source access regions and not beneath the gate. The release of carriers from the barrier/SiN_x interface increases the 2DEG density and also modifies the band structure to increase E_F - E_C (i.e. the difference between the conduction band and Fermi level, see Fig. 2.3).

In-situ electrical characterization over an ambient temperature range shows that despite the significantly increased effect of barrier/SiN_x carrier trap phenomena for InAlN-SiN_x devices than for AlGaN-SiN_x, as evidenced by the analysis of performance, radiation stability, pulsed IV and breakdown behaviour, InAlN-SiN_x HEMTs show superior thermal stability in terms of DC and RF characteristics. This is possibly due to a reduced optical phonon lifetime in the strain-free environment of the InAlN/GaN lattice matched heterojunction[146]. The dual-frequency PECVD SiN_x deposition scheme here was designed to prevent the introduction of additional strain into the system, which it appears to have done successfully despite the side-effect of parasitic trap phenomena.

The potential of InAlN HEMTs to exhibit superior thermal stability and radiation robustness to AlGaN devices shown by comparing the uncapped research level devices in this work is undermined by the trap-induced degradation incurred by non-optimised PECVD SiN_x capping, to which InAlN appears more susceptible. This highlights the requirement to further develop InAlN HEMT design, material epitaxy and device fabrication techniques in order to fully exploit the performance and reliability advantages they potentially offer industries such as the space sector. Defect trap states and internal electric fields must be managed in order for InAlN HEMTs to fully exhibit the reliability advantages offered by the a strain-free heterointerface and favourable conduction band properties allowing for advanced device geometries. In particular a

surface passivation technique that effectively suppresses RF dispersion but does not degrade DC performance and stability under stress must be developed, taking into account the high sensitivity of ultra-thin barrier InAlN HEMTs to surface electrostatics. Optimisation of SiN_x PECVD conditions[266] and surface treatments[267], thermal oxidation[266], SiN_x deposited in-situ[146] and Al_2O_3 deployed by atomic layer deposition[100] are suitable candidates worthy of investigation, and the process is examined in Section 6.2. In-situ SiN_x capping of InAlN/AlN/GaN heterostructures conducted in parallel with this work was found to collapse wafer conductivity, suggesting significant process optimisation is indeed necessary to achieve effective surface passivation. However, the results from the production level AlGaN HEMTs, with an optimised production process, combined with the demonstration of RF dispersion-free InAlN HEMTs in the literature indicate this issue is solvable and InAlN HEMTs should be further developed for applications requiring reliable operation under extreme ambient conditions such as the space sector. Due to the relative immaturity of the III-nitride HEMT technology there is no current 'standard' against which to compare the performance degradation – however, it is hoped that the results presented here would serve as one possible reference point for such attempts in the future.

5.5 Chapter Summary

This chapter has explored the robustness of III-nitride HEMTs to radiation, elevated temperatures and off-state bias stressing. Both InAlN and AlGaN HEMTs showed good radiation hardness, maintaining operation after a gamma radiation dose of 9.12 Mrad at a dose rate of 6.6 krad/hour over a period of two months, and exhibited good thermal stability by maintaining reasonable performance after storage at 250°C for four weeks. Well-optimised AlGaN HEMTs from a commercial supplier showed particularly high stability, establishing a link between optimisation of device performance and that of reliability. Potential failure routes present in InAlN HEMTs that are absent for AlGaN HEMTs were identified, particularly with regard to thermal stability and breakdown properties. These findings led to the optimistion of InAlN and AlGaN HEMTs described

in Chapter 6, and especially the optimisation of the problematic parasitic leakage routes in InAlN devices that is believed to be responsible for device failure.

6. III-nitride HEMT fabrication process optimisation

This chapter describes the successful attempts at InAlN and AlGaN HEMT fabrication optimisation. With regard to Ohmic contacts, Ti/Al/Ni/Au metal stack thickness ratios and anneal conditions were shown to be critical to InAlN HEMT performance using in-situ high temperature TEM and analysis of electrical characteristics. An optimised contact fabrication process was demonstrated for both InAlN and AlGaN HEMTs. InAlN HEMT surface passivation was also explored with an emphasis on the transfer of the PECVD SiN_x process used in AlGaN HEMT manufacture. An optimised PECVD process was demonstrated and the anomalous surface properties of InAlN HEMTs were investigated through analysis of off-state gate diode leakage behaviour.

6.1 Ti/Al/Ni/Au Ohmic contact formation

6.1.1 Ti/Al/Ni/Au Ohmic contacts to InAlN HEMTs

As discussed in Chapter 2, $In_{0.18}Al_{0.82}N$/AlN/GaN heterostructures offer high carrier densities and mobilities eliminating inherent instabilities in AlGaN HEMTs[12] associated with the highly strained AlGaN barrier layer that is significantly lattice mismatched with GaN. Exploiting the conducting properties of the 2-dimensional electron gas (2DEG) within the InAlN/AlN/GaN heterostructure requires low resistance electrical contacts, typically using Ti/Al based stacks annealed at temperatures of around 800°C, as in Fig. 6.1[72, 268]. Behaviour of Ti/Al based contact formation to AlGaN/GaN heterostructures is understood to be based on the formation of TiN_x compounds[71, 74], resulting in conduction paths facilitated by nitrogen vacancies and thermionic field-emission across ultra-thin Schottky barriers formed during annealing[269]. Recent interpretation of electrical characteristics and constructional analysis suggests InAlN/AlN/GaN structures obey similar principles[72].

Reports applying a parallel resistive network model to InAlN and AlGaN HEMTs suggest that Ti/Al/Au based contact schemes are consistent with alloy mixing of contact metals during annealing resulting in Au rich regions[270], confirmed in this work and shown

later in this chapter. Here we present analysis of Ti/Al/Ni/Au (t_{Ti}/50/50/t_{Au} nm) stacks on $In_{0.18}Al_{0.82}N$/AlN/GaN heterostructures annealed under N_2 and vacuum, and the effects of a varied t_{Au}, t_{Ti} and anneal conditions on structural and electrical properties of the contact are gauged. Contact morphology under different anneal conditions was explored, and imaging of roughening at the metal-epilayer interface by real-time in-situ high temperature transmission electron microscopy (HT-TEM) correlates with a sharp increase in measured sheet resistance.

InAlN/AlN/GaN (5/1/1000 nm) heterostructures on c-plane 2" sapphire substrates by a commercial supplier with AlN nucleation layers were grown using metal organic vapour phase epitaxy (MOVPE) (Section 3.3.1). GaN buffer layers were confirmed insulating by C-V depletion measurement, with residual capacitance under reverse bias less than 0.1 pF (the resolution of the equipment). A lift-off UV photolithographic method was used for pattern definition and a Cl_2-based inductively-coupled plasma (ICP) reactive ion etch was used to define mesa structures (Section 3.4.2). Surfaces were cleaned by 10 s dip in a HF-based solution with DI rinse and N_2 blow dry prior to Ti/Al/Ni/Au contact evaporation. The Ti stack thicknesses (t_{Ti}) used were 3, 10 and 25 nm, with Al and Ni stack thicknesses were both fixed at 50 nm throughout. Au thickness ranged from 5 to 250 nm, initially based on previous successful implementation of low resistance Ohmic contacts to n-type GaN. A rapid thermal processor (RTP) was used to anneal the samples at temperatures up to 925°C under vacuum conditions or 100 sccm N_2 flow, and allowed to cool via natural convection.

Ungated circular (CTLM) and linear (uTLM) transmission line measurement structures were used to determine sheet resistance and contact resistivity, with contact morphology monitored by optical and electron microscopy. Energy-dispersive X-ray spectroscopy (EDX) from scanning transmission electron microscopy scans was used to characterise microscopic structures formed after annealing under N_2. InAlN/AlN/GaN lamellas with Ti/Al/Ni/Au (3/50/50/50 nm) and (10/50/50/50 nm) created by focussed ion-beam etching on a copper stage were imaged by transmission electron microscopy (TEM) and heated in-situ under vacuum conditions to 980°C. The increase of temperature with time during TEM was held as close as possible to the ramping during contact annealing via RTP, trailing by approximately a factor of two due to the need to

recalibrate the TEM at elevated temperatures. The structural and electrical properties of InAlN HEMTs annealed under vacuum and N_2 were compared by Hall measurement and TLM evaluation.

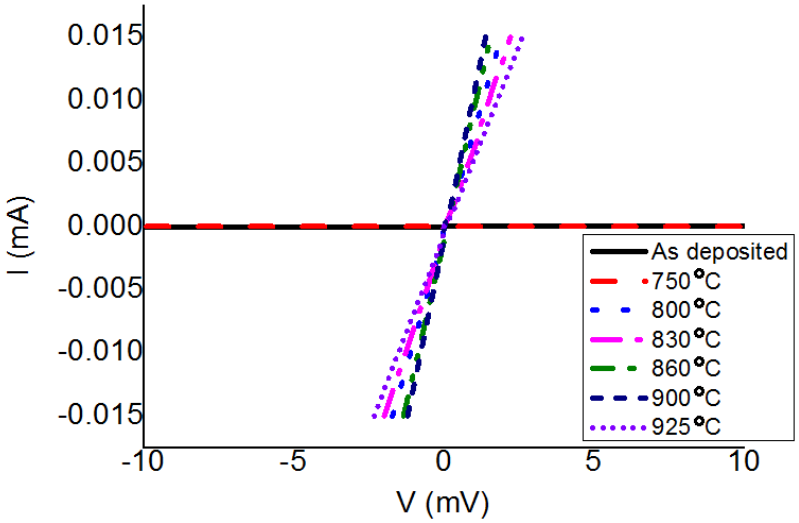

Fig. 6.1: Voltage-current profiles of InAlN/AlN/GaN heterostructures with Ti/Al/Ni/Au (10/50/50/50 nm) contacts annealed at different temperatures

Hall measurement of pre-processed InAlN/AlN/GaN epilayers yielded results of 260 Ω/□, 1320 cm^2/V.s and 1.8 x10^{13} cm^{-2} for sheet resistance, mobility and carrier density, respectively. After surface cleaning via a 10 s dip in HF-based solution sheet resistance increased to 480 Ω/□, with mobility and carrier concentration decreasing to 880 cm^2/V.s and 1.5 x10^{13} cm^{-2}, respectively, which is attributed to the removal of the native oxide layer. The change in carrier density upon HF-based cleaning is attributed to a shift in conduction band pinning at the upper barrier layer boundary due to a renewed surface chemistry. The reduction in mobility may be understood in terms of a change in barrier layer piezoelectric polarisation component due to the strain alleviated after the removal of the native oxide[147] and scattering due to remote charges[271]. Atomic force microscopy before and after the HF-based etch did not reveal any modification to surface morphology suggesting the scattering contribution due to interfacial roughness is unchanged. A higher ratio of mobility at 77 K compared to that at room temperature after the HF-based etch indicates phonon scattering due to thermal lattice vibrations is

more dominant after the removal of the native oxide, attributed to an increased decay time of longitudinal optical phonons to acoustic modes[147]. The change in polarisation charge across the system will also contribute to the shift in carrier density.

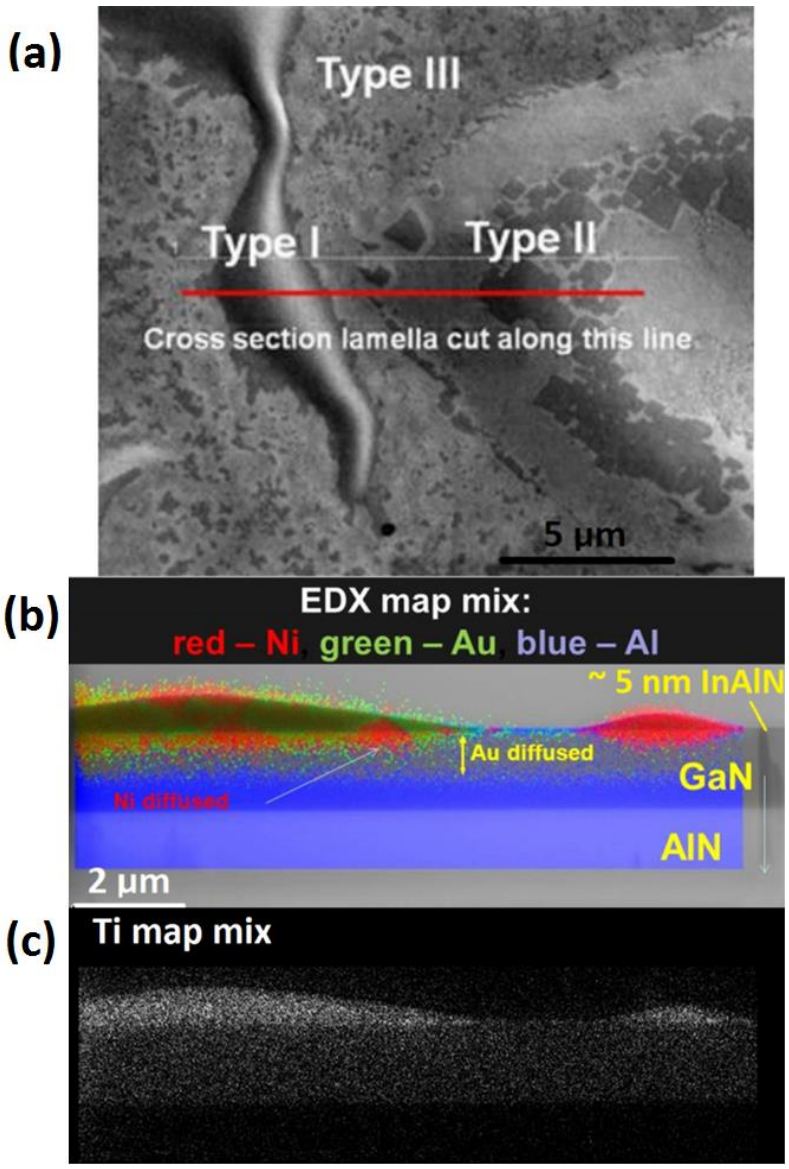

Fig. 6.2: (a) STEM and (b) EDX map of Ti/Al/Ni/Au (3/50/50/50 nm) contacts to InAlN/AlN/GaN heterostructures annealed at 850°C showing Ni, Al and Au maps, and (c) with the EDX Ti map

For Ti/Al/Ni/Au (t_{Ti}/50/50/t_{Au} nm) contacts linear current-voltage characteristics corresponding to Ohmic contact behaviour are only formed at anneal temperatures of above 750 - 800°C, as shown in Fig. 6.1. Contact resistivity ascertained from CTLM

evaluation scaled with t_{Au} after annealing at 850°C. A low contact resistivity of 1 x10^{-5} Ω.cm^2 with a 250 nm thick Au layer was accompanied by extensive, catastrophic µm-scale blistering and lateral diffusion at contact boundaries. Reducing the Au thickness to 10 nm increased contact resistance to 5 x 10^{-3} Ω.cm^2, and at t_{Au} = 5 nm contact resistance was in excess of 10^{-1} Ω.cm^2. As well as preventing out-diffusion and oxidation of underlying contact metals during annealing, a primary function of the Au layer is to reduce lateral resistivity within the contact, which is undermined by the deformation of morphology. An intermediate value of t_{Au} = 50 nm provided acceptably low contact resistance and levels of lateral diffusion during annealing. STEM imaging and EDX composition mapping of a Ti/Al/Ni/Au (3/50/50/50 nm) contact annealed at 850°C under N_2 are shown are Fig. 6.2.

STEM imaging and EDX composition mapping of a Ti/Al/Ni/Au (3/50/50/50 nm) contact annealed at 850°C under N_2 are shown are Fig 6.2(b) and (c). Ni and Au are shown to have penetrated the nitride crystal layer to a depth of order 100 nm. Three distinct morphological features are identified across contact surfaces on macroscopic scales, labelled Type I, II and III. Type I (Ni rich) and Type II (Au rich) features are separated by thin Al rich Type III regions. Ti is detected in Type I, Type II and Type III regions in equal quantities.

Surface morphology of Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) contacts with t_{Ti} = 3, 10 and 25 nm are shown in Fig. 6.3. The size and rate of development with respect to temperature of Type I, II and III regions shows a clear dependence on t_{Ti}, with the intermediate value of t_{Ti} = 10 nm exhibiting the highest stability in terms of roughening and chromatic variation. Contacts annealed under vacuum conditions at 850°C show similar surface features to contacts annealed under N_2 at similar temperatures (Fig. 6.3(d), (g) and (j)). At temperatures approaching 900°C contacts with t_{Ti} = 25 nm turned blue in colour (Fig. 6.3(l)), as did a small number of contacts with t_{Ti} = 10 nm, correlating with a sharp increase in lateral resistance to levels not associated with metals (> 1 MΩ/□) indicating the formation of electrically insulating compounds in large amounts.

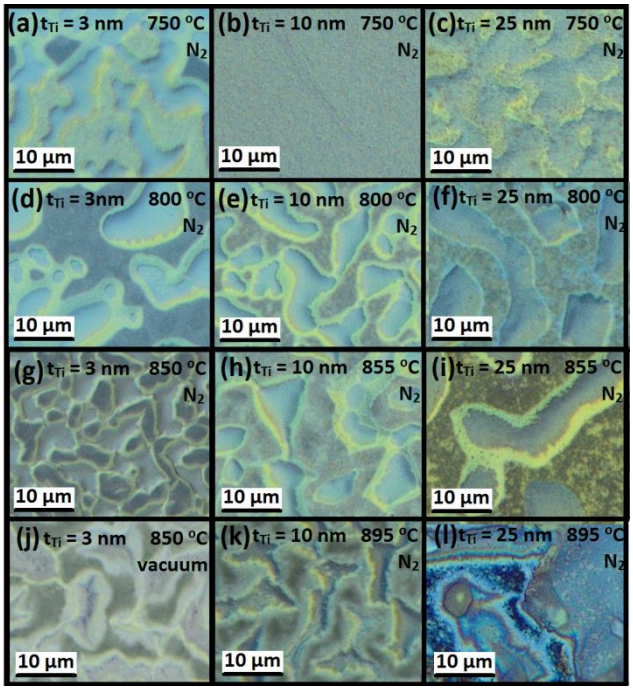

Fig 6.3: Differential contrast interference microscopy imaging of Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) on InAlN/AlN/GaN epilayers annealed for 60 s, with annotations of the t_{Ti} value and the anneal environment/temperature

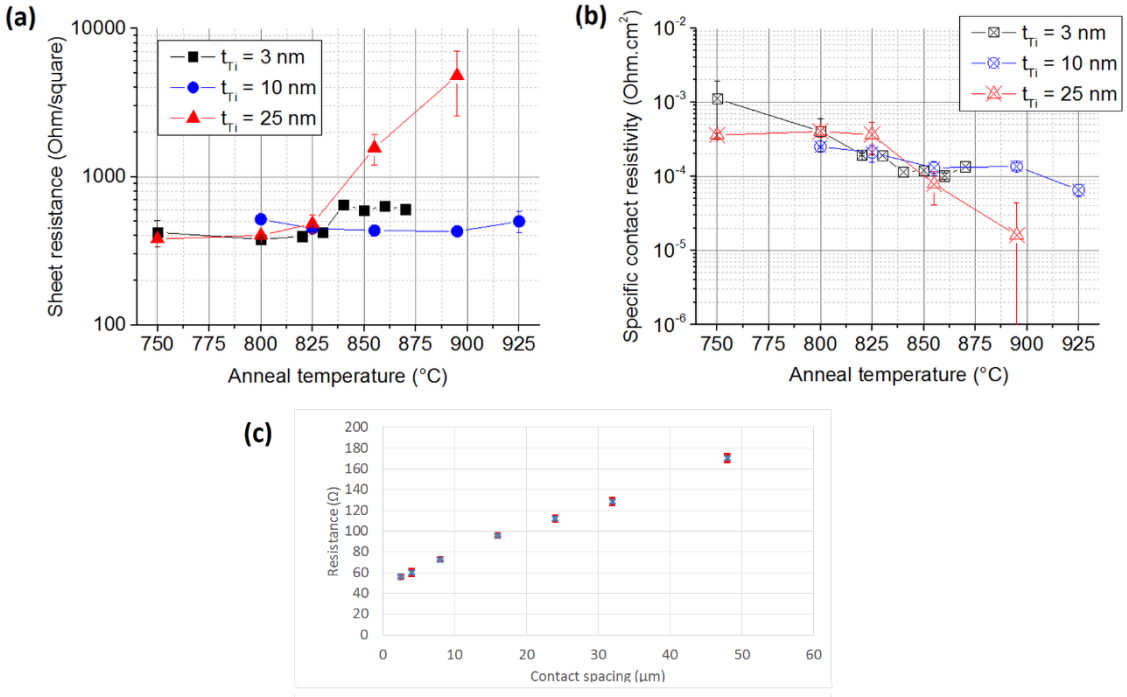

Fig. 6.4: (a) Sheet resistance and (b) specific contact resistivity of Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) contacts to InAlN/AlN/GaN heterostructures annealed at for 60 seconds under N_2 from evaluation uTLM test features. (c) shows an example TLM plot of resistance vs. contact spacing

The effect of anneal temperature on sheet resistance for different values of t_{Ti} is shown in Fig. 6.4(a). Sheet resistance is stable around the value attained by Hall measurement (~ 480 Ω/□) until rising at some critical temperature, with the extent and onset of the increase apparently dependent on the value of t_{Ti}. For t_{Ti} = 3 nm the sheet resistance abruptly rises to around 700 Ω/□ at an anneal temperature of 830°C, stabilising immediately. For the case of t_{Ti} = 25 nm a rise is apparent at the same anneal temperature without stabilization, leading to a rapid increase, whereas for t_{Ti} = 10 nm very little change is noted.

Contact resistivity is in the low 10^{-4} Ω.cm^2 range for all samples regardless of the value of t_{Ti} in the anneal temperature range 800 - 850°C, decreasing steadily as the anneal temperature increases. As shown in Fig. 6.1, contacts with t_{Ti} = 10 nm do not become Ohmic until annealed at 800°C, in contrast to the cases with t_{Ti} = 3 nm and 25 nm that provide low resistance contact at 750°C. This is presumed due to the difference in the onset of inter-metallic mixing and morphology variation seen in Fig. 6.3(a), (b) and (c). Contact resistivity in all cases decreases moderately with anneal temperature until 925°C. For t_{Ti} = 3 nm contact resistivity decreases with anneal temperature until reaching 1 x 10^{-4} Ω.cm^2 and stabilising at 830°C, the same anneal temperature at which the sheet resistance abruptly rises in the same sample set. For t_{Ti} = 25 nm the contact resistivity is stable at around 3 x 10^{-4} Ω.cm^2 until 825°C. At this point it decreases with increased anneal temperature, reaching the low 10^{-5} Ω.cm^2 range until 900°C (coinciding with the abrupt change in contact appearance as shown in Fig. 6.3(l)), when low resistance electrical contact could no longer be made.

The sheet resistance was observed to increase with ambient temperature up to 300°C in all samples and fits well to a power law relationship (1), well established to show association with optical phonon scattering due to thermal lattice vibration[71, 72, 268]. Low values of power index, γ, represent better thermal stability of R_{sh}. Fitting of $1/R_{sh}$ against temperature according to Equation 6.1 confirmed thermal degradation is due increased optical phonon scattering, and analysis over an ambient range of 30°C to 300°C (Fig. 5(a) and 5(b)) revealed an average γ value of around -2.0, typical of InAlN HEMTs[72].

$$R_{Sh} = R_{Sh0}\left(\frac{T_0}{T}\right)^{\gamma} \quad , \tag{6.1}$$

Contacts with t_{Ti} = 10 nm showed the largest relative increase in sheet resistance with ambient temperature, correlating with generally smoother contacts (Fig. 6.3) and a better stability of room temperature sheet resistance with respect to anneal temperature (Fig. 6.5(b)). For all metal stack thicknesses, annealing at 860°C increased the thermal stability of sheet resistance against temperature compared to annealing at 830°C, again correlating with the increase in contact roughening in Fig. 6.3. This suggests that roughening acts to stabilise the overall sheet resistance (which includes under the contact) against the effects of lattice vibrations at elevated temperatures, as the total sheet resistance is dominated by the temperature-independent roughness contribution from the beneath the contact, and is a significant novel aspect of this work.

Real-time in-situ HT-TEM is shown for samples with t_{Ti} = 3 nm and t_{Ti} = 10 nm in Fig. 6.6(a) and 6.6(b), respectively. The TEM beam is assumed to have had a negligible effect on the behaviour at the contact interface, although apparently affects material desorption as discussed in Appendix 3. Smooth 100 nm scale contrast variations are due to movement of the copper TEM stage at elevated temperatures. Beyond 950°C both crystal lamellas underwent desorption resulting in destruction of GaN buffer sample. This would potentially undermine the high thermal stability reported for III-nitride HEMTs in the literature[9, 11, 12, 272], although the InAlN barrier itself, which would protect the GaN channel from decomposition in a real (planar) device, appeared to remain stable up to the maximum temperature examined of 980°C (see Appendix 3). Lateral diffusion for both samples in Fig. 6.6, with t_{Au} = 50 nm, is restricted to only 20 nm after heating at 900°C. The three-dimensional structures depicted in Fig. 6.2 and 6.3 are not seen in Fig. 6.6, presumably due to the limited thickness (around 200 nm) of the lamella influencing thermal stress distributions and eliminating a degree of freedom. However, metal intermixing and slight contact deformation were observed early on below 500°C in both samples, suggesting Type I, II and III structures begin to form early in the anneal process.

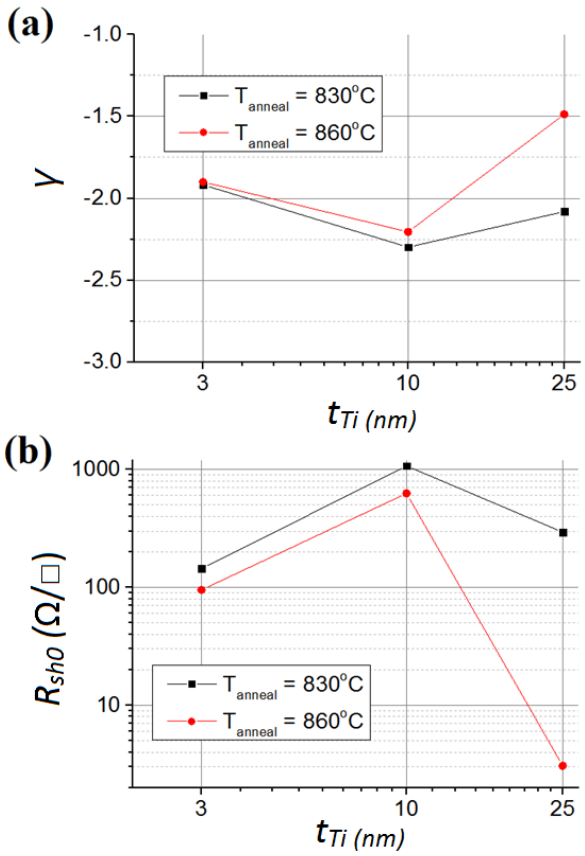

Fig. 6.5: (a) Power index, γ, from $1/R_{sh}$ against temperature plots for Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) stacks on InAlN/AlN/GaN epilayers and (b) R_{sh0} for the same

For contacts with $t_{Ti} = 3$ nm (Fig. 6.6(a)), bright patches are noticeable at the metal-semiconductor interface at temperatures coinciding with the onset of linear electrical IV characteristics. This is consistent with the established theory of Ohmic conduction being facilitated by metal inter-diffusion into the nitride semiconductor, with the bright patches indicative of a local increase in transparency to the TEM electron beam and hence a presumed decrease in thickness. Elemental analysis via EDX was not available during the high temperature analysis, but as the bright regions are on a similar scale it is expected that contact inclusions would be visible in the nitride material beneath these regions in-line with previous reports[71, 72]. A considerable increase of interfacial roughening was observed correlating with the approximate temperature range identified for an increase in sheet resistance in Fig. 6.4(a), with a local increase (from levels similar to those attained from Hall measurement) under the contact contributing to the TLM measurement[269]. At 880°C in Fig. 6.6(a) a rough metallic

feature at the metal-semiconductor interface is clearly visible for the full length of the contact, overlapping into both material regions and rough on a scale of order 10 nm.

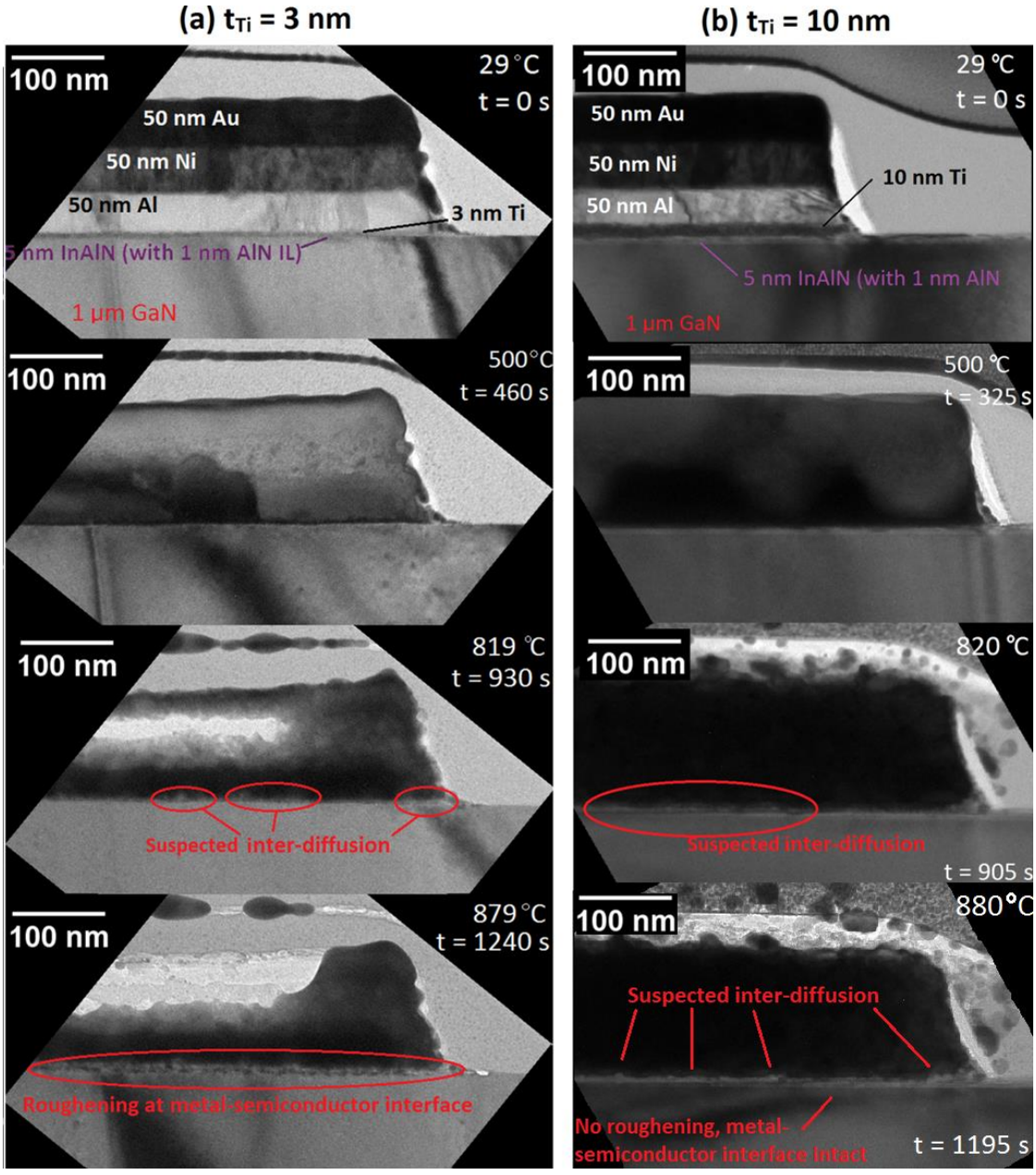

Fig. 6.6 Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) on InAlN/AlN/GaN lamella imaged by TEM and annealed under vacuum in-situ, increasing in time and temperature from top to bottom (a) t_{Ti} = 3 nm and (b) t_{Ti} = 10 nm

For t_{Ti} = 10 nm (Fig. 6.6(b)), the same bright regions appear at around 800°C, again correlating with the onset of Ohmic behaviour as in the case for t_{Ti} = 3 nm. As the

temperature increases the bright regions become larger until they dominate the interface at 880°C. The large-scale roughening at the metal-semiconductor interface for t_{Ti} = 3 nm is not present for the t_{Ti} = 10 nm sample, and the integrity of the boundary is maintained until material desorption begins to dominate at 950°C. Combined with the relative stability in sheet resistance (Fig. 6.4(a)), this is further evidence for interfacial roughening being responsible for an increase in sheet resistance when contacts are annealed above a threshold temperature, which may be controlled by optimising the stack thickness.

The relative change in contact resistance at increased measurement temperatures is shown in Fig. 6.7, with an AlGaN/GaN HEMT reference sample shown for comparison (Sample-NA from Section 6.1.2). For contacts annealed at 830°C contact resistivity generally decreases moderately with measurement temperature up to 300°C, regardless of Ti layer thickness. When annealed at 860°C the relative decrease is less pronounced across the sample set, particularly in the case of t_{Ti} = 25 nm where a relative increase is observed. This indicates the interfacial roughening identified in Fig. 6.6 contributes to modifying the thermal stability of contact resistivity as well as the sheet component; presumably via the same physical processes that stabilise the thermal dependence of R_{sh} at excessive anneal temperatures (Fig. 6.5).

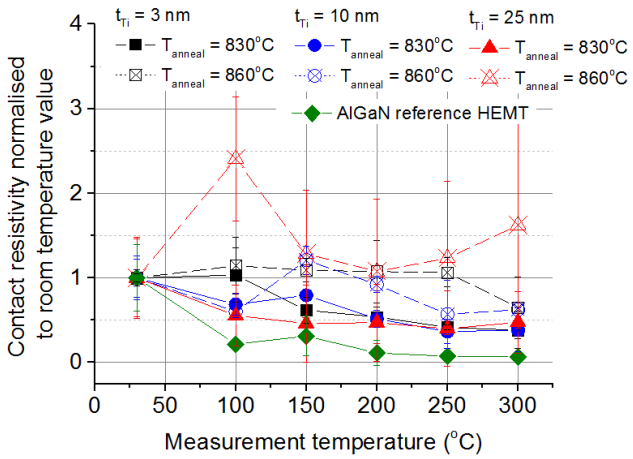

Fig. 6.7: Contact resistance against ambient temperature when annealed at 830°C and 860°C for InAlN HEMTs with various Ti stack thicknesses, and an AlGaN HEMT with Ti/Al/Ni/Au (10/50/50/50 nm) contacts annealed at 750°C for reference (Sample-NA, see Section 6.1.2)

Considerable evidence exists[71-74, 269] suggesting Ti/Al based Ohmic contacts to III-nitride heterostructures are facilitated by the reaction of contact metals with the nitride material at high temperatures. This results in lattice nitrogen vacancies that allow low resistance conduction and ultra-thin Schottky barriers with high tunnel probabilities, assuming a thermionic field-emission mechanism. Conventionally the Schottky barrier height and carrier density at the Schottky barrier interface may be obtained by extrapolation of the thermal dependence of contact resistance. For the samples in Fig. 6.7, contacts annealed at 830°C show reasonable agreement with this analysis by fitting approximately to the models described previously[72] indicating thermionic field emission is the dominant mechanism facilitating conduction. Departure from this model when contacts are annealed at 860°C further highlights the risk of over-annealing in terms of device stability.

An increase in contact resistance with temperature is reported for n-GaN layers under similar conditions[269], attributed to active epilayer-contact inter-diffusion that is more active at higher measurement temperatures. This causes domination of field-emission processes in current transport hence altering the thermal stability of the system. This is consistent with the behaviour at the contact interface identified here and the inter-diffusion of Ni and Au into the epilayer as shown in Fig. 6.2. The deviation from behaviour associated with thermionic field-emission for samples annealed at 860°C compared to 830°C in Fig. 6.7 may then be attributed to large-scale diffusion of contact metals into the nitride semiconductor, facilitated by annealing beyond some critical threshold. The anneal temperature range over which this occurs coincides with the increase in sheet resistance (Fig. 6.4(a)) and noticeable interfacial roughening in Fig. 6.6(a), suggesting the processes are related and that careful consideration of the metal stack thickness ratios is critical.

As stated in previous reports[71, 72, 268], this work confirms InAlN HEMT contacts should be annealed at a temperature within a specific window to achieve low resistance contact and avoid increasing the sheet resistance. Here we have identified the physical mechanism behind this increase in sheet resistance as roughening due to excessive inter-diffusion at the metal-semiconductor interface. This has previously been understood in terms of a decrease in the local 2DEG density as the contact metal

material diffuses deeper into the epilayer[273], which would increase the sheet resistance in a manner consistent with the results presented here. For t_{Ti} = 3 nm, the correlation with respect to anneal temperature between sheet resistance degradation and interfacial roughening as imaged by real-time TEM is evidence for this. By increasing to t_{Ti} = 10 nm the metal roughening is stabilised due to the optimised Ti/Al thickness ratio[75, 76] and excessive diffusion of the contact metal is prevented, allowing for the continual formation of conduction paths without the reduction in 2DEG density and corresponding increase in sheet resistance (Fig. 6.5). The sheet resistance and contact resistivity behaviour for t_{Ti} = 25 nm is consistent with the contact diffusing into the nitride more-so than for the t_{Ti} = 10 nm case, in line with increased contact roughening in Fig. 6.3 and previous studies[75, 76]. Elemental mapping of the 'spiking' mechanism reported to facilitate the resistive network contact architecture in InAlN HEMTs with Ti/Al/Au (30/70/70 nm)[72] reveals titanium be the dominant element present in contact inclusions. Despite the similarity to these reports of the electrical data in the work presented here (Figs. 6.4, 6.5 and 6.7) contact inclusions were not explicitly identified in Fig. 6.6, attributed to a difference in the TEM configurations used to image the samples. It is unlikely the lamella thickness influences elemental diffusion in the same way as the stress-based contact deformation associated with the Ni and Au clustering under Type I and II features in Fig. 6.2, indicating Ti is the dominant contributor to the contact inclusion 'spiking' contact formation mechanism in this study.

It is also suggested that the formation of compounds other than phases of TiN_x in response to the creation of nitrogen vacancies during annealing can have a negative impact on the ultra-thin Schottky barrier formation necessary for thermionic field-emission[72]. Native oxides on the wafer surface formed during the ICP etch[269] and not fully removed by the HF-based solution dip cleaning procedure[267] prior to contact deposition could have influenced the formation of compounds facilitating electrical contact in the stacks with t_{Ti} = 3 nm, with the limited Ti is possibly reacting fully before it can diffuse further into the epilayer. The stability of contact resistivity across the 820 < T_{anneal} < 870°C range suggests this process happens at an early stage in the anneal process, with further inter-diffusion acting to inhibit sheet resistance without providing the benefit of reduced contact resistance. Increasing t_{Ti} to 10 nm alleviated

the problem somewhat, attributed to more beneficial TiN_x formation, although at t_{Ti} = 25 nm advance roughening dominated and the contact resistance was undermined by a sharp rise in sheet resistance.

Clearly consideration of the metal stack thickness ratios is critical in combination with anneal temperature to minimize both sheet and contact resistive elements and maximize InAlN HEMT performance potential. Al/Ti and Ni/Au ratios are reported to be heavily influential to both contact resistance and morphology[73, 75, 76], which has been shown here to be a critical factor. It has also been noted that Al films of varied thickness in the stack will lead to phases of differing thermal stability, and higher annealing temperatures needed to form low resistive contacts, and that the substitution of the Au overlay by Cu, i.e. (Ti/Al/Ni/Cu) (15/100/40/100 nm Cu) annealed for 30 s at 900°C have been operated up to 1000°C in vacuum without a major change in the contact resistance[272].

In conclusion, InAlN/AlN/GaN heterostructures with Ti/Al/Ni/Au contacts were fabricated with different Au thicknesses and anneal conditions. Electrical properties were obtained by and evaluation of TLM structures and were linked to contact morphology and interfacial roughness through EDX/STEM and real-time high temperature TEM. Ohmic contacts were formed after annealing for 60 s under N_2 at 800°C, beyond which thermally-induced interfacial roughening correlates with an increase in measured sheet resistance. The dependence of the onset of an increase in sheet resistance on metal stack thickness ratios suggests the increase in R_{sh} is related to roughening beneath contact due to excessive inter-diffusion of the contact metal. A destabilisation of contact resistance with respect to ambient temperature for over-annealed samples indicated a departure from thermionic field-emission as the dominant carrier transport process. The optimal conditions with respect to metal stack thickness and anneal temperature were explored with the aim of achieving low contact resistivity without compromising sheet resistance. They were found to be a Ti/Al/Ni/Au thickness of 10/50/50/50 nm, annealed at 840°C under N_2 gas flow at 100 sccm.

6.1.2 Ti/Al/Ni/Au Ohmic contacts to AlGaN HEMTs

Section 4.1 describes the different electrical and structural characteristics of $Al_xGa_{1-x}N$/GaN heterostructures cooled after MOVPE under different conditions. The sharp nanoscale fissures in samples cooled under NH_3 and H_2 and large morphological fissures in samples cooled under N_2 and H_2, both of which seemingly penetrate to depths approaching or beyond the expected position of the 2DEG, are in this section investigated with regard to their ability to form Ohmic contacts. As in Section 6.1.1, Ti/Al/Ni/Au contacts are utilised, with the baseline anneal temperature required for low resistance linear contact being was 750°C for AlGaN, rather than > 800°C for InAlN.

The IV characteristics of the Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) contacts annealed at 750°C for 60 seconds in N_2 are shown in Fig. 6.8, and contact resistivities are stated in Table 6.1. Focussing on t_{Ti} = 3 nm, Samples-HA to HD (fissured surfaces) showed linear IV characteristics corresponding to Ohmic behaviour regardless of barrier layer composition, although a large variation in contact resistivity is noted without any apparent trend with barrier layer Al content or thickness (see Table 6.1). For low Al barrier content (x ~ 0.2) the contact resistivities were similar regardless of post-AlGaN growth cooling conditions. However, for the fissure-free samples cooled under N_2 and NH_3, contact resistivity increases with Al content until x ~ 0.3, at which point the contact becomes rectifying. This is despite an increase in the pit (threading screw dislocation) density with increased barrier layer Al content and large pit features apparently penetrating as far as the 2DEG, as is the case for Sample-ND in Fig. 4.3(h).

In order to address the rectifying behaviour of the high Al content fissure-free samples the thickness of the initial Ti layer was increased. At t_{Ti} = 10 nm contacts to samples cooled under nitrogen displayed linear characteristics, with contact resistivities of 1 x10^{-3} Ω.cm^2 and 1 x10^{-2} Ω.cm^2 at x = 0.2 and x = 0.37, respectively. Notably the contact resistivity for Sample-NA increased from 3 x10^{-4} Ω.cm^2 at t_{Ti} = 3 nm to 1 x10^{-3} Ω.cm^2 at t_{Ti} = 10 nm, while Sample-HA showed little change. For t_{Ti} = 25 nm contact linearity was reduced in samples cooled under N_2, and contact resistivity increased all cases.

Table 6.1. Barrier layer Al content for $Al_xGa_{1-x}N$/GaN heterostructures cooled in NH3 and either H_2 or N_2, and contact resistivity with Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) contacts. 'XXX' refers to non-linear contact characteristics

	Cooled under NH_3 +	Barrier layer Al content	Contact resistivity ($\Omega.cm^2$)		
			t_{Ti} = 3 nm	t_{Ti} = 10 nm	t_{Ti} = 25 nm
Sample-HA	H_2	18%	$6x10^{-4}$	$5x10^{-4}$	$7x10^{-3}$
Sample-HB	H_2	24%	$1x10^{-4}$		
Sample-HC	H_2	32%	$3x10^{-3}$		
Sample-HD	H_2	35%	$7x10^{-4}$	$9x10^{-4}$	$3x10^{-3}$
Sample-NA	N_2	20%	$3x10^{-4}$	$1x10^{-3}$	$4x10^{-2}$
Sample-NB	N_2	28%	$7x10^{-3}$		
Sample-NC	N_2	35%	XXX		
Sample-ND	N_2	37%	XXX	$1x10^{-2}$	$2x10^{-2}$

While increasing t_{Ti} to 10 nm led to Ohmic contacts for Sample ND, in general the values of contact resistivity tended to increase for all samples assessed. It is reported[73, 274] that contact stacks with low Al to Ti thickness ratios require more energy during the anneal (i.e. higher temperatures or longer times) to form low resistance contacts due to the formation of resistive AlTi phases, as was the case in Section 6.1.1. The contact resistivity of metallization with t_{Ti} = 10 nm and t_{Ti} = 25 nm to Sample-ND is shown in Fig. 6.9 where the anneal time and temperature are varied. A low value of 6 $x10^{-4}$ $\Omega.cm^2$ is achieved after annealing the t_{Ti} = 10 nm contact at 800°C for 60 seconds, comparable to the low Al content layers and samples with nanoscale surface fissures in Table 6.1, and these samples also showed better inter-device uniformity. The Sample-ND sheet resistance value of 900 Ω/□ shown in Fig. 4.6(b) is consistent in samples with lower contact resistance, confirming the fissure-free samples cooled under nitrogen do not exhibit a decrease with Al content as seen for the samples cooled under H_2. This is likely due to the increase in effective interfacial roughness (Fig. 4.3(h)) acting to suppress mobility through additional Coulombic scattering.

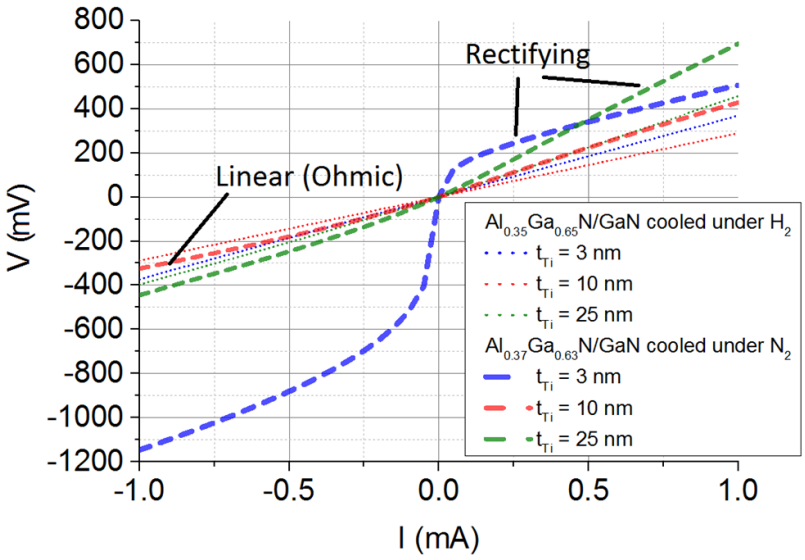

Fig. 6.8: Voltage-current profile of CTLM features (inner radius = 25 µm, outer radius 100 µm) with Ti/Al/Ni/Au (t_{Ti}/50/50/50 nm) contacts annealed at 750°C for 60 seconds under N_2 to $Al_xGa_{1-x}N$/GaN epistructures on Sample HD, x = 0.35, H_2 cool and Sample-ND, x = 0.37, N_2 cool

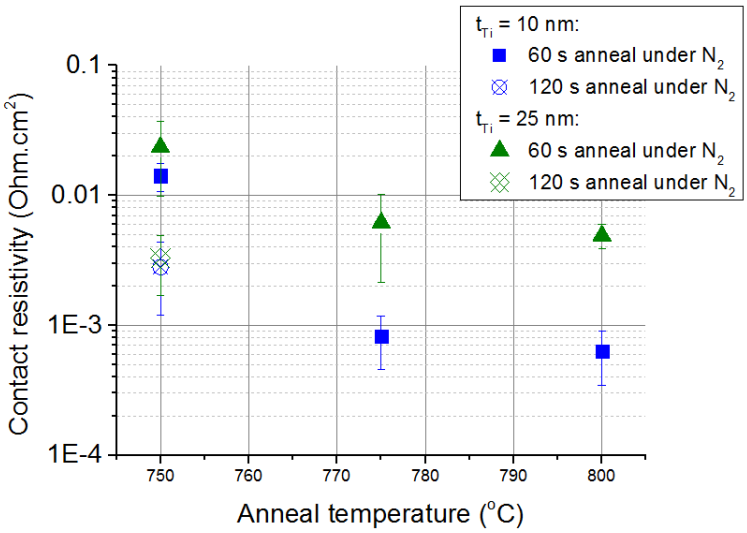

Fig. 6.9: Contact resistivity as a function of anneal temperature and time for Sample-ND for contacts with t_{Ti} = 10 nm and t_{Ti} = 25 nm

The relative variation of contact resistivity as a function of measurement temperature is shown in Fig. 6.10(a) for the Ti/Al/Ni/Au contacts (t_{Ti} = 10 nm) to Samples-HA, NA, HD and ND. For Sample-NA the profile shows a trend consistent with thermionic field emission, where 2DEG carriers increased thermal energy increases the tunnel

probability. In Sample-ND a shallower trend is noted, likely due to the increased contribution of roughening at the contact interface after additional annealing interfering with the CTLM analysis. Sample-HA and Sample-HD, with nanoscale fissures and extended pitting, show trends less consistent with pure thermionic field emission suggesting a departure from the models described previously[71] in contacts to AlGaN/GaN heterostructures, possibly a result of the same trapping phenomenon responsible for the inconsistent 2DEG density shown in Fig. 4.6(a) and Fig. 4.6(c).

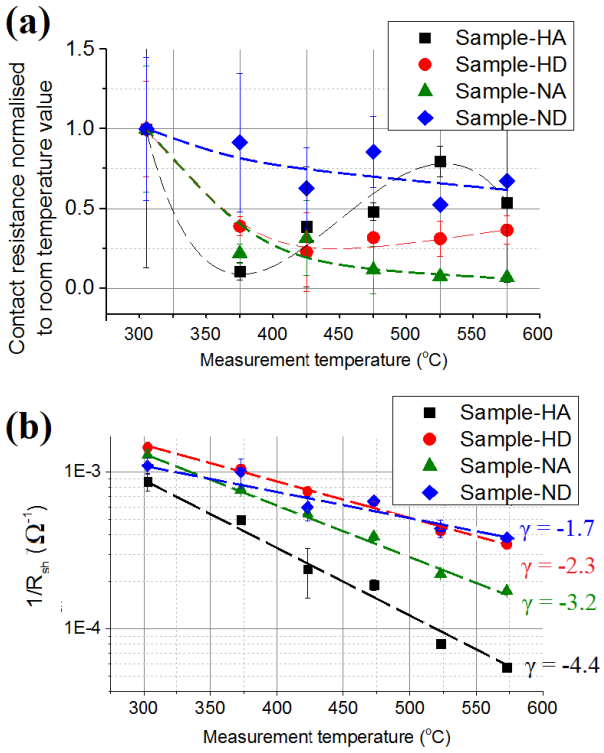

Fig. 6.10: (a) Normalised contact resistance against measurement temperature for different AlGaN barrier layer compositions and MOVPE cooling conditions with Ti/Al/Ni/Au (10/50/50/50 nm) contacts annealed at 750°C (except for 850°C in Sample-ND). Dashed lines are guides for the eye. (b) corresponding $1/R_{sh}$ against temperature

As with the InAlN HEMTs in Section 6.1.1, R_{sh} increases with temperature in all samples and fits well to the power law relationship in Equation 6.1 ($R_{sh} = R_{sh0}(T_0/T)^{\gamma}$), well established to show association with optical phonon scattering due to thermal lattice vibration. Low values of power index, γ, represent better thermal stability of R_{sh}. Plots

of $1/R_{sh}$ against temperature is shown in Fig. 6.10(b), with. γ values ranging from -4.4 for Sample-HA to -1.7 for Sample-ND. In this study high Al barrier content and fissure-free surfaces are beneficial for a thermally stable R_{sh}.

In fissure-free $Al_xGa_{1-x}N$/GaN samples, Ti/Al/Ni/Au contact resistivity increased with barrier Al content from 3 x10^{-4} Ω.cm^2 at x = 0.2, with 3/50/50/50 nm stacks providing rectifying characteristics beyond x ~ 0.3 despite surface morphology features extending to the depths of the 2DEG. Assuming a thermionic field emission charge transfer mechanism at epilayer-contact boundaries in Ohmic contacts[40] it appears that the widening of barrier layer band gap associated with increased Al content suppresses the ability of nitrogen lattice vacancies, generated after TiN_x-based contact formation during annealing, to facilitate charge transfer through the ultra-thin Schottky barriers at the metal-semiconductor interface. Increasing the Ti thickness in the metal stack to 10 nm allows for linear electrical contact to be made presumably by the generation of additional TiN_x tunnelling regions. The decrease in contact resistivity for contacts with t_{Ti} = 25 nm in all cases may be attributed to the formation of resistive alloy phases known to form during annealing with low Ti/Al metal stack ratios[73] or roughening at the contact interface suppressing the local 2DEG density[273]. Optimisation of stack thickness ratios and anneal conditions allows for a contact resistance of 6 x10^{-4} Ω.cm^2 in a fissure-free $Al_xGa_{1-x}N$/GaN heterostructure with x = 0.37, and negative contact resistance-temperature profiles consistent with thermionic field emission. This is likely due to metal diffusion into the semiconductor region facilitated by the high dislocation density and the formation of contact inclusions as described previously[71].

Epilayers with nanoscale fissures emanating from the surface to depths approaching the 2DEG eliminate a resistive component of the bulk barrier layer and form thin electronic barriers with high tunnel probabilities at the 2DEG directly. Contact resistivity does not scale with barrier layer Al content, which combined with the anomalous temperature profiles is further evidence of shallow trap phenomena associated with fissures affecting contact stability. The introduction of additional trapping is likely to lead to RF dispersion[113, 127, 275, 276] and altered breakdown properties[277, 278]) in HEMT devices, which would limit high frequency and power handling performance. Hence the poor stability and inter-device uniformity of fissured surfaces with regard to Ohmic

contact formation undermines the advantages offered by direct access to the 2DEG. Fissure-free surfaces with optimised Ohmic metallisation schemes are necessary to preserve the electronic integrity of the system. Alternatively, recessing of Ohmic contacts through selective etching is an attractive high performance alternative in HEMT fabrication[279], although like GaN capping requires an extra processing step that contributes to manufacturing time and expense.

In conclusion, nanoscale fissures were shown to allow Ti/Al/Ni/Au contacts easier access to the 2DEG channel than crack-free samples for high barrier Al content, at the expense of reduced stability and uniformity of contact resistivity. In crack-free samples with x = 0.37 contact resistance of 6 $x10^{-4}$ $\Omega.cm^2$ was achieved after optimisation of the metal stack and anneal process, showing behaviour associated with thermionic field emission and good thermal stability with respect to sheet resistance.

6.2 InAlN HEMT surface passivation optimisation

6.2.1 Optimisation of SiN_x PECVD conditions

The radiation hardness, thermal stability and off-state breakdown voltage experiments described in Chapter 5 highlight the need for effective surface passivation of InAlN HEMTs. The motivation for surface passivation and a description of the virtual gate effect and the associated RF-DC dispersion are detailed in Section 2.6.2. The work here was conducted in response to the results of thermal storage experiments in Section 5.3, where the restoration of SiN_x passivated InAlN HEMTs to pre-capped, unstressed values after 4 weeks at 250°C indicated the damage incurred during the PECVD process can be temporary rather than being irreversible, as had been previously claimed[225].

As discussed at length earlier in this thesis $In_{0.18}Al_{0.82}N$/AlN/GaN heterostructures offer high carrier densities and mobilities eliminating inherent instabilities in AlGaN HEMTs[12] associated with the highly strained AlGaN barrier layer that is significantly lattice mismatched with GaN, and are capable of operating with barrier layers below 5 nm. Management of surface chemistry is vital to achieve maximum HEMT operating

frequencies due to RF dispersion, a phenomena linked to the charging of electronic surface states that form a virtual gate and limit microwave power output[266]. The resulting gate-lag is suppressed in AlGaN HEMTs by SiN_x surface passivation that prevents surface traps encapsulating gate electrons, commonly applied by plasma enhanced chemical deposition (PECVD)[126]. Non-optimised surface passivation can cause ion damage to the nitride surface which degrades device sheet resistance, previously reported to be non-reversible[225]. Other PECVD conditions such as gas flow and temperature are also important[126], as is the layer thickness up to a threshold value of around 50 nm[266]. For InAlN HEMTs other passivation schemes are used such as atomic layer deposition (ALD) of Al_2O_3[267, 280], plasma-oxidation[266] and SiN_x formed in-situ during crystal growth[146], as well as ex-situ by PECVD[266].

In this chapter it is shown that InAlN HEMT structures are more sensitive to ion damage during PECVD of SiN_x than AlGaN HEMTs (as there is reduced surface damage at low power), and that the associated degradation in DC performance may be recovered through extended exposure to high temperature environments as seen in Section 5.3. InAlN HEMTs with optimised PECVD SiN_x layers showed improved DC characteristics and significantly reduced gate-lag in pulsed-IV measurements.

InAlN/AlN/GaN (5/1/1000 nm) and AlGaN/GaN (10/1000 nm) heterostructures on sapphire substrates were grown using metalorganic vapour phase epitaxy by a commercial supplier. Hall measurement of pre-processed (but surface cleaned in HF-based dip) $In_{0.18}Al_{0.82}N$/AlN/GaN epilayers yielded a sheet resistance of 480 Ω/□. GaN buffer layers were confirmed insulating by C-V depletion measurement, with residual capacitance under reverse bias less than 0.1 pF. A Cl_2-based inductively-coupled plasma reactive ion etch was used to define mesa structures. Ohmic contacts were Ti/Al/Ni/Au (3/50/50/50 nm) stacks annealed at 850°C and 2 μm gates consisted of Ni/Pt/Au (30/50/250 nm) stacks annealed at 400°C (see Section 3.4.2). Prior to SiN_x passivation, surfaces were cleaned by a 60 s dip in either buffered oxide etchant (BOE) or 1:1 NH_4OH:DI solution, rinsed with DI and dried with N_2. A PECVD mixed-frequency (MF) deposition technique was used to minimize the build-up of additional strain, shown to have only a minor impact on or channel resistance compared to the effect of ion damage[225]. Samples were loaded at 50°C and deposition took place at 300°C. The MF

cycle consisted of a high frequency phase at 13.56 MHz for 6 s and a low frequency phase at 187 kHz for 2 s, repeated for 15 minutes to achieve a target thickness in excess of the 50 nm above which stable performance is obtained[266]. RF power for the high frequency phase was fixed at 20 W, and samples with the low frequency phase with RF power 20 W and 10 W are designated MF-20/10 and MF-20/10, respectively. Additionally, samples with passivation layers deposited only under high frequency (13.56 MHz) conditions, with RF power at 20 W, are designated HF-20.

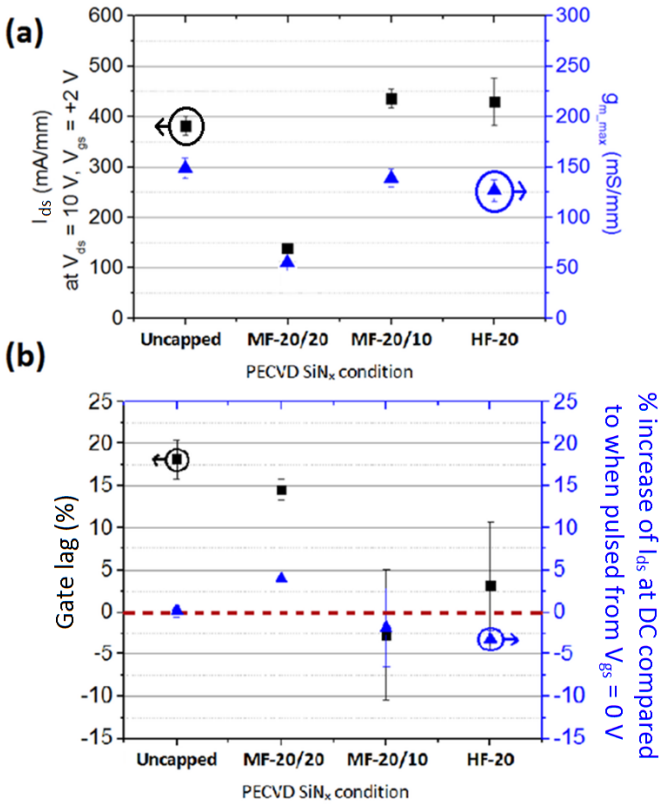

FIG 6.11: Effect of SiN_x PECVD condition for InAlN HEMT passivation on (a) DC channel transfer characteristics (b) gate-lag and increase in DC current over when pulsed from V_g = 0 V

It is worth noting that the uncapped and MF-20/20 SiN_x passivated InAlN HEMTs described here are seperate to those referred to in the high temperature storage experiments in Section 5.3, being processed in two separate fabrication runs. However, devices manufactured using the same process in consecutive runs were found to have

the same electrical behaviour within statistical limits, and the two sets are used interchangeably to assist in this analysis.

DC measurement of HEMTs was performed prior to single gate pulse measurements, with the source grounded, the drain voltage held continuously at 10 V and the gate voltage pulsed to values between 0 V and 1.5 V from quiescent points of V_g = 0 V (on-state) and V_g = -3 V (off-state). Pulse duration was 500 ns with a duty cycle of 0.5%. High temperature storage experiments consisted of samples being placed under vacuum conditions in a dark chamber at 250°C for 4 weeks in an unbiased state, with DC characterisation performed ex-situ at room temperature at intervals of 1 week, with the InAlN and AlGaN HEMT results discussed in Section 5.3 using a MF-20/20 SiN_x scheme.

Fig. 6.11(a) shows the effect of the SiN_x PECVD condition on maximum drain current (I_d when V_d = 10 V and V_g = 2 V) and peak transconductance ($g_{m\text{-}max}$) for InAlN HEMTs when measured at DC. No difference was found between samples cleaned prior to passivation with NH_4OH:DI and BOE solutions. Samples with the passivation scheme MF-20/20 show a severe degradation of saturation current, transconductance and on-resistance compared to the uncapped case, accompanied by both an increase in leakage current and change in threshold voltage from -1.6 V (Fig. 6.12(a)) when uncapped to -1.8 V after passivation (Fig. 6.12(b)). When the RF power during the low frequency stage of the PECVD was reduced from 20 W to 10 W, as for MF-20/10, DC performance was comparable to the uncapped case. MF-20/10 samples showed reduced leakage properties compared to the MF-20/20 case (although still an increase compared to uncapped devices) and threshold voltages of -2.0 V, Samples with the HF-20 scheme compared reasonably with the uncapped case in terms of saturation current, transconductance and on-resistance, showing leakage properties intermediate between MF-20/20 and MF-20/10 with a of threshold voltage -1.7 V.

The relative difference between device current in open-channel configuration when measured at DC compared to when pulsed from V_g = 0 V, for different SiN_x PECVD conditions is shown in Fig. 6.11(b). For the uncapped case negligible difference is observed. With MF-20/20 SiN_x passivation DC current is higher than when measured

under pulsing by 4%. This is in contrast to samples with MF-20/10 and HF-20 passivation, in which the DC current is 2% and 3% lower compared to when pulsed, respectively.

Gate-lag (Fig. 6.11(b)) is defined here as the fractional decrease in on-state current when the device is pulsed from a quiescent point of V_g = 0 V (on-state) compared to pulsing from V_g = -3 V (off-state). Uncapped devices show a gate-lag of around 17%, confirming the presence of a virtual gate and a requirement to implement surface passivation to maximise high frequency capabilities. Passivation with the MF-20/20 scheme provided only a modest reduction in gate-lag, undermined by already poor device performance when measured at DC. Reducing the PECVD low frequency phase RF power from 20 W to 10 W resulted in successful suppression of gate-lag, with an average value of gate-lag for samples with MF-20/10 close to zero, though an increase in standard deviation of the lag was observed between devices. Passivation with HF-20 provided similar results to those for MF-20/10.

Fig. 6.12 shows a selective, more detailed summary of the results of thermal storage (4 weeks at 250°C under vacuum followed by three weeks at room temperature) of InAlN HEMTs with SiN_x PECVD MF-20/20, discussed in qualitatively in Section 5.3. The time constant for fitted exponential curves are shown where appropriate. As discussed previously, uncapped InAlN HEMTs show initial threshold voltage values of -1.6 V, showing a negative shift to -2.1 V after one week at 250°C before stabilizing. Leakage current shows a broad range of values, below 1 mA/mm in all cases. After 2 weeks, a number of devices show high leakage above 1 mA/mm under reverse bias, compromising off-state capability. Maximum drain current is stable in all cases at around 400 mA/mm, as are peak transconductance and on-resistance. For InAlN HEMTs with MF-20/20 SiN_x passivation, the scheme seen to be the most detrimental to device performance (Fig. 6.11), threshold voltage is stable at -1.8 V throughout thermal storage. Off-state leakage is stable throughout thermal storage within the range 0.1 – 1 mA/mm, with improved inter-device uniformity compared to when uncapped (Fig. 5.8(a)). Initial maximum drain current is around 150 mA/mm. A significant increase in maximum drain current to 300 mA/mm after just 1 week (Fig. 6.12(a)) was followed by a continued increase before stabilization at around 400 mA/mm after 3 weeks, the same value measured in devices without SiN_x capping prior to thermal storage.

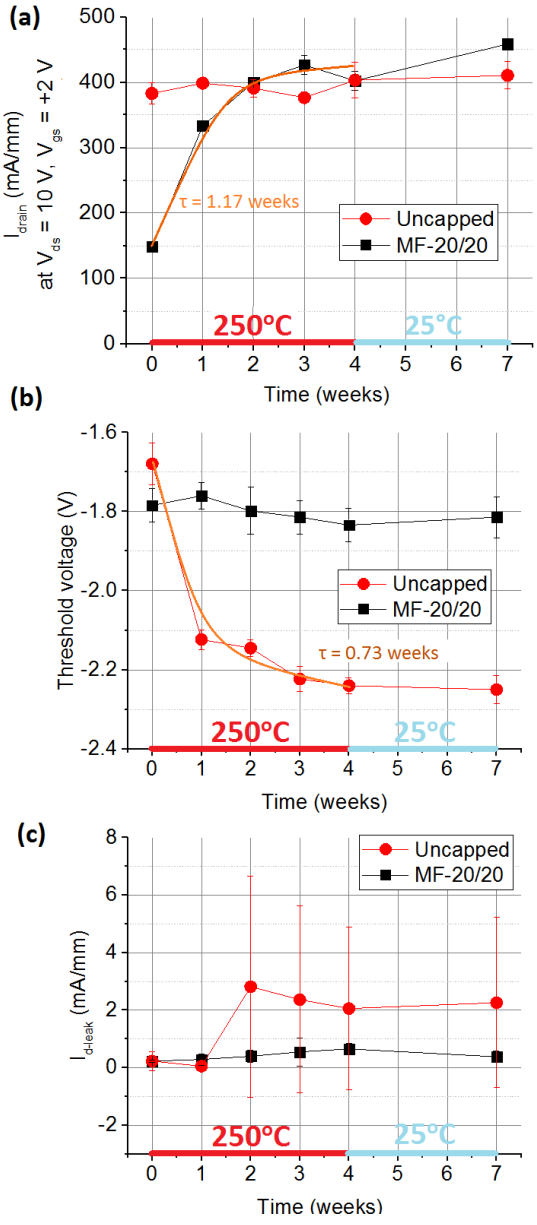

Fig. 6.12: Evolution of (a) Saturated drain current (b) threshold voltage and (c) drain leakage current during thermal storage (see Section 5.3 for full I_d-V_g plots)

The results show the sensitivity of InAlN HEMTs to PECVD conditions when passivating with SiN_x. In the case of MF-20/10 an RF power of 10 W during the low frequency deposition phase was sufficiently low to prevent damage to the nitride surface, resulting in negligible changes in DC performance after passivation and a successful suppression of gate-lag and the virtual gate effect. Increasing the low frequency RF power to 20 W caused the effects of N^- ion damage to dominate device electrical behaviour, as

evidenced by the poor overall performance of samples with MF-20/20 passivation. Similar behaviour has been reported in AlGaN HEMTs[225] although with an increased damage threshold of above 30 W RF power during the low frequency PECVD phase compared to below 20 W for the InAlN HEMTs in this work. This may be due to the different surface chemistry of InAlN or be a result of thinner barrier layers used in InAlN HEMTs and consequent increased proximity of the channel to the epilayer surface, often cited as an advantage over AlGaN[266].

The performance of samples with the passivation scheme HF-20 was only slightly poorer than in the MF-20/10 case, where the increased inter-device variation of DC characteristics may be attributed to local fluctuations in the strain field that affect polarisation charge in the active region[266]. Therefore the inclusion of a low frequency phase during PECVD passivation of InAlN HEMTs is justified to manage the secondary effect of strain build-up in the SiN_x layer, although consideration of surface ion damage should be the primary consideration.

AlGaN HEMTs with 10 nm barrier layers and either no dielectric capping or a MF-20/20 PECVD SiN_x scheme were also fabricated and included in the high temperature storage experiments (Section 5.3). AlGaN HEMTs showed only a minor reduction in DC performance upon MF-20/20 SiN_x passivation, with a reduction in channel current of 35% compared to an ~80% reduction in the case of InAlN HEMTs for the same process, as seen in Fig. 6.11(a). Throughout thermal storage, uncapped AlGaN HEMTs and those with MF-20/20 SiN_x passivation showed analogous behaviour to InAlN HEMTs. Unlike for InAlN HEMTs leakage was stable in the uncapped case at less than 10 µA/mm throughout the experiment. Threshold voltage showed a positive shift from -1.3 V to -0.9 V, in contrast to the negative shift for InAlN HEMTs under the same conditions (Fig. 6.12(b)), suggesting different trap species are dominant for InAlN and AlGaN. AlGaN HEMTs with PECVD SiN_x MF-20/20 passivation showed a maximum drain current recovery from 180 mA/mm to 280 mA/mm after 4 weeks at 250°C, a return to values measured prior to surface passivation as in the case of InAlN HEMTs. Trap-like behaviour identical to that seen in Fig. 6.3(d) was observed after 4 weeks at 250°C for SiN_x passivated AlGaN HEMTs, which also recovered to pre-capped values upon room temperature annealing, identical behaviour to that seen for InAlN HEMTs.

Analysis of electrical behaviour across the sample set suggests the damage incurred during the low frequency phase during PECVD at excessive RF power values is temporary and a result of charge trapping at the barrier/SiN_x interface. This is consistent with the degradation of DC performance, comparison of pulsed and DC current and high gate-lag[126] as shown for InAlN HEMTs with MF-20/20 SiN_x passivation in Fig. 6.11. Carriers may be thermalized out of deep-level interface traps by storage at high temperature, restoring the 2DEG density and local electric fields to retain device performance. Fitting of the exponential time constant extracted from Fig. 6.12(a) suggests a deep donor interface trap energy of ~2.5 eV relative to the conduction band assuming a typical capture cross section of 3×10^{-16} cm^{-2}, broadly consistent with previous reports[158, 281-283] (a more thorough technique like deep-level transient spectroscopy[284] would be required for a more accurate analysis). The thermal stability of the SiN_x layer presents an upper limit on the extent of carrier thermalization permissible, although all InAlN and AlGaN HEMTs examined here showed generally good stability under extended high temperature storage.

Fitting of the uncapped InAlN HEMT threshold voltage time constant (τ = 0.73 weeks, Fig. 3(b)) indicates a donor state with an activation energy of ~2.5 eV relative to the conduction band in the InAlN barrier directly beneath the gate. The stabilization of threshold voltage in InAlN HEMTs with SiN_x passivation with respect to the uncapped case combined with the improved leakage properties (Fig. 6.12(c)) suggests the inclusion of a passivation layer acts to redistribute the slow-release charge drift to prevent a build-up beneath the gate. This is supported by the scaling of gate diode reverse leakage current with contact area and corresponding behaviour at elevated temperatures in Section 6.2.3.

Previous reports state that Fermi-level pinning occurs due to the formation of native oxides only after the high anneal temperatures necessary to form low resistance Ohmic contacts[285], and has been shown to be the initial cause of RF dispersion[266] and associated with increased levels of leakage. In this work it is shown that the resulting virtual gate effects that are responsible for limiting HEMT high frequency performance may be alleviated through surface passivation of SiN_x by optimised PECVD for InAlN devices through slight modification of the standard processes used for AlGaN HEMTs,

without the need for more exotic techniques that can add complexity to device fabrication[146, 266]. This was evidenced by the improved DC characteristics and reduced gate lag in the optimised SiN_x passivation schemes in Fig. 6.11. The stabilization of threshold voltage in InAlN HEMTs with SiN_x passivation with respect to the uncapped case in Fig. 6.12(b) combined with the different leakage properties suggests the inclusion of a passivation layer acts to provide a slow-release channel to prevent charge build-up beneath the gate.

To summarise, InAlN HEMT surface passivation by PECVD of SiN_x was explored with respect to electrical performance and virtual-gate effects. Surface damage due to ion bombardment during the low frequency phase of a mixed frequency PECVD technique was found to degrade both DC and high frequency performance at a threshold RF power of less than 20 W, significantly lower than the equivalent limit for PECVD of SiN_x in AlGaN HEMT passivation. This damage is the result of carrier trap generation and may be recovered after storage at high temperatures for extended periods for both InAlN and AlGaN HEMTs. Reducing the PECVD low frequency RF power allows for optimised SiN_x passivation by balancing the effects of heavy ion damage and accumulation of strain.

6.2.2 InAlN HEMT passivation using Al_2O_3 deployed by ALD

In parallel to the SiN_x PECVD process optimisation described in Section 6.2.1, trials for a passivation scheme using Al_2O_3 deposited by atomic layer deposition (ALD) were conducted. ALD is a 'softer' process than PECVD, relying more on the chemical interaction of the precursors and epilayer surface than physical bombardment, such as to eliminate the risk of ion damage during deposition and the associated degradation of DC performance[267]. The DC and pulsed characterization technique were identical to those described in Section 6.2.1. The ALD procedure used TMAl and H_2O as reaction precursors, used a deposition temperature of 300°C and did not involve plasma excitation[286-288]. Thicknesses of 1, 2, 3 and 4 nm were used. Unlike the case of PECVD of SiN_x, the ALD of Al_2O_3 was performed prior to any additional device fabrication in

order to fully monitor the effects of the layer on the InAlN/AlN/GaN heterostructure conductivity, avoiding convolution with the effects of processing. An extended surface cleaning stage (BOE for 60 s rather than 10 s, with DI rinse and N_2 dry) took place immediately prior to metal evaporation to etch through the Al_2O_3 layer for Ohmic and Schottky contact formation. AFM on the ALD Al_2O_3 covered surface showed no change in the surface morphology, consistent with the highly conformal nature of ALD. Hall measurement of InAlN HEMT samples after ALD of 2 nm of Al_2O_3 revealed results similar to those which were uncapped, i.e. with variations within statistical limits.

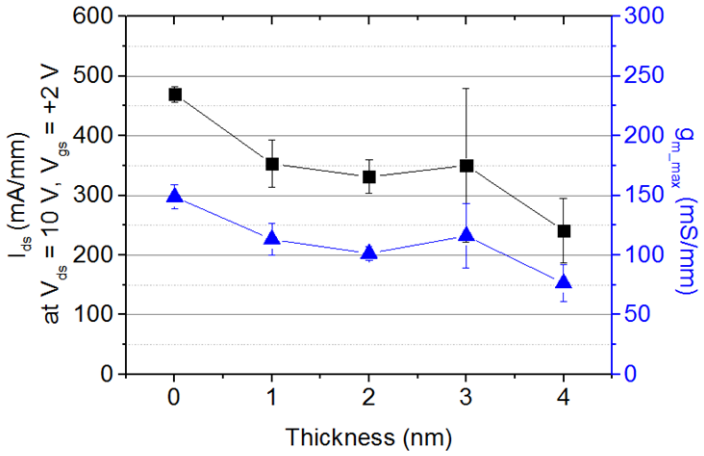

Fig. 6.13: Maximum drain current and peak transconductance for InAlN HEMTs passivated with ALD of Al_2O_3 of various thicknesses

Fig. 6.13 shows the effect of ALD of Al_3O_3 on InAlN HEMT transfer characteristics. A 20% reduction in maximum drain current and peak transconductance compared to the uncapped case is observed for thicknesses of 1 nm and 2 nm. At 3 nm the results are less consistent and by 4 nm a further reduction to around 50% of pre-capped values is noted. The extended 60 s BOE surface clean prior to metal evaporation was sufficient to etch through the ALD Al_2O_3 layer for efficient Ohmic contact formation, as evidenced by the relative stability of contact resistivity as measured by CTLM in Fig. 6.14. The corresponding sheet resistance increase from levels similar to those attained from Hall measurement in pre-processed samples to a high value of 1500 Ω/□ when the Al_2O_3

thickness exceeds 2 nm. This is consistent with the degradation of Al_2O_3 during the Ohmic contact anneal stage (850°C, 60 s , N_2 flow), necessary to generate Ohmic contact (Section 6.1.1), as Al_2O_3 with thicknesses exceeding 2 nm are reported to undergo microcrystallisation and an associated reduction in channel conduction[267, 289, 290]. Hence for Al_2O_3 to be used as a surface passivation layer in InAlN HEMTs it must be 2 nm thick or less, utlilize a contact fabrication process that does not include a high temperature anneal or deposit the Al_2O_3 layer after the contacts have been annealed.

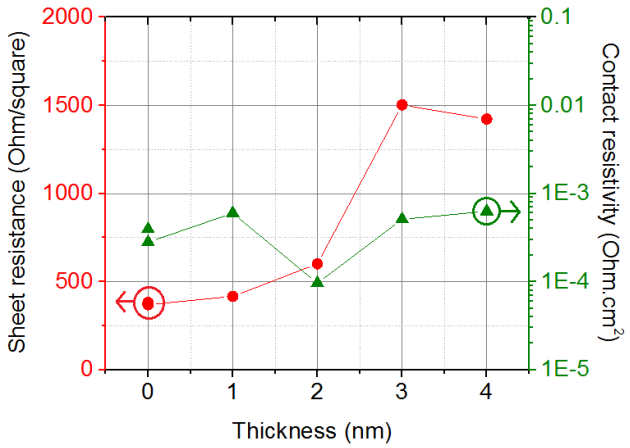

Fig. 6.14: Sheet and contact resistance for InAlN HEMTs passivated with ALD of Al_2O_3 of various thicknesses measured using CTLM

The results of pulsed—IV characterization (pulse width = 500 nm, duty cycle = 0.5% as in Section 6.2.1) are shown in Fig. 6.15. Under this ALD Al_3O_3 scheme the gate-lag compared to the uncapped case is not reduced, signalling the failure of surface passivation. This is suspected to be due to the relatively high deposition temperature of 300°C, where microcrystallization may have already occurred. Optimisation of the ALD scheme is the subject of research elsewhere, where the process parameters and surface conditions are tuned to provide atomic-layer level structural control[267, 280].

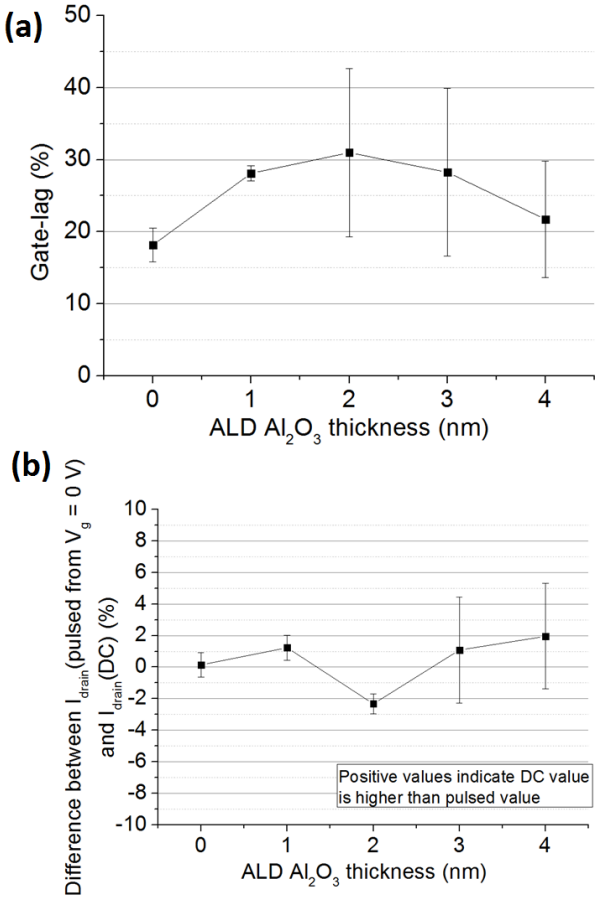

Fig. 6.15: Maximum available drain current and peak transconductance for InAlN HEMTs passivated with ALD of Al_2O_3 of various thicknesses

In conclusion, Al_2O_3 passivation of InAlN HEMTs by ALD was demonstrated with only a modest reduction in DC performance. Evaluation of the pulsed-IV characteristics indicated the scheme fails to successfully passivate the InAlN HEMT surface and a virtual gate effect still dominates electrical performance, indicating significant process optimisation is still required. The degradation of device performance for layers thicker than 2 nm confirms the inability of Al_2O_3 layers to maintain their functionality beyond this critical thickness after being subject to the anneal conditions necessary for Ohmic contact formation. Microcrystallization of the Al_2O_3 presents a clear challenge with this approach, and the process must be adjusted to accommodate for the effect of the high temperature Ohmic contact anneal.

6.2.3 Gate leakage in InAlN HEMTs with SiN_x and Al_2O_3 passivation

The results of DC and pulsed IV measurements on InAlN HEMTs both without surface passivation and with SiN_x or Al_2O_3 capping, detailed in Section 6.2.1 and 6.2.2, suggest that trapped charge causes parasitic circuit elements that are detrimental to device performance. The high temperature storage experiments described in Section 5.3 further indicate that this effect is influenced by the presence of a dielectric layer, which was then shown to be further dependent on the deposition condition. In Section 5.2 the reduced off-state reverse bias breakdown voltages in uncapped InAlN HEMTs compared to those with SiN_x passivation was in contrast to the AlGaN HEMT case, where the uncapped devices showed increased breakdown voltages compared to those with SiN_x capping. By considering these factors it becomes clear that understanding the parasitic leakage mechanisms in InAlN HEMTs is critical to the manufacture of devices with fulfilled performance and reliability potential. Clearly the leakage properties of InAlN HEMTs are non-trivial and must be understood in order to lay the groundwork for future device optimisation, as this section aims to do.

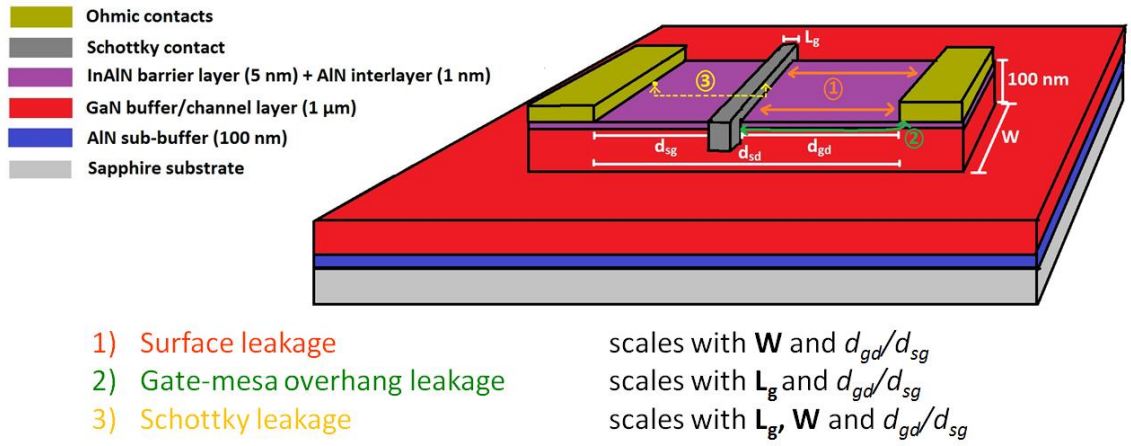

Fig. 6.16: Schematic showing possible gate leakage routes in InAlN HEMTs

Leakage in bulk GaN is generally due to intrinsic defects and may be reduced by optimising the epitaxial crystal quality – an ongoing area of research for a wide range of applications (as discussed in Section 2.1). From a device perspective leakage at the gate electrode is an important factor to be considered during the design stage, and analysis of its behaviour under different conditions can be revealing. Fig. 6.16 shows a schematic of an uncapped InAlN HEMT with annotations of the possible gate-leakage routes; 1) surface leakage, 2) gate-mesa overhang leakage and 3) conventional Schottky leakage. Surface leakage would presumably be facilitated by tunnelling between defect states as is reported in the case of AlGaN HEMTs at low temperatures[291, 292]. Gate-mesa overhang leakage (i.e. leakage through the epilayer sidewall) is shown here for completeness, as a depletion region at the device edge is expected to form after the mesa isolation processing stage, confirmed using Silvaco simulations. Conventional Schottky leakage refers to conduction from the 2DEG to the metal-semiconductor interface (see Section 2.4.2) through conductive screw dislocations via Poole-Frenkel emission, a well-described mechanism whereby carriers gain enough energy under an applied electric field for thermal excitation to be sufficient for conduction across the interface.

As indicated in Fig. 6.16 the different potential leakage mechanisms should scale with device dimensions such as width (W), gate-length (L_g) and the relative terminal spacings. Fig. 6.17 shows a gated-TLM (gTLM) test feature, with Ohmic and Schottky contacts arranged in a configuration that represents parallel HEMTs with constant width and a varied gate-length (but constant gate-drain and source-gate distances). The current-voltage characteristics of gTLM Schottky diodes were evaluated for InAlN HEMTs without dielectric capping (uncapped) and with SiN_x, as described in Section 6.2.1. The different gate lengths acted as Schottky contacts with different areas, with the aim of identifying a dominant leakage mechanism for each surface condition and fully understanding the origin of parasitic charge transfer in InAlN HEMT devices. InAlN HEMTs with ALD of Al_2O_3 from Section 6.2.2 were also included, with the sample with an Al_2O_3 thickness of 2 nm chosen as a mid-range reference sample.

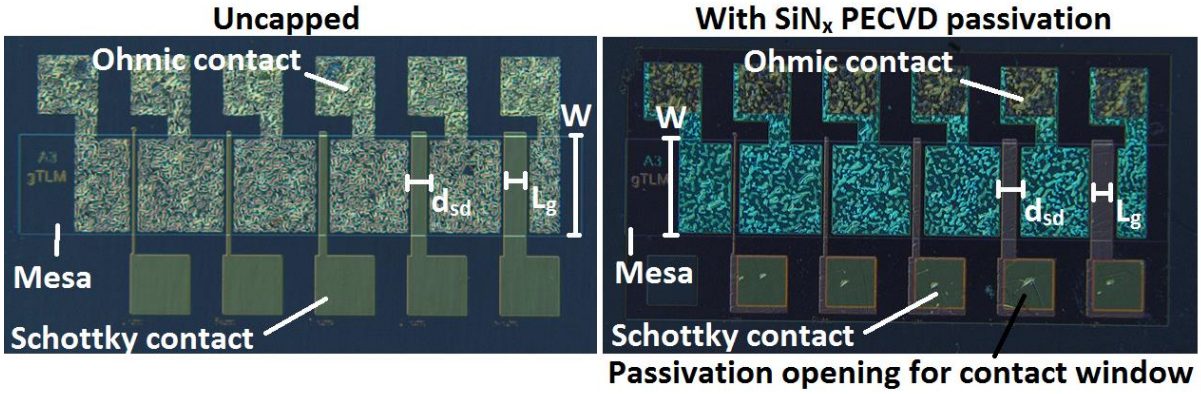

Fig 6.17: InAlN HEMT gTLM structures used to evaluate Schottky diodes. Gate-drain and source-gate distances are equal for all gate lengths.

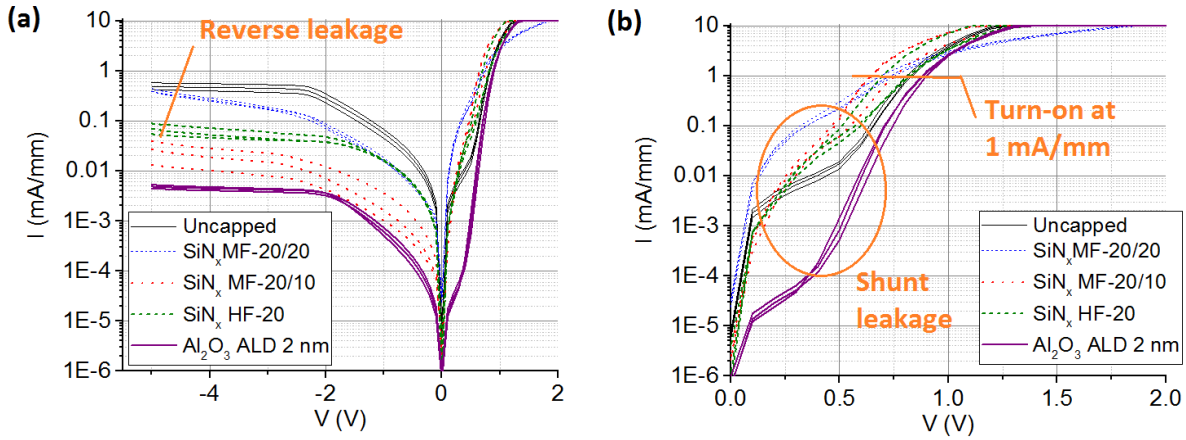

Fig. 6.18: Current-voltage profiles of InAlN HEMT gTLM Schottky diodes with a gate-length of 2 µm for different surface passivation conditions (a) forward and reverse bias (b) forward bias only

Fig. 6.18 shows current-voltage profiles of gTLM Schottky diodes for InAlN HEMTs with different surface conditions where, the gate-length used is 2 µm, resulting in a similar configuration to in the HEMT structures described throughout Chapter 5. In reverse bias the leakage saturates after around -3 V. Reverse leakage here is defined as the current when measured at V = -5 V. Prior to the diode turning on, at between 0.6 and 1.0 V, a shunt leakage contribution is also definable. In this configuration InAlN HEMTs with 2 nm of Al_2O_3 capping provide the lowest amount of leakage. Uncapped HEMTs have

the largest degree of leakage in reverse bias, followed by HEMTs with MF-20/20 SiN_x passivation and then the schemes with that exhibit improved device performance, MF-20/10 and HF-20 (see Section 6.2.1 for details).

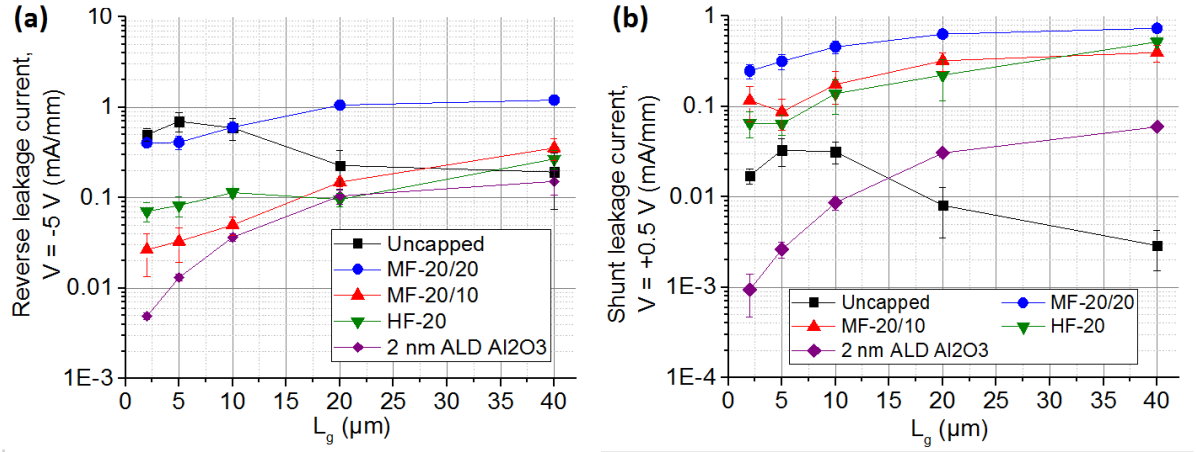

Fig. 6.19: Scaling of gTLM Schottky diode (a) reverse leakage at V = -5 V and (b) shunt leakage at V = +0.5 V for InAlN HEMTs with different surface passivation conditions

The scaling of reverse leakage with gate-length (i.e. Schottky contact area) is shown in Fig. 6.19(a). For the uncapped case the leakage current shows a slight decrease, from around 0.5 mA/mm at L_g = 2 µm to around 0.2 mA/mm at L_g = 40 µm. For samples with SiN_x and Al_2O_3 surface capping the reverse leakage current increases with gate-length, as the area beneath the gate available for carrier tunnelling from the 2DEG is expanded. The MF-20/20 SiN_x sample set shows consistently poor leakage, with 0.4 mA/mm at L_g = 2 µm and 1.1 mA/mm at L_g = 40 µm. For the samples with leakage currents less than 0.1 mA/mm at L_g = 2 µm (those with 2 nm ALD of Al_2O_3 or SiN_x using the MF-20/10 or HF-20 PECVD schemes) leakage was similar (around 0.1 mA/mm) at L_g = 20 and 40 µm in all cases.

For the forward bias shunt leakage (Fig. 6.19(b)) the uncapped case again exhibited a decrease with increasing gate-length/Schottky contact area, in contrast to the sample sets with either SiN_x or Al_2O_3 passivation. InAlN HEMTs with the SiN_x PECVD MF-20/20 scheme consistently showed the highest amount of leakage, and the 2 nm Al_2O_3 ALD scheme was again the most resistive for the L_g = 2 µm.

The results confirm the leakage properties of InAlN HEMT structures are dominated by activity at the upper InAlN epilayer boundary. For the SiN_x and Al_2O_3 passivated devices, the scaling of leakage current with Schottky contact area is consistent with the conventionally understood mechanism for leakage at Schottky barriers, the via Poole-Frenkel mechanism. This indicates the origin of the dominant leakage contribution is the 2DEG channel, rather than along a surface tunnel route.

For the uncapped case the apparent negative trend in leakage current with contact area is more difficult to explain, with conventional Schottky barrier penetration eliminated. This would suggest surface leakage facilitated by tunnelling between defect states is responsible, although in this case there would not be any variation expected with contact area. The apparently inverse relationship may be related to poor wafer uniformity, as evidenced by the range of leakage values between devices.

The converging of reverse leakage values at gate-lengths above 20 µm in the majority of cases (except SiN_x MF-20/20) suggests that in that configuration the same mechanism dominates leakage in all cases. Considering the large contact area it is assumed this mechanism is Schottky barrier penetration via the Poole-Frenkel effect assisted by conductive threading dislocations[291, 293], a critical threshold of which are presumed responsible for the unified leakage properties. For the SiN_x MF-20/20 passivated case an additional contribution is present independent of contact area, presumably related to the ion damage incurred during PECVD (Section 6.2.1).

As reported previously for InAlN[292] and AlGaN[291] HEMTs, different leakage routes can be active under different conditions, and may be identified by their relative change under a varied ambient temperature. In Poole-Frenkel emission processes electrons are thermally excited from electrically isolated defect states into a conductive continuum, thereby allowing transmission through an otherwise rectifying Schottky barrier, encouraged by the applied electric field. Consequently an increase in ambient temperature increases the tunnel probability and an increase in gate-leakage should be detected, as appears to be the case for the SiN_x capped InAlN HEMTs in Fig 6.20(b)). For tunnelling processes, identified as Fowler-Nordheim emission in AlGaN HEMTs below 150 K[291], the escape probability and hence leakage current should be dependent on

the local field strength only, and not temperature, correlating with the relative lack of a change in diode leakage with temperature for the uncapped InAlN HEMTs in Fig 6.20(a).

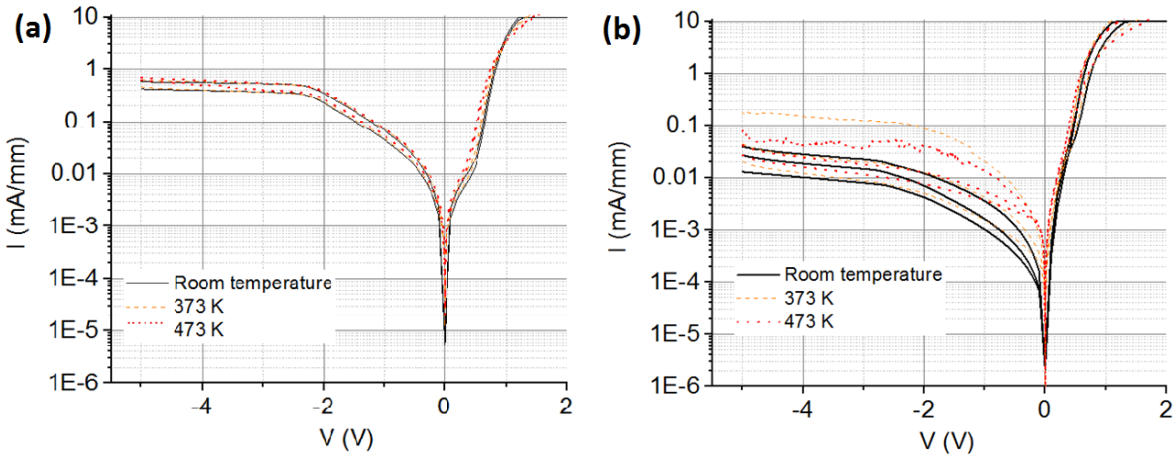

Fig. 6.20: InAlN HEMT Schottky diode (L_g = 2µm) current–voltage characteristics at elevated temperatures for (a) uncapped and (b) with PECVD MF-20/10 SiN_x

Fig. 6.21 shows the relationship between (a) reverse leakage and (b) shunt leakage with temperature from room temperature to 473 K for InAlN HEMT gTLM Schottky diode structures with different surface passivation conditions and gate-lengths. The results show that for large Schottky contact areas (i.e. L_g = 40 µm), uncapped and SiN_x or Al_2O_3 passivated HEMTs show similar leakage behaviour. For smaller contact areas (L_g = 2 µm) the passivation layers most effective at eliminating gate-lag effects, SiN_x PECVD schemes MF-20/10 and HF-20 (Fig. 6.11(a)), show a greater relative increase in gate-diode leakage at elevated temperatures compared to the uncapped case and that with non-optimised MF-20/20 SiN_x or ALD Al_2O_3 passivation.

Analysis of the behaviour of leakage under different surface passivation conditions provides information on the physical mechanisms involved. For the shunt (forward) leakage variation at elevated temperatures in Fig. 6.21(b), all samples show a relatively large increase in leakage for L_g = 40 µm. This thermal dependence is consistent with Poole-Frenkel emission across the rectifying junction at the gate, where the large gate area in this case makes that the dominant mechanism. For the smaller gate lengths of

L_g = 2 µm, the samples with optimised surface passivation show a larger increase in shunt leakage than those uncapped and with non-optimised MF-20/20 SiN_x, suggesting the dominance of competing mechanisms in the latter cases where an increased proportion of the total leakage current is facilitated by temperature independent processes, i.e. Fowler-Nordheim tunnelling.

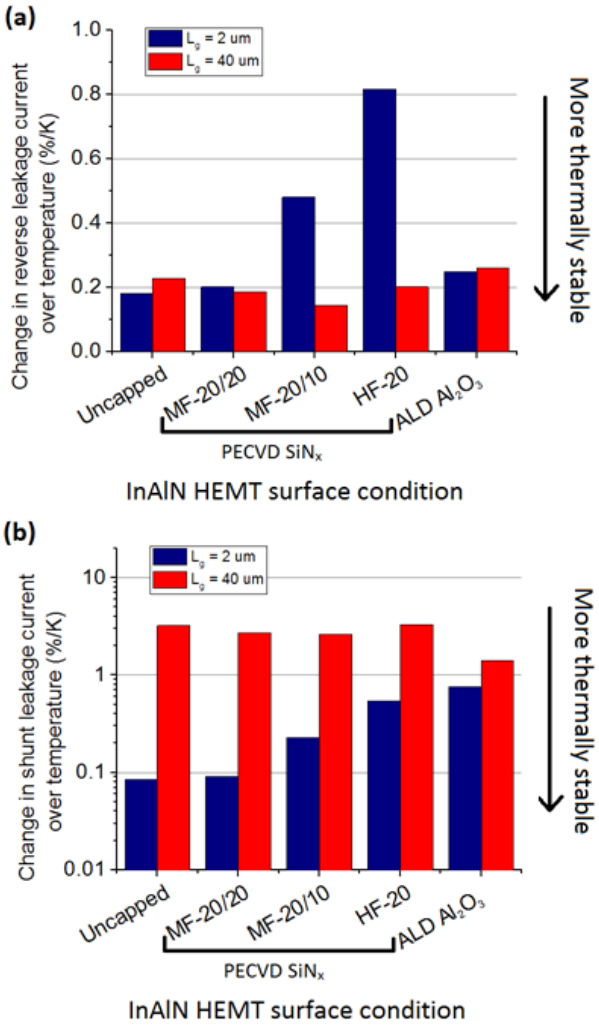

Fig. 6.21: Scaling of gTLM Schottky diode (a) reverse leakage (V = -5 V) and (b) shunt leakage (V = +0.2 V) with temperature from 298 – 473 K for InAlN HEMT structures with different surface passivation conditions and gate-lengths.

For the reverse leakage increase with temperature in Fig. 6.21(a) a similar result is shown for L_g = 2 µm, confirming the different dominating physical mechanisms behind

leakage in InAlN HEMTs with optimised and non-optimised surface conditions. At L_g = 40 µm all samples show similar values, again suggesting the same mechanism is dominating for all samples at large gate lengths. There is however generally less of an increase in leakage at elevated temperatures than when L_g = 2 µm, contrary to the shunt leakage case in Fig. 6.21(b). This may be due to an increased contribution of the material sheet resistance at reverse bias in this configuration, which would act to the increase the overall resistance at elevated temperatures (Equation 6.1, Section 6.1.1). Another possibility is the increase Schottky contact area being in contact with a large number of threading dislocations, passing a critical number such that carriers can tunnel through to the 2DEG via a temperature-independent tunnelling process. In either case the effect shows no significant dependence on the surface passivation condition in Fig. 6.21(a).

In HEMT device design the gate-length is set as low as is practically possible to reduce parasitic impedance and maximize the high-frequency response (see Section 2.6.1), resulting in sub-µm gate lengths being dominant. Clearly in this regime InAlN HEMTs are subject to significant identifiable leakage mechanisms separate to conventional thermally-assisted Schottky emission that dominate device behaviour. The correlation of tunnel-like leakage behaviour (Fig. 6.21(a) and (b)), gate-lag of up to 20% (Fig. 6.11(b)) and a reconciliation of reverse leakage values at increased Schottky contact areas (Fig. 6.19(a)) all contributes evidence for a parasitic network of defect states associated with the InAlN barrier layer. The suppression of gate-lag and restoration of Schottky-like contact behaviour for optimised passivation schemes (PECVD SiN_x MF-20/10 and HF-20) strongly indicates this is a surface effect.

The results are consistent with the conclusions drawn regarding the thermal storage experiments in Section 5.3 and those in Section 6.2.1, where the inclusion of a SiN_x surface passivation layer resulted in a fundamental difference in performance change with temperature compared to the uncapped case. For uncapped InAlN HEMTs the change in threshold voltage after thermal storage was presumable facilitated by the surface tunnelling mechanisms, which were not active in the SiN_x capped samples. Rather, in the MF-20/20 SiN_x case, the leakage was dominated by ion damage from the PECVD process. The presence of a tunnel leakage pathway in the uncapped case also explains the discrepancy in InAlN HEMT breakdown voltage, detailed in Section 5.2. For

AlGaN HEMTs the breakdown voltage was above 300 V for the uncapped case, reduced to around 150 V with the inclusion of an MF-20/20 SiN_x passivation layer. This is easily understood by considering the SiN_x layer as the breakdown route, with the dielectric failure compromising the device off-state capability. For uncapped InAlN HEMTs breakdown voltage was around 130 V, rising to around 200 V with the inclusion of the MF-20/20 SiN_x passivation layer. In this case it is now clear that the temperature-independent leakage mechanism identified in this section, most likely Fowler-Nordheim tunnelling that is highly sensitive to electric fields[291], provides uncapped InAlN HEMTs with a relatively unstable breakdown pathway under high reverse bias. The fact that this behaviour is contrary to the AlGaN case and predominantly a surface effect highlights the contradicting material properties of InAlN, in the same way as the different response to storage at high temperature in Section 5.3.

Fig. 6.22 shows the relative decrease in on-state saturation current with temperature for the uncapped case and with SiN_x and Al_2O_3 passivation. The uncapped case shows the highest reduction, representing the worst thermal stability. MF-20/20 SiN_x is apparently thermally stable, although the low initial maximum current values (Fig. 6.11(a)) and variation over extended periods at high temperature (Section 5.3) undermine this value. Well-optimised SiN_x passivation schemes MF-20/10 and HF-20 show an increased robustness to high temperatures compared to the uncapped case, as well as showing the lowest amount of gate-lag (Fig. 6.11(b)). Logically this suggests an improved stability of sheet resistance (as the contacts were identical in all cases). It is believed that the mobility temperature coefficient should not be affected by the presence of a surface passivation layer, and the improved thermal stability is attributed to a suppression of carrier surface recombination at elevated temperatures, preventing a depletion of the 2DEG and an associated modification of the local band structure as was believed to be the case for the AlGaN samples with nanoscale surface fissures on Section 4.1. This is consistent with the MF-20/10 and HF-20 SiN_x samples providing a reduced amount of gate-lag, as the surface recombination states are the same as those responsible for the virtual gate effect. The 2 nm ALD Al_2O_3 passivation scheme shows good thermal stability, although this again undermined by the high gate-lag (Fig. 6.15)

and presence of tunnel-like leakage properties (Fig. 6.21) which indicate a capacity for failure under extended stress.

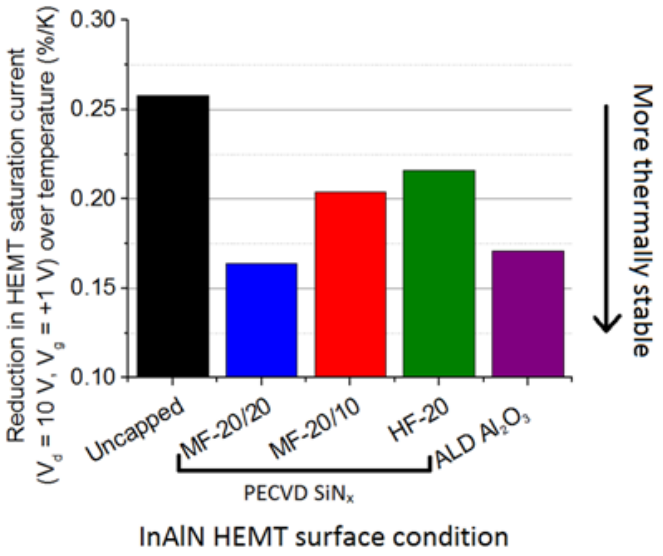

Fig. 6.22: The relative decrease in HEMT saturation current when measured over a 298 – 473 K temperature range

6.3 Chapter summary

In this chapter III-nitride HEMTs have been optimised in terms of their electrical performance. AlGaN HEMT Ohmic contacts were optimised, specifically with regard to the barrier layer alloy composition and the presence of surface nanoscale fissures. InAlN HEMT Ohmic contacts were analysed in more detail still, with the effect of roughening under the contact and the resulting effect of sheet resistance being quantified for the first time using state-of-the-art in-situ high temperature TEM. Finally the issue of surface passivation and off-state leakage, the factors to which the failure under external stress in Chapter 5 were attributed, were addressed. The PECVD conditions for SiN_x passivation of InAlN HEMTs were found to be critical, with InAlN surfaces more sensitive to ion damage than AlGaN, and ultimately shown to have an effect on the high frequency performance and thermal stability.

7. Conclusion and outlook

In this work InAlN HEMTs have been explored with respect to their suitability for use in space-based applications. The InAlN HEMT system is based on the more established AlGaN HEMT, a high power, high frequency technology commercially available as of 2006[7]. It is of particular interest to the space industry, as it theoretically offers improved device performance while suppressing supposed failure routes in AlGaN HEMTs, principally through the ability to lattice-match to GaN at an alloy composition of $In_{0.18}Al_{0.82}N$ and the consequent elimination of heteroepitaxial strain, and an increase in thermal stability and radiation hardness.

This thesis compares the manufacturing process of InAlN and AlGaN HEMTs, from the semiconductor crystal growth stage to transistor device fabrication, integrated with an extensive performance and reliability analysis of materials and devices. AlGaN HEMTs manufactured in-house were compared to an optimised commercially available devices, allowing a link between device performance optimisation and reliability to be established. Through identification of the physical mechanisms responsible for limiting device performance and reliability, applicable to both InAlN and AlGaN material systems, InAlN HEMT epitaxy and device fabrication processes that improve performance and provide a holistic understanding of device operation were demonstrated.

The structures consist of III-nitride semiconductor multi-layer stacks grown by MOVPE on sapphire substrates, on top of which metal contacts are patterned to facilitate controlled current flow via a 2DEG that exists close to the epilayer surface, in between a GaN channel layer and a thin (< 20 nm) barrier layer consisting of InAlN or AlGaN. For similar epilayer stack thicknesses and device geometries, InAlN/GaN heterostructures were shown to surpass AlGaN/GaN with respect to current transport owing to the increased 2DEG density arising from the high Al content of the lattice-matched $In_{0.18}Al_{0.82}N$ barrier layer. This was undermined by an increased dominance of surface trap phenomena in the InAlN case, resulting in anomalous off-state leakage behaviour and enhanced sensitivity to surface passivation techniques.

AlGaN/GaN heterostructures were grown by MOVPE and fabricated into AlGaN HEMTs to provide a reference for the challenges of III-nitride HEMT production. GaN buffer layers were confirmed to be semi-insulating by C-V measurement, using an AlN growth nucleation layer for a smooth transition from the sapphire substrate. The effect of an increased Al composition in the AlGaN barrier layer was explored with respect to the structural and electrical characteristics of the epilayer, where increased heteroepitaxial strain manifested as an increased 2DEG concentration and the formation of nanoscale surface fissures. The latter were shown to only form under cooling after MOVPE with H_2 and NH_3 but not under N_2 and NH_3, and to have an adverse effect on HEMT performance and thermal stability. The behaviour was linked to electronic trap states that result from the formation of the fissures under non-optimised growth conditions.

At an alloy composition of $In_{0.18}Al_{0.82}N$ the high Al content provides increased charge polarisation at the heterointerface, allowing InAlN/GaN heterostructures to be lattice-matched and scaled to thicknesses less than 10 nm, beneficial for HEMT high frequency performance. However, InAlN is a more challenging material to produce by MOVPE than AlGaN owing to the vastly different atomic properties of In and Al, resulting in a narrowed window of growth conditions in which to optimise InAlN/GaN heterostructures. A 1 nm AlN interlayer was included based on reports in the scientific literature, which was then optimised with respect to electrical performance by optimisation of MOVPE growth conditions. At barrier layers of 5 nm InAlN/AlN/GaN heterostructure mobility and carrier concentration were strongly dependent on interfacial roughening and surface recombination, respectively. These factors were managed through consideration of the thermal redistribution of the appropriate crystal layers and surface stability during the necessary change in reactor temperature when growing GaN, AlN and InAlN, respectively. The origin of Ga auto-incorporation in InAlN layers grown by MOVPE, a topic debated between research groups internationally, was confirmed to be the desorption of Ga-containing compounds during the switch in growth conditions from those of GaN to those needed for InAlN. A reactor cleaning procedure was demonstrated conclusively to effectively suppress unwanted Ga incorporation in nominal InAlN layers.

The high Al content in lattice-matched InAlN HEMT barrier layers results in a large band gap and high thermo-chemical stability, close to that of AlN. These properties are attractive from a design perspective, giving potential for improved device scaling and durability. From a manufacturing viewpoint the same properties present challenges in production and characterization. The robust properties of InAlN necessitated adjustment of the mesa isolation device fabrication stage and prevented photo-chemical monolayer etching for a comprehensive depletion measurement by electrolytic C-V, relatively trivial processes in the case of AlGaN HEMTs.

For Ohmic contact formation through annealing of Ti/Al/Ni/Au stacks, electrical characteristics of InAlN HEMTs were shown to be highly sensitive to roughening at the metal-semiconductor interface. Optimised InAlN HEMT Ohmic contacts were demonstrated through modification of the metal stack thickness ratio and anneal conditions, assisted by in-situ high temperature TEM. Contacts to InAlN HEMTs require a higher anneal temperature for low resistance transfer than AlGaN HEMTs due to the increased bond strength in the nitride layer and subsequent difficulty in creating the nitrogen lattice vacancies that facilitate conduction.

InAlN HEMTs were shown to suffer from severe virtual gate effects when the air-exposed surface was InAlN, i.e. uncapped devices. An initial SiN_x PECVD surface passivation process adapted from the literature (optimised for use with AlGaN HEMTs) was ineffective at suppressing virtual gate effects and severely reduced InAlN HEMT DC performance. This was shown to be due to the increased sensitivity of the InAlN surface to ion bombardment damage during the low-frequency stage of the mixed-frequency PECVD process. An optimised PECVD technique was shown to reduce gate-lag without affecting DC performance. The presence of a temperature-independent surface leakage route was linked to the virtual gate effect in uncapped devices and attributed to quantum tunnelling between surface defect states.

InAlN and AlGaN HEMTs were shown to be generally robust against temperatures of 250°C for extended periods. Furthermore, no significant change was observed in electrical characteristics after a 9.2 Mrad dose of ^{60}Co 1 MeV gamma radiation at a dose rate of 6.6 krad/hour or after 1 Mrad delivered at the higher dose rate of 420 krad/hour

across all sample sets. For the 6.6 krad/hour dose rate, InAlN HEMTs showed superior stability in terms of drift of DC parameters with increased dose compared to AlGaN HEMTs manufactured in parallel. However, the inclusion of a non-optimised SiN_x passivation layer compromised InAlN HEMT robustness to radiation and resulted in a catastrophic reduction in DC performance, not seen in the AlGaN case. Well optimised, high performance AlGaN HEMTs (with effective surface passivation) from an external commercial source showed negligible change in DC characteristics during radiation exposure, confirming the suitability of III-nitride HEMTs for applications requiring radiation hardness and strongly indicating the same production defects limiting device performance are responsible for limitations on reliability.

Both InAlN and AlGaN HEMTs were shown to exhibit high thermal stability, with in-situ measurements showing only a fractional decrease in performance up to 200°C and an ability to remain robust after storage at up to 250°C for extended periods. Degradation of the SiN_x passivation layer was again identified as an initial obstacle to long-term durability after exposure to extreme environments. Furthermore InAlN and AlGaN HEMTs were shown to have breakdown voltages of above 100 V in all cases through off-state bias step-stress experiments. Uncapped AlGaN HEMTs exhibited breakdown voltages of above 300 V, reduced significantly with the inclusion of SiN_x passivation. InAlN HEMTs with SiN_x showed roughly equal breakdown properties to those of SiN_x passivated AlGaN devices, with electrical breakdown of the dielectric layer presumed responsible. For uncapped InAlN HEMTs the significantly reduced breakdown properties were attributed to the presence of the surface leakage route described above.

For these reasons, this work has confirmed InAlN HEMTs as a viable candidate for continued development for use in next generation space applications. The opportunity for lattice matching InAlN to GaN at an Al alloy content of 82% allows the system to take advantage of the attractive material properties found in AlN. Manufacturing processes used in AlGaN HEMT production are transferrable to InAlN providing the necessary adjustments, detailed in Chapter 6, are adhered to. This presents a rewarding challenge that will enable InAlN HEMTs to fulfil their clear performance and reliability potential.

To further prove this, InAlN HEMTs with the optimised fabrication procedures outlined in Chapter 6 should be subject to experiments such as those in the gamma radiation hardness, thermal stability and off-state breakdown study in Chapter 4, as well as heavy-ion and on-state lifetime experiments. It is perhaps regrettable that the reliability experiments conducted here took place prior to the optimisation of the InAlN HEMT SiN_x PECVD process, although practically the results were the primary motivation toward achieving the latter. Regardless, the inclusion of the optimised commercial AlGaN HEMTs in the radiation and breakdown experiments was sufficient to demonstrate the superb robustness of III-nitride HEMTs and their suitability for operation under extreme conditions. Given that the InAlN HEMTs described in this work represent an immature technology relative to AlGaN HEMTs, it is expected that InAlN HEMTs manufactured with optimised crystal growth and device fabrication processes would surpass the current (as of 2015) AlGaN technology in terms of performance and reliability.

Regarding InAlN/GaN heterostructures grown by MOVPE, research efforts should be focussed on a few key areas. Intrinsic crystallographic defects are responsible for trap phenomena in the GaN channel/buffer layer, and have been shown elsewhere to be responsible for RF-dispersion in the form of drain-lagging in III-nitride HEMTs. The production of high crystal quality GaN is important for a range of applications and is expected to continue to improve, to the benefit of AlGaN and InAlN HEMT technologies.

Given the clear issue with InAlN surface states as exemplified by this work, it is not surprising that InAlN HEMT surface passivation is an active research topic[93, 97, 146, 266, 280, 294]. The prospect of in-situ surface passivation during MOVPE is attractive, to prevent any exposure of the InAlN surface to conditions other than those in which it is formed. An ultra-thin GaN capping layer has been shown[146] to facilitate in-situ SiN_x passivation of InAlN HEMT structures, which may provide a future route to device optimisation. Given that the SiN_x passivation layer presented a limitation on the long-term thermal stability of HEMT devices in this work, other passivation materials may have to be considered. Atomic layer deposition of Al_2O_3 showed potential as an alternative InAlN HEMT passivation scheme in this work, although the ineffectiveness at addressing the gate lag was disappointing. The optimisation of the SiN_x PECVD process is however encouraging, and indicates the ALD condition could be optimised to suppress

virtual gate effects and take advantage of the robust material properties of Al_2O_3, paving the way for a passivation scheme with improved thermal stability[267, 280]. AlN/GaN HEMTs with ultra-thin barrier layers (< 4 nm) and an oxide layer between the barrier and gate have been demonstrated elsewhere[98] with high cut-off frequencies but poor breakdown properties. The performance benefits of a reduced gate-channel separation without compromising the integrity of the 2DEG make this a worthy avenue of investigation. This approach has been shown to facilitate normally-off operation in InAlN HEMTs[44]. This is represents an important achievement that will allow for improved circuit power efficiency as well as a reduced need for failure contingencies, and marks a maturity milestone for the InAlN HEMTs[17] following on from the earlier achievement of the same in commercially available AlGaN HEMTs[6].

InAlN HEMTs have been shown to be capable of maintaining operation at temperatures of up to 1000°C[11, 272]. Failure is linked to the degradation of contact metals. For the Ti/Al/Ni/Au the anneal temperature represents a limit on the thermal stability, beyond which degradation would limit performance, although this may be relaxed through the substitution of Au and Ni for more stable metals like Cu. Similarly the thermal stability of the Ni/Pt/Au gate used here may be improved through the development of a Pt or W based Schottky contact scheme.

8. References

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9. Appendix

9.1 Appendix 1: Additional radiation hardness data

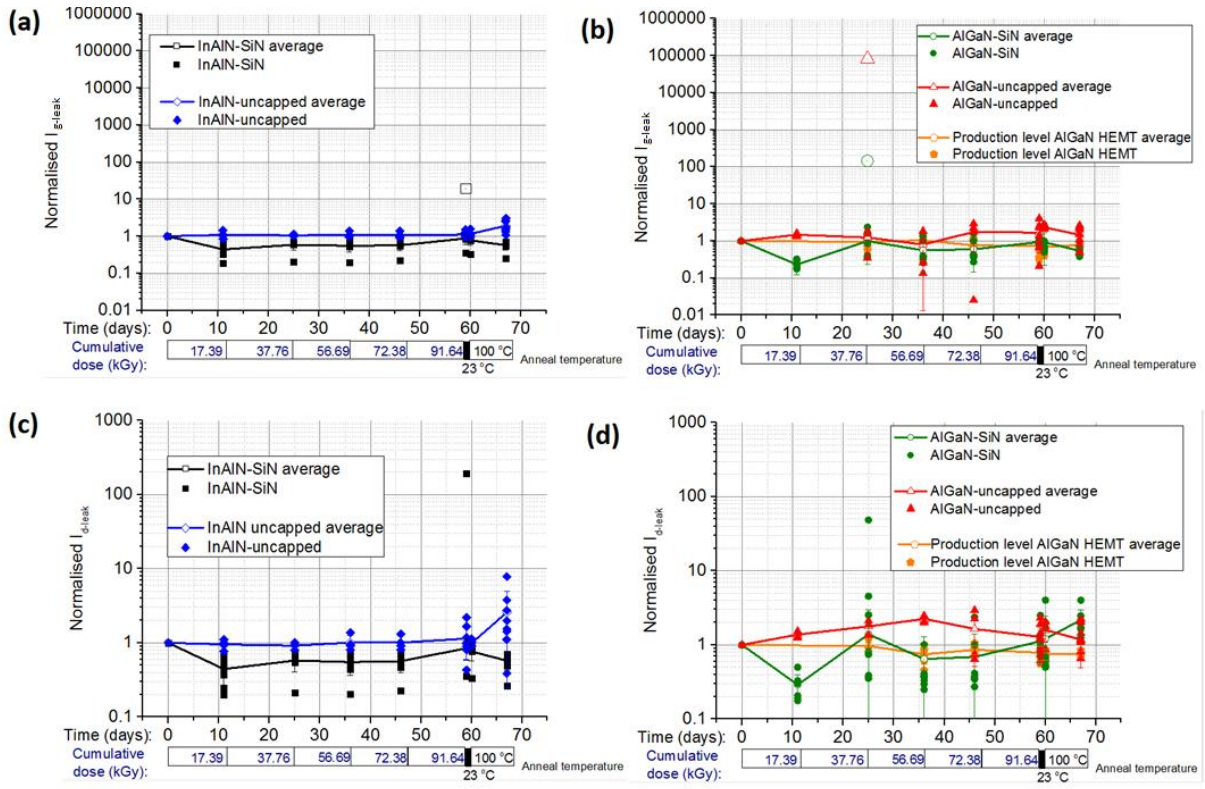

Fig. A1.1: Change in $I_{d\text{-}leak}$ ((a) and (b)) and $I_{g\text{-}leak}$ ((c) and (d)) in InAlN ((a) and (c)) and AlGaN ((b) and (d)) HEMTs during radiation exposure and post-irradiation annealing.

This appendix provides additional supplementary data to the InAlN and AlGaN HEMT radiation hardness experiments described in Section 5.1. Fig. A1.1 shows the off-state drain leakage ($I_{d\text{-}leak}$) and gate leakage ($I_{g\text{-}leak}$) for InAlN and AlGaN HEMTs with and without SiN_x passivation over the course of the radiation exposure and post-irradiation annealing. Values are normalised to show the relative change, and it should be noted that SiN_x passivated devices have high initial leakage currents, surpassing 1 mA/mm. This is reduced after radiation exposure up to a dose of 9.2 Mrad, when it increases again, correlating with the change in transconductance in Fig. 5.2 and 5.3.

Fig. A1.2 shows the change in saturated drain current (I_{dss}) and off-state gate leakage ($I_{g\text{-}leak}$) measured in SiN_x passivated InAlN and AlGaN HEMTs during radiation exposure

and post-irradiation annealing compared to reference devices not exposed to radiation. InAlN-SiN_x reference devices show an instability in I_{dss} with time, which seems to be aggravated by gamma radiation (Fig. A1.2(a)). AlGaN-SiN_x HEMTs show generally stable I_{dss} regardless of radiation exposure (Fig. A1.2(b)). For both InAlN and AlGaN SiN_x passivated HEMTs leakage is generally stable in the reference samples, showing an overall decrease in irradiated devices.

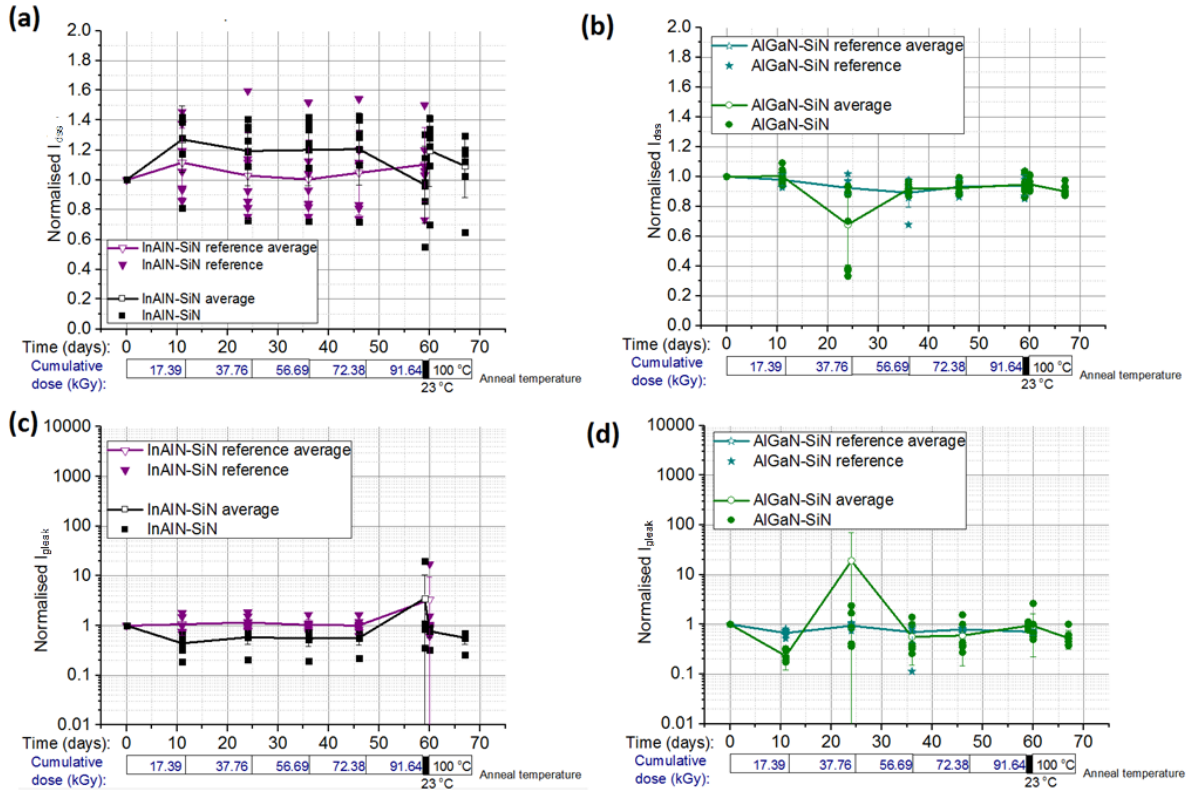

Fig. A1.2: Change in I_{dss} ((a) and (b)) and $I_{g\text{-}leak}$ ((c) and (d)) in InAlN ((a) and (c)) and AlGaN ((b) and (d)) HEMTs during radiation exposure and post-irradiation annealing.

9.2 Appendix 2: Summary of device simulations

The simulation of electronic devices using specially designed software packages is a common practice used in their optimisation and understanding. Silvaco is a commercially available finite-element device simulation package and was used to provide support to experiments in this work. The ATLAS BLAZE module was utilised due to its ability to model devices fabricated using advanced materials[42]. AlGaN HEMTs have been successfully simulated using this approach[276]. InAlN was not listed in the ATLAS material library, meaning material properties had to be measured experimentally or extracted from the scientific literature and then entered as input into the simulation.

III-nitride materials are a recent innovation compared to Si and III-V technologies, and consequently less is understood about the physical mechanisms that dominate device behaviour, such as polarisation effects and surface recombination (see Chapter 2). In this sense simulations can be helpful, by comparing simulated data to experimental results and analytically investigating device operation. It also limits the usefulness of the simulation to the user's ability to virtually recreate the physical environment present in a real device and also the physical mechanisms available in a given simulation package.

During the course of this project InAlN and AlGaN HEMTs were simulated using the Silvaco ATLAS package, with the aim of replicating experimental results of device fabricated in parallel. The limited computational resources available and a number of (at the time) poorly understood challenges in material epitaxy and device fabrication prevented the bridging of experimental and simulated results. InAlN and AlGaN HEMTs were successfully simulated, with results qualitatively matching those measured experimentally and seen in the scientific literature (i.e. shape of I_d-V_g and I_d-V_d plots). Example III-V MOSFET devices included in the simulation package were also simulated.

Fig. A2.1 shows the simulation of a basic InAlN HEMT device. Generic conductor material (with a low work function) is placed in direct contact with the 2DEG at the InAlN/GaN heterojunction to account for the complex Ohmic conduction mechanisms that prohibit accurate simulation (Section 2.4.2). From this case material and device properties (such as mobility, gate length, Ohmic resistance etc.) were modified and the effect on the

corresponding I_d-V_g and I_g-V_g and high frequency response results were analysed. This process acted as a guide to device design (Section 3.6), giving an idea of the optimal device dimensions and material properties that were then considered alongside practical targets for crystal epitaxy and device fabrication, resulting in the design that was implemented on the lithography masks.

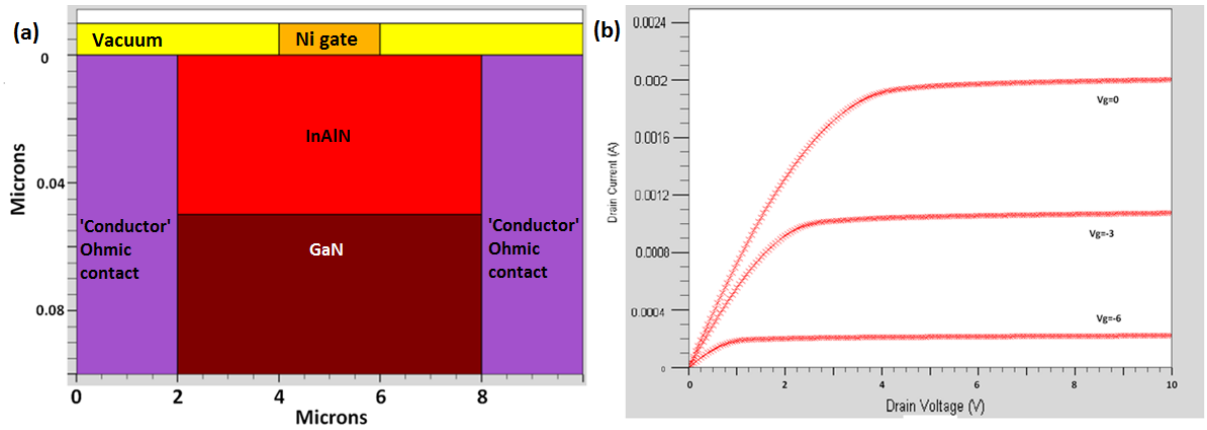

Fig. A2.1: (a) Cross section schematic of a simulated InAlN HEMT device and (b) corresponding I_d-V_d plot

Further functionality of the simulation is expressed in Fig, A2.2, where a 'cutline' taken across the simulated InAlN HEMT is shown in terms of the local valence and conduction band energy levels. By correctly introducing computational models to account for polarisation at the heterojunction, electron recombination at the InAlN surface, electronic trap phenomena and others the simulation becomes more accurate and more complex. As more experimental discoveries were made about the physical processes dominant in InAlN HEMTs, i.e. interfacial roughening (Section 4.2), electronic trapping (Chapter 5), Ohmic contact thermionic emission (Section 6.1) and surface leakage (Section 6.2), the simulations became too complex and computation time became impractical.

It is thought that optimisation of the model used here would allow for successful simulation of InAlN HEMTs in the future, encouraged by the successful simulation in this work of devices with reduced channel dimensions. As more experimental materials data

is published for InAlN finite-element device simulation is expected to become a critical tool for InAlN HEMT production. However, device simulation was not the main focus of this work and as such the simulations here can only be thought of as approximations to real devices. Despite this the changes in DC output as discussed in Section 3.6 were confirmed for III-V devices and are generally applicable to all FET type devices.

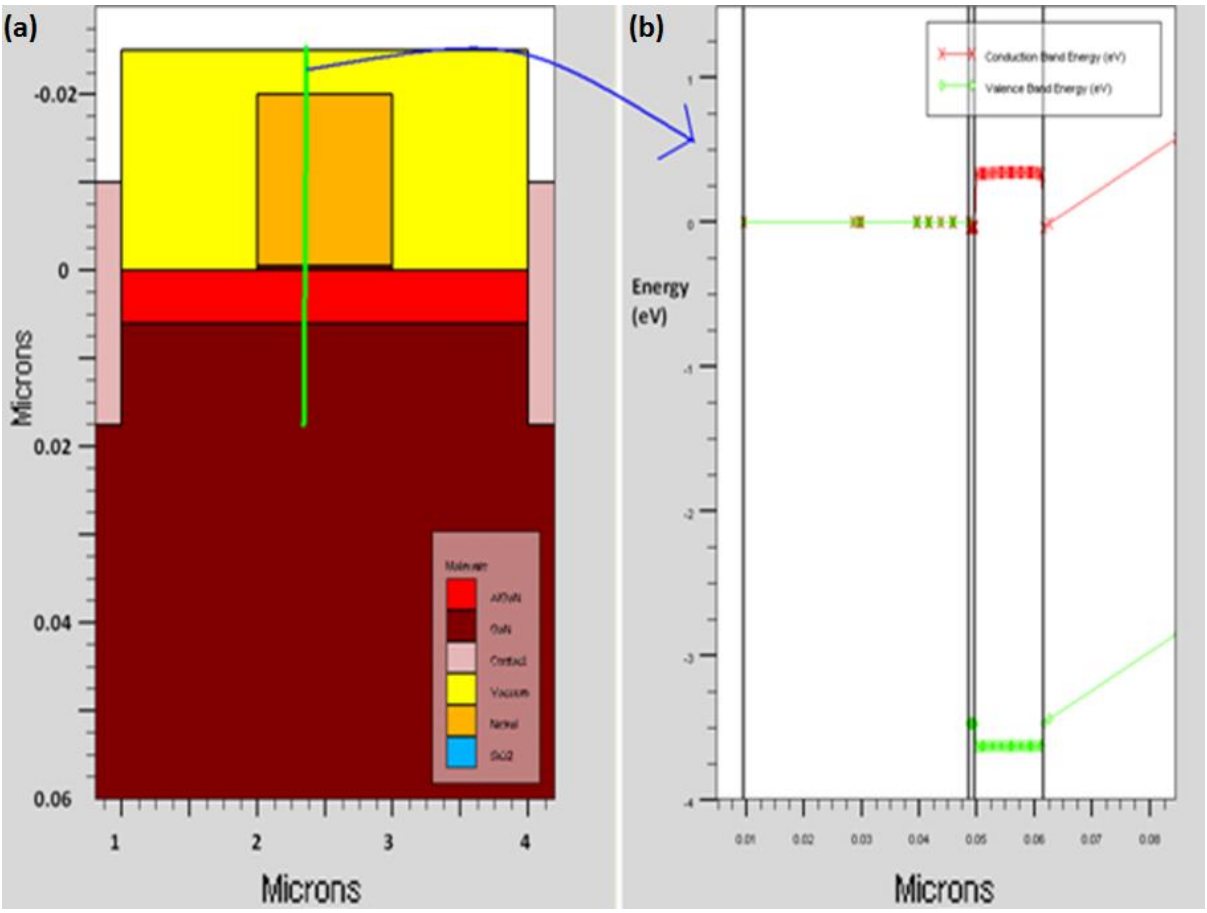

Fig. A2.2: (a) Cross section schematic of a simulated InAlN HEMT device with a 'cutline' and (b) corresponding valence and conduction band profiles along the cutline

9.3 Appendix 3: Effect of TEM beam exposure on thermal desorption

This appendix builds on the results of the in-situ high temperature TEM analysis of InAlN HEMTs from Section 6.1.1. Fig. 6.6 shows the effect of high temperatre exposure on the III-nitride semiconductor to metal contact interface up to 880°C. Beyond this temperature the III-nitride material began to desorb, as in Fig. A4.1.

The metal contact shows lmited desorption up to 960°C in contrast to the GaN buffer layer which is mostly disappeared (Fig. A4.1(a)). The InAlN barrier layer remains even at 960°C, encouraging for the future high temperature use of InAlN HEMTs in which the GaN buffer is protected by the InAlN barrier from atmospheric desorption.

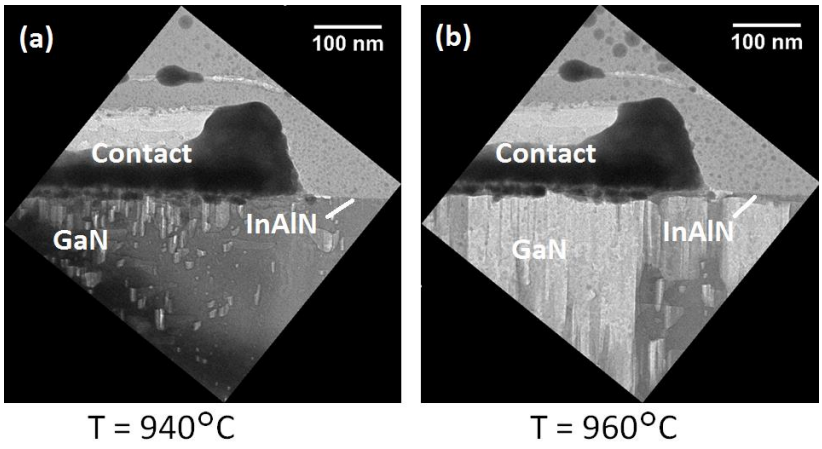

Fig. A4.1: InAlN HEMT Ohmic contact after annealing at (a) 940°C and (b) 960°C under vacuum conditions and imaged in-situ by high temperature TEM

The highest temperature reached during the TEM measurement was 980°C. Upon completion of the high temperature TEM measurement the sample was cooled by natural convection back to room temperature. Prior to sample unloading an image was taken at a reduced zoom to generate a final image of the full sample. This is shown in Fig. A4.2.

A distinct difference is noted between the areas focussed on during high temperature TEM and those not in the field of view. In areas not exposed to the TEM beam, the metal contact shows a higher rate of desorption than that within the TEM beam area. The opposite is true for the III-nitride semiconductor material, which appears to have a higher desorption rate when exposed to the TEM beam.

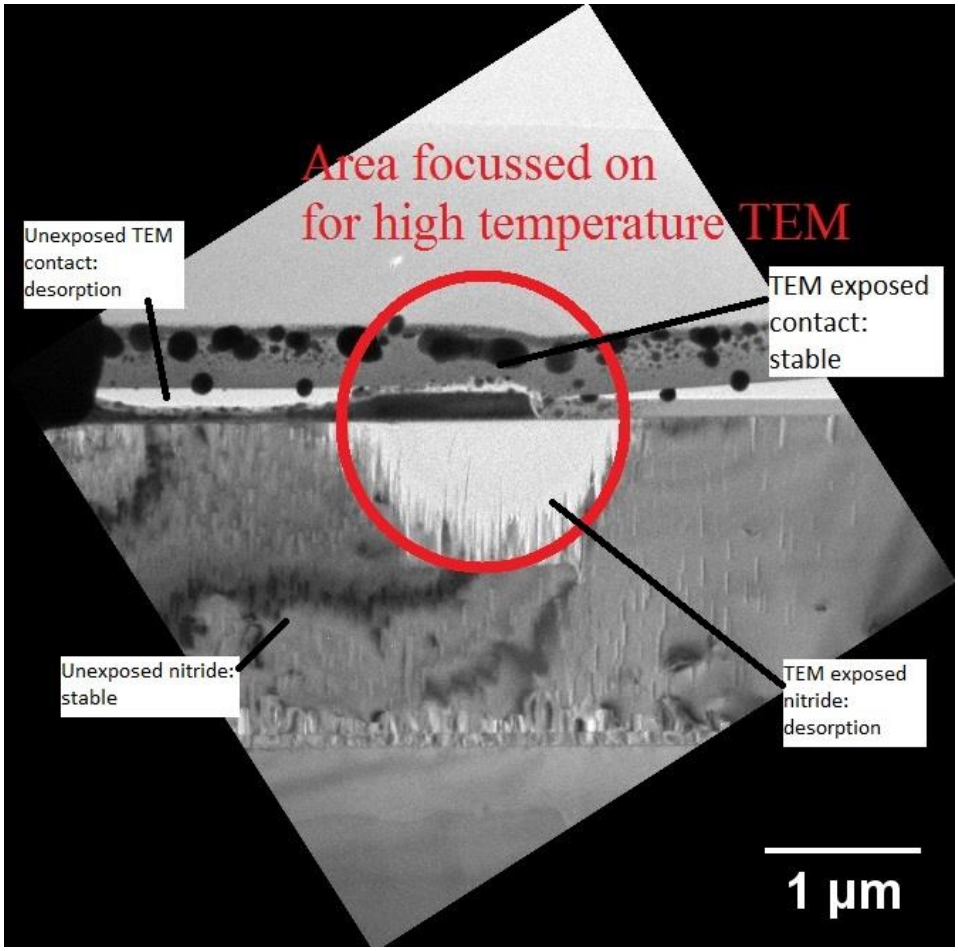

Fig. A4.2: InAlN HEMT Ohmic contact after annealing at 980°C under vacuum conditions and imaged in-situ by high temperature TEM upon cooling to room temperature, at reduced zoom

The TEM beam may be considered as a stream of electrons that pass through the sample and are redetected after scattering to generate the image. Therefore the sample is essentially conducting electricity during the imaging process, with the current profile confined to the area being imaged. Fig. A4.2 appears to suggest that the desorption rate of materials under high temperature is dependent on the charge flowing through the

area of interest. Furthermore the image in Fig. A4.2 indicates that metals and semiconductors behave in qualitatively different ways under such conditions.

To the author's knowledge no known physics currently accounts for such an effect, and further investigation is clearly warrented. This is of interest from a purely academic standpoint (i.e. the discovery of new physical mechanisms) and for designers wishing to explore the use of high reliability electronics to explore extreme high temperature environments in-situ.

10. Table of abbreviations

Institutions and organizations

ESA	-	European Space Agency
ESTEC	-	European Space Research and Technology Centre
JUICE	-	Jupiter Icy Moon Explorer
UKNC	-	UK Nitrides Consortium

Device abbreviations

BJT	-	Bipolar junction transistor
IGBT	-	Insulated gate bipolar transistor
FET	-	Field-effect transistor
MOSFET	-	Metal-oxide-semiconductor field-effect transistor
MESFET	-	Metal-semiconductor field-effect transistor
JFET	-	Junction field-effect transistor
HFET	-	Heterostructure field-effect transistor
HEMT	-	High electron mobility transistor
MMIC	-	Monolithic microwave integrated circuit

Process and measurement abbreviations

AFM	-	Atomic force microscopy
ALD	-	Atomic layer deposition
CTLM	-	Circular transmission line model
C-V	-	Capacitance-voltage profiling
CCS	-	Close-coupled showerhead
ECCI	-	Electron channelling contrast imaging
EC-V	-	Electrolytic capacitance-voltage profiling
EDX	-	Energy-dispersive X-ray spectroscopy
FIB	-	Focussed ion beam
gTLM	-	Gate transmission line model
HF	-	High frequency
ICP	-	Inductively-coupled plasma

MBE	-	Molecular beam epitaxy
MF	-	Mixed frequency
MOVPE	-	Metalorganic vapour phase epitaxy
MOCVD	-	Metalorganic chemical vapour deposition
PCM	-	Process control monitoring
PECVD	-	Plasma-enhanced chemical vapour deposition
RBS	-	Rutherford Backscattering Spectrometry
RSM	-	Reciprocal space map
RTP	-	Rapid thermal processor
SEM	-	Scanning electron microscopy
SIMS	-	Secondary ion mass spectroscopy
STEM	-	Scanning transmission electron microscopy
TEM	-	Transmission electron microscopy
TFE	-	Thermionic field-emission
TLM	-	Transmission line model
uTLM	-	Linear (ungated) transmission line model
WDX	-	Wavelength-dispersive X-ray spectroscopy
XPS	-	X-ray photoelectron spectroscopy
XRD	-	X-ray diffraction

Device and process parameters

2DEG	-	2-dimensional electron gas
2DHG	-	2-dimensional hole gas
a, c	-	Crystal lattice vectors
C_{gate}	-	Gate capacitance
C_{gd} C_{gs} C_{sd}	-	Capacitance (gate-drain, gate-source, source-drain)
C_{oxide}	-	Oxide capacitance
d	-	Interpanar spacing
$d_{g\text{-}d}$ $d_{g\text{-}s}$ $d_{s\text{-}d}$	-	Contact separation (gate-drain, gate-source, source-drain)
DIBL	-	Drain-induced barrier leakage
E_c	-	Conduction band
E_F	-	Fermi level
E_V	-	Valence band
E_g	-	Band gap
$f_{MAG10dB}$	-	Frequency at which maximum available gain = 10 dB
f_{max}	-	Unity power gain cut-off frequency
f_t	-	Unity current gain cut-off frequency
FOM	-	Figure of Merit
FWHM	-	Full-width half maximum
g_m	-	Transconductance
g_{m_max}	-	Maximum transconductance
(h,k,i,l)	-	Miller indices
I_{dss}	-	Saturation drain current (V_{ds} = 10 V, V_{gs} = 0 V)
I_{dss+}	-	Saturation drain current (V_{ds} = 10 V, V_{gs} = +1 V)
$I_{ds\text{-}max}$	-	Maximum drain current (V_{ds} = 10 V, V_{gs} = +2 V)
$I_{g\text{-}leak}$ $I_{d\text{-}leak}$ $I_{s\text{-}leak}$	-	Leakage current (gate, drain, source)
I_{gd} I_{gs} I_{sd}	-	Current (gate-drain, gate-source, source-drain)
IL	-	Interlayer
L_g	-	Gate length
L_{gd} L_{gs} L_{sd}	-	Inductance (gate-drain, gate-source, source-drain)

L_T	-	Transfer length
MAG	-	Maximum available gain
N	-	Number of gate fingers
n_s	-	Sheet carrier concentration
P_{MAX}	-	Maximum power output
$\underline{\mathbf{P}}_{PZ}$	-	Piezoelectric polarisation
$\underline{\mathbf{P}}_{SP}$	-	Spontaneous polarisation
$\underline{\mathbf{P}}_{tot}$	-	Total polarisation
PAE	-	Power added efficiency
Q_e	-	Electron charge
Q_{XY}	-	Quiescent point
R_c	-	Contact resistance
R_{gd} R_{gs} R_{sd}	-	Resistance (gate-drain, gate-source, source-drain)
R_{on}	-	On-resistance
R_{sh}	-	Sheet resistance
RF	-	Radio frequency
rms	-	Route-mean-square
S-S_{th}	-	Subthreshold swing
t_{Au}	-	Gold layer thickness
$t_{barrier}$	-	Barrier layer thickness
t_{Ti}	-	Titanium layer thickness
T_{anneal}	-	Anneal temperature
T_{GaN}	-	GaN growth temperature
T_{InAlN}	-	InAlN growth temperature
v_{sat}	-	Saturation velocity
V_{bi}	-	Built-in voltage
V_{BK}	-	Breakdown voltage
V_{drain} V_{source} V_{gate}	-	Voltage (drain, source, gate)
V_{gd} V_{gs} V_{sd}	-	Voltage (gate-drain, gate-source, source-drain)
V_T	-	Threshold voltage
W	-	Device width
Z_0	-	Characteristic impedance
Δ	-	Sub-band correction term
ε_r	-	Relative dielectric constant
γ	-	Sheet resistance thermal stability power index
λ	-	Wavelength⁄MOSFET channel length modulation term
$\sigma_{interrface}$	-	Polarisation charge
Φ	-	Work function
$\Phi_{barrier}$	-	Schottky barrier height
ρ_c	-	Specific contact resistivity
θ	-	X-ray scattering angle
μ	-	Mobility
ω	-	X-ray scattering angle

11. Table of tables

12. Table of figures