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Quantum confinement-induced semimetal-to-semiconductor evolution in large-area ultra-thin $PtSe_2$ films grown at 400 °C

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In this work, we present a comprehensive theoretical and experimental study of quantum confinement in layered platinum diselenide ($PtSe_2$) films as a function of film thickness. Our electrical measurements, in combination with density functional theory calculations, show distinct layer-dependent semimetal-to-semiconductor evolution in $PtSe_2$ films, and highlight the importance of including van der Waals interactions, Green's function calibration, and screened Coulomb interactions in the determination of the thickness-dependent $PtSe_2$ energy gap. Large-area $PtSe_2$ films of varying thickness (2.5–6.5 nm) were formed at 400 °C by thermally assisted conversion of ultra-thin platinum films on Si/SiO_2 substrates. The $PtSe_2$ films exhibit *p*-type semiconducting behavior with hole mobility values up to 13 $cm^2/V{\cdot}s$. Metal-oxide-semiconductor field-effect transistors have been fabricated using the grown $PtSe_2$ films and a gate field-controlled switching performance with an I_{ON}/I_{OFF} ratio of >230 has been measured at room temperature for a 2.5–3 nm $PtSe_2$ film, while the ratio drops to <2 for 5–6.5 nm-thick $PtSe_2$ films, consistent with a semiconducting-to-semimetallic transition with increasing $PtSe_2$ film thickness. These experimental observations indicate that the low-temperature growth of semimetallic or semiconducting $PtSe_2$ could be integrated into the back-end-of-line of a silicon complementary metal-oxide-semiconductor process.

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INTRODUCTION

Two-dimensional (2D) transition metal dichalcogenides (TMDs) have attracted extensive interest as this class of layered materials exhibit electronic properties from semimetals to semiconductors. In addition, their properties may significantly change when moving from bulk to ultra-thin films due to strong spin–orbit coupling (SOC).[1–3] These properties open up new opportunities in bandgap engineering for future optical and electronic devices. In addition, TMDs have the potential to form atomically abrupt heterostructures from materials that are not lattice matched.[4] TMD materials are also promising with respect to the integration of memory, logic, photonic, sensor, and general input/output functions above conventional silicon-integrated circuits in the back-end-of-line (BEOL) provided low thermal budget processes can be developed at ≤400 °C.[5]

2D atomic crystals of platinum diselenide ($PtSe_2$) exhibit distinct electronic structures and properties. $PtSe_2$ is a layered material in which individual atomic layers are stacked together by van der Waals (vdW) interactions. Although the bulk crystal is a semimetal with a slight indirect overlap of the conduction and valence bands,[6] monolayer (ML) $PtSe_2$ has been revealed to be a semiconductor.[7,8] Thus, $PtSe_2$ has attracted growing attention due to its high performance in photocatalysis for water splitting,[7] gas and pressure sensors,[9,10] electronics,[11] optoelectronics,[12] and as a potential candidate for spintronics and valleytronics[8] applications.

In 2015, Wang et al.[8] reported that the surface of a Pt(111) crystal can be selenized to form ML $PtSe_2$ at 270 °C. This method is convenient to yield large-area films up to millimeter size and allows the band structure of ML $PtSe_2$ to be studied. However, the metallic Pt substrate hinders electronic applications where an insulating substrate is generally needed. Although atomically thin $PtSe_2$ flakes with different thickness can be mechanically exfoliated from the bulk crystals[13,14] and are very well suited for fundamental studies, this approach is not scalable. Recently, the growth of $PtSe_2$ films on sapphire substrates by chemical vapor deposition (CVD) at 900 °C[15] and $PtSe_2$ synthesis through direct reaction of metal platinum foil and selenium powder under high pressure and high temperature (600–800 °C)[16] have been reported. $PtSe_2$ films grown on sapphire substrate by CVD at 500 °C was recently reported indicating how the doping type of the films can be modified by the stoichiometry of the $PtSe_2$ films by a rapid or slow cool down process, which modifies the Se precursor supply.[17] In ref.,[18] 1 ML to 22 ML $PtSe_2$ films have been grown on bilayer graphene/6H-SiC (0001) substrates by molecular beam epitaxy, which in principle could be extended to grow large size films on dielectric substrates.

In this study, the electronic structure and carrier transport properties of $PtSe_2$ films with different thicknesses are investigated theoretically and experimentally. First-principles calculations considering vdW interactions for pristine $PtSe_2$ films are performed. Calibration of Green's function with screened Coulomb interaction (*GW*) is utilized to predict the quantitative values of the

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bandgap energy. The bandgap opening in few-layer $PtSe_2$, reported in other works,[7,8,14,19–23] is shown to depend strongly on the simulation framework, with a progressive increase in the $PtSe_2$ energy gap when considering density function theory (DFT), to DFT with the addition of vdW interactions, and finally to DFT with vdW interactions and screened Coulomb interaction. The Bohr radius provides an estimation of when the quantum effects modify the band structure. The Bohr radius of 10 nm is calculated for bulk $PtSe_2$ with electron-effective mass of $0.22 \times m_0$ and bulk $PtSe_2$ dielectric constant of 40.[24] Within this simulation framework, we investigate the impact of Pt vacancies on the $PtSe_2$ band structure and the density of states (DoS). For ML and bilayer structures, our atomic-scale simulations reveal that Pt vacancies lead to the creation of localized energy states in the bandgap and a shift in the Fermi level towards the $PtSe_2$ valence band.

To explore these effects experimentally, we have synthesized large-area $PtSe_2$ films by thermally assisted conversion (TAC) of pre-deposited Pt layers at 400 °C on Si/SiO_2 substrates. Hall measurements of the $PtSe_2$ films reveal *p*-type majority carriers for all TAC-grown $PtSe_2$ films with mobilities in the range of 5–13 $cm^2/V{\cdot}s$. Back-gated $PtSe_2$ metal-oxide-semiconductor field-effect transistors (MOSFETs) demonstrate *p*-channel behavior, consistent with the experimental van der Pauw Hall measurements of the large-scale films. The Hall analysis and the back-gated $PtSe_2$ MOSFET characteristics are both consistent with the theoretical calculations, showing *p*-type $PtSe_2$ films and a transition from semimetallic behavior for films from 5 to 6.5 nm to a semiconducting behavior for a film thickness of 2.5 to 3 nm.

RESULTS

First-principles ab initio calculations

Bulk $PtSe_2$ is a semimetal with trigonal symmetry, where Pt atoms are coordinated by six neighboring Se atoms. In ultra-thin $PtSe_2$ films a bandgap opens up. The effects of quantum confinement (QC) determine the value of the confinement-induced bandgap in the $PtSe_2$ thin films. Ab initio techniques are applied to study $PtSe_2$ thin films. Standard theoretical methods for calculating band structure based on DFT are well known to under-estimate the predicted bandgaps primarily due to approximations for the electronic exchange and correlation energies. VdW interlayer interaction in layered materials such as $PtSe_2$ improves the structural and electronic properties description obtained by DFT calculations. Hence, we have incorporated vdW interaction in our calculations by adding a nonlocal vdW term to local and semi-local exchange correlation functionals. In addition, to provide further improved quantitative description of the bandgap energies, *GW* (G: Green's function and W: screened Coulomb interaction) calibration in combination with a many-body perturbation theory is also implemented.[25] Green's function theory provides quasi-particle energies using the electron self-energy operator containing the effects of exchange and correlations with other quasi-particles.

Figure 1a illustrates the band structure of a ML $PtSe_2$ film. The ML $PtSe_2$ exhibits an indirect bandgap of 1.2 eV when *GW* correction is not accounted for. The band structure of bulk $PtSe_2$ is shown in Supplementary Fig. 1, which exhibits the semimetallic characteristic and is in good agreement with literature,[14] where both electron and hole pockets coexist at the Fermi surface. With the increase of number of PtSe2 layers, the energy level of valence band maximum (VBM) exceeds that of conduction band minimum (CBM), leading to overlap of bands and hence semiconductor-to-semimetal evolution. In the *GW* calculations, the method in ref. [26] has been used enabling improved convergence in the bandgap energies with a reduced set of empty states. Due to the computational demands of *GW* calculations, this approach was applied to films between 0.5 and 2 nm thickness and used to extrapolate the effect of QC for thicker films as shown in Fig. 1b. A decrease in bandgap energy by increasing the number of layers has been shown to be due to interlayer coupling and screening effects, which change the electronic wave function hybridization in the valleys of both the valence and conduction bands.[27] As can be seen in Fig. 1b, bandgap values calculated using DFT, DFT + vdW, and *GW* calibration are 1.2 (0.15) eV, 1.2 (0.51) eV, and 2.43 (1.5) eV for ML (bilayer) $PtSe_2$ film, respectively. In other words, comparable bandgaps to conventional semiconductors are expected in thin $PtSe_2$ films; for example, bilayer and trilayer $PtSe_2$ films have bandgaps comparable with GaAs and Ge, respectively. Our predicted bandgap values are benchmarked against other values from literature in Fig. 1b.

The role of vacancies is also investigated from first-principles using fully relativistic electronic structure calculations based on DFT implemented in OpenMx[28] and QuantumATK.[29] The electronic energy within the framework of Kohn–Sham DFT is calculated using pseudo-atomic localized basis functions. The localized basis functions allow the consideration of larger supercell dimensions and hence lower vacancy density. The effect of SOC must be considered in $PtSe_2$ films due to its strong effect in the 5*d* orbitals of the transition metal atoms. Grimme's dispersion correction for the vdW interaction is also incorporated in our calculations.[30] Periodic boundary conditions are applied to create simulation supercells and the cell dimension along the film growth axis is chosen to be >2 nm to avoid any interaction between the periodic images of the neighboring slabs. The geometries are fully relaxed until the force acting on each atom is <0.01 eV/Å. The structure consists of a single defect in $6 \times 6 \times 1$ supercell corresponding to defect density of 2.3×10^{13} cm^{-2}. The periodic images of the point defects are more than 2 nm apart from each other, where defect–defect interaction is negligible. In the calculation of point defects, instead of removing the atom from the lattice, it is replaced by an "empty" atom. Empty atoms are basis functions in the vacancy center with zero pseudopotential cores and zero number of electrons. These basis set orbitals can be populated to host a finite electron density in a region where there are no real atoms. The lattice parameters of the relaxed pristine $PtSe_2$ film after geometry optimization are shown in Supplementary Fig. 2. After the geometry optimization of the structure with the Pt vacancy, the position of the point-defect neighbor atoms is modified in comparison with their position in the pristine structure as shown in this figure. The Se atoms at the top layer next to the Pt vacancy move outward, while the Se atoms at the bottom layer move downward. This movement of the Se atoms results in a slight shrinkage of Pt-Se bond lengths ($b_{Pt\text{-}Se}$) near the vacancy from 2.54 to 2.51 Å and an increase in the diagonal separation between the Se-Se atoms from $2 \times b_{Pt\text{-}Se} = 5.08$ to 5.45 Å, as indicated in the Supplementary Fig. 2, and are consistent with the previously reported results (ref. [23] and ref. 45 therein; ref. [31] and ref. 42 therein).

Using supercells in studying the effects of vacancies is inevitable in first-principles calculations. However, as the size of the supercell increases, the corresponding first Brillouin zone (BZ) shrinks and as a result bands of the supercell are extremely "folded" into the first BZ. Therefore, it is challenging to analyze the effects of vacancies and impurities perturbation and to directly compare the folded bands with the reference band structure of a primitive cell or with the experimental results obtained by angle-resolved photoemission spectroscopy (ARPES) measurements. A procedure to unfold the primitive cell Bloch character hidden in the supercell eigenstates is known as "unfolding." By applying the unfolding procedure, the band structure of a supercell will be mapped to the band structure of a reference primitive cell.[32,33] Utilizing linear combination of atomic orbital basis sets in the presence of a perturbation, such as vacancy, allows mapping of the symmetry breakers, which perturb the band structure.

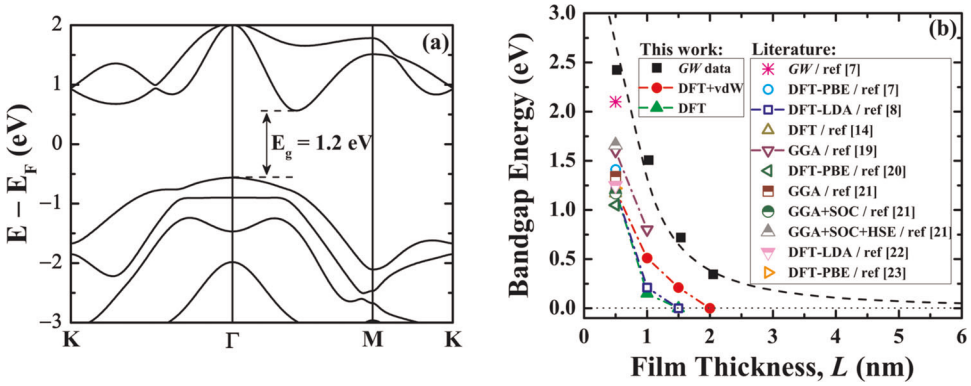


Fig. 1 Thickness-dependent bandgap of platinum diselenide ($PtSe_2$) films from first-principles calculations. **a** Band structure of a monolayer pristine $PtSe_2$ film obtained from our density function theory (DFT) calculations. **b** Bandgap energy versus $PtSe_2$ film thickness from our DFT (solid green), DFT corrected by van der Waals interactions (solid red), and calibrated by *GW* calculations (solid black). Dash-dotted lines are guide for the eye. The black dashed curve shows a power law fit a/L^{β}, where L is the film thickness with a and β as fitting parameters. Data from the literature is benchmarked in this figure. PBE: Perdew–Burke–Ernzerhof; LDA: local density approximation; GGA: generalized gradient approximation; SOC: spin–orbit coupling; HSE: Heyd–Scuseria–Ernzerhof

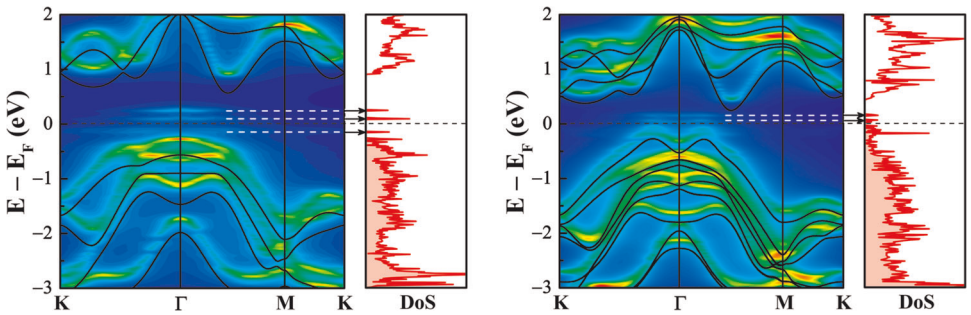


Fig. 2 Effects of Pt vacancy on the band structure of platinum diselenide ($PtSe_2$) films. Unfolded band structure of (left) monolayer $PtSe_2$ and (right) bilayer $PtSe_2$ film with Pt vacancy shown using contour plots of total weight intensity. The primitive cell band structure of pristine $PtSe_2$ is shown using black solid lines, which are in excellent agreement with band structures experimentally obtained by angle-resolved photoemission spectroscopy (ARPES) measurements for monolayer[8] and bilayer[18] $PtSe_2$. Total density of states (DoS) of each film is shown in the right panel. The localized states corresponding to the Pt vacancy are located close to the edge of the valence band within the bandgap and are shown by arrows. Zero of the energy shows the Fermi level. These results indicate indirect bandgap nature of monolayer and bilayer $PtSe_2$ films. The calculated band structures also indicate an increased hole mobility moving from the monolayer to the bilayer structure in $PtSe_2$

The unfolded band structures of the ML and bilayer $PtSe_2$ films with a Pt vacancy are shown as contour plots in Fig. 2. The primitive cell band structure of the pristine structure is shown by black solid lines as a reference. As mentioned above, SOC is considered, which provides a band structure that could directly be comparable with spin-ARPES measurements. As can be seen in Fig. 2, the CBM of the ML and bilayer $PtSe_2$ films is located halfway between the Γ and M points. In the $PtSe_2$ ML, the VBM is located at the Γ point, while there are two peaks in the valence band edge at either side of the Γ point (M-shape signature) for the bilayer $PtSe_2$, which are in excellent agreement with previously reported band structures experimentally obtained by ARPES measurements for ML $PtSe_2$[8] and bilayer $PtSe_2$.[18] The band structure of ML $PtSe_2$ supercell with Pt vacancy before unfolding is presented in Supplementary Fig. 3, which in comparison with Fig. 2 demonstrates that the unfolded band structure of the supercell can be directly compared with corresponding pristine unit cell structures.

The unfolding method also reveals vacancy-induced almost-flat localized energy states within the bandgap indicating high carrier mass and hence low mobility and strong localized nature of vacancies in these supercells, which can also be realized from partial density of states (DoS) presented in Supplementary Fig. 4. The total DoS on the right panel of Fig. 2 is mapped to the band structure, where arrows indicate the defect-induced states. In this figure, the energy axis is referenced to the Fermi energy (E_F), and as can be seen, the Fermi level is shifted towards the valence band edge in the case of Pt vacancy, indicating that the Pt vacancy results in a *p*-type characteristic of the $PtSe_2$ films. Another important outcome of this study is that on the contrary to most of the other ultra-thin TMDs, indirect-to-direct transition of bandgap is not observed in ML $PtSe_2$ film (ref. [34] and references therein).

Experimental results

In this study, $PtSe_2$ thin films are synthesized by TAC of pre-deposited Pt layers on Si/SiO_2 substrates. A growth temperature of 400 °C was used, and growth was achieved directly on the Si/SiO_2 substrate (see the Methods section for more details). In order to investigate the influence of QC effects in $PtSe_2$, films with different thicknesses are prepared. Cross-sectional transmission electron microscope (XTEM) images of the as-grown films with 0.7 and 1 nm Pt nominal thickness as the staring material are shown in Fig. 3, illustrating the layered structure and polycrystalline nature of the $PtSe_2$ films after conversion. The $PtSe_2$ film thicknesses are 2.5–3 and 5–6.5 nm for the two Pt starting films after the TAC process. XTEM images of the transferred films are shown in Supplementary Fig. 5, demonstrating successful film transfer. Raman spectra of the $PtSe_2$ films grown from various Pt thicknesses, that is, 0.7, 1, and 1.5 nm, are shown in Supplementary Fig. 6.

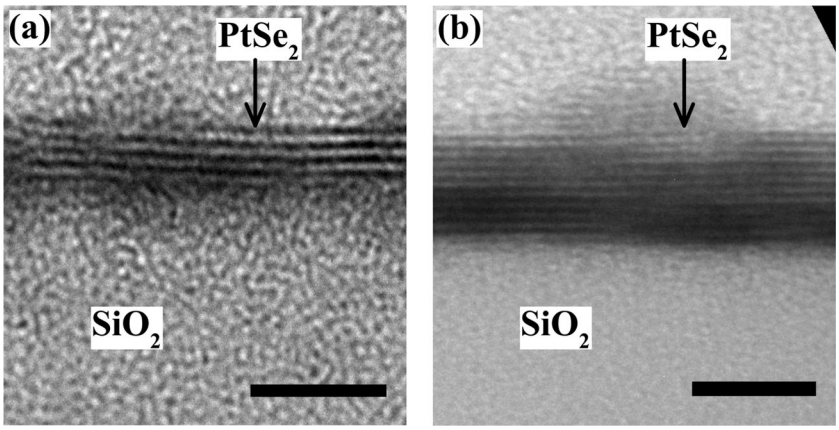


Fig. 3 Physical analysis of the platinum diselenide ($PtSe_2$) films by transmission electron microscopy (TEM). Cross-sectional TEM image of as-grown **a** 2.5–3 nm and **b** 5–6.5 nm $PtSe_2$ sample. In both samples, the $PtSe_2$ is layered and each layer is parallel to the underlying oxide surface. Scale bar is 5 nm

Table 1. Resistance and Hall-effect properties (assuming a unity Hall factor) of $PtSe_2$ films with various $PtSe_2$ film thicknesses

Starting Pt film nominal thickness	0.7 nm Pt	1 nm Pt	1.5 nm Pt	1.5 nm Pt (post transfer)
Number of MLs and thickness range of converted $PtSe_2$ from HR-XTEM	5–6 MLs 2.5–3.0 nm	10–12 MLs 5–6.5 nm	Not available	Not available
Carrier type	*P*	*P*	*P*	*P*
Hall mobility ($cm^2/V{\cdot}s$)	7.9	5.6	12.7	13.4
Sheet resistivity (Ω/sq)	5.0×10^5	2.1×10^4	3.4×10^3	4.6×10^3
Sheet carrier concentration (cm^{-2})	1.6×10^{12}	5.4×10^{13}	1.4×10^{14}	1.0×10^{14}
Sheet Hall coefficient (cm^2/C)	4.0×10^6	1.2×10^5	4.4×10^4	6.2×10^4
Resistivity ($\Omega{\cdot}cm$)[a]	1.3×10^{-1}–1.5×10^{-1}	1.0×10^{-2}–1.4×10^{-2}	Not available	Not available
Carrier concentration (cm^{-3})[a]	6.3×10^{18}–5.3×10^{18}	1.1×10^{20}–8.3×10^{19}	Not available	Not available

$PtSe_2$ platinum diselenide, *ML* monolayer, *HR-XTEM* high-resolution cross-sectional transmission electron microscope
[a]Resistivity and carrier concentration is calculated based on actual $PtSe_2$ film thickness from XTEM

As pointed out earlier, $PtSe_2$ films are synthesized on centimeter-scale substrates allowing us to perform Hall measurements. From four-point *I–V* measurements and Hall measurements, we determined the resistivity, the majority carrier type, the carrier density, and the Hall mobility of the $PtSe_2$ films. The Hall-effect measurements are performed in a van der Pauw configuration with a LakeShore Model 8404 AC/DC (alternate current/direct current) Hall-effect measurement system. See the Methods section for more details. The room temperature Hall-extracted properties of the $PtSe_2$ films are summarized in Table 1. A typical two-point *I–V* characteristic is shown in Supplementary Fig. 7. The sample has an almost square area of 1 cm^2. To ensure reproducibility, 5–6.5 nm $PtSe_2$ samples were made on different occasions over the course of 3 months. The Hall-effect measurement results of the two different batches made with 3-month intervals are shown in Supplementary Table 1, confirming the reproducibility of the process. Very consistent Hall data are obtained growing the $PtSe_2$ films on different substrates, for example, sapphire, results of which are shown in Supplementary Table 2.

The few-layer structure and the approximate thickness of the $PtSe_2$ films, examined by high-resolution XTEM (HR-XTEM), are presented in Fig. 4a. As can be seen, the $PtSe_2$ thin films synthesized from 0.7 to 1 nm Pt starting nominal thickness are 2.5–3 and 5–6.5 nm thick, corresponding to 5–6 and 10–12 atomic layers, respectively. Films are all planar and layered along the XTEM lamella and are polycrystalline, with several nanometer-sized crystalline domains. Hall-effect measurements on all $PtSe_2$ films indicate *p*-type dominant carrier type, consistent with our atomic-scale simulation including the effects of Pt vacancies in the films (see Fig. 2). The presence of grain boundaries and vacancies is not unexpected given the polycrystalline nature of the films. It is important to note that adsorbates could also be contributing to the *p*-type behavior observed in the $PtSe_2$ films; hence, an investigation of how the ambient and pressure influence the electrical properties of the $PtSe_2$ films would be valuable in terms of providing a more complete understanding of the factors, which impact the carrier type and carrier density in $PtSe_2$ films. This is the area of an on-going study. The Hall measurements in Table 1 indicate an increase in sheet carrier concentration, and a corresponding decrease in sheet resistivity, as the $PtSe_2$ thickness increases. This is consistent with a semiconductor-to-semimetal evolution in ultra-thin $PtSe_2$ films calculated with our atomic-scale simulations (Fig. 1). As presented in Table 1, the Hall hole mobility values are in the range of 5 to 13 $cm^2/V{\cdot}s$.

To further explore the electrical properties of the $PtSe_2$ films, back-gated FETs were fabricated by patterning Ni/Au metal stack as the source and drain metal contacts to the $PtSe_2$ films on ~85 nm SiO_2 on p^{++}-Si (Si/SiO_2), followed by defining channel regions of different lengths and widths through etching (see Methods section for details). The p^{++}-Si is used as a shared "metal" back-gate electrode. A polymer-support film transfer

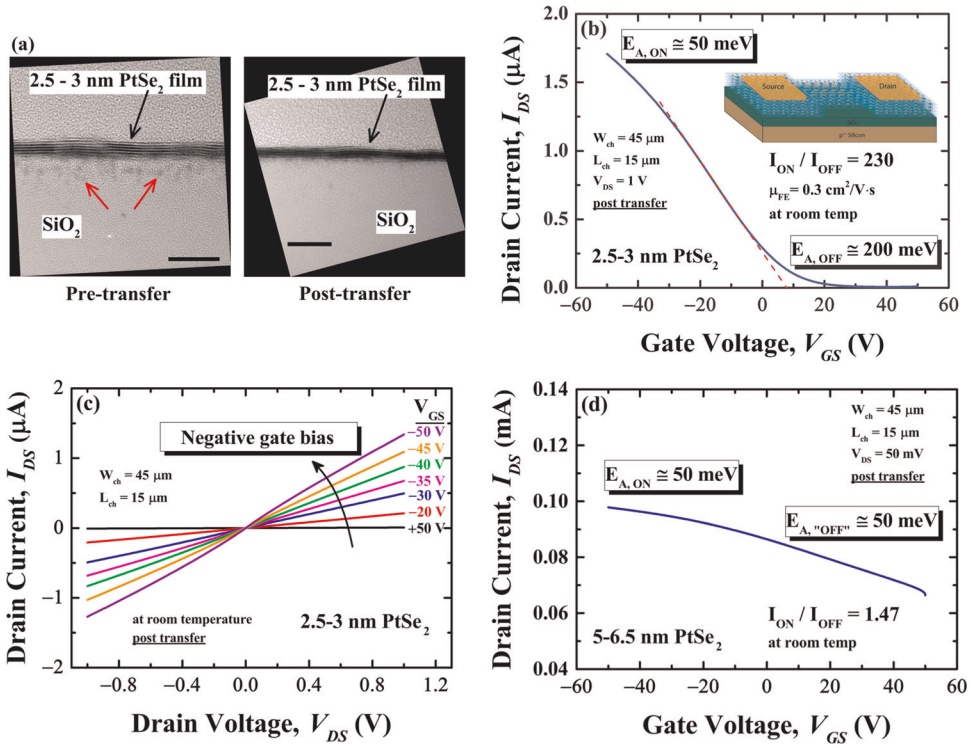


Fig. 4 Cross-sectional transmission electron microscopy (XTEM) of platinum diselenide ($PtSe_2$) films and electrical characterization of $PtSe_2$ back-gate devices. **a** Cross-section TEM image of $PtSe_2$ film with thickness of 2.5–3 nm (left) before and (right) after transfer. Red arrows point to the dark regions under the $PtSe_2$ film inside the oxide. Scale bar is 10 nm. **b** Room temperature transfer characteristic of a back-gated field-effect transistor (FET) device with a channel thickness of 2.5–3 nm $PtSe_2$, a channel length of 15 μm, and channel width of 45 μm at $V_{DS} = 1$ V. *P*-type characteristic and high ON/OFF ratio of 230 has been measured. Field-effect mobility is $\mu_{FE} = 0.3\ cm^2/V{\cdot}s$. **c** Room temperature output characteristic of the same device as in **b** illustrating linear and symmetric variation of the channel current with the drain voltage. **d** Transfer characteristic of a device with channel length of 15 μm and channel width of 45 μm, and $PtSe_2$ channel thickness of >5 nm at $V_{DS} = 50$ mV, showing very small current modulation. $E_{A,\ ON}$ and $E_{A,\ OFF}$ in **b** and **d** are the activation energies at "ON" and "OFF" states, respectively. **b** and **d** demonstrate the layer-dependent quantum confinement (QC)-induced bandgap opening reflected in the electrical characteristics of the $PtSe_2$ FETs

process was carried out to allow transfer of the $PtSe_2$ films from their original synthesized Si/SiO_2 substrates onto an unprocessed Si/SiO_2 for the fabrication of back-gate FETs (see Methods section for details). The motivation for the $PtSe_2$ film transfer is evident from Fig. 4a, indicating potential diffusion of Pt into the underlying SiO_2 during the film synthesis,[35] shown by the red arrows. A range of samples were diced from the same growth run to allow transfer and processing of nominally identical $PtSe_2$ films. The layered structure and the exact thickness of the $PtSe_2$ films (as-grown and transferred) are evaluated by TEM images as shown in Fig. 4a, demonstrating the successful $PtSe_2$ film transfer. $PtSe_2$ back-gated MOSFETs were fabricated using conventional complementary metal-oxide-semiconductor (CMOS) processing steps, on as-grown and transferred $PtSe_2$ films, with different thicknesses. Details of device fabrication are provided in the Methods section. MOSFETs with different channel lengths and widths were fabricated and typical transfer and output characteristics of the fabricated transistors are shown in Fig. 4b, c. The transfer and output characteristics highlight decreased drain current with positive gate voltage indicating *p*-type transport behavior of the $PtSe_2$ films consistent with the Hall measurements of large-area films. The I_{ON}/I_{OFF} ratio for the $PtSe_2$ MOSFET shown in Fig. 4b is 230, which is higher than previous reports for room temperature operation of $PtSe_2$ devices with channel thickness values in the range 2.5–3 nm.[13,17] The same characteristic in semi-log scale is shown in Supplementary Fig. 8a. In the case of the $PtSe_2$ MOSFET based on a channel thickness of 5–6.5 nm (see Fig. 4d), the I_{ON}/I_{OFF} ratio decreases to 1.4.[36] Based on the DFT calculations, this is consistent with a suppression of QC effect, and hence to the decrease in channel bandgap, as $PtSe_2$ film becomes thicker (see Fig. 1b). Devices with different channel dimensions show similar qualitative behavior of FET devices with *p*-type channels as shown in Supplementary Figs. 8b and c. Further experimental evidence to support the transition from a semimetal to a semiconductor with decreasing $PtSe_2$ thickness is evident from the activation energy (E_A) of the drain current in the ON state and OFF state of the transfer characteristics, as shown in Fig. 4b, d for the 2.5–3 nm and 5–6.5 nm $PtSe_2$ samples, respectively. The activation energy is extracted from temperature-dependent measurements shown in Supplementary Fig. 9. For the 5–6.5 nm $PtSe_2$ sample, the vdW and *GW* corrected DFT calculations extrapolated to 5–6.5 nm (see Fig. 1b) indicate a close to zero energy gap. This is confirmed by the lack of modulation of the $PtSe_2$ current with gate voltage and the activation energy of the current, which is 50 meV across the gate voltage sweep. By contrast, as shown in Fig. 4b for the 2.5–3 nm $PtSe_2$ device, the activation energy changes from 200 meV in the OFF state to 50 meV in the ON state. It is noted that the OFF state current activation energy of 200 meV is close to the extrapolated theoretical bandgap of the $PtSe_2$ at 2.5 nm, which is ~250 meV (see Fig. 1b).

From the characteristic presented in Fig. 4b and using $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W_{ch}}{L_{ch}} C_{ox} \mu_{FE} V_{DS}$, where $W_{ch} = 45$ μm is the channel width, $L_{ch} = 15$ μm is the channel length, and $C_{ox} = \varepsilon_0 \varepsilon_r / t_{ox}$, where $\varepsilon_r = 3.9$ and $t_{ox} = 85$ nm, and C_{ox} is the capacitance per unit area, we extract the field-effect mobility of $\mu_{FE} = 0.3\ cm^2/V{\cdot}s$. As expected, the field-effect mobility is smaller than the Hall-effect extracted mobility. This calculation represents the lower limit on the channel hole mobility, as contact resistance will result in a

reduced voltage drop across the channel. To investigate this point, we calculated the channel resistance $R_{ch} = \rho_{ch}L_{ch}/(W_{ch}t_{ch}) \approx 10^5\ \Omega$, where ρ_{ch} is the channel resistivity (see Table 1). Considering the total resistance $R_{tot} = V_{DS}/I_{DS} \approx 3.4 \times 10^6\ \Omega$ at a given back-gate bias of $V_{GS} = 0$ V, we obtain a large contact resistance of $R_c = (R_{tot} - R_{ch})/2 \approx 1.65 \times 10^6\ \Omega$ compared to the channel resistance; hence, the actual voltage drop across the channel would be $V_{ch} \approx 0.03$ V. Using V_{ch} instead of V_{DS} in the g_m equation, we obtain $\mu_{FE} \approx 10\ cm^2/V{\cdot}s$, which is close to the value obtained from Hall analysis and comparable to reported mobility for CVD-grown films.[17] It is important to note that the corrected μ_{FE} value of $\approx 10\ cm^2/V{\cdot}s$ is only an indicative value at the given V_{GS} since the channel and contact resistances are expected to vary with the gate field. The polycrystalline nature of our synthesized $PtSe_2$ films could be another origin of the relatively low mobility compared to previously reported values of 7–210 $cm^2/V{\cdot}s$ obtained from mechanically exfoliated $PtSe_2$ flakes.[14] However, considering the benefits of our growth process, namely, the low synthesis temperature, scalability and ease of controlling layer thickness, and the back-gated MOSFET characteristics in Fig. 4b and c, this is quite promising for a *p*-channel material formed at 400 °C. Contact engineering could further improve the device performance by structuring $PtSe_2$ films, benefiting from thick "bulk" semimetallic regions as source and drain contacts, and thin semiconducting channel connecting source and drain regions.[37,38] Due to the linear behavior of the output characteristic of the FETs (Fig. 4c), the possibility of a Schottky barrier-limited field-effect mobility is discarded.[39] This linear behavior could also be attributed to the small band offset at the source and drain contacts with respect to the edge of the valence band of the channel region in the case of Pt vacancies (see Fig. 2). Many reports in literature have indicated an ambipolar behavior in the transfer characteristic for TMD-based MOSFETS.[40,41] Our devices do not indicate an ambipolar response, and are consistent with a tunnel junction for holes and a Schottky barrier for electrons at the $PtSe_2$/Ni interface.

Electrical behavior of the $PtSe_2$ FETs was also characterized at different temperatures. The variation of the drain current activation energy with back-gate voltage is shown in Supplementary Fig. 9. For the transferred $PtSe_2$ film, in Supplementary Fig. 9a, the activation energy changes from 190 meV in the OFF state, which is close to the extrapolated $PtSe_2$ bandgap, to around 50 meV in the ON state. In the case of the non-transferred $PtSe_2$ films (see Supplementary Fig. 9b), the extracted E_A is in the range of 140–160 meV and does not change by the back-gate voltage. This result, in conjunction with the TEM analysis in Fig. 4a, indicates an interaction of the Pt with the SiO_2 substrate during growth, which prevents back-gate modulation of the current. The effect is removed after $PtSe_2$ film transfer, where back-gate modulation of the drain current and variation in the associated activation are evident. In the case of the $PtSe_2$ films with a thickness >5 nm, shown in Supplementary Fig. 9c, the extracted E_A is around ~50 meV and demonstrates no variation with back-gate voltage consistent with our atomic-scale simulations (see Fig. 1), suggesting very small bandgap for a >5 nm $PtSe_2$ films. These results demonstrate that bulk $PtSe_2$ exhibits metallic-like properties, in clear contrast to the semiconducting few-layer $PtSe_2$.

As shown in Supplementary Fig. 10, for the transferred film with 2.5–3 nm $PtSe_2$ channel thickness, the I_{ON}/I_{OFF} of a typical device ($W_{ch} = 40$ µm and $L_{ch} = 15$ µm) increases with reducing temperature. From Supplementary Fig. 10, it is evident that the temperature dependence of the drain current activation energy is primarily driven by the 200 meV activation energy of the OFF state current, which results in the increase of I_{ON}/I_{OFF} from ~80 (at 30 °C) to $\sim 4.5 \times 10^2$ (at −50 °C). From a technology point of view, room temperature characteristics of FET devices is of most importance; nonetheless, by extrapolating the temperature-dependent data of Supplementary Fig. 10, the I_{ON}/I_{OFF} could increase to $>1.5 \times 10^5$ at 20 K, which would be comparable with the previously reported ratio on an exfoliated $PtSe_2$ flake at cryogenic temperatures.[13]

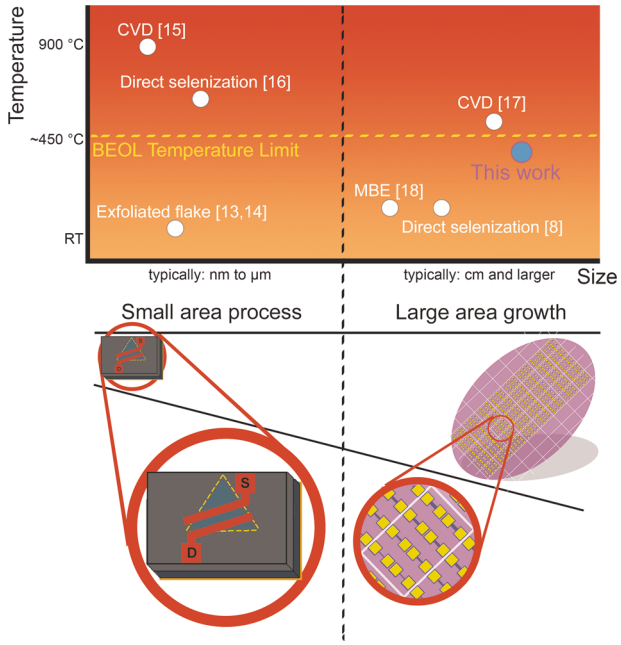


Fig. 5 Process temperature of platinum diselenide ($PtSe_2$) formation versus sample size. BEOL: back-end-of-line; CVD: chemical vapor deposition; MBE: molecular beam epitaxy

DISCUSSION

Considering the potential technology implications of this work, TAC of Pt to $PtSe_2$ is a scalable process that can be achieved at 400 °C. Figure 5 shows the results presented in this work compared to alternative approaches to form $PtSe_2$, which have been reported in the literature. The figure plots the maximum temperature of the process against the area of the $PtSe_2$ samples formed. The plot highlights that the TAC process can form $PtSe_2$ below the BEOL thermal budget limit for silicon CMOS (at around 450 °C), and importantly, this growth is achieved on amorphous SiO_2. This opens up the possibility that these films could be integrated into the BEOL of a silicon CMOS process, to provide semiconducting or semimetallic layers above conventional integrated circuits.[42] For the samples presented in this work, it was necessary to transfer the $PtSe_2$ films, with evidence that Pt was interacting with the SiO_2 near-surface region during $PtSe_2$ formation. This motivates the need to study in detail the potential interaction of the Pt with the SiO_2, as well as exploring insulating diffusion barriers, which could circumvent the need for $PtSe_2$ film transfer. This is an area of ongoing research.

In conclusion, this work presents a theoretical and experimental study of QC effects in layered $PtSe_2$ films as a function of film thickness. $PtSe_2$ films with layer numbers increasing from 1 to 4 were studied by ab initio simulations with fully relaxed structures. VdW interactions and *GW* calibration have shown significant modification in the bandgap energy of the films, predicting QC-induced bandgaps comparable with conventional semiconductors for ML (2.43 eV) and bilayer (1.50 eV) $PtSe_2$ consistent with film thickness less than the calculated Bohr radius. The influence of Pt vacancies on the $PtSe_2$ band structure considering SOC has been investigated, indicating that a Pt vacancy acts as an acceptor, moving the Fermi level towards the $PtSe_2$ valence band edge. Large-area $PtSe_2$ films with different thicknesses were synthesized by a TAC process at 400 °C on Si/SiO_2 substrates. The $PtSe_2$ films exhibit a *p*-type nature with mobility values in the range of

5–13 $cm^2/V{\cdot}s$ as measured by van der Pauw Hall characterization. Back-gated FET devices with different channel dimensions were fabricated using CMOS standard photolithography and etching showing room temperature I_{ON}/I_{OFF} of excess 230 for a 2.5–3 nm $PtSe_2$ film, which drops to about 1.4 for 5–6.5 nm $PtSe_2$ channel, consistent with the ab initio simulations of a semimetal-to-semiconductor transition due to QC effects in thin films.

Our theoretical and experimental results demonstrate the potential for large area growth of polycrystalline $PtSe_2$ thin films for applications in the next generation of nanoelectronic devices. The ability to form layered $PtSe_2$ at 400 °C on an amorphous SiO_2 substrate, with hole mobilities exceeding 10 $cm^2/V{\cdot}s$, opens up potential applications in areas such as flexible electronics and integrating new functions into the BEOL of existing semiconductor technologies.

METHODS

Details of DFT and *GW* calculations

$PtSe_2$ electronic structures are calculated using DFT as implemented in OpenMX[28], QuantumATK[29] and Quantum Espresso.[43] OpenMX and Quantum Espresso calculate the electronic energy within the framework of Kohn–Sham DFT using pseudo-atomic localized basis and plane wave basis functions, respectively. The plane wave calculations are performed with an energy cutoff of 180 Rydberg and $16\times16\times1$ *k*-point Monkhorst–Pack grid. Norm-conserving pseudopotentials and generalized gradient approximation (GGA) for the exchange correlation potential[28,44] are considered. Numerical atomic orbital basis sets of s3p3d2 are used for both Pt and Se atoms in OpenMX. Green's function theory provides quasi-particle energies using the electron self-energy operator containing the effects of exchange and correlations with other quasi-particles. The Yambo program is used in this work to perform the *GW* calibration to quasi-particle energies within first-order perturbation theory starting from the Kohn–Sham eigenstates.[45] The effective Coulomb interaction is set to zero in real space within the vacuum region such that quasi-particles do not interact with their periodic images.[46] As a result, the periodicity of the structure is reduced using a cutoff for the Coulomb interaction in the direction transverse to the $PtSe_2$ film. In the *GW* calculations, the method in ref. [26] has been used enabling improved convergence in the bandgap energies with a reduced set of empty states as well as requiring the *GW* correction to be applied for individual *k*-points of interest. A $16\times1\times1$ *k*-point Monkhorst–Pack grid in the irreducible BZ is used with all *G*-vectors included in the *GW* calculations.

Materials synthesis

$PtSe_2$ thin films were synthesized using a TAC process similar to that previously described for MoS_2 and WS_2,[47] $MoSe_2$ and WSe_2,[48] and $PtSe_2$.[9,11] Pt layers of different thicknesses were sputtered onto Si/SiO_2 substrates using a Gatan precision etching and coating system. The Pt samples were selenized in a quartz tube furnace with two independently controlled heating zones. Pt samples were loaded in the primary heating zone and heated to 400 °C. The Se source Se powder (Sigma-Aldrich, 99.99%) was loaded in the secondary heating zone, which was heated to the melting point of Se (~220 °C). Ar/H2 (9:1), with a flow rate of 150 sccm, was used to transport the vaporized Se to the Pt samples. A rotary vane pump was used to evacuate the system and keep it under vacuum, and the pressure during selenization was typically ~0.7 Torr. A dwell time of 2 h was used to ensure complete selenization.

Hall-effect measurements

The Hall-effect measurements were performed in a van der Pauw configuration[49] with a LakeShore Model 8404 AC/DC Hall-effect measurement system.[50] The system can provide DC or AC magnetic fields over a variable range up to ± 1.7 T (DC) or a fixed range up to ~1.2 T root mean square at a frequency of 0.1 or 0.05 Hz. The measurements in this work were performed at room temperature. The main parameters directly applied, measured, and extracted with the Hall-effect measurement system are the measured Hall voltage, $V_H = IBR_{H\text{-sheet}}$ (where $R_{H\text{-sheet}} = R_H/t$) = $(IBh_f)/(n_s e) = IB\mu_H\rho_s = (IB\mu_H RW)/L$, where I is the applied excitation current, B is the applied DC or AC magnetic field, $R_{H\text{-sheet}}$ is the extracted sheet Hall coefficient (and R_H is the Hall coefficient), n_s is the extracted sheet carrier concentration (where the carrier concentration (n) is given by $n = n_s/t$), h_f is the applied Hall factor (equal to unity for this work), μ_H is the extracted Hall mobility, ρ_s is the measured sheet resistivity by four-point measurement, where $\rho_s = (\pi F_{AB}(R_A + R_B)/(2\ln(2)))$, with the resistivity given by $p = t\rho_s$, and R_A and R_B are the measured four-point orthogonal resistances, and F_{AB} is the solution to the van der Pauw equation and is proportional to the ratio of the perpendicular four-point orthogonal resistances between the equivalent geometrical contacts (*i.e.*, R_A and R_B). F_{AB} is between 0 and 1.0 depending on the accuracy of the solution to the van der Pauw equation (all results reported here are between 0.99 and 1.0).

Transmission electron microscopy

XTEM was prepared using a Dual Beam Focused Ion Beam (FIB) FEI Helios NanoLab 600i. A 50 nm carbon layer, which was followed by a 300 nm platinum layer, were deposited within the Dual Beam FIB by electron beam-induced deposition and 2 µm-thick carbon layer with ion beam-induced deposition. These three layers were grown for protection before the milling process. The lamella was prepared and thinned down to less than 200 nm thickness. The thinning at 30 kV was finished by polishing at 5 kV to reduce the ion beam-induced damage to a <2 nm thin layer on both sides. TEM analysis was performed using a JEOL JEM-2100 at 200 kV in bright field mode.

Back-gated device fabrication and electrical characterization

Back-gate field-effect transistors were fabricated by patterning source and drain metal contacts using standard photolithography followed by e-beam evaporation of Ni (20 nm)/Au (200 nm) and lift-off process. The $PtSe_2$ film was then patterned using a photoresist mask and an SF_6-based inductively coupled plasma etch to form the channel, as shown in the inset of Fig. 4b. Electrical transport properties of the back-gated devices were measured with a semiconductor device parameter analyzer (Agilent B1500a) and using Cascade semi-automated probestation at room and different temperatures.

Film transfer process

The synthesized as-grown $PtSe_2$ thin films were transferred onto unprocessed Si/SiO_2 substrates using a typical polymer-support transfer technique. Polymethyl methacrylate (PMMA, MicroChem) was spin coated onto the as-grown $PtSe_2$. The SiO_2 layer under the $PtSe_2$ was removed by a wet-etching process using 2 M sodium hydroxide at room temperature. After cleaning in de-ionized water, the $PtSe_2$ with PMMA layers were transferred onto the substrates. The PMMA was removed by immersion in acetone at room temperature for 20 min.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

L.A. conducted the theoretical calculations and atomic-scale simulations. N.M., C.O.C. and C.P.C. synthesized $PtSe_2$ films and performed spectroscopic characterization. F.G. conceived and designed the experiments and the mask layout, performed Hall-effect measurements, film transfer and device fabrication, and electrical characterization. S. M., K.F.B., and J.L. helped with device characterization. G.M. performed TEM. R.S., T.S.-L., R.D., E.C. and R.E.N. performed other sample characterizations. F.G. and L.A. wrote the manuscript. P.K.H. and G.S.D. helped with the planning of the experiments and the interpretation of the results, and supervised the project. All authors discussed the results and reviewed the manuscript.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-019-0116-4).

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