Title	Structural and Electrical Properties of HfO2/n-InxGa1-xAs structures (x: 0, 0.15, 0.3 and 0.53)
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Publication date	2009-10
Original Citation	Hurley, P.K., O'Connor, E., Monaghan, S., Long, R., O'Mahony, A., Povey, I.M., Cherkaoui, K., MacHale, J., Quinn, A., Brammertz, G., Heyns, M.M., Newcomb, S., Afanas'ev, V.V., Sonnet, A., Galatage, R., Jivani, N., Vogel, E., Wallace, R.M. and Pemble, M. (2009) 'Structural and Electrical Properties of HfO2/n-In x Ga 1-x As structures (X: 0, 0. 15, 0. 3 and 0. 53)', ECS Transactions, 25(6), pp. 113–127. https://doi.org/10.1149/1.3206612.
Type of publication	Article (peer-reviewed)
Link to publisher's version	https://doi.org/10.1149/1.3206612 - 10.1149/1.3206612
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Download date	2026-09-17 21:53:51
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In this work results are presented of an investigation into the structural and electrical properties of HfO_2 films on GaAs and $In_xGa_{1-x}As$ substrates for x: 0.15, 0.30, and 0.53. The capacitance-voltage responses of the GaAs and $In_xGa_{1-x}As$ (x: 0.15 and 0.30) are dominated by an interface defect response. Analysis of these samples at 77K indicates that the defect density is > $2.5x10^{13}$ cm^{-2}. For the $HfO_2/In_{0.53}Ga_{0.47}As$ system, 77K capacitance-voltage responses indicate surface accumulation is achieved. The results are consistent with a high defect density, with an energy level ≥0.75 eV above the valence band in the $HfO_2/In_xGa_{1-x}As$ system, where the defect energy with respect to the valence band, does not change with the composition of the $In_xGa_{1-x}As$. The $HfO_2/In_{0.53}Ga_{0.47}As$ interface exhibits two defects at 0.3eV ($1.7x10^{13}cm^{-2}eV$) and 0.61eV ($1.5x10^{13}cm^{-2}eV$) above the valance band edge. The defect at 0.61eV is removed by forming gas annealing at 325ºC.

Introduction and Motivation

The last forty years have seen dramatic developments in computing power, information storage and digital communication technologies. The driving force behind these developments has been in large part due to the on-going miniaturisation of metal oxide semiconductor field effect transistors (MOSFETs), which are the fundamental switching elements of integrated circuits. The scaling of MOSFET dimensions from values of around 10 μm in the early 1970's to values of around 65 nm in 2007 was achieved without changing the basic device concept or the silicon and SiO_2 materials which constitute the device.

A material change at the device level was introduced in late 2007, with the incorporation of a HfO_2 based high dielectric constant (high-*k*) material into the gate stack of the 45 nm MOSFETs to reduce gate current leakage (1). This represents the most significant development in MOSFET processing since the first devices were realised in the

early 1960's and was achieved based on approximately ten years of academic and industrial research (2,3). The HfO_2 gate insulator is used in conjunction with separate metal gate electrodes for the *n* and *p* channel MOSFETs and a thin (typically ~ 10 Å) silicon dioxide based (SiO_x) interfacial layer (IL). Scaling of the $HfO_2/SiO_x/Si$ system for future technology nodes requires a reduction in the thickness of the SiO_x IL oxide. However, this results in a reduction in carrier mobility in the MOSFET inversion layer (4,5), which has been attributed to the presence of charge in the high-*k* gate stack (6) and the possible contribution of remote phonon scattering from the high-*k* layer (7- 15). One potential solution is the heterogeneous integration onto a silicon platform of high mobility semiconductors, such as germanium for *p* channel devices and III-V compound semiconductors for the complementary *n* channel devices. Many III-V substrate options have been reported including, GaAs (16- 20), $In_xGa_{1-x}As$ (21- 24), InAs and InSb (25). Indeed, the viability of using such high mobility materials has been given new impetus following the recent demonstration of III-V integration onto a silicon platform (26). In relation to the benefit of high mobility channels over silicon, a number of recent theoretical papers have questioned the advantage at channel lengths below 35 nm (27,28). However, experimental results do demonstrate the benefit of III-V channels over silicon in terms of performance and power consumption for metal gate InGaAs transistors down to ~25 nm channel lengths (29).

One of the principle challenges associated with the formation of insulating gate III-V MOSFETs is the characterisation and passivation of electrically active defects at the interface between the III-V semiconductor and the high dielectric constant (high-*k*) gate oxide. Peak interface state density (D_{it}) values are typically in the range 10^{12} to 10^{13} $cm^{-2}eV^{-1}$, and remain at least one order of magnitude too high for practical device applications (30,31,32, 33, 34). In this paper we will extend on the initial report in (34) by presenting a detailed study of the electrical and structural properties of the $HfO_2/n\text{-}In_xGa_{1-x}As$ system for x: 0, 0.15, 0.30, and 0.53. The primary aim of the work was to study the effect of reducing the energy gap from 1.41eV (GaAs) to 0.75eV ($In_{0.53}Ga_{0.47}As$) on electrically active defects at the $HfO_2/In_xGa_{1-x}As$ interface using capacitance-voltage and conductance-voltage analysis over varying temperature (77K to 348K) and frequency (1kHz to 1 MHz).

Experimental Details

The experimental matrix was comprised of $HfO_2/n\text{-}In_xGa_{1-x}As$ MOS capacitors formed on indium (In) concentrations of 53%, 30%, 15% and 0% (i.e., GaAs substrates). For the case of the 53% In concentration, the $In_{0.53}Ga_{0.47}As$ layers were grown by metal organic vapour phase epitaxy (MOVPE), lattice matched to InP(100) substrates. The 30% and 15% $In_xGa_{1-x}As$ epitaxial layers were grown on GaAs(100) substrates. The details of the $In_xGa_{1-x}As$ epitaxial layer thickness and doping concentration, and the thickness and doping of the buffer layers are provided in Table I.

TABLE I. Details of the Substrates and Epitaxial Layers used in this Study			
In %	**Substrate Details**	**Buffer Layer Details**	**$In_xGa_{1-x}As$ Epitaxial layer**
53	InP (100) S doped (1-3)x10^{18}	0.3μm InP S doped 2x10^{18} MOVPE	2μm, $In_{0.53}Ga_{0.47}As$ S doped 4x10^{17} MOVPE
30	GaAs (100) Si: 5x10^{17}	0.35μm GaAs Si: 1x10^{17}/cm^3 MBE	50 nm $In_{0.30}Ga_{0.70}As$ Si: 1x10^{17}/cm^3 MBE
15	GaAs (100) Si: 5x10^{17}	1μm GaAs Si: 1x10^{17}/cm^3 MBE	30 nm $In_{0.15}Ga_{0.85}As$ Si: 1x10^{17}/cm^3 MOVPE
0	GaAs (100) Si: 5x10^{17}	------	-------

All HfO_2 layers were deposited in a separate ALD reactor at a temperature of 250^{o}C by alternating pulses of H_2O and the Hf precursor TDMA-Hf ($Hf[N(CH_3)_2]_4$), the first pulse being that of the Hf precursor. The nominal thickness of the HfO_2 layer was 9 nm. The samples were exposed to air prior to dielectric deposition. MOS structures were completed by vacuum evaporation of ~ 100 nm of Pd or Pt using a deposition rate of 2.5 Å/s, by either a lift-off process or through a shadow mask, to define MOS capacitors of various areas. Back ohmic contacts were formed by vacuum evaporation of a multi-layer stack comprised of Ni, Ge and Au layers, followed by a 350^{o}C, 30s second anneal in N_2.

The HfO_2 layer was deposited either directly on the native oxides of the $In_xGa_{1-x}As$ or GaAs surface, or following an ex-situ three-stage surface pretreatment. The ex-situ three-stage surface pretreatment was performed sequentially as follows: 3.7% HCl, 3 minutes at 25^{o}C; 3% NH_4OH, 3 minutes at 25^{o}C; 1% $(NH_4)_2S$, 5 minutes at 75^{o}C; rinse in deionized water; blow dry wafers with N_2. Forming gas annealing (5%H_2/95%N_2) was performed cumulatively after gate metallization, at 250^{o}C and 325^{o}C for 30 minutes. The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were recorded using an Agilent 4284Aor 4294A LCR and an Agilent B1500 meter following open calibration. The measurements at room temperature were performed on wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air environment (dew point $\leq$-65^{o}C). Measurements at liquid nitrogen temperatures were performed on-wafer in a cryogenic probe station.

Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam (FIB) thinning procedures (35) in an FEI 200 Workstation and examined at 200kV in a JEOL2000FX.

Experimental Results and Discussion

Structural Analysis

Following HfO_2 deposition and Pd metal gate formation, the samples were examined using TEM to determine the thickness of the HfO_2 layer and to investigate if any IL oxides exist between the III-V substrate and the HfO_2 layer film. Selected TEM micrographs are

presented in Figures 1 (a) to 1 (d) to illustrate some of the main microstructural observations seen in the Pd/HfO_2/$In_xGa_{1-x}As$/InP(GaAs) samples.

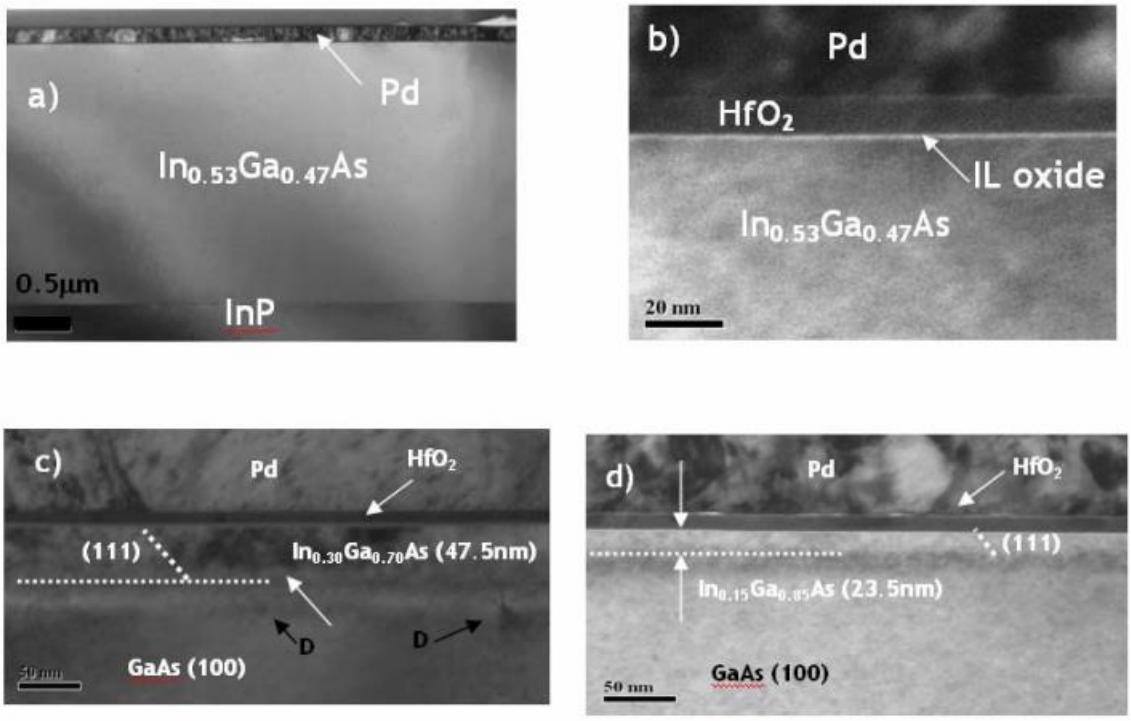

Figure 1. High resolution cross section transmission electron micrographs of (a) Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP structure, illustrating the InP(100) substrate, the $In_{0.53}Ga_{0.47}As$ layer (2.095μm) and the Pd gate layer (~120nm). The HfO_2 thin film is not visible at the magnification level in this TEM cross section. No defects are detected in the $In_{0.53}Ga_{0.47}As$ epitaxial layer for a range of cross sectional images, (b) higher magnification image of the Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP structure, illustrating the HfO_2 layer (9.5nm) and the presence of a (1.0nm) IL oxide between the HfO_2 layer and the $In_{0.53}Ga_{0.47}As$ substrate, (c) Pd/HfO_2/$In_{0.30}Ga_{0.70}As$/GaAs structure, indicating a 47.5nm $In_{0.30}Ga_{0.70}As$ layer containing (111) stacking faults (white dotted line), and dislocations (D). Note: defects appear to extend into the GaAs(100) substrate. The HfO_2 layer is 9.3nm with a 0.9nm IL oxide, (d) Pd/HfO_2/$In_{0.15}Ga_{0.85}As$/GaAs structure, indicating a 23.5nm $In_{0.15}Ga_{0.85}As$ layer containing (111) stacking faults (white dotted line). The HfO_2 layer is 14.0 nm with a 1.1 nm IL oxide. The samples shown in Figure 1 did not experience the back contact metal formation and 350ºC, 30s second anneal in N_2. Note the evidence of delamination in this sample between the Pd metal and the HfO_2 layer, which could result from the TEM cross section process.

The TEM images shown are for ALD deposition on the $In_xGa_{1-x}As$ native oxides, (i.e., no three stage pre-treatment prior to the ALD HfO_2). From bright and dark field TEM images there is no evidence of defects in the $In_{0.53}Ga_{0.47}As$ (2.095μm) epitaxial layer on the InP (100) substrate, see Figure 1 (a), as expected for the lattice matched 53% In concentration InGaAs layer. The Pd/HfO_2/GaAs structure also indicated no defects in the GaAs substrate (not shown). All samples indicate the presence of an interlayer (IL) oxide between the ALD HfO_2 film and the $In_xGa_{1-x}As$ substrate. The thickness of the IL oxide ranges from 0.9 to 1.3nm, with the values summarized in Table II. The IL oxide was also present for samples which experienced the three stage surface pre-treatment prior to the ALD, and is not reduced in thickness by the three stage surface pre-treatment. The IL oxide

is fully amorphous[1], however the HfO_2 layer is a mixed amorphous/crystalline film, exhibiting crystallites which extend through the film from the IL oxide to the Pd metal gate. The presence of partial crystallization of the HfO_2 film is of particular interest, as the samples examined experienced no annealing following the ALD deposition, indicating that the partial crystallization of the HfO_2 film on $In_xGa_{1-x}As$ substrates occurs during the ALD growth at 250°C.

The 47.5nm $In_{0.30}Ga_{0.70}As$ and 23.5nm $In_{0.15}Ga_{0.85}As$ layers grown on GaAs (100), both exhibit a high density of defects in the InGaAs layer. See Figure 1 (c) and 1 (d) respectively. This is expected as the layer thickness is beyond the critical thickness which is typically reported for growth of InGaAs growth on GaAs (see Table II). The defects are comprised of (111) stacking faults and dislocations. Close inspection of the TEM images reveals that the (111) stacking faults in the $In_xGa_{1-x}As$ (x: 0.3, 0.15) layer extend to the $HfO_2/In_xGa_{1-x}As$ interface.

TABLE II. Summary of TEM Micro-Structural Observations

In %	HfO_2 Thickness (nm)	Interlayer Oxide Thickness (nm)	Comment	$In_xGa_{1-x}As$ Epitaxial layer thickness/critical thickness on GaAs (nm)
53	9.5	1.0	No defects detected in $In_{0.53}Ga_{0.47}As$ epitaxial layer	----
30	9.2	0.9	(111) stacking faults and dislocations in the $In_{0.30}Ga_{0.70}As$ layer. Defects extending to the GaAs substrate	47.5nm/~12nm
15	14.0	1.1	(111) stacking faults and dislocations in the $In_{0.30}Ga_{0.70}As$ layer. Defects extending to the GaAs substrate	23.5nm/~20nm
0	11.4	1.3	No defects detected in GaAs substrate	----

Electrical Analysis: Capacitance-Voltage and Conductance

$HfO_2/In_xGa_{1-x}As$ system. The C-V responses at room temperature (295K) with ac signal frequencies from 1 kHz to 1 MHz for the 53% In, 30%In, 15%In and GaAs MOS structures are shown in Figures 2 (a), 2 (b), 2 (c) and 2 (d) respectively. The C-V responses are for the $In_xGa_{1-x}As$ or GaAs surface with no surface pretreatment. The same general trends in the frequency dependence of the C-V responses were obtained for the MOS structures using the ex-situ three-stage surface pre-treatment before the ALD HfO_2 deposition.

[1] The IL oxide is found to be primarily comprised of gallium oxide from electron energy loss spectroscopy on HfO2/ $In_{0.53}Ga_{0.47}As$/InP formed using the same Hf precursor.

The GaAs, $In_{0.15}Ga_{0.85}As$ and $In_{0.30}Ga_{0.70}As$ MOS samples exhibit a large dispersion of capacitance with the ac measurement signal frequency in the gate voltage region 0 to +4 volts. This effect has been widely reported for GaAs MOS samples [see for example (30, 32, 33)], with reports also for $In_xGa_{1-x}As$ sample for x < 0.53 (31). For the case of the $In_{0.53}Ga_{0.47}As$ sample, the dispersion in the capacitance for positive bias is considerably reduced compared to the lower (x<0.53) indium content samples. The average dispersion of the measured capacitance per decade of frequency from 1 kHz to 1 MHz is shown in Figure 3. It is noted that the Pd/HfO_2/*n*-$In_xGa_{1-x}As$ MOS structures were measured before and after the back metal contact formation. The CV response with varying frequency was not modified by the back metal contact formation, ruling out the contribution of series resistance to the observed frequency dependence of the capacitance at positive gate voltage.

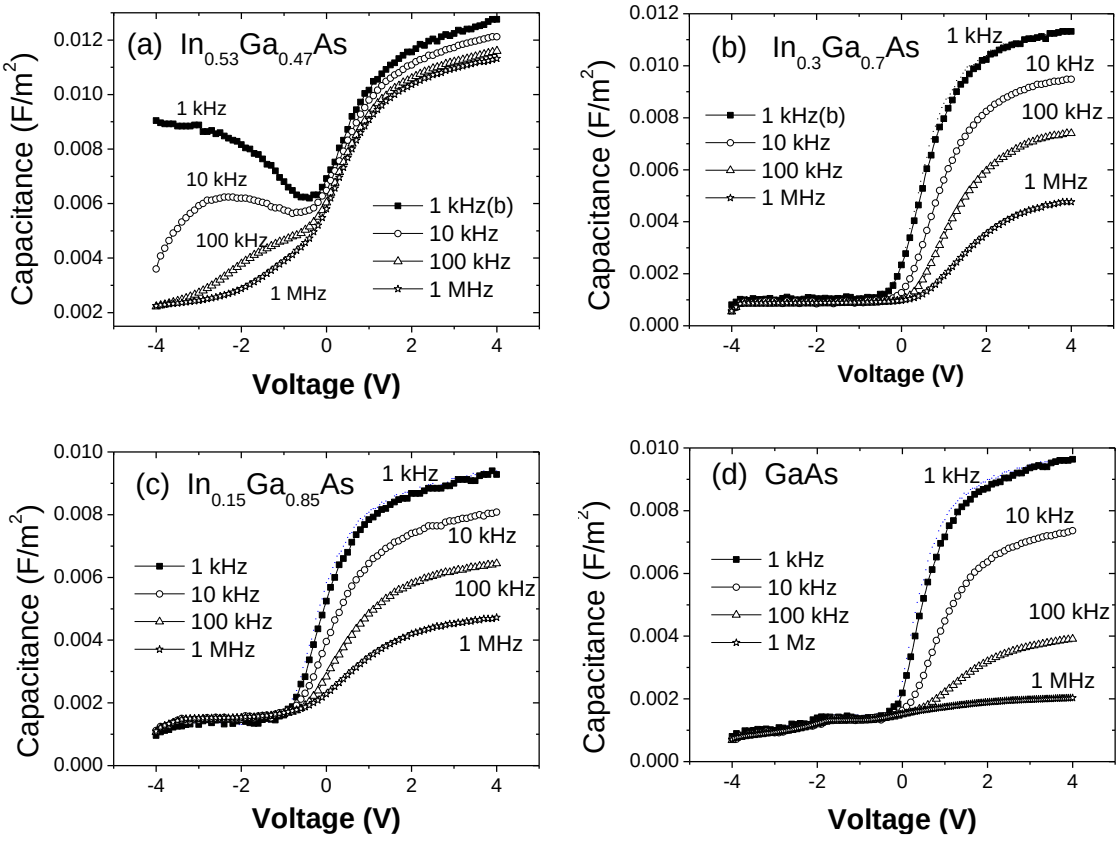

Figure 2. Multi-frequency (1 kHz to 1 MHz) C-V responses measured at room temperature (298K) on a Cascade probe station for: a) Pd/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$/InP, b) Pd/HfO_2/*n*-$In_{0.30}Ga_{0.70}As$/GaAs, c) Pd/HfO_2/*n*-$In_{0.15}Ga_{0.85}As$/GaAs and d) Pd/HfO_2/*n*-GaAs MOS.

The increase of the capacitance towards the nominal oxide capacitance at low measurement frequencies (1 kHz) in Figures 2 (b), (c) and (d), does not necessarily imply the accumulation of free carriers (electrons) at the HfO_2/*n*-$In_xGa_{1-x}As$ interface. To provide a specific example we consider a mono-energetic defect level with a density D_{it} =1x10^{13} cm^{-2} located at an arbitrary position (E) in the $In_xGa_{1-x}As$ energy gap. The charge, Q_{it} [C/cm^2], in the defect level is simply given by, $q.D_{it}.f_d(E)$, where q is the electronic charge and $f_d(E)$ is the Fermi Dirac distribution of the defect level occupancy. The capacitance associated with the defect (C_{it}), is by definition, the rate of change of the surface charge

with respect to the surface potential. Assuming a full quasi-static C-V response of the defect level, this yields a peak interface trap capacitance, C_{it} ~ 0.15 F/m^2 (see Figure 4). This capacitance is larger than the gate oxide capacitance, which for 9nm of HfO_2 (k=18) is 0.018 F/m^2. This value of accumulation capacitance will be further reduced from the nominal value of 0.018 F/m^2 due to the presence of the interlayer (IL) oxide and the finite differential capacitance of the $In_xGa_{1-x}As$ layer. In this case, it is clear that for a mono-energetic defect level, with a density D_{it} =1x10^{13} cm^{-2}, the interface trap capacitance will exceed the substrate capacitance (C_s) and the oxide capacitance (C_{ox}). As C_{it} appears in series with C_{ox}, the measured capacitance will acquire a value of the maximum expected accumulation capacitance due to the high C_{it} contribution, without the presence of free carriers at the $HfO_2/In_xGa_{1-x}As$ interface.

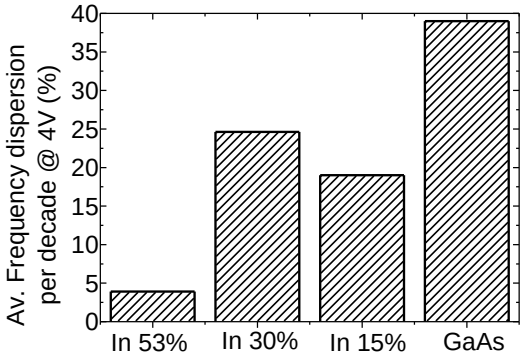

Figure 3. The average frequency dispersion per decade of frequency at a gate voltage of + 4 volts for the varying indium % $HfO_2/In_xGa_{1-x}As$ MOS structures.

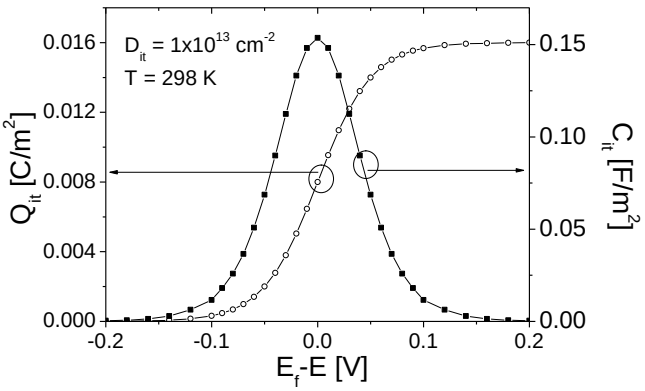

Figure 4. Interface trap charge and quasi-static capacitance associated with a mono-energetic trap level with a density of 1x10^{13} cm^{-2} at 298K.

The calculation in Figure 4 assumes a full quasi-static response of the interface defect level. In practical measurements, the interface defect will exhibit a dependence on the ac signal frequency of the C-V measurement originating from the emission rate, e_n, of the electrons in the defect level to the conduction band edge (36, 37), where e_n is proportional to the exponential of the energy difference between the interface defect (E_t) and the conduction band edge (E_c) (38).

The exponential dependence of the emission rate on the sample temperature provides an experimental approach to further examine if the C-V response exhibited by the $HfO_2/In_xGa_{1-x}As$ MOS structures in Figures 2 (a) to 2 (d) originates from an interface trap capacitance or is a consequence of accumulation of electrons at the HfO_2/n-$In_xGa_{1-x}As$ interface. By cooling the samples to 77K using liquid nitrogen, the emission rate reduces exponentially, freezing out the interface state capacitance (C_{it}) response. In this case the filling of the interface defects will follow the slowly varying DC gate bias, but will not contribute an interface trap capacitance to the total measured capacitance. In the case of a mono-energetic defect level, the capacitance acquires a constant and frequency independent value as the defect level is occupied, and once the defect state is fully occupied, the capacitance increases toward surface accumulation without an ac signal frequency dependence (39).

The experimental results comparing the 295K and the 77K multi-frequency C-V responses for the 53% In, 30%In, 15%In and GaAs MOS structures are shown in Figures 5 (a), 5 (b), 5 (c) and 5 (d) respectively.

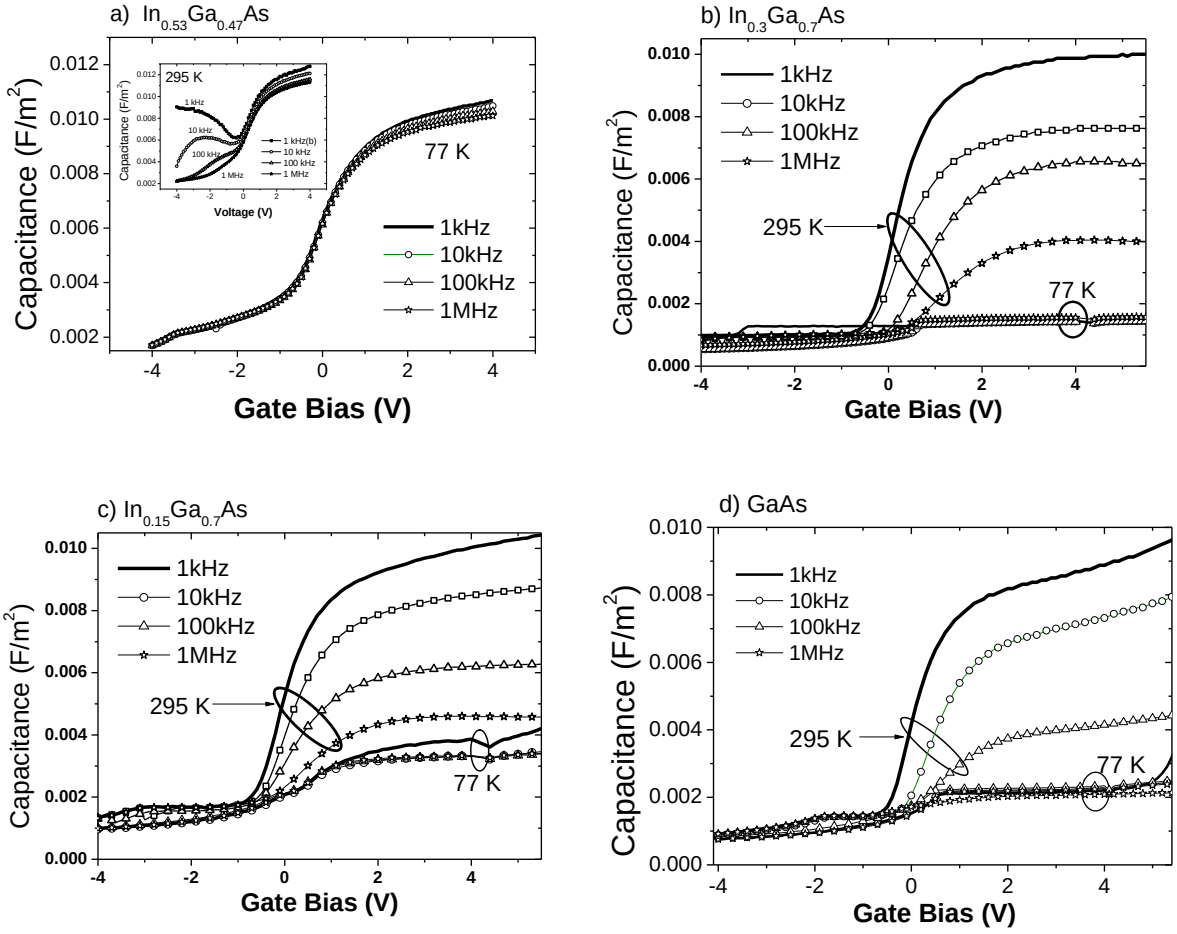

Figure 5. Multi-frequency (1 kHz to 1 MHz) C-V responses measured at room temperature (295K) and liquid nitrogen (77K) for: a) Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP: inset is the 295K data, b) Pd/HfO_2/$In_{0.30}Ga_{0.70}As$/GaAs, c) Pd/HfO_2/$In_{0.15}Ga_{0.85}As$/GaAs and d) Pd/HfO_2/GaAs MOS.

In the case of the Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP structure (Figure 5 (a)), the capacitance at 77K and +4 volts is not changed from the value recorded at 295K. This is strong evidence that in the case of the Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP, surface accumulation of electrons can be achieved. This is consistent with recent reports, indicating that high drive current (30 – 170 mA/mm) and effective mobility (>1000 cm^2/Vs) can be achieved with $In_{0.53}Ga_{0.47}As$ MOSFETs (21, 40). In addition, the expected minimum capacitance for the $4x10^{17}cm^{-3}$ *n* type doping in the $In_{0.53}Ga_{0.47}As$ layer, and an oxide capacitance of 0.011 F/m^2, is ~ 0.002 F/m^2, which is the close to the value measured at 295K and 77K, indicating the Fermi level at the HfO_2/$In_{0.53}Ga_{0.47}As$ interface can be modulated by the gate voltage. The CV response at 295K for gate voltages < -1 volts, however, is not indicative of inversion at the HfO_2/$In_{0.53}Ga_{0.47}As$ interface (see inset of Figure 5 (a)). The measured capacitance moves through a peak value and subsequently decreases (see for example the 10 kHz CV response), which is indicative of an interface defect response (34). For the case of a

minority carrier inversion response, the capacitance acquires a constant value in inversion, where the magnitude of the inversion capacitance increases with decreasing ac signal frequency (41). This region of the C-V response is considered later in the paper.

In the case of the 30%In, 15%In and GaAs MOS structures, Figures 5 (b), (c) and (d), the capacitance response at positive gate voltage changes significantly at 77K. Essentially, the capacitance becomes independent of the measurement frequency and exhibits an approximately constant value over a wide gate voltage range. This is consistent with the filling of an interface defect and confirms that the frequency dependent increase of capacitance at 295K is due to an interface trap capacitance response.[2] The constant capacitance at 77K implies that the Fermi Level at the $HfO_2/In_xGa_{1-x}As$ (x: 0, 0.15, 0.30) interface is pinned at a fixed energy, and all additional gate charge is compensated by charging on the $HfO_2/In_xGa_{1-x}As$ interface defects, preventing the formation of an electron surface accumulation layer.

Modeling of the frequency dispersion in the C-V and G-V data at 295K for the 30%In, 15%In and GaAs MOS structures has not been attempted in this work, and previous studies have indicated that the type of frequency dispersion present in Figures 5 (b) - (d), cannot be adequately modelled (33, 42) using the conventional interface defect model (43). It is possible, however, to provide a lower limit to the interface defect concentration for the 30%In, 15%In and GaAs MOS samples from the voltage range of the constant capacitance at 77K. The charge in the defect level at 77K, ΔQ_{it}, is simply given by $\Delta Q_{it} = \Delta V_g \, . \, C_{ox}$, where ΔV_g is the extent of the constant capacitance at 77K and C_{ox} is the capacitance of the HfO_2 and IL oxide [F/m^2]. This yields *minimum* interface state densities of $2.5x10^{13}$ cm^{-2}, acceptor like defects, at the $HfO_2/In_xGa_{1-x}As$ interface (x: 0, 0.15, 0.30). This is a minimum value of the interface state density, as over the bias range examined at 77K, surface accumulation was not achieved. This density of interface defects would prevent inversion mode MOSFET behavior, and the C-V observations are consistent with a recent publication where drain currents for $Al_2O_3/In_{0.2}Ga_{0.8}As$ MOSFETs were three orders of magnitude lower than $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSFETs, fabricated using the same process (21).

Measurements of the $HfO_2/In_xGa_{1-x}As$ samples using internal photoemission (IPE) indicate that, within experimental limitations, the decrease in the energy gap moving from GaAs (1.42eV) to $In_{0.53}Ga_{0.47}As$ (0.75eV) occurs due to an increase in the electron affinity (44). These results taken together with the C-V analysis indicate a high density ($>2.5x10^{13}$ cm^{-2}) of acceptor like states at the $HfO_2/In_xGa_{1-x}As$ interface, with an energy level $\geq$0.75 eV above the valence band in the $HfO_2/In_xGa_{1-x}As$ system, where the defect energy with respect to the valence band, to a first approximation, does not change with the composition of the $In_xGa_{1-x}As$. As a consequence, the defect enters the $In_{0.53}Ga_{0.47}As$ conduction band in the case of the $HfO_2/In_{0.53}Ga_{0.47}As$ structure.

This does not imply that the defect is electrically insignificant. While the defect energy with respect to the $In_{0.53}Ga_{0.47}As$ valence band does allow inversion mode $In_{0.53}Ga_{0.47}As$ MOSFETs operation, the defect density ($>2.5x10^{13}cm^{-2}$), now in the conduction band, is comparable to the inversion charge density. When the Fermi level reaches the defect energy

[2] For the 77K measurements, at gate voltages 7 to 9 volts, the capacitance exhibits a sharp increase with gate voltage (not shown). The capacitance is still dependent on the measurement frequency, so is not representative of surface accumulation. Further work is required to establish if this effect is related to interface defects or the onset of oxide conduction on the capacitance.

level it will be pinned, and any additional gate charge will be compensated by charging of the interface defect level over the voltage range where the defect is occupied (> 4 volts from the results in Figures 5 (b) - (d)). The consequence will be a rapid decrease in transconductance with gate voltage, and an apparent decrease in the inversion layer mobility. These effects are observed experimentally in $In_{0.53}Ga_{0.47}As$ MOSFETS (40, 45, 46).

By using a gallium sub oxide (Ga_2O) interfacial layer resulting from electron beam evaporation from a Ga_2O_3 source (47,48), and through the use of silicon inter-layers (49), surface accumulation in GaAs MOS structures has been achieved, indicating that these approaches either remove or significantly reduce the defect located ≥ 0.75eV above the GaAs valance band. However, to date, the results achieved using electron beam evaporation of Ga_2O_3 or silicon inter-layers have not been achieved using ALD to form a high-*k* layer directly on $In_xGa_{1-x}As$ surfaces.

It is noted that from the results in Figure 3, that the average frequency dispersion per decade for the 30% Indium structure does not follow the expected trend with increasing indium concentration. A possible explanation is that the (111) stacking faults observed in the TEM images (see Figure 1 (c)), which reach the $HfO_2/In_{0.30}Ga_{0.70}As$ interface, are a source of additional interface defects and associated frequency dispersion. Structural defects in the $In_xGa_{1-x}As$ epitaxial layer which reach the $HfO_2/In_xGa_{1-x}As$ surface being the *sole source* of the interface states can be discarded, as the HfO_2/GaAs structure, with no TEM evidence of substrate defects, exhibits the largest frequency dispersion.

<u>$HfO_2/In_{0.53}Ga_{0.47}As$ system</u>. The experimental results at 77K and 295K indicate accumulation can be achieved at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. However, interface defects still remain in the energy gap at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface, as is evident from the frequency dependence of the 295K C-V response at negative gate bias (see Figure 2 (a)). To quantify the interface defect concentration, the $Pd/HfO_2/In_{0.53}Ga_{0.47}As$/InP devices were analysed using the conductance method (43). The analysis method inherently assumes the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in depletion where only majority carriers interact with the interface traps, and an accurate estimate of D_{it} can be extracted. If the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in weak inversion, the analysis will significantly overestimate the D_{it} value (50). Series resistance corrections were estimated for all devices and found to be negligible.

Figures 6 (a) and (b) show room temperature C-V responses (1 kHz to 1 MHz) for the unpassivated $Pd/HfO_2/In_{0.53}Ga_{0.47}As$/InP structure and following post 325ºC forming gas anneal, respectively. The FGA results in a noticeable reduction in the frequency dispersion both in accumulation (+4 V) and also in the transition region from depletion to accumulation at gate voltages from ~ 0V to 1V. The CV dispersion for gate voltages in the range -1V to -4V, which is characteristic of interface defects, is also visibly reduced following 325ºC FGA. Figures 6(c) and (d) show the corresponding G_p/ω versus ω characteristics at selected gate voltages for an unpassivated $Pd/HfO_2/In_{0.53}Ga_{0.47}As$/InP structure, and following the FGA, respectively. G_p is the equivalent parallel conductance calculated from the measured capacitance and conductance following the approach of E. H. Nicollian and A. Goetzberger (43). The measurement temperature is 75ºC for all devices, as no G_p/ω peaks were observed at -50ºC and 25ºC.

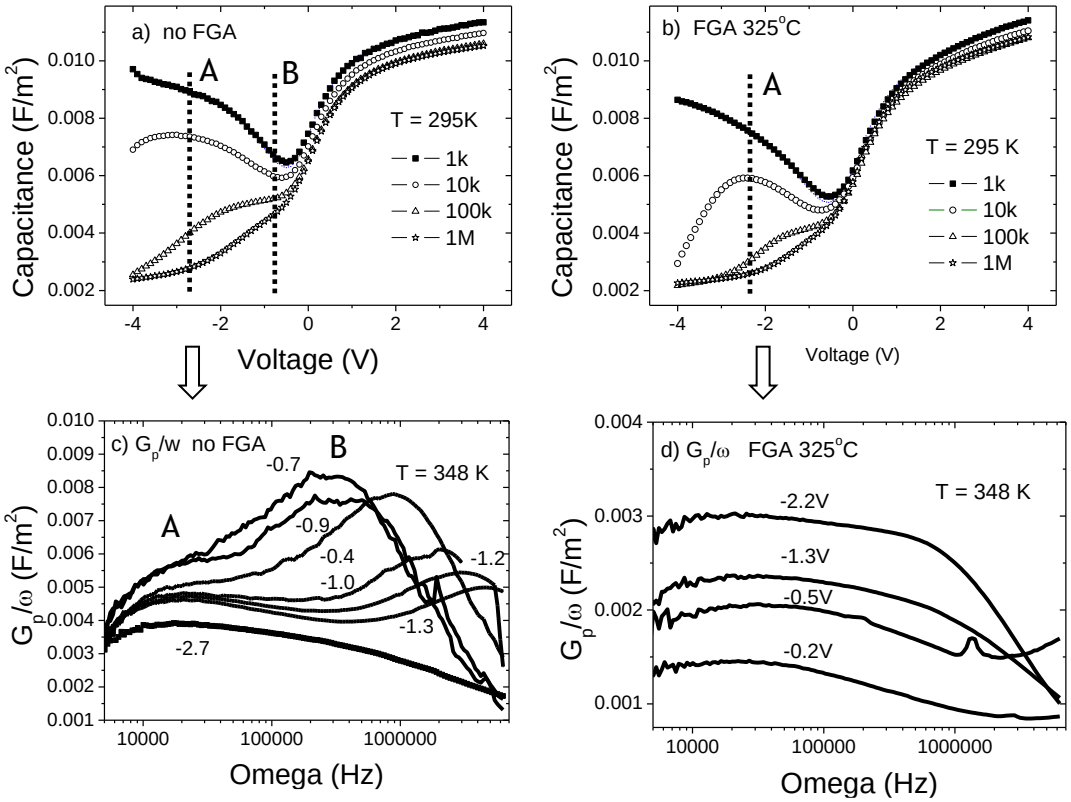

Figure 6. Room temperature C-V frequency variation (1 kHz to 1 MHz) (a) unpassivated, and (b) post 325ºC forming gas anneal, Pd/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$/InP devices. The corresponding Gp/ω versus ω characteristics are shown for the (c) unpassivated and (d) post 325ºC forming gas anneal, Pd/HfO_2/$In_{0.53}Ga_{0.47}As$/InP structure.

The plot in Figure 6 (c) shows two maximum peak profiles at low (~20,000 Hz) and high (~200,000 Hz) angular frequencies, and at different gate voltages within depletion, which may possibly be characteristic of two defects with distinct energy levels, which are termed (A) and (B), respectively. Similar methods have been used to analyse multiple defects in Si/SiO_2 systems (51). Based on fitting of the G_p/ω versus ω plots a peak D_{it} of 1.7 x 10^{13} cm^{-2} eV^{-1} is calculated for defect (A) and 1.5 x 10^{13} cm^{-2} eV^{-1} for defect (B). Figure 6 (d) shows the G_p/ω versus ω plots for the $HfO_2/In_{0.53}Ga_{0.47}As$ device following FGA at 325ºC, which exhibits a broad profile similar to that reported by Mui et al., for $Si_3N_4/In_{0.53}Ga_{0.47}As$ interfaces (32). No peak for defect (B) is evident while for defect (A) the D_{it} is estimated to be 1.0 x 10^{13} cm^{-2} eV^{-1}, which represents a reduction of ~40% in the density of defect (A). This is also a slight reduction of the defect (A) D_{it} after the three stage surface pre-treatment (1.6 x 10^{13} cm^{-2} eV^{-1}) (not shown). Moreover, the FGA or the three stage surface pre-treatment removes the contribution of defect (B) to below detectable limits. This removal of defect (B) following forming gas annealing is consistent with the defect being related to a dangling bond orbital of Ga, As or In.

The form of the C-V response observed in Figure 6 (b), has been reported for different $In_{0.53}Ga_{0.47}As$ surface preparations (24, 30), different high-*k* oxide layers (52), different

high-*k* deposition methods (53) and for samples with and without IL oxides, indicating that the defect (A) originates from the $In_{0.53}Ga_{0.47}As$ surface, as opposed to the IL or high-*k* oxide, with vacancies or surface dimers as the possible origin of the interface states.

The energy levels of defects (A) and (B) can be estimated from the 77K C-V response in Figure 5 (a). At this temperature, we assume that the interface defect contribution to the measured capacitance can be neglected, and the surface potential is estimated directly from the capacitance, which is determined by the depletion region edge. Using a static dielectric constant of 13.9 for the $In_{0.53}Ga_{0.47}As$, the defects (A) and (B) are located at 0.30 eV and 0.61 eV above the highest energy in the $In_{0.53}Ga_{0.47}As$ valence band, E_v.

The interface state analysis for the $HfO_2/In_{0.53}Ga_{0.47}As$ are summarized in Table III.

TABLE III. Summary of Defects at the $HfO_2/In_{0.53}Ga_{0.47}As$ Interface

Defect	Energy level with respect to E_v [eV]	*Peak* Density from Conductance Analysis [$cm^{-2}eV^{-1}$] [1]			Comments
		as deposited	*Three stage surface pre-treatment*	*Forming gas annealing (350°C)*	
A	0.3	$1.7x10^{13}$	$1.6x10^{13}$	$1.0x10^{13}$	Donor Type [2] Only slightly reduced by forming gas annealing and a three stage surface pretreatment
B	0.61	$1.5x10^{13}$	---- [3]	---- [3]	Removed by forming gas annealing at 325°C and a three stage surface pretreatment

[1] The conductance analysis yields the peak interface state density in units of [$cm^{-2}eV^{-1}$]. As the energy gap for $In_{0.53}Ga_{0.47}As$ is 0.75eV, the integrated density in units of [cm^{-2}] is < $1.2x10^{13}$ cm^{-2}.
[2] The donor like nature of this defect is evident from the change in flat band voltage with equivalent oxide thickness (not shown).
[3] Reduced to below detectable limits using conductance analysis.

Conclusions

In conclusion, in this paper we have presented results on the structural and electrical properties of the $HfO_2/n\text{-}In_xGa_{1-x}As$ system for x: 0, 0.15, 0.3, and 0.53. The HfO_2 layer was deposited by ALD using ($Hf[N(CH_3)_2]_4$) and H_2O. The analysis of the microstructural properties of the $HfO_2/n\text{-}In_xGa_{1-x}As$ samples using TEM indicates the presence of an interlayer (IL) oxide between the HfO_2 and the $In_xGa_{1-x}As$ substrates for all samples with an IL thickness between 0.9 and 1.3nm. The IL oxide is present in samples deposited on the native oxide and following a three stage chemical pre-treatment, indicating that removal of the native InGaAs oxides is either limited, or not present, for the ALD process using ($Hf[N(CH_3)_2]_4$) and H_2O.

The capacitance-voltage responses at 295 K for the GaAs and $In_xGa_{1-x}As$ (x: 0. 0.15 and 0.30) structures are dominated by an interface defect response. C-V measurements at 77K, indicate an acceptor like interface defect with a density > $2.5x10^{13}$ cm^{-2}. For the $HfO_2/In_{0.53}Ga_{0.47}As$ system, 77K C-V responses indicate that surface accumulation is achieved. The C-V results are consistent with a high defect density, with an energy level ≥0.75 eV above the valence band in the $HfO_2/In_xGa_{1-x}As$ system, where the defect energy

with respect to the valence band, to a first approximation, does not change with the composition of the $In_xGa_{1-x}As$.

Based on conductance analysis, two defects are detected at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. Defects (A) and (B) are located at 0.30 eV and 0.61 eV above the $In_{0.53}Ga_{0.47}As$ valence band, with D_{it} peak values of 1.7×10^{13} cm^{-2} eV^{-1} calculated for defect (A) and 1.5×10^{13} cm^{-2} eV^{-1} for defect (B). Defect B is reduced to below detectable limits using forming gas annealing at 325°C, or by a three stage surface pre-treatment (34). The removal of defect (B) to below detectable levels following forming gas annealing is consistent with the defect being related to a dangling bond orbital of Ga, As or In. Defect (A) is largely unaffected by surface pre-treatment, consistent with the defect originating from vacancies or dimers at the $In_{0.53}Ga_{0.47}As$ surface.

Acknowledgments

The authors at Tyndall National Institute acknowledge Science Foundation Ireland (Grants 05/IN/1751 and 07/SRC/I1172) and the INTEL/IRCSET studentships scheme for financial support of this work.

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