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Micro-transfer print integration of high-speed photodetectors to SOI platform

Hemalatha Muthuganesan



Thesis submitted in partial fulfilment of the requirements
of the degree of Doctor of Philosophy

at the
Department of Physics,
University College Cork,
National University of Ireland

Supervisor: Brian Corbett
Co-supervisor: Prof. Frank Peters
Head of Department: Prof. Paul Callanan

February 2024

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List of Acronyms

a-Si ..... Amorphous Silicon

AlInAs ..... Aluminium indium arsenide

APS ..... Advanced Plasma Sources

AFM ..... Atomic Force Microscopy

BOE ..... Buffered Oxide Etch

BCB ..... Benzocyclobutene

CMP ..... Chemical Mechanical Planarization

CV ..... Capacitance-Voltage

ER ..... Etch rate

FDTD ..... Finite-Difference Time-Domain

GC ..... Grating Coupler

GDS ..... Graphic Design System

HEMT ..... High Electron Mobility Transistor

InGaAs ..... Indium gallium arsenide

InP ..... Indium phosphide

IR ..... Infra-Red

ICP ..... Inductive Coupled Plasma

I-V ..... Current-Voltage

LER ..... Lateral etch rate

LIDAR ..... Light Detection and Ranging

LOR ..... Lift-Off Resist

MTP ..... Micro-Transfer Printing

MOCVD ..... Metal Organic Chemical Vapour Deposition

NTT ..... Nippon Telegraph and Telephone

nid ..... not-intentionally doped

NRZ ..... Non-Return-to-Zero

OOK ..... On-Off Keying

PD ..... Photodetector

PICs ..... Photonic integrated circuits

PMGI ..... Polydimethylglutarimide

PDMS ..... polydimethylsiloxane

PECVD ..... Plasma-Enhanced Chemical Vapor Deposition

PR ..... Photoresist

PAM .....Pulse-Amplitude Modulation

RC ..... Resistance-Capacitance

SiN ..... Silicon Nitride

SIMS ..... Secondary Ion Mass Spectroscopy

SEM ..... Scanning Electron Microscopy

SOI ..... Silicon On Insulator

SiO_2 ..... Silicon dioxide

TE ..... Transverse-Electric

TLS ..... Tunable Laser Source

UV ..... Ultra-Violet

UTC ..... Uni-Travelling Carrier

VER ..... Vertical etch rate

WLI ..... White Light Interferometry

XRD ..... X-Ray diffraction

XPS ..... X-Ray Photoelectron Spectroscopy

List of Publications

First author publications

1. **Hemalatha Muthuganesan**, Enrica Mura, Shivangi Chugh, Cleitus Antony, Emanuele Pelucchi, Paul Townsend, Xingzhao yan, Mehdi Banakar, Ying Trran, Callum Littlejohns and Brian Corbett, *"100 Gbps PAM4 ultra-thin photodetectors integrated on SOI platform by micro transfer printing"*, in Optics Express, pp.36273-36280, October 2023.

2. **Hemalatha Muthuganesan**, James O'Callaghan, Fatih Bilge Atar, Agnieszka Gocalinska, Kevin Thomas, Emanuele Pelucchi and Brian Corbett,*"Dual sacrificial layer stratergy for highly efficient transfer printing of InP devices"*, in process.

Other publications

1. **Yang Liu**, Zhi Li, Fatih Bilge Atar, Hemalatha Muthuganesan, Brian Corbett, Lai Wang, *"Integration of high-performance InGaAs/GaN photodetectors by direct bonding via micro-transfer printing"*, in ACS Applied Materials and Interfaces, pp.10996–11002, February 2024.

Conference posters

1. **Hemalatha Muthuganesan**, Ali Uzun, Samir Ghosh, James O Callaghan, Fatih Bilge Atar and Brian Corbett, "Effective release and transfer print of telecom wavelength devices", IEEE International 3D Systems Integration Conference, May 2023.

2. **Hemalatha Muthuganesan**, Enrica Mura, Emanuele Pelucchi, Callum Littlejohns, Xingzhao Yan, Mehdi Banakar, Ying Tran and Brian Corbett, "Micro-transfer printed InGaAs photodetector on SOI platform", IEEE Silicon Photonics Conference, April 2023.

3. **Hemalatha Muthuganesan**, Fatih Bilge Atar, Agnieszka Gocalinska, Emanuele Pelucchi and Brian Corbett, "New and efficient sacrificial layer for transfer printing technology", European Conference on Integrated Optics, May 2022.

Declaration

I, Hemalatha Muthuganesan hereby declare that, unless otherwise stated, this work is my own, and that it has not been submitted for another degree, either at University College Cork or elsewhere.

Signed: Hemalatha Muthuganesan

Abstract

Photonic integrated circuits (PICs) offer a pivotal solution to meet the escalating demands of data bandwidth and used in data centres, LIDAR and optical sensing. Among various approaches, micro-transfer printing emerges as a rapid and universally compatible integration technology to generate PICs. To implement this technology, it is necessary to separate the devices from their original substrate using a release layer and transfer print them to designated location on target wafer. This enables the heterogeneous integration of numerous active devices from multiple wafers onto a single wafer, resulting in a compact and highly functional PIC. In addition to being a room temperature process, it is also cost-effective allowing reuse of expensive III-V substrates. This thesis demonstrates the application of micro-transfer printing technology in integrating ultra-thin, high-speed InGaAs photodetectors with silicon waveguides through various coupling mechanisms.

The thesis begins with optimizing the optical power coupled between the waveguide and the photodetector (PD), as even a small gap between them leads to optical mode loss at the interface. A co-planar in-fill idea is experimented by transfer printing the PD's absorber region at the same height as silicon waveguide. To fill the gap, evaporated amorphous silicon (a-Si) with a refractive index of 3.1 in the telecom wavelength range is utilized. This strategy aims to achieve maximum coupling.

In transfer printing process, it is crucial to efficiently release the PD coupons along with smooth interface, for successful printing on target wafer. This work introduces for the first time, a combination of InGaAs and AlInAs as release layers for InP based devices yielding double the etch rate and almost isotropic etch compared to individual release layers (InGaAs or AlInAs). This facilitates direct bonding of the PD coupons to the target wafer since the interface roughness is extremely low as 0.2 nm over an area of 10 μm x 10 μm, contributing to high-speed of the PD.

An excellent selectivity of 5410 is obtained with InP, which is 3.4 times higher than AlInAs and 7 times higher than InGaAs as release layers. These outcomes are accomplished at room temperature thus saving time, cost, and energy for the entire process.

The above optimized processes are used in integration of high-speed InGaAs photodetector to SOI platform, by direct bonding, with 100 % yield. An ultra-thin 675 nm epitaxial stack is grown with dual release layer on InP substrate, where a PD of size 21 x 57 μm^2 is fabricated. Such small dimension has the potential to fit 1 million devices on a 75 mm InP wafer. The same photodetectors are coupled to silicon waveguides via evanescent, grating and butt coupling mechanisms on the same target wafer. These PDs exhibit a maximum responsivity of 0.6 A/W, 47 nA dark current and with a data communication rate of 50 Gbps with on-off keying.

In future, this unique integration approach can be universally applied to any III-V active device like lasers and modulators to realise compact and high performance photonic integrated circuits.

Acknowledgements

Foremost thanks to my supervisor, Brian Corbett, for providing this life-changing opportunity. He had been immensely supportive throughout, in guiding me all along. Learnt valuable life lessons along with technical insights.

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My sincere and heartfelt thanks to Amma, Appa and Anna for their constant support, trust and everything they have done since the day I was born, to make me experience all the joy that they have dreamed.

Finally, I bow my head to God for always being with me and guiding me in right direction and giving me the power to stride along the right path.

Remembering couplet number 108 from a classic Tamil book named “Thirukkural”,

Transliteration:“Nandri marappadhu nandru-andru nandru-alladhu andre marappadhu nandru.”

Meaning: Never forget the help one offers. Also try to forget the ungrateful acts of others.

To

Matha Pitha Guru Deivam
Meaning: Mother, Father, Teacher and God.

Chapter 1

Introduction

In today's world, the demand for enhanced connectivity is universal, impacting various facets of our daily lives. There is a pressing need for tremendous amount of data transfer and increased internet speed as our reliance on digital technologies has undergone a substantial surge. This involves critical activities like remote work, online education, tele-medicine, video conferencing, cloud storage services and even in entertainment pursuits such as gaming and high-definition video streaming. This surge in data has led to a significant increase in network traffic worldwide, reaching trillions of gigabytes in data centers [1]. Regardless of the application, users expect reduced latency and minimized buffering times to facilitate uninterrupted interactions.

Meeting these demands is crucial for sustaining and advancing our increasingly digital and interconnected world. Data communication is evolving dynamically with innovations like Internet of Things and 5G connectivity enabling interconnectivity of devices. This evolution necessitates not only faster internet speeds but also high bandwidth to efficiently handle the increasing amount of data being transferred as represented in Figure 1.1.

This chapter gives an overview of how photonic integrated circuits comes as a solution to meet the surge in data and bandwidth requirements. Details of various integration techniques are provided with attention to micro-transfer printing technology and elaboration of its process details. Motivation of this thesis is presented with the scope of this work along with thesis outline of all chapters.

1.1 Photonics solution

The challenging scenario of surging data requirement is addressed by utilizing light for information transfer. Analogous to electronics where electrons serve as information carriers, photonics is the science and technology of generating, controlling and detecting photons (particles of light). Unlike electrons, photons are immune to electro magnetic interference and hence can flow alongside each other without interaction. This facilitates loss-less transmission and aids high bandwidth.

In photonics, data is transmitted using optical fiber for long distances with minimal signal degradation compared to electrical conductors, resulting in faster and more reliable data transmission. Lowest-ever transmission loss of 0.14 dB/km at 1550 nm wavelength has been demonstrated in a Germanium free silica-core optical fiber [2]. Moreover, the broad spectrum of light facilitates simultaneous transmission of multiple data channels, significantly enhancing the bandwidth in contrast to conventional copper-based systems. Photonics technology, specifically Wavelength-Division Multiplexing (WDM), plays a crucial role by allowing multiple data streams to be conveyed over different light wavelengths within a single optical fiber, effectively multiplying the available bandwidth [3].

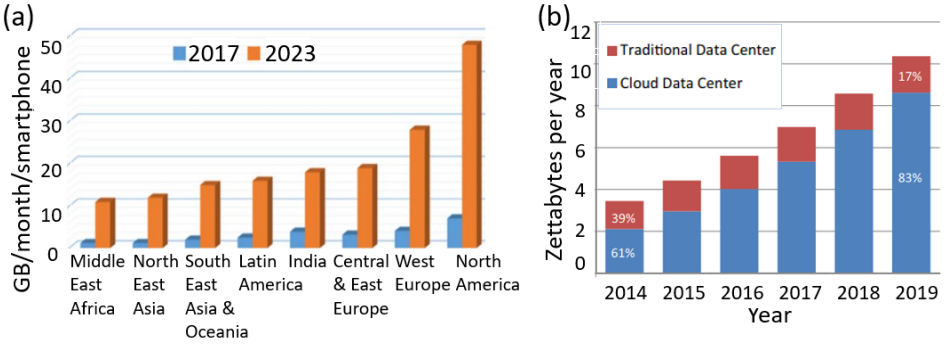


FIGURE 1.1: (a) Data traffic in gigabytes per month per smartphone is compared for 2017 and 2023 [4] and (b) Worldwide data center traffic growth in zettabytes [1].

In summary, photonics has become the backbone of modern telecommunications networks by revolutionizing data transport and internet speed by harnessing the unique properties of light. An efficient optical communication system can be built based on photonics principles for both short and long distance data transmissions. It provides high-speed and high-bandwidth with lower signal loss, essential for meeting the increasing demands of interconnected world.

1.1.1 Photonic integrated circuits

The aforementioned benefits of photonics find practical application in photonic integrated circuits (PICs) which is an assembly of multiple photonic, electrical, thermal and other components to form a functional chip. These PICs are employed in telecommunication networks, data centers, sensors and biophotonics. In data centers, PICs are instrumental for optical interconnects, facilitating fast and energy-efficient communication between servers and networking equipment. Demand for PICs are ever increasing with growing data centres and telecom industry. PIC market shows phenomenal growth from $\sim$ 190 M$ in 2013 and estimated at $\sim$ 3.5 B$ by 2024 [5]. Ireland's electricity consumption by data centres increased by a remarkable 31 % between 2021 and 2022 as reported by central statistics office website in 'Data Centres Metered Electricity Consumption 2022' statistics (https://www.cso.ie/en/releasesandpublications/). PICs enables miniaturization and integration of complex optical systems, leading to compact, high performance and scalable solutions across diverse applications. In addition to facilitating robust alignment they also enable packaging flexibility, thus reducing cost and increasing handling ease of broadband devices. Photonics research and market has escalated in past decade due to enhancement of the performance of photonic components and improvement in integration complexity [6] and [7]. The number of components built into these PICs increase with every year due to further miniaturization of devices as shown in Figure 1.2. The benefits of miniaturizing a PIC are its higher integration capacity saving the cost associated with materials and packaging, along with enhanced speed and better thermal management.

Designing a PIC necessitates a material platform capable of fabricating both passive and active components. Passive elements, such as low-loss waveguides, splitters, couplers and filters, enable the efficient propagation and manipulation of light. Active components, including lasers, modulators, photodetectors and amplifiers play dynamic roles in generating, modulating and detecting optical signals. However, achieving best performance for all these functionalities, at a specific wavelength, within a single material platform poses a great challenge. This is due to the fact that different material platforms excel in specific devices, presenting distinct advantages and limitations. This requirement for designing a photonic circuit is attained by the concept of integration. Essentially, there are four primary approaches to realize highly functional PICs that incorporate both active and passive devices such as, generic integration of III-V on InP substrate, monolithic silicon photonics, III-V heterogeneously integrated on silicon-on-insulator (SOI) and III-V epitaxially grown on silicon [8]. The best-performing devices from diverse material platforms are combined to take leverage of the strengths of each material.

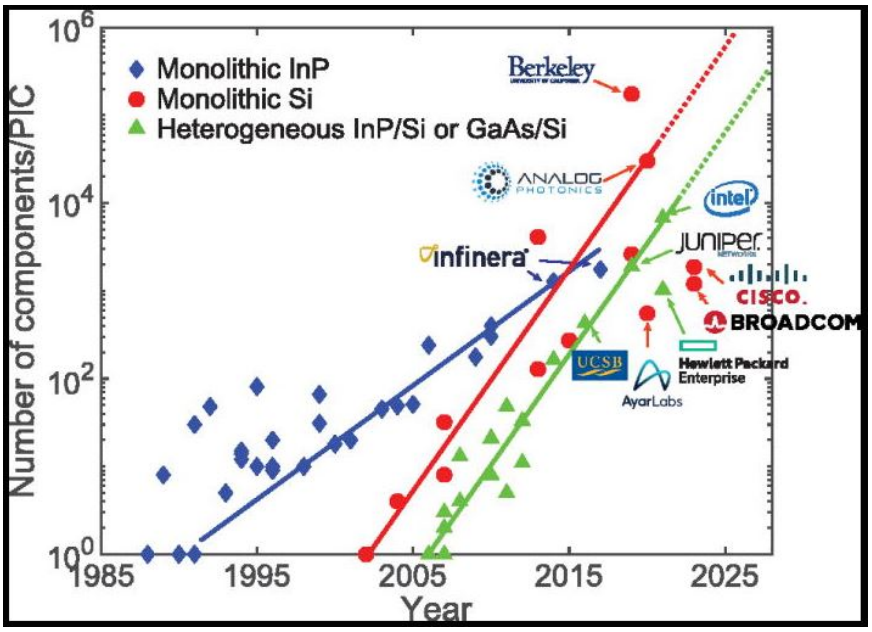


FIGURE 1.2: Number of photonic integrated circuits in InP and Si substrates increase every year due to miniaturization [6].

1.1.2 Silicon photonics

Silicon photonics is a technology that integrates all photonic components into a silicon-based platform to create a photonic integrated circuits. Silicon (Si) is a group IV semiconductor with an indirect bandgap of 1.12 eV (1107 nm). Extensive research is underway to explore SOI based PICs in response to the growing demand for increased bandwidth [9–11].

The SOI platform has several advantageous properties. Firstly, its waveguides exhibit high refractive index contrast both laterally and vertically, enabling effective optical confinement for low-loss propagation. This feature facilitates the fabrication of compact circuits, accommodating multiple devices within a small footprint. Secondly, silicon's compatibility with existing Complementary Metal-Oxide-Semiconductor (CMOS) manufacturing capabilities enables the integration of both photonic and electronic components on the same chip. This seamless integration facilitates communication between optical and electronic circuits [12] and [13]. Moreover, this CMOS compatibility also facilitates cost-effective mass production enhancing scalability and commercial viability of silicon-based PICs. Thirdly, silicon is transparent from 1.1 μm to 2 μm and beyond, making it suitable for tele-communication wavelengths (1310 nm and 1550 nm) passive devices. Thus SOI platform is versatile, capable of fabricating both passive [14], [15] and [16] and active functionalities like transceivers [17] and [18], synthesizers [19] and

optical interconnects within electronic integrated circuits [20]. Active features are achievable through Ge detectors [21], lateral p-n junction modulators [22] and more recently lasers [23].

While silicon photonics offers numerous advantages, it does have its own set of limitations. Firstly, Silicon photodetectors exhibit sensitivity in the visible and near-infrared (NIR) wavelengths. However, due to its bandgap, silicon is unable to detect light within the required telecommunication spectrum. To overcome this limitation, Germanium (Ge) [24] photodetectors are integrated into the silicon platform as shown in Figure 1.3. Germanium semiconductors possess an indirect bandgap of 0.67 eV (1850 nm) and they can efficiently absorb light within the wavelength range of approximately 1.1 μm to 1.6 μm. Secondly, the indirect bandgap nature of both silicon and germanium renders them less ideal for traditional laser applications due to their low emission efficiency. As a result, integration with III-V semiconductors becomes essential to realize lasers [25] in silicon platform. Hence, the integration of silicon with germanium and other III-V semiconductors is imperative to achieve efficient active devices like photodetectors, lasers, modulators and transceivers [26].

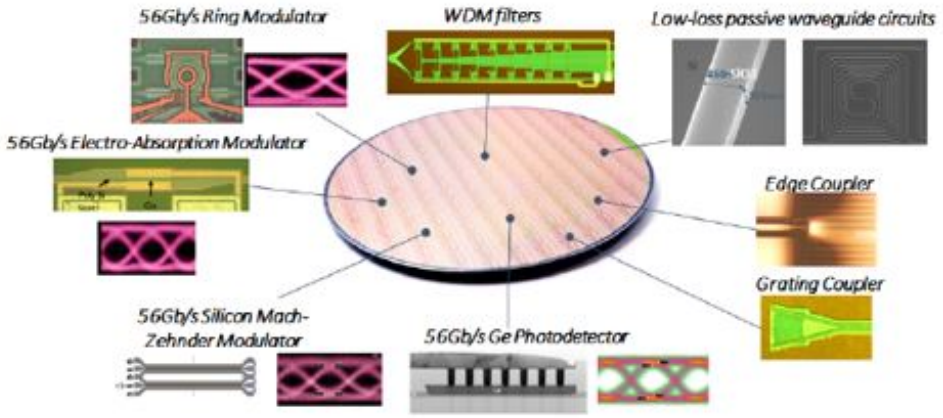


FIGURE 1.3: Fully integrated silicon photonic platform from imec with Ge photodetectors [24].

Hence, a heterogeneous approach that integrates active devices with SOI, leveraging the strengths of diverse material systems, remains an exceptionally appealing solution.

1.1.3 Heterogeneous integration

It is recognized that no single platform can encompass all the necessary functionalities for a PIC hence this section deals with the integration of multiple platforms. This approach utilizes unique strength of each platform, achieving flexibility and diversity in the incorporated devices and their operational wavelengths.

The integration process can be broadly categorized into two divisions namely hybrid integration and heterogeneous integration [27]. Hybrid integration involves assembling, fully developed and tested PICs or devices from different material platforms into a single unit during the packaging stage like flip-chip bonding [28]. This technique is employed in industries because it enables the incorporation of readily fabricated and pretested superior active devices, leading to a high circuit yield. However, flip-chip integration faces challenges related to throughput and the need to meet high alignment accuracy requirements.

On the other hand, heterogeneous integration combines diverse material platforms into a unified PIC during the fabrication stage itself, resembling the concept of monolithic integration. This method offers the advantage of precise alignment between waveguides and devices, resulting in minimal optical coupling loss during transitions.Various methodologies can be employed for accomplishing heterogeneous integration. Among these methods are wafer bonding and micro-transfer printing, which will be elaborated upon in the following discussion.

1.1.3.1 InP integration

InP (Indium Phosphide) is a III-V semiconductor, characterized by 1.3 eV bandgap and transparency spanning from 953 nm to 2 μm (0.6 eV to 1.3 eV) and beyond. The benefits of this integration lie in the utilization of standardized industrial integration processes, resulting in the attainment of stable and reproducible performance. TU Eindhoven has been at the forefront of pioneering generic photonic integration technology [29]. The success of this model is evident, with InP-based integration technology currently being commercially offered by JePPIX [30] and Infinera.

Photonic integration on the InP platform involves the growth of lattice matched ternary and quaternary epitaxial stacks on InP substrate. Subsequently, these epitaxial stacks undergo etching to facilitate butt-coupling, followed by passive layer regrowth and additional processing to transform them into optoelectronic devices. This establishes a platform for integrating advanced photonic functionalities on a single chip [31], [32] and [33].

This method offers flexibility in positioning lasers, amplifiers, high-performance modulators and photodetectors covering both C and L bands. This versatility allows for the testing of the entire circuit on the wafer and the current fabrication facilities are well-equipped to efficiently meet the growing demand for PICs, positioning InP as a cost-effective solution.

The challenge in InP integration is that, it necessitates multiplt epitaxial growth on an InP wafer for processing, introducing a dependency on the limited size of InP wafers. This limitation, in turn, imposes constraints on the number of PICs that can be accommodated within a given wafer size. The performance of lasers on native III–V substrate is considered state of the art, however their high cost due to rarity of material and smaller wafer size is a barrier compared to silicon. Both InP and silicon platforms have their own pros and cons [34].

1.1.3.2 Wafer bonding

Wafer bonding is a widely used integration technique where unprocessed III-V materials are bonded onto SOI substrate. Subsequent wafer-level processing is then conducted to fabricate photonic devices. General wafer bonding involves molecular, metal and adhesive bonding based on the type of interfacial material [35]. The versatility of this approach is demonstrated [36] through the successful integration of various active devices, such as phase modulators, amplifiers and photodetectors. This approach offers the advantage of straightforward optical alignment and enables high throughput since the processing is conducted at the wafer level.

However, this approach faces certain challenges. The primary concern is the wastage of costly III-V material during processing, accompanied by associated expenses. Additionally, the back-end process flow requires modification to integrate III-V devices, introducing complexity. Another issue arises from the fact that testing III-V devices is only feasible after their integration into the final wafer. This introduces the risk of certain devices not performing optimally, thereby impacting the overall compound yield. Combining two different material systems is possible, but it often necessitates compromises, presenting significant challenges in the integration process.

1.1.3.3 Micro transfer printing

This thesis utilizes a new heterogeneous integration technique known as micro-transfer printing (MTP) and its process and advantages are detailed here. This technique was first developed by Rogers group at University of Illinois in 2004 [37] and [38]. The core principle underlying MTP is the rate-sensitive adhesion between solid objects and the stamp, driven by the viscoelastic nature of the polymer stamp. Transfer printing is executed by leveraging kinetic control of adhesion to the elastomeric stamp [39] and [40]. A polymer material known as polydimethylsiloxane (PDMS) is utilized as the stamp, featuring either a single or multiple posts. These

posts are designed to have the same size and pitch like that of the devices on the native (source) wafer. The devices processed in source wafer and transferred are termed as "coupon" and the final wafer to which the devices are printed are referred to as "target wafer".

Step by step procedure of transfer printing of a photodetector (PD) coupon from the source wafer is depicted in Figure 1.4 (a). The stamp is accurately positioned over the coupon (Figure 1.4 b) and then lowered to apply an overdrive pressure on the coupon. The PD coupon adheres to the stamp, as observed in Figure 1.4 (c). The micro-transfer print tool is automated to move the stamp with the coupon to the target wafer, which, in this case, is a patterned SOI wafer. To ensure accurate alignment on the SOI target, imaging software is employed and the system automatically aligns to the desired print location (Figure 1.4 d) using fiducials on both the target and the coupon. The printed PD coupon is precisely aligned to the Si waveguide as programmed (Figure 1.4 e). Subsequent post-processing steps are carried out, leading to the final testable PD, as illustrated in Figure 1.4 (f).

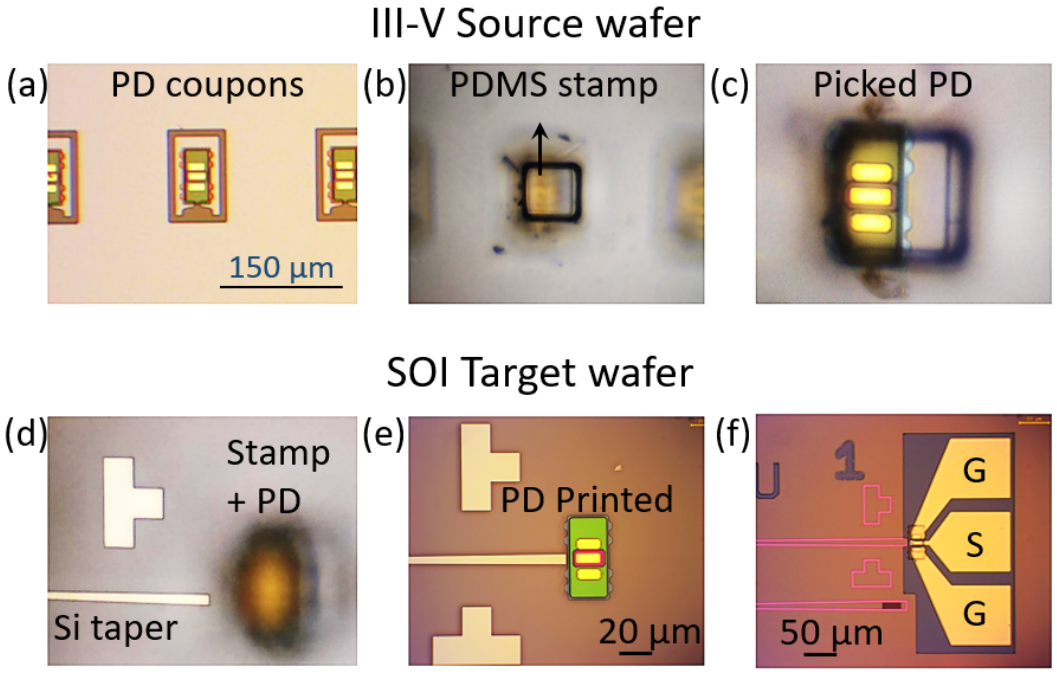


FIGURE 1.4: Sequential micro-transfer printing (MTP) process: (a) An array of released PD coupons on the source wafer, (b) In the MTP process, the PDMS stamp approaches the PD coupon on the source wafer, (c) The stamp picks up the PD coupon by applying an overdrive and breaking the tethers, (d) The stamp, carrying the PD, hovers over the target wafer with Si waveguides and MTP alignment marks and (e) The PD coupon is printed on the target wafer with precise alignment using imaging software.

Transfer printing technique allows the idea of scalability and area magnification, as illustrated in Figure 1.5. We can achieve a high density of coupons on the costly III-V source wafer, which can subsequently be printed onto the target wafer(s) at specified locations.

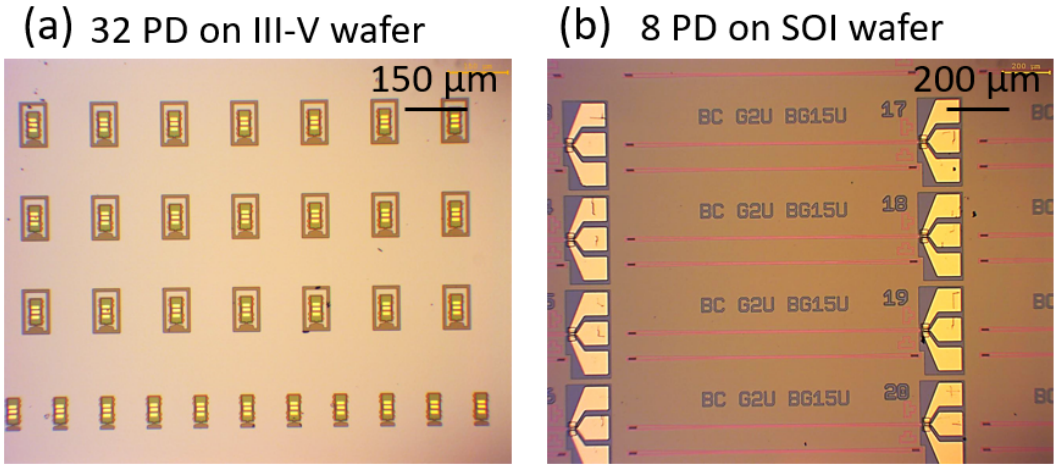


FIGURE 1.5: (a) InP source wafer displaying a densely packed array of PD coupons and (b) PD coupons transferred to the SOI target wafer, demonstrating the scalability and area magnification of the MTP technique.

This technique enables the transfer of micron-sized thin films or devices in a massively parallel manner at specified locations as demonstrated by printing 2850 chips using 30 x 95 array of elastomer post [41]. MTP achieves high throughput at room temperature, with a single cycle time ranging from 30 to 45 seconds [42]. It facilitates efficient utilization of expensive III-V materials by transferring only fully processed devices. Moreover, it offers the opportunity to integrate multiple III-V-based devices onto a single platform, as depicted in Figure 1.6. The devices can be precisely printed on the target wafer with a high alignment accuracy of ± 1 μm [43] as claimed by X-Celeprint, which I could make more precise to ± 200 nm for my photodetectors due to its smaller dimensions and individual printing optimizations.

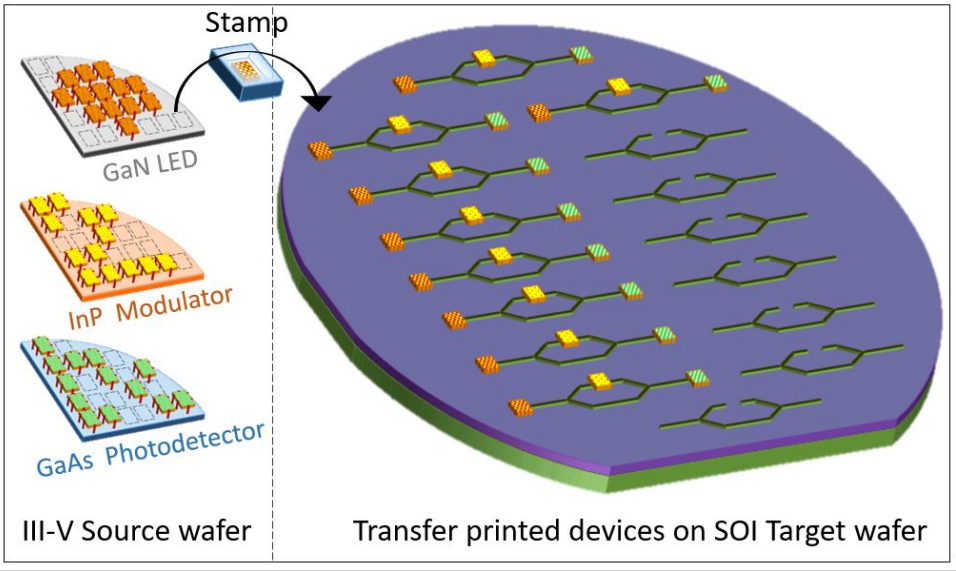


FIGURE 1.6: Schematic of compact photonic integrated circuit using micro transfer printing.

Unlike wafer bonding, MTP requires minimal modifications in back-end processing while retaining the advantages of optical alignment. Similar to flip-chip integration, MTP allows for the complete fabrication and testing of devices on the native substrate before transferring them to the final wafer, achieving high throughput. Thus, MTP combines the benefits of both wafer bonding and flip-chip integration.

Numerous active devices, including III-V distributed-feedback laser (DFB) lasers, optical transmitters, mode-locked lasers, tunable lasers, single-photon sources and Uni-traveling-carrier (UTC) photodetectors, have been successfully demonstrated. These devices exhibit optimal performance on various platforms such as Si, SiN, GaAs and $LiNbO_3$ through the utilization of transfer printing technology [44] and [45].

1.2 Novelty of thesis

The primary goal of the thesis is to towards a compact photonic integrated circuit using micro-transfer print technology. The original idea is to employ co-planar integration of thin InP based lasers, modulator and photodetectors to silicon waveguides. By keeping the active device thickness (quantum wells plus metal) within a few hundred nanometers, high mode overlap with silicon can be achieved.

Two significant challenges emerged during the integration of thin devices with silicon. The first challenge pertains to co-planar integration, which will be detailed in Chapter 2. The second challenge involves design issues of thin lasers, which will be discussed in Chapter 5 under the future work section.

In this study, we demonstrate the integration of thin photodetectors via co-planar in-fill fashion, alongside other coupling mechanisms such as grating and evanescent coupling.

- In photodetectors, unlike lasers, the impact of metal contacts is less critical, however, challenges with the in-fill mechanism persist.
- Issues related to material deposition, planarization and patterning have been resolved. Although some further improvements in patterning the in-fill material is required, to achieve lossless coupling.
- Additionally, we have optimized the sacrificial layer to enhance the coupon undercut process and improve transfer print quality.

- Overall, by employing the new dual sacrificial layer and leveraging grating and evanescent coupling mechanisms, we successfully demonstrate high-speed performance of 100 Gbps after post-processing for transfer-printed photodetectors.

1.3 Thesis outline

- **Chapter 2: Coupling mechanisms for heterogeneous integration**

  This chapter explores three vital coupling mechanisms between photodetector and silicon waveguides, essential for efficient PIC operation. The chapter starts with an overview of the SOI wafer, followed by discussion on grating couplers with theory and simulation optimizations. Then evanescent coupling is outlined with mode propagation from the silicon waveguide to the photodetector without tapering. Detailed simulations of optical mode absorption and interface loss are explained for all three coupling methods. Finally, it covers thorough processes for butt-coupling and its planarization using amorphous silicon co-planar in-fill, with its characterization. All coupling issues are studied through simulation and processing analyses. These optimized mechanisms play a pivotal role in integrating photodetectors onto the SOI platform, as further discussed in chapters 4.

- **Chapter 3: Dual sacrificial layer for direct bonding**

  This chapter concentrates on refining the sacrificial layers and wet-etch process in InP coupons, for transfer printing. The critical factors like thickness and choice of sacrificial material is experimentally optimized. A novel dual release layer, combining AlInAs and InGaAs materials, is introduced and extensively studied for its impact on interface smoothness, crystalline nature of etch, etch rate and selectivity. The standard wet etchant is a 1:2 solution of ferric chloride and water. A comprehensive analysis of different dilutions, examining their etch rate, selectivity and linearity is executed. The key characteristics of the dual release layer are high etch rate and improved selectivity at room temperature, saving time, cost and energy. Notably, it allows for the direct bonding of coupons to the target surface without the need for adhesives.

- **Chapter 4: Transfer printing of ultra-thin InGaAs photodetectors**

  This chapter details the transfer-printable ultra-thin InGaAs photodetector, highlighting the significance of its uni-traveling carrier epitaxial structure for high-speed photodetection. Results encompass a thorough analysis of dark current characteristics, responsivity and capacitance-voltage measurements, comparing outcomes across butt, grating and

evanescent coupled photodetectors. High-speed measurements, including S21 characteristics and 100 Gbps eye diagrams (post-processing) results and analysis are presented specifically for grating and evanescent coupled photodetectors.

- **Chapter 5: Conclusion and future work**

  This chapter provides a concise overview of the key results of the thesis, accompanied by recommendations for future research.

- **Appendix**

  The appendix provides a summary of various dry and wet etches used. It also includes supplementary details for Chapter 3, including mask designs and the rationale behind individual sample pieces for each undercut experiment. Additionally for Chapter 4, details of epitaxial stack, tether design, process flow for source wafer fabrication are provided along with details of calculating the optical power reaching the photodetector.

Chapter 2

Design and process of coupling mechanisms for photodetector

2.1 Introduction

Photonic circuits rely on the transfer of optical signals between different components such as waveguides, modulators and detectors. Obtaining maximum coupling efficiency is crucial in the coupling mechanisms engaged. This ensure minimal signal loss during the transfer, thus maximizing the overall performance of the circuit.

This chapter will address the light transfer between silicon waveguide and the transfer printed photodetector, within the same SOI chip, via three coupling methods. Namely co-planar butt coupling, grating coupling and evanescent coupling as shown in Figure 2.1. Each method shall be elaborated with simulations and detailed processing steps. The optimization of these coupling mechanisms depend on the active device transferred onto the SOI wafer and the thickness of silicon waveguide layer.

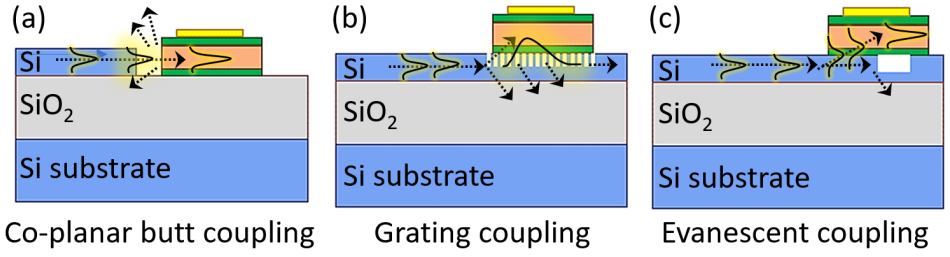


FIGURE 2.1: Schematic of different coupling mechanisms: (a) Butt coupling to in-plane device, (b) Grating coupling to out of plane component and (c) Evanescent coupling.

The chapter starts with an introduction to the SOI wafer design, laying the foundation for subsequent discussions. This is followed by the theory and simulation of grating couplers. A detailed simulation of mode transfer in 2D evanescent coupling is provided. Additionally, simulations focusing on light absorption in PDs and interface loss for each coupling mechanism is also stated. Finally, the fabrication process of co-planar butt coupling mechanisms is discussed, addressing challenges, presenting observations and proposing potential solutions.

2.2 SOI wafer for coupling

This section provides an overview of how all three coupling mechanisms are implemented on a single SOI chip. This wafer is anticipated from a multi-project wafer (MPW) run facilitated by Cornerstone, featuring silicon patterns illustrated in Figure 2.2 (a and b). Subsequent simulations are conducted based on this wafer design. It is expected that in the future, the fabricated photodetectors will be transfer printed onto this SOI wafer.

The SOI wafer features a 500 nm thick crystalline Si waveguide layer on top of 3 μm thermal silica (SiO_2) buried oxide on a silicon substrate. The wafer is configured with input and output grating couplers, optimized for transverse electric (TE) mode coupling. It includes a 0.5 mm long, 450 nm wide single-mode waveguide with 0.7 mm long tapers, as illustrated in Figure 2.2 (a). Additionally, the wafer also includes designs with an input coupler and the output side consisting of tapered design, as depicted in Figure 2.2 (b). The structures are defined by etching a shallow trench (300 nm deep) with a width of 5 μm around the structures as labelled in Figure 2.2 (i) .

Co-planar coupling involves integrating a thin PD with its absorber layer in plane with the silicon waveguide. For this purpose, Si waveguide design without grating coupler at the output (Figure 2.2 b) is chosen, where red dotted lines mark the area of transfer printing (TP). Since the region is uneven and in order to align PD in-plane with silicon, the red dotted region is selectively etched into buried oxide to facilitates co-planar butt coupling as shown in Figure 2.2 (c to f). The gap between PD and Si (Figure 2.2 f) is infilled with refractive index matching material amorphous silicon (a-Si).

Earlier demonstration of such coupling has been shown for lasers [46]. They have achieved significant gain in a thin quantum well stack by strategically decoupling carrier and optical mode confinements in perpendicular directions. However, their approach involves a complex

fabrication process demanding meticulous control, which have been optimized over a decade. The co-planar in-fill process, we demonstrate also has certain processing challenges and we have overcome some of them although it is yet to be made perfect. Our approach offers several advantages. It seamlessly integrates with any foundry process, being implemented on the SOI platform. It is cost-effective, enabling mass production with a replicable nature.

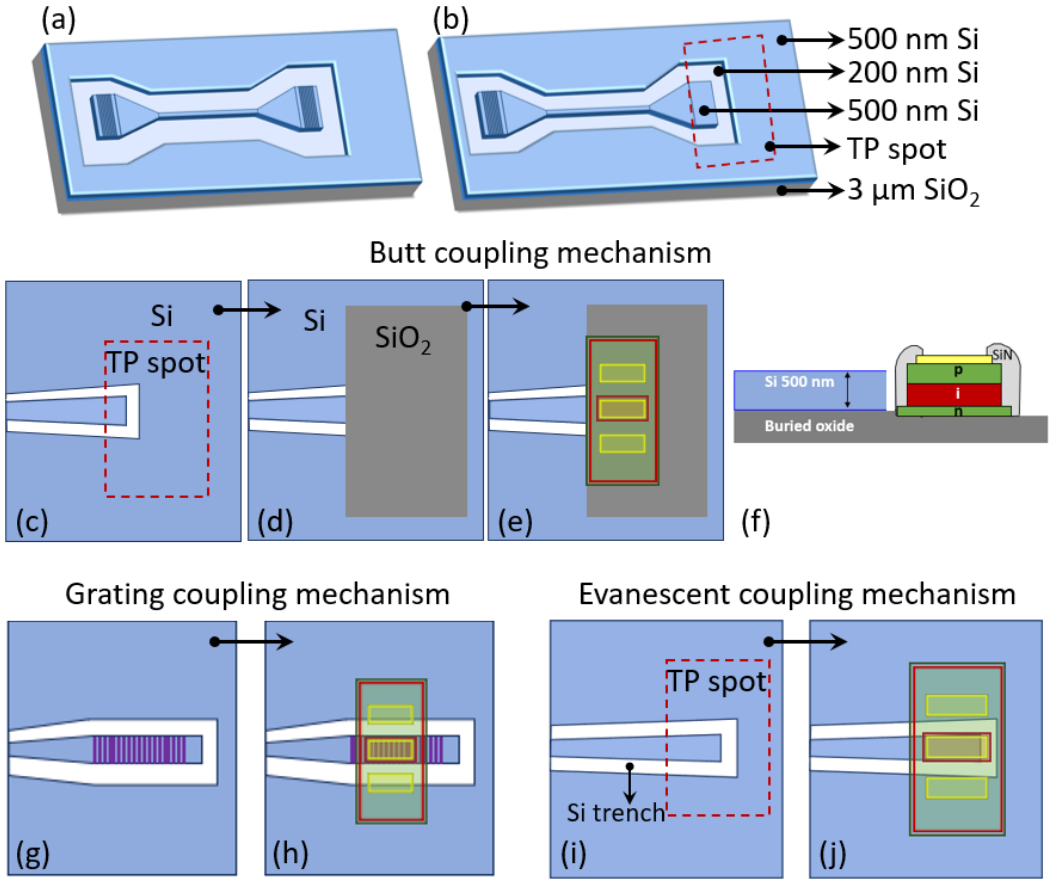


FIGURE 2.2: Schematic of starting SOI wafers consisting of (a) Both input and output grating couplers and (b) input coupler with tapered output, with transfer print (TP) region of PD shown by red dotted lines, (c) Utilizing a tapered output design for butt-coupled PD, (d) trench formation into buried oxide enabling co-planar transfer printing of PD (e) transfer printed PD inside the trench and (f) its cross section view. (g) Output GC before transfer printing and (h) Output GC with printed PD on top. (i) Output taper prior to printing and (j) Transfer printed PD onto tapered silicon, for evanescent coupling.

The expected performance metrics of the grating couplers (GC) received from Cornerstone are outlined in Figure 2.3, where the plot is supplied by Cornerstone. These couplers demonstrate a coupling efficiency ranging from 5 dB to 6 dB per coupler, with a 1 dB bandwidth exceeding 30 nm and a center wavelength falling between 1550 nm to 1570 nm. For the grating coupling of the photodetector, the SOI pattern depicted in Figure 2.2 (a), is utilized, positioning the PD on top of the output grating coupler as depicted in Figure 2.2 (g and h).

In the case of evanescent coupling for the photodetector, the same SOI pattern utilized for butt coupling (Figure 2.2 b) is employed. The distinction lies in the absence of etching in this configuration, instead, PD coupons are directly transfer printed onto the red dotted region as depicted in the schematic top view of Figure 2.2 (i and j). Typically, silicon is laterally tapered to facilitate mode coupling to the PD evanescently [47], but in this instance, no specific tapering down (reducing lateral width: from higher taper width to lower taper width) design is implemented, to squeeze the mode from silicon to PD. While this choice incurs some coupling loss, the trench at the end of the silicon taper aids in directing the mode towards the PD. Furthermore, this approach offers ease of implementation and multiple application possibilities, along with the simplicity of the process.

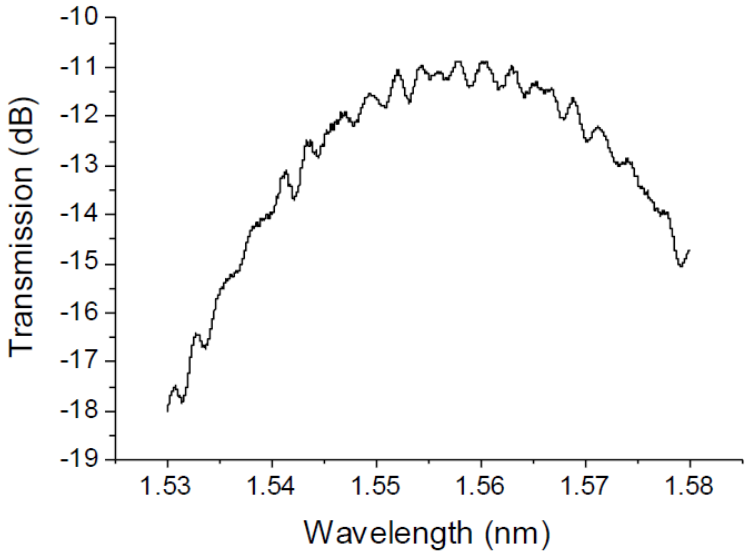


FIGURE 2.3: Cornerstone provided above plot of measured coupling efficiency for their MPW grating couplers on 500 nm SOI for 1550 nm TE mode.

Following this overview, a comprehensive examination of the theory and simulation of grating couplers is presented to enhance understanding of their operation and characteristics.

2.3 Grating coupler theory

Grating couplers are diffractive structures formed by periodic change in refractive index, created by etching deep trenches in the silicon (SOI) waveguide. These couplers are engaged to dramatically change the direction of light from vertically out of plane, for example from vertical fiber to chip or vice versa. They are highly sensitive to wavelength and polarization of light. Surface grating couplers are beneficial for chip level testing at arbitrary coupling positions on

chip. The diffraction behaviour of the grating coupler is described by the Bragg condition of phase matching as given in Equation 2.1 and illustrated by wave-vector diagram [48].

$$\mathcal{K}Sin\theta + mG = \beta_m \tag{2.1}$$

where $\mathcal{K}$ is wave vector of incident light give by Equation 2.2, m is the order of diffraction, G is the grating vector given by Equation 2.3 and β is propagation constant of the coupled light given by Equation 2.4.

$$\mathcal{K} = \frac{2\pi n_m}{\lambda_o} \tag{2.2}$$

$$G = \frac{2\pi}{\Lambda} \tag{2.3}$$

$$\beta = \frac{2\pi n_{eff}}{\lambda_o} \tag{2.4}$$

$$n_{eff} = [F \times n_o] + [(1 - F) \times n_e] \tag{2.5}$$

where n_m is refractive index of medium, Λ is the grating period or pitch, λ_o free space wavelength of light desired to be coupled and n_{eff} is effective refractive index of the mode calculated using Equation 2.5. Where F stands for fill factor in coupler, F and (1-F) are the ratio of unetched width to pitch length and etched width to pitch Λ respectively. The refractive index of unetched and etched regions are given by n_o and n_e as show in Figure 2.4 (b), which is zoom in of 2D grating coupler simulation using Ansys lumerical finite difference time domain (FDTD) as in Figure 2.4 (a).

Substituting Equations 2.2, 2.3 and 2.4 in 2.1, gives the final formula in Equation 2.6 to calculate the grating pitch for maximum coupling of light from grating coupler to the device. Both input and output grating couplers are symmetric in nature, so the light coupled from vertical fiber at an angle θ to the silicon waveguide is same as the out-coupled light from the waveguide to the device.

$$\Lambda = \frac{\lambda}{n_{eff} - n_c Sin\theta} \tag{2.6}$$

The light propagating from waveguide needs to be diffracted up in right order and the field profile of diffracted light should match with receiving fiber or device. In a grating coupler there is also downward radiating wave which is leaked to substrate.

There are two means of suppressing the loss due to downward propagation and adding them to upward diffracted light as suggested by [49]. Only a simple grating coupler simulation is shown here without the changes required to increase upward diffraction. Either by incorporating

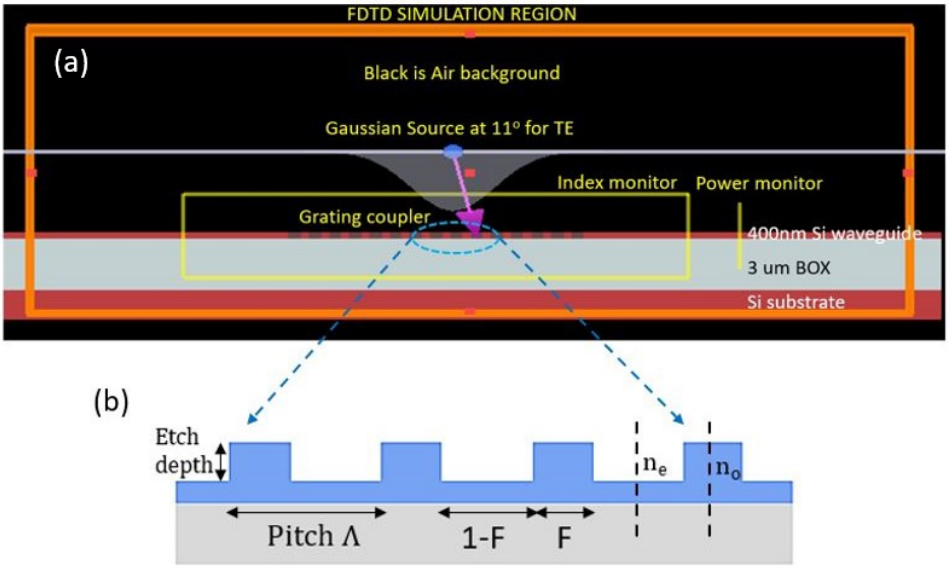


FIGURE 2.4: Simulation of grating coupler: (a) Screenshot from a 2D Lumerical simulation showing the in-coupling of light from a Gaussian source to a waveguide and (b) Zoom-in of the grating coupler detailing its pitch, fill factor and etch depth.

Bragg mirror in the substrate at suitable height or by varying buried oxide thickness to achieve constructive interference between substrate reflected and upward diffracted wave. This is not a straight forward solution as the wafers are mostly purchased, so cannot add mirrors or optimize buried oxide thickness. Since it is difficult to redirect the downward radiating light, at first place we can prevent it from happening by employing a grating profile optimization by tuning teeth width and depth inducing destructive interference for the downward wave. This technique is referred as apodization.

2.3.1 Grating coupler simulation

Up to this point, we have explored the theoretical aspects of grating couplers. This section delves into the design and optimization of grating couplers tailored for a 400 nm SOI substrate, specifically targeting the TE mode at a wavelength of 1550 nm. These designs were meticulously refined for fabrication on SOI chips at Tyndall, although this plan did not come to fruition, due to the optimization required in the electron beam lithography process at that point. Instead, in practice, we have employed Cornerstone's grating couplers designed for a 500 nm SOI substrate. Nonetheless, the knowledge obtained from the design process for the 400 nm SOI grating couplers are shared in this section.

The SOI used in simulation consists of 400 nm Si waveguide, with 3 μm buried oxide beneath. A 1550 nm TE, fundamental mode is launched vertically by a Gaussian source over the grating coupler at an angle of 11° and the coupled light into the waveguide is measured using frequency-domain field and power monitor in FDTD. A Gaussian source with waist radius of 4.5 μm is used to compare with experiments where a single mode input fiber of 10 μm diameter is used with a polarization of 90° which specifies TE mode, with a centre wavelength of 1550 nm and a span of 150 nm. The initial pitch of the grating is calculated using the Equation 2.6 starting with 50 % fill factor F to and the values of n_o and n_e are obtained from simulations to obtain n_{eff}. The grating coupler design for 1550 nm wavelength after parameter sweeps is shown in Figure 2.5 (a). Parametric sweeps are carried out to finalize 215 nm of etch depth and 600 nm of grating period as seen in Figure 2.5 (b and c).

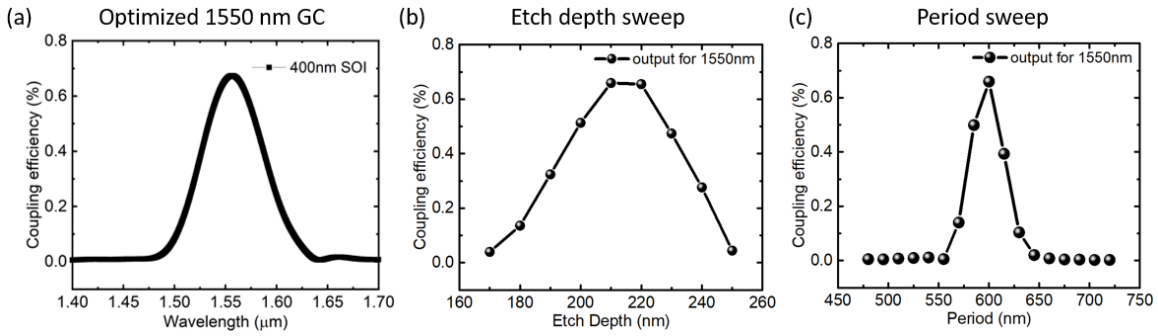


FIGURE 2.5: For 1550 nm grating coupler: (a) Optimized coupling efficiency of 66 % with 3 dB bandwidth of 71 nm, (b) Plot showing dependence of grating coupling with variation in etch depth and (c) Period sweep.

For a fixed input angle of fiber, wavelength and etch depth, only grating period is varied in Figure 2.5 (c), where a deviation of around 10 nm in the grating period leads to a 10 % decrease in coupling efficiency. The same situation (10 nm change causing 10 % reduction of coupling efficiency) is observed for etch depth as well from Figure 2.5 (b), for fixed input angle, grating period and duty cycle. Such sensitivity arises from $\mathcal{K}$-space matching [49], which accounts for differences in the propagation vector of guided modes introduced by the grating coupler. This is influenced by both the effective refractive index (n_{eff}) and the wavelength, as depicted in Equation 2.4. The n_{eff} depends on the etch depth; deeper etching results in less material remaining in the coupler, thereby reducing the calculated n_{eff} and affecting the propagation constant. Consequently, deeper etches facilitate coupling with longer wavelengths to maintain the ratio of n_{eff} by wavelength as per Equation 2.4. To enhance robustness, multiple sets of grating couplers are fabricated with various combinations of period and duty cycle around optimized values from simulations. This approach ensures that some couplers perform optimally

for the achieved etch depth. However, in the context of MPW runs, constrained wafer space and the capability of MPW runs to achieve the desired etch depth and performance lead to the exclusion of multiple sets of couplers.

The finalized design features a grating pitch of 600 nm, an etch depth of 210 nm and comprises 18 grating periods. With a Gaussian source input angle of 11°, this optimized simulation gives a coupling efficiency of 66 % with 3 dB and 1 dB bandwidths of 71 nm and 41 nm in FDTD, respectively. In this setup, approximately 18 % of the incident light is diffracted into the air, while 15 % is leaked into the substrate. Compared to the grating coupler design discussed in [50], this design boasts a 16 % higher efficiency and approximately 10 nm wider 1 dB bandwidth.

The coupling efficiency of this straightforward 2D grating coupler design can be further enhanced through the incorporation of a Bragg reflector in the buried oxide layer and the implementation of apodization in the grating coupler. These modifications would serve to reduce substrate and diffraction losses, thereby increasing the amount of light coupled into the silicon waveguide and strengthening the performance of the grating coupler.

2.4 Evanescent coupling simulation

This section details evanescent coupling through 3D FDTD simulation. For these simulations, the absorber InGaAs material is provided with only real value of refractive index and the imaginary part of the refractive index is maintained at zero. So there is no mode absorption in the photodetector. This enables the observation of mode transfer from the silicon waveguide to the InGaAs PD through the interaction of the tail of the propagation mode as depicted in Figure 2.6. However this is not the real scenario.

The top view of the evanescent coupled PD along xz plane is illustrated in Figure 2.6 (a and b). Although these images are repetitive, they are included again for clarity regarding axis orientation. Figure 2.6 (c) offers a 3D schematic with x-y-z axis orientation as utilized in the simulation. In Figure 2.6 (d), a screenshot from the simulation is provided, showcasing color bars representing refractive indices. The PDs used in the simulation have a length of 20 μm and mirror the actual fabricated PDs discussed later, with complete epitaxial stack details provided in Appendix Figure A.3. This image is oriented along the x-y plane and incorporates the silicon trench.

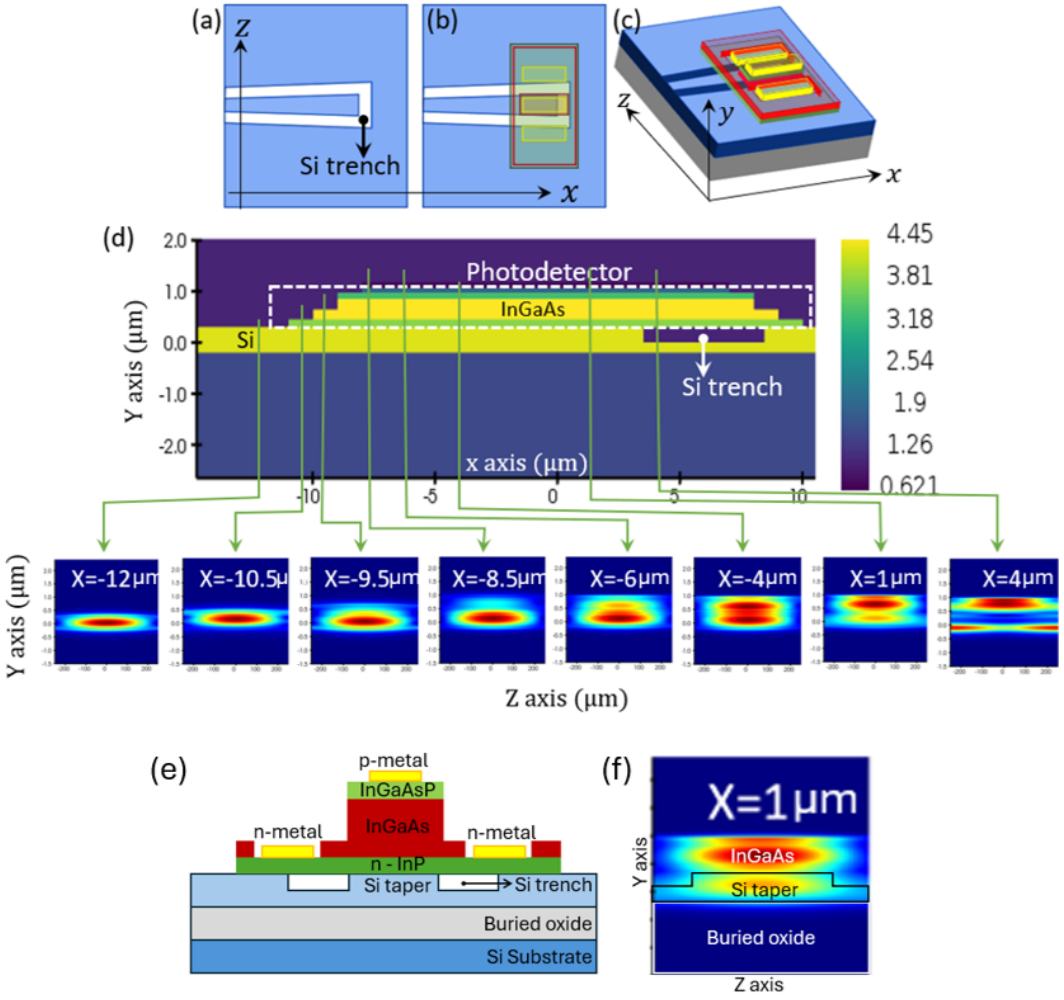


FIGURE 2.6: Evanescent coupling: (a) Top view of SOI with trench around silicon taper region, (b) Transfer printed III-V photodetector on top of silicon taper and trench, (c) 3D schematic of SOI with transfer printed PD with x-y-z axis marked, (d) Simulated refractive index profile along x-y longitudinal-section of the PD. The arrows lead to images showing optical mode in z-y plane perpendicular to the propagation direction (x- axis), (e) Cross-section image of PD on SOI along z-y plane and (f) As a comparison to cross-section schematic diagram, simulated cross-section is provided at x = 1 μm, showing mode transition from silicon taper to PD in z-y plane.

The mode transfer from silicon to III-V can be observed from the longitudinal-section images presented in Figure 2.6 (d) and its branches. Initially, at x = -12 μm, the mode is entirely confined within the silicon. As the III-V device commences (around x = -10.5 μm), the mode gradually transitions upwards, progressing through InP and eventually reaching InGaAs (x = -9.5 μm). After traversing a length of approximately 12 μm, at x = -4 μm, an equal distribution of the mode is observed between the III-V material and silicon. Subsequently, at the start of the trench in the silicon, the majority of the mode becomes confined within the III-V layer. In the trench section, at x = 4 μm, the optical mode in silicon is leaking towards the boundary. This is due to the reduced silicon thickness at the trench region forcing the modes to leak to

unetched silicon outside the trench, as shown in Figure 2.6 (c) along z-y plane. This illustrates how the trench aids in shifting the mode from silicon to III-V. To understand the branch out simulations better, a cross-section image along z-y plane of the PD on SOI is shown in Figure 2.6 (e). One of the branch out image at X = 1 μm is zoomed out, to emphasize the mode transition from silicon taper to PD.

Furthermore, in actual case, the materials of the PD is modeled with an imaginary index, a significant portion of the modes is absorbed by the PD even before reaching the silicon trench, in contrast to what is observed in above mode transfer. The absorption in PD will be explained in the following section for all coupling mechanisms.

2.5 Simulation of photodetector absorption

This section details simulations comparing light absorption in a 20 μm long photodetector for various coupling mechanisms. These are 2D FDTD simulations along the longitudinal section, where the optical mode propagates in the silicon waveguide, couples, and is absorbed in the transfer-printed photodetector, as depicted in the schematic in Figure 2.1. Unlike the previous section, these simulations use both real and imaginary refractive index values for the photodetector to emphasize mode absorption. A script from the Lumerical website was used to calculate absorbed optical power per unit volume due to material absorption, with the results presented in Figure 2.7 (b, d, and f).

The refractive index profile, with a color bar, is provided for the longitudinal section of the photodetector in Figure 2.7 (a, c, and e). The mode absorption is shown in Figure 2.7 (b, d, and f). Since there is no absorption of the optical mode in silicon waveguide and buried oxide, these regions appear as a dark blue monotone in the simulated intensity profiles. The photodetector region, marked by a white rectangle, displays light blue shades, indicating mode absorption within the photodetector.

Since these are 2D simulations, accurately estimating the percentage of mode absorption is challenging. A 3D simulation with the exact dimensions of the photodetector could provide a precise value for mode absorption, closely mimicking actual results, but it was not conducted due to the extensive time required for these simulations. Mode absorption also depends on the amount of light coupled into the photodetector in each scenario, which is influenced by the

processing and transfer printing details of the photodetector, as these determine the interface loss.

In the literature on InGaAs photodetectors integrated into silicon platforms, the percentage of mode absorbed and measured responsivity are provided for butt coupling ([51], [52]), grating coupling ([53], [54]), and evanescent coupling ([55], [56]) mechanisms. The measured responsivity for the PD used in this thesis is discussed in Chapter 4, under the section "Responsivity Measurement" (see Figure 4.15).

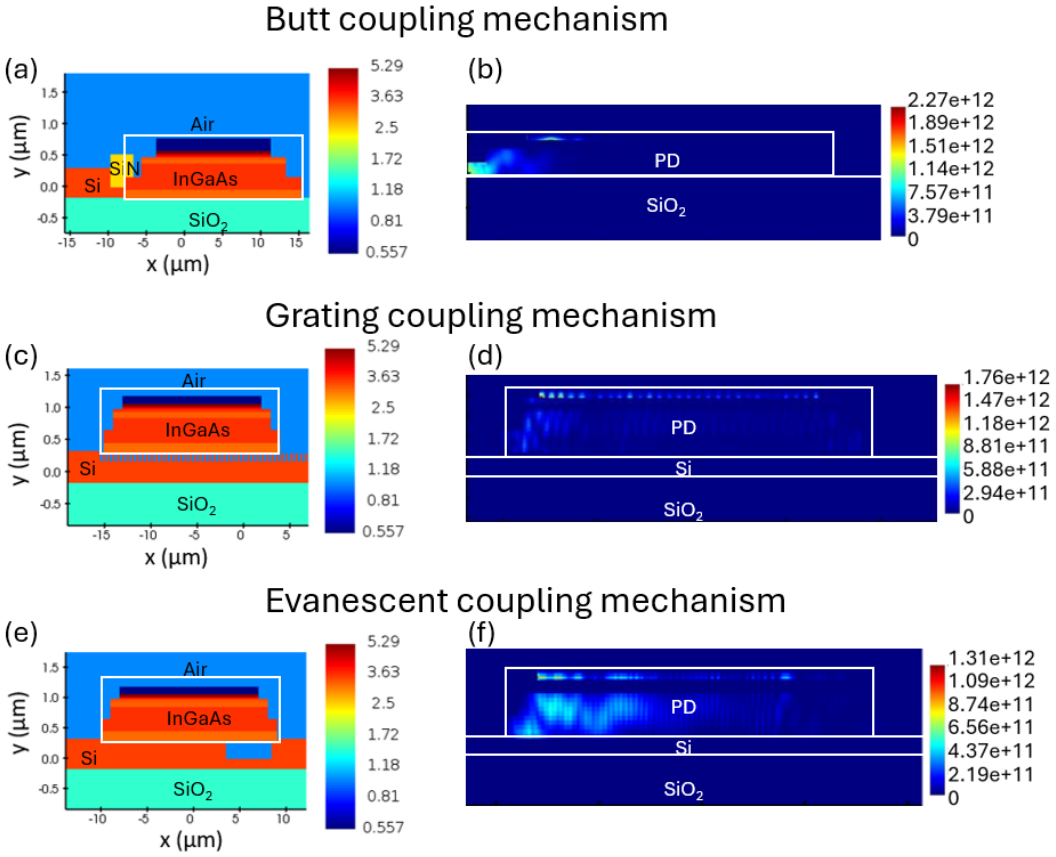


FIGURE 2.7: Optical absorption distribution in the detectors as calculated from FDTD simulations. (a) Illustrates the refractive index profile of a butt-coupled PD, printed in-line with Si waveguides and (b) Presents simulation result of mode absorption. (c) Depicts refractive index profile of a grating-coupled PD and (d) Simulation exhibits higher light absorption in grating coupled PD compared to butt coupled PD. (e) Represents refractive index profile of an evanescent-coupled PD printed on top of the tapered ridge region of the waveguide and (f) Simulation displays maximum light absorption in the evanescent-coupled PD, compared to other coupling scenarios.

In the case of butt coupling Figure 2.7 (a and b), it is anticipated that there will be a gap 'g' of approximately 1 μm between the Si waveguide and the PD during the transfer printing process. The simulation aligns the PD such that the waveguide and absorbing layer are in-line, mirroring the actual transfer printing process onto the SOI chip. The simulation results

provided in Figure 2.7 (b) illustrate the mode propagation in the Si waveguide and subsequent absorption in the PD. Minimal absorption is observed in butt-coupled PD due to lower light coupling from the waveguide to the PD, attributed to scattering and reflection losses at the interface. Further elaboration on these factors will be provided in the following section.

For grating coupling, the mode diffracts towards the PD positioned on top (Figure 2.7 c and d). The mode diffraction occurs along the length of the grating coupler, as evident in Figure 2.7 (d), spanning the length of the grating teeth. It is observed that maximum absorption occurs at the beginning of the PD itself and gradually decreases along its length due to the reduced optical mode diffraction in the later part of the coupler. To take advantage of this, the PD is transfer printed at the starting of the grating coupler. The PDs are fabricated with their P mesa width matching the grating couplers width to effectively absorb diffracted light. It is seen that the amount of light absorbed in grating coupling is higher than in the butt coupling case.

In evanescent coupling, the photodetector (Figure 2.7 e and f) is positioned at the end of the silicon taper, encompassing the trench in the SOI wafer. It is noted that the majority of the mode is absorbed in the first half of the PD itself. The absence of silicon compels the mode to propagate upwards towards the photodetector, in addition to reflection and scattering.

Indeed, as depicted in Figure 2.7 (b, d and f), there is a noticeable rise in PD absorption, progressing from butt coupling, through grating coupling and reaching a peak in evanescent coupling.

2.6 Simulation of interface loss

This section discuss about various losses encountered in all three coupling mechanisms during the propagation of modes from the silicon waveguide to the photodetector, specifically at the silicon-air and air-PD interface. This juncture is crucial as the optical mode undergoes coupling from one material to another with differing refractive indices. To analyze these losses, 2D FDTD longitudinal simulations are conducted. The simulations utilize frequency-domain field and power monitors positioned at various locations to estimate the extent of loss.

2.6.1 Co-planar butt coupled PD

A schematic of the co-planar butt-coupled PD with monitor locations is illustrated in Figure 2.8 (a). It is worth noting that the actual simulation run incorporates additional monitors compared to the schematic depiction. For co-planar coupling, a trench is created in the silicon, and the PD is transfer-printed into this trench. This configuration allows the PD absorber and silicon waveguide to be at the same height, facilitating a smooth mode transition in a co-planar manner. A block of silicon nitride is positioned between the waveguide and the PD, serving the purpose of encapsulation required during the fabrication process of the coupon (refer to appendix Figure A.6 for more details).

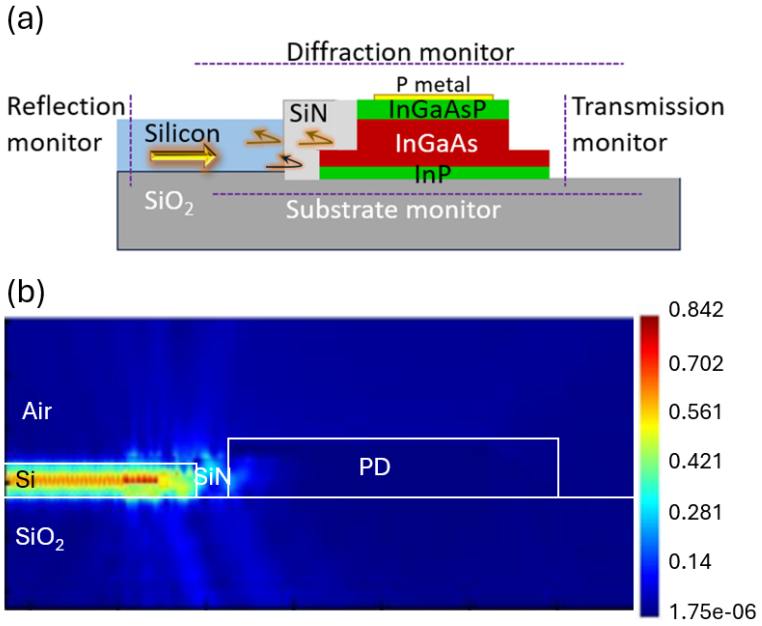


FIGURE 2.8: Distribution of light delivered from the Si waveguide to the butt coupled InGaAs detector as calculated from FDTD simulations: (a) Schematic illustration depicting longitudinal sections of mode propagation from the silicon waveguide to the photodetector, with monitors strategically positioned at various locations to assess contributions to losses and (b) Simulated intensity profile showing optical mode scattering and reflection loss.

Figure 2.8 (b) shows a mode source of 1550 nm wavelength with the fundamental TE mode propagating in the silicon waveguide. The light blue shades at the interface indicate the mode loss into air and oxide. It is measured that only 40 % of the light is effectively coupled to the photodetector, which is low, as the remaining 60 % lost in various ways, most of which is accounted for below.

Si-SiN interface reflection $\sim$ 7 %

Air-SiN interface reflection $\sim$ 11 %

Si-InP interface reflection $\sim$ negligible %

Si-InGaAs interface reflection ∼ negligible %

SiN-air interface reflection ∼ 11 %

SiN-InP interface reflection ∼ 5 %

Substrate leakage loss ∼ 10 %

Upward diffraction loss ∼ 3 %

Total reflection loss behind source ∼ 7 %

Future PD designs can mitigate losses arising from Si-SiN and SiN-InP interface reflections by implementing patterned in-fill with a-Si in interface and modifying the PD design to eliminate the need for a SiN encapsulation layer. This enables closer integration of the PD with the silicon waveguide, while transfer printing.

2.6.2 Grating coupled PD

Grating coupled PD is schematically presented in Figure 2.9 (a) along with simulated intensity profile representing mode lost in light blue shades in air and oxide in Figure 2.9 (b).

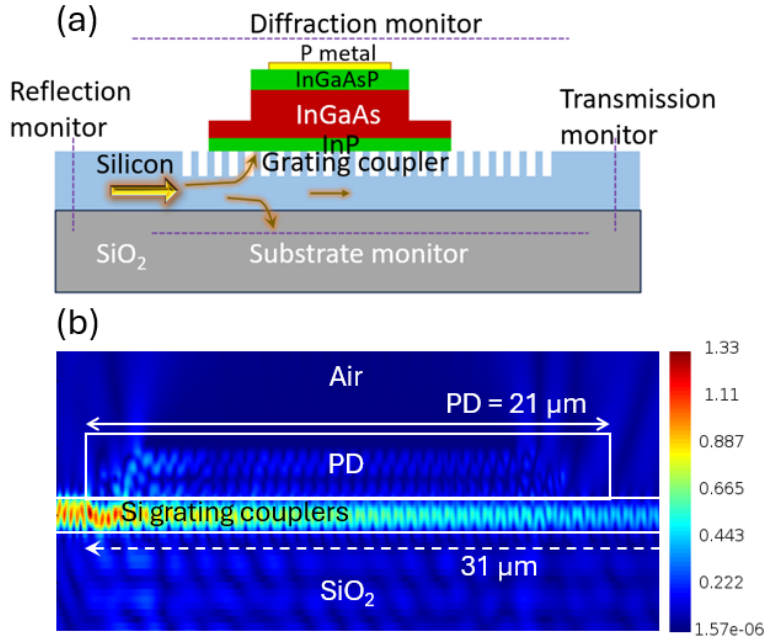


FIGURE 2.9: Distribution of light transferred from the Si waveguide to the grating-coupled InGaAs detector, as calculated by FDTD simulations (a) Schematic diagram of longitudinal sections of PD showing mode propagation from silicon waveguide to photodetector, via grating coupler diffraction and (b) Simulated intensity profile showing optical mode diffracted and scattering into air and leaked into substrate from the grating coupler.

The 21 μm long photodetector is transfer-printed at the beginning of the 31 μm long output grating coupler. This placement ensures that the photodetector captures the maximum amount

of diffracted light from the grating coupler right at the start. In this design, approximately 62 % of the light is coupled to the photodetector, with the remaining light being lost in various ways. Along the length of the coupler, light is diffracted both upwards and downwards. The upward-diffracted light at the start of the coupler is absorbed by the photodetector. Beyond the photodetector length, the light diffracted upwards is lost to the air, noted as "upward diffraction loss". The light diffracted downwards is lost to the silicon substrate, referred to as "substrate leakage loss". Additionally, any light transmitted beyond the grating coupler is categorized as "transmission loss". Figure 2.9(b) shows the simulated intensity profile around the transfer-printed photodetector. The image captures light propagating along the length of the grating coupler, as well as light scattered into the air and lost in the substrate. This snapshot is cropped to provide a detailed view around the photodetector and does not cover the entire length of the grating coupler, so the transmission loss is not visible in this image.

Substrate leakage loss $\sim$ 29 %
Upward diffraction loss $\sim$ 6 %
Transmission loss is negligible after grating coupler.
Total reflection loss behind source $\sim$ 2.5 %

These losses can be mitigated and transformed into upward diffraction to the photodetector through various methods. The primary source of loss is substrate leakage, which can be addressed by incorporating a Bragg mirror at the substrate or adjusting the buried oxide thickness. However, these two techniques pose challenges in a generic SOI wafer. Apodization of the grating structure could enhance the maximum diffraction of light into the photodetector at the outset, resulting in increased absorption in the photodetector.

2.6.3 Evanescent coupled PD

The evanescent coupling mechanism is illustrated in Figure 2.10. This includes the cross-section, top view and longitudinal section of the SOI wafer presented in Figure 2.10 (a, b and c), respectively. As mentioned earlier, the silicon patterns are created by etching a 5 μm wide trench to a depth of 300 nm around the waveguide and taper regions. As schematically depicted in Figure 2.10 (d), the photodetectors are printed near the silicon taper end, covering the trench section with the simulated intensity profile given in Figure 2.10 (e).

Simulations indicate that nearly 94 % of the light is coupled from the silicon waveguide to the PD, with additional losses such as,

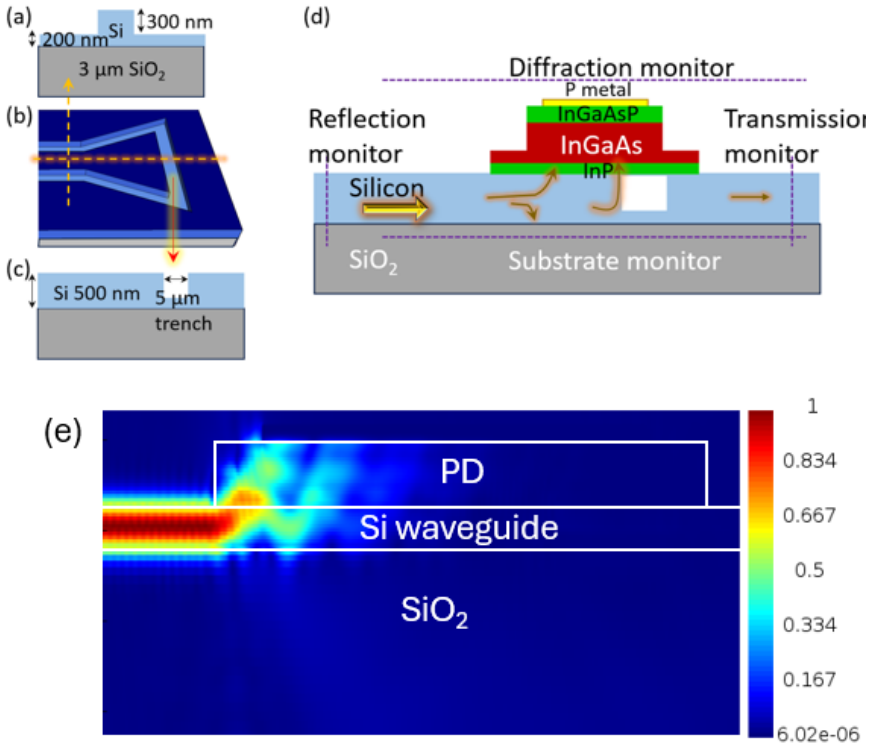


FIGURE 2.10: Light distribution from the Si waveguide to the evanescent-coupled InGaAs detector, as determined by FDTD simulations.(a) Cross-sectional view across rib-etched silicon waveguide, (b) Top view of the silicon waveguide with a tapering end, displaying trench etch around the patterns, (c) Longitudinal section along the waveguide, taper and trench, (d) Schematic diagram of longitudinally sectioned evanescently coupled photodetectors illustrating the mode propagation from the silicon waveguide to the photodetector and (e) Simulated intensity profile showing substrate leakage in light blue shade beneath the silicon waveguide.

Substrate leakage loss ~ 0.3 %

Upward diffraction loss ~ 0.15 %

Transmission loss is negligible Total reflection loss behind source is negligible

2.6.4 Summary of simulations

The summary of above simulations are provided in Table 2.1. We evidently see that percentage of light coupled is increasing from butt coupling to grating coupling with highest in evanescent coupled PD.

TABLE 2.1: Simulation summary of light coupled to photodetector for different coupling mechanisms, with prominent reason for loss and with solutions to reduce loss.

Method of coupling	**Light coupled**	**Reason for loss**	**Solutions**
Co-planar	40 %	Interface reflections	Smooth index transition
Grating	62 %	Substrate leakage	GC apodization [49]
Evanescent	94 %	Transmission	Taper down design [47]

The majority of loss in co-planar butt coupling stems at the interface, when the mode transition from the waveguide to the PD. This occurs because the mode encounters numerous interfaces and at each transition in refractive index, the mode experiences scattering and reflection. One potential solution to overcome this challenge is to fill the gap with a index matching material.

In the case of grating coupling, as mentioned earlier, the dominant source of loss is substrate leakage. This issue can be addressed by optimizing the patterning of the grating pitch to minimize leakage.

On the other hand, evanescent coupling already demonstrates satisfactory performance. However, there is still some light that remains unabsorbed by the PD and is transmitted. This issue can be mitigated by properly tapering down the silicon, thereby enabling maximum mode coupling to the PD.

2.7 Co-planar infill process

Having covered simulations, this section talks about the process optimizations, focusing solely on co-planar butt coupling. This decision is because, grating and evanescent coupled PD does not involve much processing except for establishing bond pads. However, for co-planar coupling, after establishing bond pads, our objective was to fill the gap with a similar refractive index material of amorphous silicon. As a result, various trials of in-fills were conducted in advance using dummy silicon samples. This involved etching long, narrow trenches in the samples and attempting to fill them with amorphous silicon. The deposition of a-Si was conducted using Plasma Enhanced Chemical Vapour Deposition (PECVD) and an evaporator, followed by various planarization techniques, which will be elaborated upon shortly. Subsequently, the optical characterization of the a-Si film was performed to determine its refractive index and absorption properties.

2.7.1 Method of deposition

To deposit the amorphous silicon film, we utilized etched patterns in dummy silicon wafers and tested two different deposition methods: plasma-enhanced chemical vapor deposition (PECVD) and evaporation.

150 nm of a-Si is deposited by PECVD on a patterned silicon sample, where the chamber is maintained at a temperature of 200 $°C$ and involves Argon (43 sccm) and Silane SiH_4 (58 sccm) gases generating a deposition rate of 5.6 nm/s. The deposited samples are cleaved across the trenches to visualize the film quality. The cross-section image in Figure 2.11 (a and b), shows 150 nm of not smooth a-Si deposited on trench sidewalls. This porosity would lead to loss of optical mode while propagation through the voids present in the film due to scattering and dispersion. It is possible to get a smoother a-Si film by optimizing the PECVD process.

Second method of evaporation of a-Si was carried out using Leybold Optics-Syrus Pro 710 evaporator. Here lanthanum and tungsten boats were used and the process was carried out in a chamber with temperature starting at 20 $°C$ and reaching a maximum of 80 $°C$, evaporating a-Si at a rate of 0.2 nm/s. The SEM cross section image in Figure 2.11 (c) reveals a highly smooth evaporated a-Si on trench sidewalls.

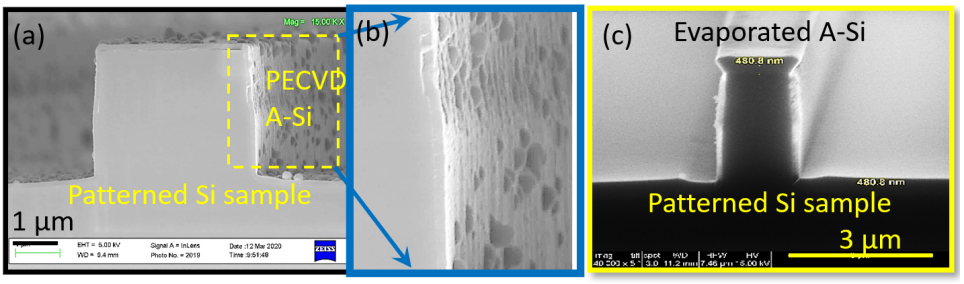


FIGURE 2.11: SEM cross-section images showing a-Si on sidewalls of trenches (a) By PECVD deposition technique (b) Zoom-in image of sidewalls showing porous a-Si and (c) Smooth film of evaporated a-Si.

Comparing above two techniques, evaporated a-Si is better than PECVD for two reasons. Primarily, although evaporated a-Si has lower deposition rate (leading to longer process time), it has desired film quality expected for low loss mode propagation. Second reason is related to process temperature of 200 $°C$ in PECVD, as thermal cross-linking happens in photoresist above 140 $°C$, which hardens the resist making it difficult to strip from the sample. Hence evaporation is preferred as it is a low temperature process and straightforward to deal with photoresist.

2.7.2 Planarization of evaporated a-Si

In actual device processing, it is preferable to retain a-Si only in desired areas while removing it from other parts of the sample. This removal process can be achieved through two methods: chemical mechanical planarization technique (CMP) or photoresist lift-off technique.

CMP is CMOS compatible process and it is executed using a series of steps as shown in Figure 2.12 (a), a 400 nm of a-Si is evaporated over trench etched in silicon sample. The evaporated sample is polished using slurry in CMP tool, since it is mechanical method, it is non-selective between a-Si and silicon sample, it smoothen both the materials. Further, it is difficult to control the extent of etch precisely as there is no way of monitoring the thickness planarized. This leads to the danger of flattening the actual III-V material. Thus the optimization process is challenging, we proceeded with photoresist lift-off technique as discussed below as it was repeatable.

For photoresist lift-off technique, bi-layer resists were used on silicon sample, starting with lift-off resist (LOR) PMGI SF11 spin followed by lithography resist S1813 as shown in Figure 2.12 (b.1). On lithographic exposure S1813 gets developed only in exposed region, whereas LOR

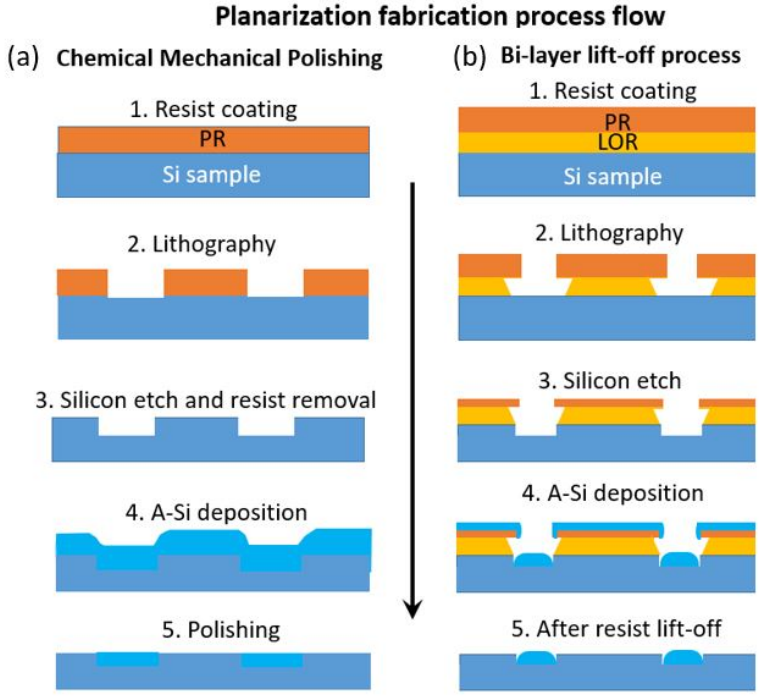


FIGURE 2.12: Schematic of fabrication process flow for selective removal of a-Si (a) Through chemical mechanical polishing and (b) Bi-layer photoresist lift-off technique.

can develop laterally to get an undercut profile, even in unexposed parts as shown in Figure

2.12 (b.2). Then exposed Si is etched using Cl_2 (20 sccm) and N_2 (40 sccm) creating trenches, followed by evaporation of a-Si as in Figure 2.12 (b.3 and b.4). The LOR's re-entrant profile ensures discontinuity of evaporated film. Finally, the planarization is achieved by stripping the resist using microposit 1165, which removes the a-Si as well on top of the resists on areas other than the trench as expected (Figure 2.12 b.5). **Analysis**: SEM cross section of the lift-off sample reveals a wavy pattern along trench edges and consisting of four regions as illustrated in Figure 2.13 (a and b) and details are explained below.

1. Non-vertical Si etch: The sidewalls of trench are slanted as they take the slope of photoresist on top while etching. A vertical Si etch can be obtained by transferring the etch from resist to oxide first and the from oxide to silicon (Figure 2.13 b, bottom right of image, numbered 1).

2. Extra lateral etch: Apart from the trench, Si surface was etched, along the sides of the trench (Figure 2.13 b, top right of image, numbered 2). Generally all areas are protected with resist, these sides are the regions of undercut area of lift-off resist. This can be prevented by reducing development time during lithography process, which leads to less undercut and lower lateral etch in silicon.

3. Side bump: A-Si evaporation generates a bump along the sides of trench in lateral etched area. Again this can be averted by stopping extra lateral etch (Figure 2.13 b, top of image, numbered 3).

4. Evaporation profile: A-Si has a slanted profile, which is inherent to evaporation via lift-off technique (Figure 2.13 b, numbered 4).

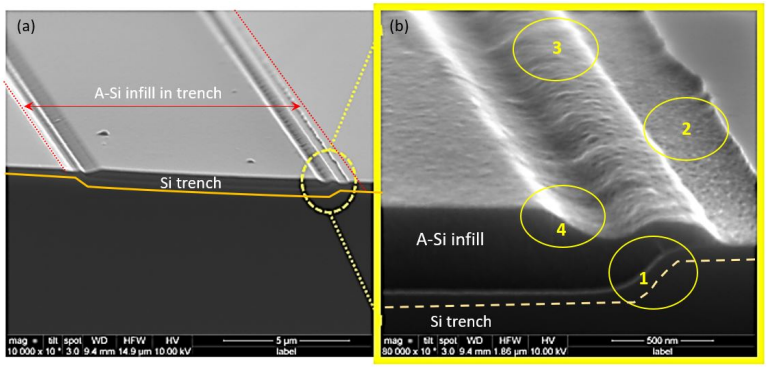


FIGURE 2.13: (a) Cross section SEM image showing a-Si infill in a trench and (b) Zoom-in image showing wavy edges slanted etch profile and slanted a-Si evaporation.

2.7.3 Refining the planarization process

This section details the additional steps incorporated into the lift-off process to address the previously discussed issues. The revised process begins with a thin 220 nm oxide deposition, as shown in Figure 2.14 (a). This is followed by a lithography process with a reduced development time, resulting in less undercutting, as seen in Figure 2.14 (b) and the corresponding SEM image in Figure 2.15 (a). Next, the exposed region undergoes an oxide etch using C_4F_8 (10 sccm) and H_2 (15 sccm) and He (175 sccm), as shown in Figure 2.14 (c). More details on etch rates for different gas ratios are provided in Appendix Table A.3. This is followed by a 400 nm silicon etch using SF_6 (75 sccm) and C_4F_8 (55 sccm), leading to a vertical Si sidewall profile, as depicted in Figure 2.14 (d) and in the SEM image in Figure 2.15 (b), due to the transfer of the etch profile from the SiO_2 on top [57]. Now since the silicon etch is over, sample can be safely developed more to generate undercut required for the lift-off process (Figure 2.14 e). This is followed by a buffered oxide etch (BOE) to selectively etch the thin oxide (Figure 2.14 f). Doing this process at this stage, the lateral side etch is also prevented and a desired undercut profile is also created for proper lift-off. Finally 400 nm thick a-silicon is evaporated in the trench (Figure 2.14 g) and the process is completed by lifting off the photoresist (Figure 2.14 h) with the SEM image in Figure 2.15 (c).

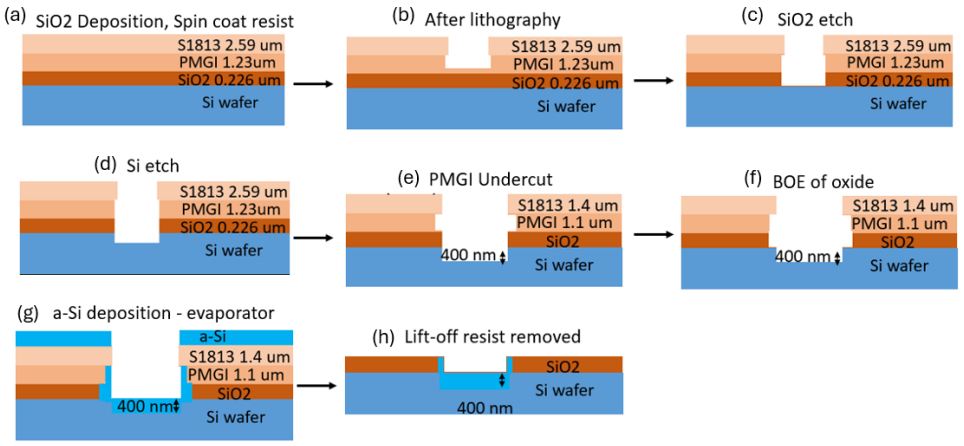


FIGURE 2.14: Modified schematic of fabrication process flow for planarization of lift-off process. (a) Oxide deposition and bi-layer resist spin coating, (b) Partially undercut of photoresist, (c) oxide etch, (d) followed by silicon etch, (e) complete undercut of photoresist, (f) wet etch to remove oxide laterally, (g) evaporation of a-silicon and (h) photoresist lift-off process.

Analysis: The wavy pattern has been resolved successfully due to the modifications in process flow but in this run 'rabbit ear' pattern was observed on trench sides. It is due to resist hardening from SF_6 based plasma used in oxide and Si etches [58], which was removed by sonicating the sample in microposit 1165 for 45 minutes and followed by peeling off a sticky

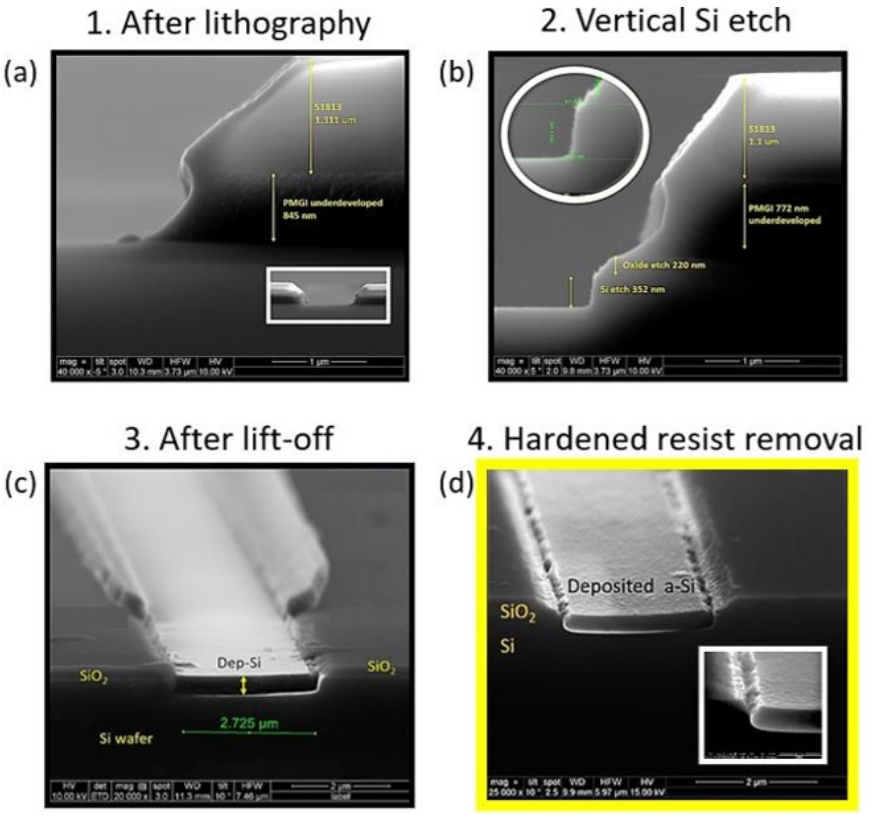


FIGURE 2.15: Cross section SEM images (a) After bi-layer lithography showing s1813 photoresist with sloped sidewall and partially undercut PMGI resist beneath it, (b) Dry etching of thin oxide, followed by silicon, inset showing vertical etch in silicon, (c) a-Si infill in a trench, after lift-off, with 'rabbit ear' structure on either side due to resist hardening and (d) Final image after sonication to remove those rabbit ears, with zoom-in image showing slanted a-Si evaporation.

tape on the sample as seen in Figure 2.15 (d). However, using sticky tape is not a permanent solution.

2.7.4 Characterization of evaporated a-Si

The quality of a-Si film is analyzed using atomic force microscopy (AFM), Raman and Infra-Red (IR) spectrometer and ellipsometer as discussed below.

The film smoothness is measured over 10 μm × 10 μm using Bruker AFM, which gives an RMS roughness of 0.5 nm before evaporation and 0.4 nm after, for 450 nm of a-Si evaporation evaporated on glass substrate as pictured in Figure 2.16 (a and b). There is change in roughness as desired.

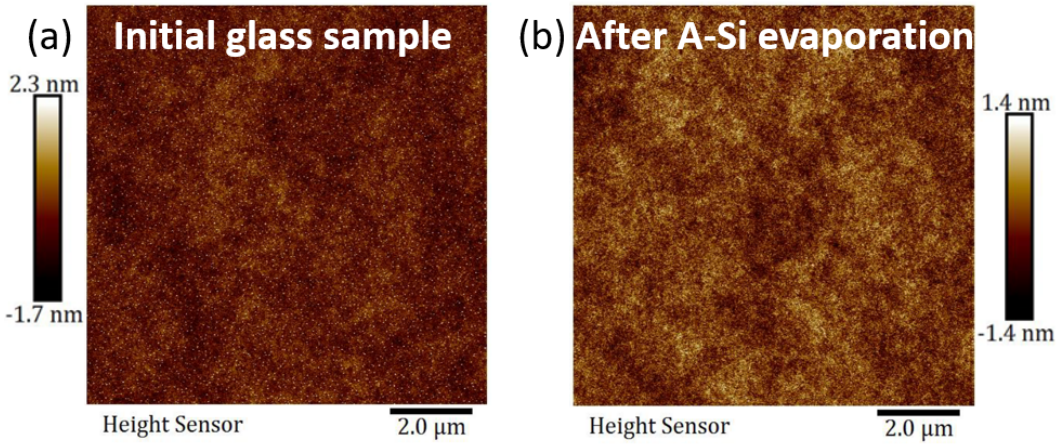


FIGURE 2.16: AFM roughness for 450 nm a-Si on glass substrate (a) Before evaporation and (b) After a-Si evaporation.

Raman measurements were carried out using Renishaw inVia microscope to observe fingerprints of Si-H bonds. Figure 2.18 (a) gives Raman measurement result showing low intensity peaks for Si-H bond, signifying lower absorption at infrared wavelengths [59] and [60].

IR measurements are done with light propagating from air to 450 nm of a-Si evaporated on glass substrate. At infra-red range, reflection and transmission measurement for a 450 nm thick evaporated a-Si were carried out using Perkin-Elmer 950 spectrometer whose results are shown in Figure 2.18 (b). It is observed that at 1310 nm around 70 % of the light is transmitted with a low absorption. The reflection is 30 % as the light faces a large change in refractive index. The refractive index of a-Si can be estimated from Fresnel equation as given in Equation 2.7 for perpendicular incident of light (Figure 2.17).

$$R = \left|\frac{n_1 Cos\theta_i - n_2 Cos\theta_t}{n_1 Cos\theta_i + n_2 Cos\theta_t}\right|^2 \tag{2.7}$$

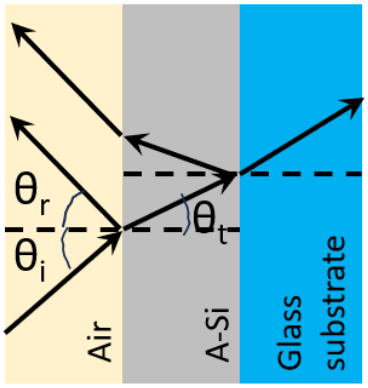


FIGURE 2.17: Schematic showing reflection and transmission in thin film at each interface.

where R is reflection percentage, n_1 is refractive index of the first medium (air) and n_2 is refractive index of second medium (a-Si). Knowing R to be 30 % and n_1 to be 1, refractive index of evaporated a-Si film comes out to be $\sim$ 2.9. And in actual device case, the light would be propagating from silicon waveguide to a-Si in-fill as shown earlier in Figure 2.7 (a). In that situation, refractive index of silicon is 3.45 and a-Si is 2.9, which leads to a reflection as low as 8 %. Thus with low absorption and reflection, majority around 90 % of light is expected to get transmitted after a-Si film in real device scenario. All the above experiments were done without Argon plasma during evaporation.

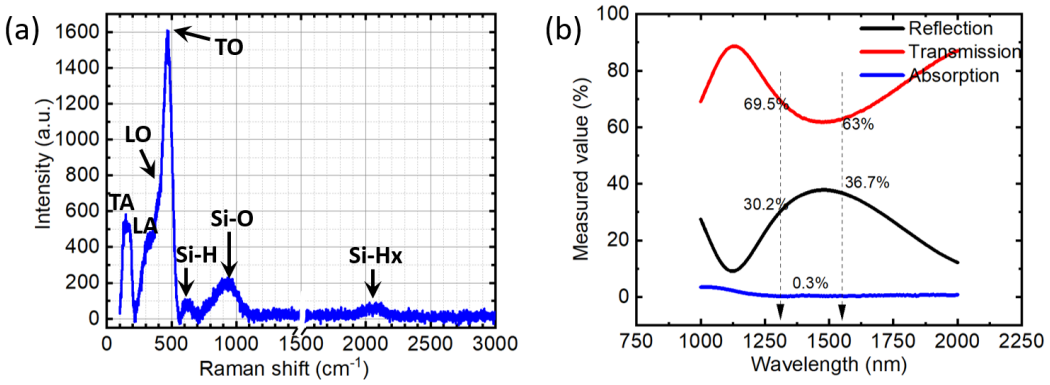


FIGURE 2.18: (a) Raman spectra showing Si-H footprints and (b) IR spectrometer measurement plot from air to a-Si incidence showing least film absorption.

To compare the quality of the films, two samples of a-Si with the same thickness were evaporated. One sample was evaporated without an ion beam, and the other using Argon plasma in Advanced Plasma Sources (APS). The refractive index (n) and extinction coefficient (k) of the films were measured using an ellipsometer.

The absorption coefficient (Alpha) is calculated from extinction coefficient as shown in Equation 2.8. The variation of the refractive index and absorption coefficient with wavelength is plotted in Figure 2.19 (a, b and c) respectively. Absorption depends on film thickness and wavelength of operation. For ellipsometer measurements, when 450 nm thick films were used, there were interference oscillations for which the fit was poor with high error value and had difficulty in obtaining the refractive index. Hence a lower thickness of 70 nm evaporated films is engaged for this measurement alone.

$$Alpha = \frac{4\pi k}{\lambda} \tag{2.8}$$

It is observed that plasma-based evaporation of a-Si films results in a higher refractive index and slightly increased loss, attributed to film densification during the plasma-based evaporation process. Thus evaporated a-Si films without ion beam was used further in this thesis and for

which we obtain a refractive index $\sim$ 3.1 in the telecom range which matches with value deduced from infra-red spectrometer measurement (2.9). This is comparable with literature [61], refractive index of 2.9 is measured for substrate temperature of 100 $°C$ using electron beam evaporation method. From Figure 2.19 (b and c) it can be noted that the absorption coefficient of a-Si is nearly 2000 cm^{-1} at 1550 nm. The light propagating through 1 μm of this amorphous silicon would result in an absorption loss of 18 % at 1550 nm.

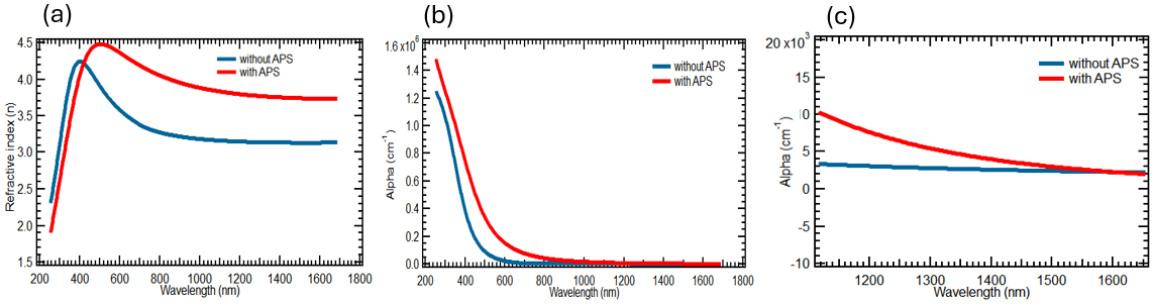


FIGURE 2.19: Ellipsometer data comparing films with and without Argon plasma during evaporation are presented as follows: (a) Refractive index, (b) Absorption coefficient (Alpha) plotted across all wavelengths, and (c) a zoomed-in plot showing loss in the telecom region.

2.8 Conclusion and discussion

This chapter discussed three different coupling mechanisms for transfer printed III-V photodetector on SOI with their simulation showing absorption to PD and interface loss and process optimization for co-planar in-fill with a-Si.

The grating coupler mechanism is detailed, achieving $\sim$ 66 % coupling which can be further improved by reducing substrate leakage. Evanescent coupling is approached specifically without using the conventional taper down technique. This was possible due to trench present in silicon, which scatters the mode upwards to the III-V device. Followed by experimental details of co-planar in-fill technique with details on evaporation and ways of planarization. A-Si film is characterized and found to be very smooth with RMS roughness value of 0.4 nm over 10 $\mu m \times$ 10 μm.

Overall learning is that in-fill techniques play a crucial role in maximizing optical coupling. However, butt coupling approach involves lot of challenges as shown, and we have overcome some. If all these are optimized, it could potentially achieve up to 98 % power coupling. The grating coupling and evanescent coupling of PD to silicon, was the easiest to realize as it required no special processing on the SOI as in butt-coupled approach.

However, grating couplers are inherently sensitive to wavelength and polarization which is a drawback. For instance, even if the transfer printed photodetector can detect wide range of wavelengths, this sensitivity of GC would limit its functions to specific range supported by grating coupler input. And also, there is a significant substrate leakage of coupled input light, which could be mitigated through grating teeth apodization. This helps in reducing the mismatch between scattering intensity distribution from the GC and Gaussian distribution of coupled fiber [62].

The evanescent approach, although has the least loss, would benefit from a taper down design in silicon. Each coupling approach requires a specific design for optimal performance in responsivity and bandwidth of the transfer printed PD. The final choice depends on the intended application and compatibility of the process with other devices in the photonic integrated circuit.

Chapter 3

Dual sacrificial layer for transfer printing

3.1 Introduction

In transfer printing, the coupon is detached from the source wafer by wet etching the sacrificial layer, which links the III-V substrate to the coupon. Until now, either indium gallium arsenide (InGaAs) or aluminium indium arsenide (AlInAs) has served as the sacrificial layer for InP-based devices [63]. The InGaAs sacrificial layer produces a smooth coupon interface post-release, but its anisotropic etching behavior with $FeCl_3$ wet etchant presents challenges. InGaAs exhibits faster etching along <010> lattice planes, at a 45° angle to the major axis, compared to those parallel or perpendicular to it. Consequently, coupons must align along the <010> plane to accelerate undercutting. However, this requirement limits optimal wafer space usage and complicates lithographic processes. Additionally, the slow etch rate results in increased vertical etching of InP, with a InGaAs/InP selectivity of 735 [64]. This vertical etching creates a dish-like profile, unfavourable for transfer printing and causing loss of InP epitaxial material.

Compared to InGaAs, the AlInAs sacrificial layer offers nearly isotropic and faster etching with $FeCl_3$ wet etchant [65]. However, interface roughness observed in coupons from epitaxial growths conducted at Tyndall's MOCVD poses a challenge. This roughness hampers the adhesion of the coupon to the target surface during transfer printing, thereby decreasing the print yield.

To address the above mentioned challenges, this chapter proposes a novel dual sacrificial layer approach instead of individual sacrificial layers of AlInAs or InGaAs. It combines InGaAs release layer on top of AlInAs release layer, benefiting on the advantageous properties of each layer. This combination enables isotropic coupon release, faster etch rates and improved selectivity to InP compared to individual layers, along with smooth coupon interface, with the reasons detailed further in the chapter. Notably, these benefits are achieved at room temperature thereby saving time, cost and energy, unlike the lower temperatures required for undercutting with individual release layers. All the wet etch experiments are conducted at room temperature in this chapter, unless otherwise specified. Experiments are conducted to determine the optimal thicknesses of InGaAs and AlInAs. Additionally, it is shown for the first time that a more diluted mixture of ferric chloride to water (1:5) exhibits a more linear etch rate and higher selectivity to InP, surpassing the regularly used 1:2 dilution ratio.

3.1.1 Review of etchant for InGaAs and AlInAs

Numerous studies have investigated wet etching of InGaAs and AlInAs using diverse etchants. A comprehensive overview of InGaAs etch rates along <001> and <011> planes, emphasizing their selectivity to InP is listed in [66]. A compilation of list of wet etchants, including hydrofluoric acid, hydrochloric acid, citric acid, ferric chloride and succinic acid, detailing etch rates, selectivity and stopping layers are provided in [67]. An extensive collection of literature on wet etchants used for III-V semiconductors up to 2000 is offered in [68]. Etch rates and planes for InGaAs/InP and AlInAs/InP heterostructures wet etched using sulphuric-hydrogen peroxide and phosphoric-hydrogen peroxide mixtures is tabulated in [69]. Highly selective wet etching of InGaAs on InAlAs using an adipic acid – ammonium peroxide mixture is discussed in [70]. Selective wet etching of InGaAs/AlInAs over InP using a succinic acid-hydrogen peroxide mixture is described in [71]. Etching of InGaAs, AlInAs and InP by a citric acid-hydrogen peroxide mixture is recounted in [72].

The etch rate of InGaAs <010> varies across different wet etchants. For instance, in citric-peroxide solution, it is 175 nm/min, in phosphoric peroxide, it is 315 nm/min and in ferric chloride, it peaks at 1330 nm/min. Thus InGaAs exhibits fourfold higher etch rate in ferric chloride than in phosphoric-peroxide and an eight-fold higher etch rate in ferric chloride compared to citric-peroxide mixtures as analyzed in [64]. Among the studies mentioned earlier, it is observed that ferric chloride proves most effective for wet etching of InGaAs and AlInAs

in terms of both etch rate and selectivity over InP. Hence, this chapter delves into the benefits of varying the dilution of the ferric chloride mixture for etching the dual sacrificial layer, comparing its advantages to individual layers.

3.2 Experimental methods

To investigate the consequence of varying thickness and understand the role of InGaAs and AlInAs in dual release layer, four wafers are grown as shown in Table 3.1. These wafers are grown by MOCVD method at Tyndall National Institute. These wafers are grown on (100)-oriented InP substrate, according to European-Japanese standard, with a common top layer of 1 μm thick n-InP. The top surface or working surface of (100) InP wafer is shown in Figure 3.1, with planes perpendicular to it, where [011] is major axis and [01$\bar{1}$] is minor axis. Each wafer consists of lattice matched AlInAs grown on InP substrate and a lattice matched InGaAs grown on top of AlInAs. For easy reference, these wafers are labelled using the following nomenclature, where first number indicates InGaAs thickness and second number shows AlInAs thickness. For instance, W20-500 designates a wafer with a 20 nm InGaAs release layer and a 500 nm AlInAs release layer on the InP substrate. Out of the four grown wafer, two of them have the same AlInAs thickness (W0-500 and W20-500), while the remaining two have identical InGaAs thickness (W400-100 and W400-50).

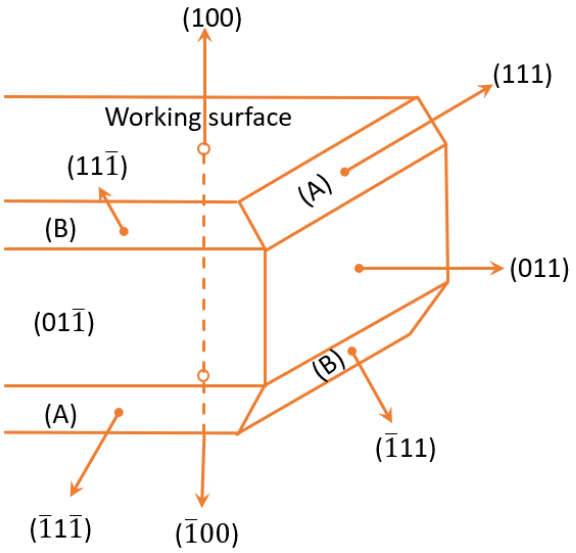


FIGURE 3.1: 3D crystal plane diagram showing relative location of lattice planes in III-V compound semiconductor [73].

Note that all wafers in Table 3.1 are solely compared in interface analysis section, where the influence of InGaAs thickness is tested. This limitation arises because wafer (W0-500) with only AlInAs release layer is no longer available. The AFM data for W0-500 and W20-500 used in interface analysis is from an earlier time, with the sample no longer available for other measurements. Therefore, all other measurements like etch rate, linearity and selectivity is compared between W400-100 and W400-50 wafers, for different etchant dilutions as well.

TABLE 3.1: Variation in thickness of release layers InGaAs and AlInAs.

Epitaxial layers	**W0-500**	**W20-500**	**W400-100**	**W400-50**
InP	1 μm	1 μm	1 μm	1 μm
InGaAs	0 nm	20 nm	400 nm	400 nm
AlInAs	500 nm	500 nm	100 nm	50 nm
InP substrate n doped				

3.2.1 Mask design

The wafers are patterned using a mask design whose full details are provided in appendix Figure A.1. To measure the etch rate along various lattice planes, the mask consists of some wagon wheel structures as shown in Figure 3.2, which will be detailed in this section. Notably, in these wagon wheels, there is an amplification of lateral etch of the wedges due to tip retraction, inherent to their geometric structure [74]. The pattern comprises of numerous wedges forming a circular pattern. Figure 3.2 (a, b and c) are the mask design taken from Klayout, where the purple regions are protected with a hard mask, while white regions are etched to create coupons, enabling wet etchant access from all white regions to undercut the release layer.

Three different wagon wheels are employed in the design, where Figure 3.2 (a), features 72 evenly spaced 5° -wide wedges arranged in a circular fashion, spanning a diameter of 2 mm. This setup allows for simultaneous measurement of etch rates along 72 lattice planes. The widest width of an individual wedge is 67 µm, tapering down to a minimum width of 10 µm near the pattern's center. Additionally, there are circular patterns comprising 12, 30° -wide wedges (Figure 3.2 b) and 8, 45° -wide wedges (Figure 3.2 c), with maximum width $\sim$ 500 μm to narrowest width near center $\sim$ 100 μm. Patterns in Figure 3.2 (b and c) are designed to endure longer etch duration, as the wheel with 72 wedges will float away first due to their smaller width, preventing measurement of undercut.

These mask designs are transferred to wafers using lithography and etching techniques as discussed in further sections (Figure 3.3). Before immersion in the wet etchant, the wagon wheel without any undercut is depicted in Figure 3.2 (d), where the green region represents the hard mask and the background is the etched region. Upon immersion in the dilute ferric chloride wet etchant, it undercuts the release layer. During undercutting, the lattice planes perpendicular to the starting faces are etched. The etch length is measured using a microscope, starting from the outer boundary of the wedge to the inner black line created by the absence of material during undercut, as marked in Figure 3.2 (e). For instance, the etch length noted for 0° or [011] in graphs indicates the amount of etch in the plane perpendicular to the major axis, as depicted in Figure 3.2 (f). These etch length or undercut measurements have an error of ± 2 μm as shown in appendix Figure A.2 comparing microscope and SEM undercut measurement.

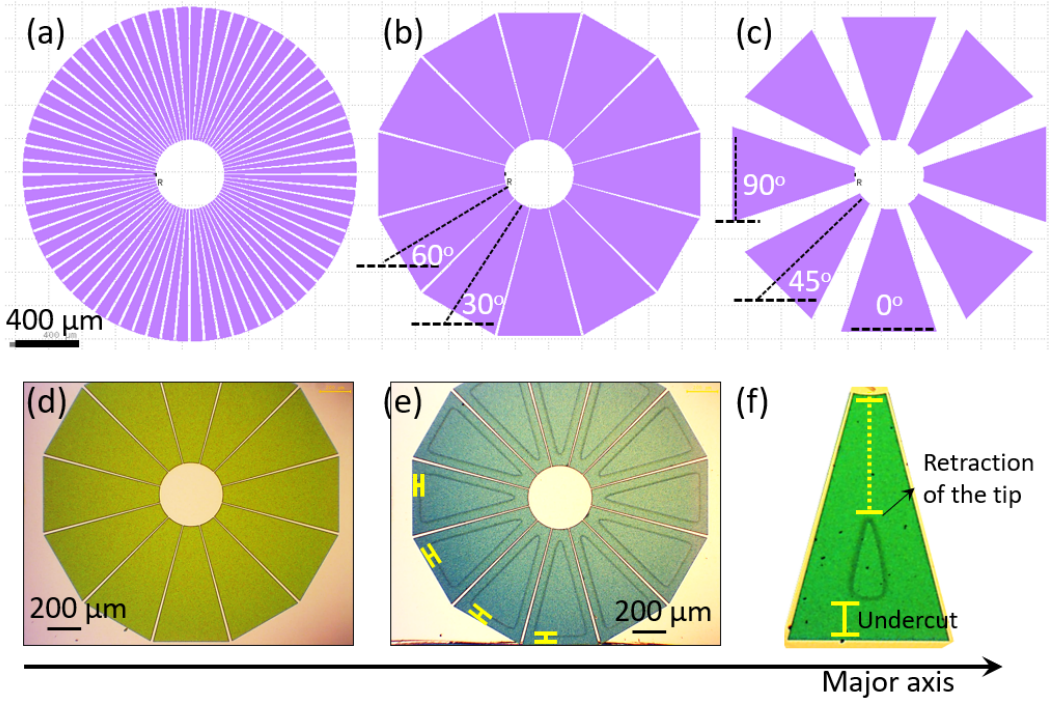


FIGURE 3.2: Wagon wheel mask design (a) Wheel with 72 wedges spaced at 5°, (b) Wheel with 12 wedges spaced at 30° and (c) Wheel with 8 wedges spaced at 45°. These wagon wheel design are patterned on wafers: (d) Unreleased 12 wedge wheel, (e) Partly released wheel, showing undercut and (f) Zoom in of a wedge showing retraction of the tip.

3.2.2 Process to measure undercut

It is crucial to quantify the extent of undercut in the release layer, by the wet etchant. This undercut measurement can be carried out through two methods, either a top view using a microscope or a cross-sectional view in a scanning electron microscope (SEM). While SEM

provides more accurate and precise measurements, it poses challenges in cleaving expensive samples for each measurement, especially in achieving a smooth cleave along all lattice planes. Therefore, microscopy is predominantly employed in this study to measure the length of the undercut. However, the presence of tethers on top of coupons obstructs microscope observations, as the photoresist absorbs visible light. Consequently, coupons without tethers are utilized for microscope observations, as illustrated in Figure 3.3. These coupons are intentionally partly undercut for analysis purposes, as a complete undercut would cause the coupon to float off the substrate in the wet etchant, given the absence of tethers.

A schematic process flow for the fabrication of coupons to measure undercut is shown in Figure 3.3. Beginning with the dual release layer in the epitaxial stack (Figure 3.3 a), a thin layer of dielectric material (silicon nitride) is deposited, serving as a hardmask (Figure 3.3 b). Subsequently, the epitaxial stack is patterned and etched through the release layer and 200 nm of substrate, resulting in the formation of the coupon (Figure 3.3 c). This step also exposes the release layer, which is then removed through a wet etch process, utilizing diluted ferric chloride at room temperature. Due to the faster etch rate of AlInAs compared to InGaAs [65], AlInAs is etched more rapidly, providing access to InGaAs from beneath, as depicted in Figure 3.3 (d). Subsequently, these coupons are withdrawn from the etchant after a partial undercut and their etch lengths are measured using a microscope for various observations.

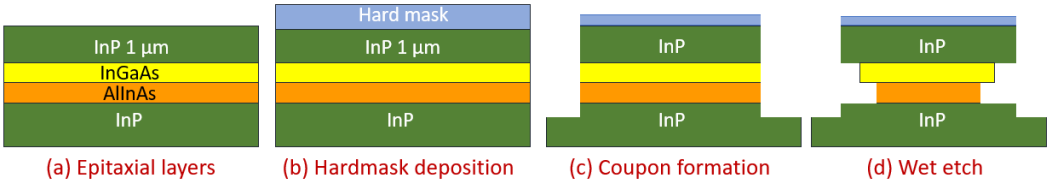


FIGURE 3.3: Schematic cross-section of fabrication process flow (a) Starting epitaxial stack, (b) Dielectric deposition, (c) Coupon etch till substrate and (d) Wet etch showing faster AlInAs lateral etch than InGaAs.

3.2.3 Process to measure interface

Microscope observations provide information solely about the undercut and do not offer details about the coupon interface, which is underside of the coupon, interface (of release) with InP. For interface analysis, complete undercutting of the sacrificial layers is necessary, requiring tethers to hold the coupons after removing the release layers. Similar fabrication steps to Figure 3.3 are followed until the coupon formation stage. Subsequently, photoresist tethers are established, as depicted in Figure 3.4 (d). The next step involves the complete removal of the dual release

layer through wet etching with dilute ferric chloride and water mixture (Figure 3.4 e). A scotch tape is then placed on top of the released coupons and pulled, as shown in Figure 3.4 (f). The manually applied force breaks the tethers connecting the coupon to the substrate, causing the coupons to adhere to the tape and exposing the interface, as demonstrated in Figure 3.4 (g), for further measurements. The surfaces of these completely released coupons are then utilized for all surface analyses, including SEM, AFM and Raman spectroscopy Figure 3.4 (h).

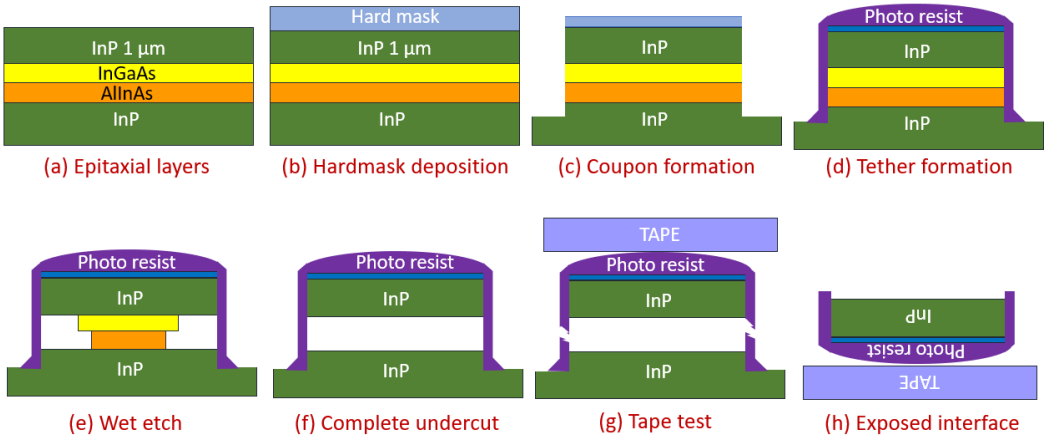


FIGURE 3.4: Cross section schematic of fabrication process flow for interface analysis (a) Starting epitaxial stack, (b) Dielectric deposition, (c) Coupon etch till substrate, (d) Tether formation, (e) Coupon undercut in process, shown with partial release of sacrificial layers, (f) Completely released coupon, (g) After complete undercut, coupon is pulled out using a tape by breaking tether and (h) Adhered coupons to tape revealing coupon interface for further analysis.

Following processing, each wafer is cleaved into smaller pieces for further experimentation. As a result, the cleaved samples exhibit different patterns exposing various lattice planes. For instance, some samples gets wagon wheel patterns with 12 wedges, exposing 0°, 30°, 60° and 90° planes, while other sample consist of wagon wheel patterns with 8 wedges, with 0°, 45° and 90° planes. Consequently, certain graphs in the results section may lack data points for specific angles due to variations in the patterns across cleaved samples.

3.3 Results and discussion

It is important to consider in wet etching whether the process is diffusion-limited or reaction-limited. The rate of a diffusion-limited process is determined by the speed of etchant transport, while the rate of a reaction-limited process depends on the speed at which the components react. Adequate agitation facilitates the movement of the etchant into the surface, increasing the etch rate in the case of a diffusion-limited process. Conversely, agitation has no impact

on the etch rate in a reaction-limited process. The impact of agitation is evaluated at room temperature using a ferric chloride and water mixture (1:2) on W400-100 samples. This involves undercutting one piece of the sample with agitation and leaving another sample without agitation (still) for 20 minutes.

The sample is agitated using a magnetic stirrer set to 380 revolutions per minute. Figure 3.5 compares the etch lengths between still and agitated samples, measured for different lattice planes. Two observations are made: firstly, there is no significant difference in etch lengths among different lattice planes, indicating nearly isotropic etching for W400-100 sample. Secondly, overlapping measurements for agitated and non-agitated samples, within the error bar, suggest that this is a reaction-limited process, where the rate of component reaction takes precedence and agitation does not influence the etch rate.

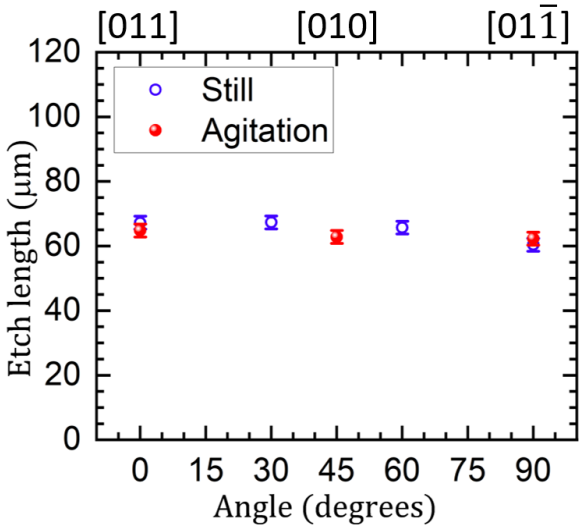


FIGURE 3.5: Plot showing etch lengths with and without agitation for 20 min in different directions related to major axis <011> as 0°. Showing undercut process is reaction-limited and independent of agitation.

3.3.1 Analysis of ferric chloride dilutions

To date, our undercut process for micro-transfer printing has utilized a 1:2 mixture of ferric chloride and water, as documented in previous studies [75, 76]. Here, five distinct dilutions of ferric chloride is experimented, at room temperature using a W400-100 wafer, with coupons released over a 20-minute period.

Etch rates are plotted in μm per minute, representing the amount of release material that is undercut (etch length), within a specific duration of wet etching. The results are shown in

Figure 3.6, exhibiting slightly varying etch rates across different crystal planes. Surprisingly, it is observed that both the 1:2 and 1:5 dilutions of ferric chloride and water yield comparable etch rates across all crystal planes. Despite the higher water content in the 1:5 mixture, it is observed to have the same etch rate as that of the 1:2 ratio. This indicates that ferric chloride saturates in 1:2 mixture. Doubling the water content from 1:5 to 1:10 and similarly from 1:10 to 1:20 results in a halving of the etch rates.

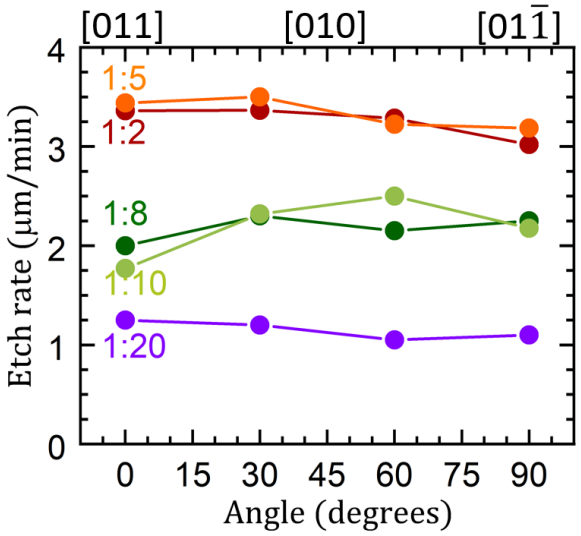


FIGURE 3.6: Variation in etch rate along different crystal planes are presented for varying dilutions of ferric chloride and water.

For a deeper understanding of the behaviour of ferric chloride, the paper by Flynn et al. [77] offers a detailed analysis of the hydrolysis and precipitation of Fe(III) from aqueous solutions of its inorganic salts, including nitrate, perchlorate, chloride and sulfate. The calculated pH levels for the ferric chloride mixtures employed in our study are 0.97 for the 1:2 ($FeCl_3 : H_2O$) solution and 1.12 for the 1:5 solution. These values fall within the same range of dissolved Fe(III) concentrations as reported in [77]. Hence, we understand that although the 1:2 mixture appears to contain more ferric chloride, its low pH causes saturation in the solution. Consequently, the amount of active or unsaturated ferric chloride might be expected to be similar in both the 1:2 and 1:5 mixtures.

As a result, there is negligible disparity in the etch rate between the 1:2 and 1:5 solutions. Given the similarity in etch rates between these two dilutions, a comparison is made in further experiments, between 1:2 and 1:5 mixture, on characteristics such as linearity, selectivity and crystalline axis dependence. If proven that these properties are comparable in both the 1:2 and 1:5 dilutions of ferric chloride, it would be preferable to utilize the more diluted 1:5 solution for

releasing coupons. Not only it is better for the personal safety but it also reduces unnecessary chemical wastage into the environment.

3.3.2 Etch characterization

This section explains how the dual release layer is more effective with higher etch rates compared to individual release layers from other works. A discussion of the various etch rates involved, resulting from the combination of InGaAs and AlInAs layers, thereby enhancing the speed of etching is presented. All measurements are solely reported at room temperature, as satisfactory results were achieved compared to earlier works. Hence, exploration of undercut processes at lower or higher temperatures was not pursued.

Etch rates are measured for wafers with different thicknesses of dual release layers and compared with reported values from earlier works in Table 3.2. These etches are conducted at room temperature for 10 minutes using a 1:2 dilution of ferric chloride and water. It was observed that the etch rate for AlInAs is more than double that of InGaAs [65]. However, when the thickness of InGaAs is increased to 400 nm in W400-100 and W400-50, there is a noticeable increase in etch rate to 4.3 μm/min. The provided etch rates are averages of <010>, <011> and <01$\bar{1}$> etch rate values along these lattice planes, as explained in Table 3.3. This provides the individual etch rates along 0°, 45° and 90°, respectively and their averages for the W400-100 and W400-50 wafer.

Overall, two key observations arise from this experiment. Firstly, a dual release layer with a 400 nm thick InGaAs component exhibits thrice higher etch rate than InGaAs and 1.3 times higher than AlInAs individual layers, as detailed in Table 3.2. Moreover, it also achieves more isotropic undercutting, as evidenced by the values tabulated for different lattice planes in Table 3.3. Secondly, it is noted that a change in AlInAs thickness from 100 nm to 50 nm does not affect the etch rate.

TABLE 3.2: Comparison of etch rates (ER) among different release layers, at room temperature for 10 minutes undercut in 1:2 dilution of ferric chloride and water.

Wafers	**Lattice planes**	**ER for 1:2 dilution**
InGaAs [64]	<010>	1.5 μm/min
AlInAs [65]	<011>	3.3 μm/min
W400-100	<010>, <011>, <01$\bar{1}$>	4.3 μm/min
W400-50	<010>, <011>, <01$\bar{1}$>	4.2 μm/min

TABLE 3.3: Etch rates along individual lattice planes are provided for dual release layer of W400-100 and W400-50.

ER along lattice planes	**W400-100**	**W400-50**
<011> 0°	4.36 μm/min	4.0 μm/min
<010> 45°	4.52 μm/min	4.62 μm/min
<01$\bar{1}$> 90°	4.03 μm/min	4.03 μm/min
Average ER	4.30 μm/min	4.22 μm/min

The observed increase in etch rate is attributed to several factors as detailed below. In the case of individual release layers, only the lateral etch rate of either InGaAs or AlInAs is involved. However, in a dual release layer, there is a contribution from three etch rates, as illustrated in the Figure 3.7. There may also be difference in capillary forces, which are difficult to measure. At room temperature, R1 represents the lateral etch rate of AlInAs along <011>, measured at 3.3 μm/min [65], while R2 represents the lateral etch rate of InGaAs along <010>, measured at 1.5 μm/min and R3 denotes the vertical etch rate of InGaAs, measured at 530 nm/min [64]. Though there may be slight differences in temperature and doping between references and this work, it is assumed that R1 > R2 > R3.

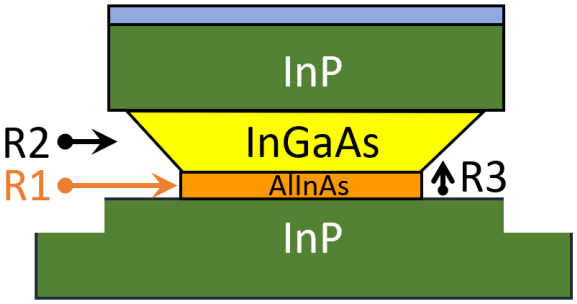


FIGURE 3.7: Schematic cross section of W400-100 wafer, undercut with three etch rates involved. R1 is lateral etch rate of AlInAs (3300 nm/min), R2 is lateral etch rate of InGaAs (1450 nm/min) and R3 is vertical etch rate of InGaAs along <100> is 530 nm/min.

Since the etch rate of AlInAs is twice that of InGaAs and is isotropic, AlInAs begins to laterally undercut more rapidly. Once the AlInAs is etched, InGaAs becomes accessible from beneath along <100>, with the etch rate R3. This faster etching of AlInAs along with vertical etching of InGaAs, is crucial for improving the overall etch rate. Although R3 is relatively small at 530 nm/min, it is more than sufficient for vertical etch as the release layer thickness are in order of hundreds of nanometers, while the coupon dimensions are in tens of micrometers. In the case of W400-100, for instance, 400 nm of InGaAs release layer can be etched vertically in less than a minute, once AlInAs is etched. Thus, having a 100 nm of AlInAs layer below the InGaAs facilitates the ingress of the etchant in the vertical direction, resulting in faster etching of InGaAs, matching that of AlInAs. The combination of all three etch rates results in an overall higher etch rate for dual release layers (W400-100 and W400-50), enabling the rapid release of coupons.

Furthermore, since AlInAs exhibits isotropic lateral etching, which allows for the vertical etching of InGaAs, it overcomes the crystalline dependence of InGaAs, contributing to faster as well as nearly isotropic etching, in dual release wafers (W400-100 and W400-50). With this information, we proceed to investigate the influence of etchant dilutions of 1:2 and 1:5 on the etch rates across different lattice planes (isotropic nature) and examine linearity over various etch duration. These experiments solely utilize wafer W400-100, as it exhibits similar etch rates to W400-50, hence, only one of the wafers is tested.

3.3.2.1 Isotropic nature

In this section a thorough analysis is done to understand if the dual release layer is exhibiting almost isotropic nature, by analyzing multiple lattice planes. This would prove if dual release stack has overcome the anisotropic nature of InGaAs, when used as an individual release layer. For this purpose the wagon wheel design from Figure 3.2 (a), is employed. The W400-100 samples are undercut using 1:2 and 1:5 diluted ferric chloride and water mixture, for 5 minutes at room temperature. The results are depicted in Figure 3.8 (a and b) after undercutting. Etch lengths along all directions are illustrated with error bar of $\pm$ 2 µm.

No particular trend is detected from both graphs regarding slow etching planes, since etch lengths for all lattice planes are in same range. It is observed that the etch length remains consistent across all directions, as evidenced by all data points falling within the error range. Therefore, we conclude that the dual release layer (W400-100) exhibits an almost isotropic

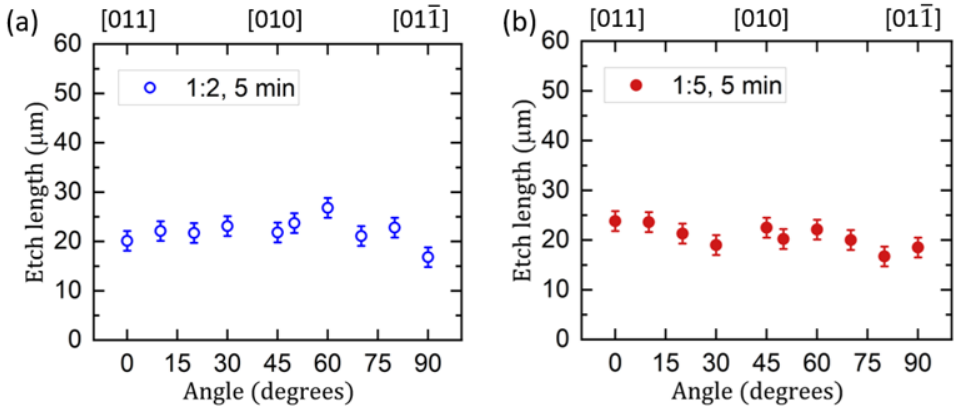


FIGURE 3.8: The measurements are conducted at room temperature on a W400-100 wafer (a) The undercut in a ferric chloride and water solution at a ratio of 1:2 and (b) At a ratio of 1:5.

nature for both ferric chloride dilutions. The same behavior is expected from wafer W400-50 as well.

3.3.2.2 Linearity of etch rate based on dilution

Linearity measurements are conducted to observe the trend in etch rate with an increase in etch duration, providing further insight into the above discussion. Typically, the etch length is expected to gradually decrease over time due to the difficulty in removing the dissolved sacrificial material and accessing underneath of wider coupons. Examining whether the etch length exhibits a linear increase with time is crucial, particularly when undercutting coupons with significantly large dimensions.

This section utilizes only wafer W400-100 throughout, at room temperature, since the etch rate of W400-100 and W400-50 is similar, experiment is done using only one of them, employing ferric chloride dilutions of 1:2 and 1:5. For each time duration and for every dilution (basically for every data point), the etch length is investigated using separate sample pieces from W400-100 and the reason for this choice is explained in appendix Figure A.2. To assess linearity, longer etch duration (up to 4 hours) are required, to ascertain the point at which the etching process reaches saturation. This necessitates the use of large-dimensional coupons to prevent complete undercutting and floating off. In this context, coupons with dimensions of 1 mm width and lengths of 1 mm, 1.5 mm and 2 mm are employed, as illustrated in Figure 3.9 (a and b). The green rectangles represent the coupons from a top view, owing to the dielectric deposited during coupon etching. The black inner boundary indicates the extent of undercut beneath the coupon, measured as etch length from the coupon boundary. As etch duration

increases, the undercut also increases, leading to a corresponding shrinkage of the black inner boundary. This evolution is evident when comparing the etch time of 120 minutes and 233 minutes in Figure 3.9 (a and b) respectively.

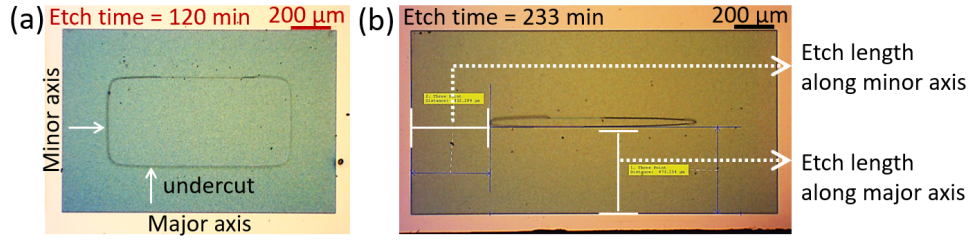


FIGURE 3.9: Rectangular coupons used to measure undercut for etch time of (a) 120 min and (b) 233 min.

For various etch time, etch lengths are plotted for 1:2 and 1:5 dilutions in Figure 3.10 (a and b). The etch lengths are measured from the major axis <011>, utilizing flat planar etch fronts from the large squares and rectangular coupons. Measurements are conducted for increasing etch duration in both the 1:2 and 1:5 dilutions of ferric chloride and water.

As depicted in Figure 3.10 (a), for the initial 20 minutes, the 1:2 dilution exhibits a slightly higher etch rate. However, beyond this point, the 1:5 dilution takes the upper hand, with the difference in the etch length between 1:2 and 1:5 consistently widening. This behavior can be attributed to the occurrence of precipitation in (1:2) mixtures with low pH values, as reported in [77].

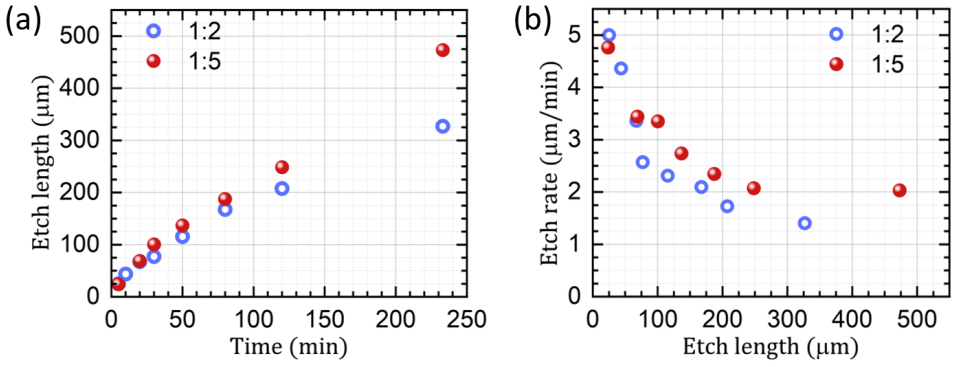


FIGURE 3.10: (a) Linearity of etch length and (b) Change in etch rate for increasing etch lengths along major axis.

Slower saturation of 1:5 is clearly plotted in Figure 3.10 (b), with gradual drop of etch rate compared to 1:2. A noteworthy observation is that, even after an extensive four-hour etching period, both the 1:2 and 1:5 dilutions have not reached the complete saturation stage. The saturation stage is characterized by the point at which the wet etchant becomes saturated with released sacrificial material and when undercut cannot proceed further. In the case of the 1:2

dilution, the undercut distance per side of the coupon stands at 325 μm, while for the 1:5 dilution, it is 475 μm. This substantial undercut distance proves advantageous for releasing wider coupons and thin films (in application required). For example, etch length saturation has been observed beyond one hour itself after undercutting 15 μm, where 20 % hydrofluoric acid is employed to remove 200 nm of SiO_2 sacrificial layer [78].

3.3.2.3 Influence of AlInAs thickness on etch rate

Although we have seen earlier from Table 3.2, that there is not much difference in etch rate due to a change in the AlInAs thickness, this section explores to see if there is any difference in etch rate with longer etch duration as shown in Figure 3.11. For this experiment wafer

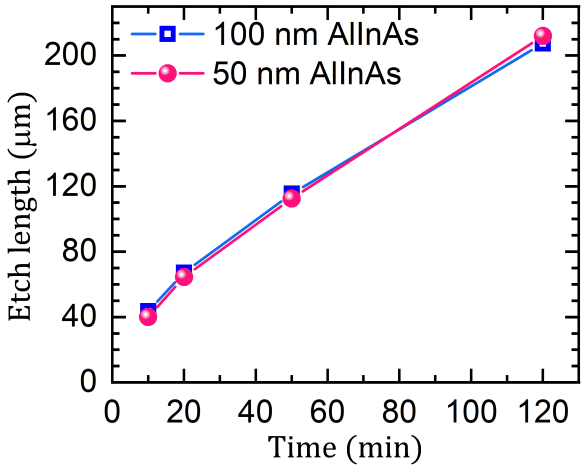


FIGURE 3.11: Relationship between etch length and time is plotted for dual release layer with 400nm InGaAs and varying 50 and 100 nm AlInAs thickness at room temperature using diluted ferric chloride (1:2).

W400-100 and W400-50 is employed with fixed 400 nm InGaAs release layer with 100 nm and 50 nm AlInAs release layer respectively. Linearity measurements are performed using a diluted ferric chloride solution (1:2) at room temperature. As depicted in Figure 3.11, both thicknesses exhibit similar behavior, displaying identical etch lengths at specific etch duration and following the same linearity trend. While a lower thickness of AlInAs might theoretically impact stiction related to surface tension and wetting properties of the liquid, this experiment demonstrates that reducing AlInAs thickness from 100 nm to 50 nm does not introduce a difference in capillary action on the wet etchant.

3.3.2.4 Slow etching planes

Until now, the sample has been examined under a microscope to measure etch lengths after the undercut process. However, in this section, the samples are cleaved to observe the cross-section in SEM. This allows for the examination of the evolution of undercut in the release layers and the observation of the angle of slow etching planes in both InGaAs and AlInAs.

Various literature discusses the anisotropic nature of wet etching in III-V semiconductors. It arises from variations in the density of dangling electrons across crystal planes. The (111) planes are characterized by the highest atom density exhibit slower etching rates. The (111)A planes featuring group III surface atoms etch more slowly than the (111)B planes with group V surface atoms [66] and [79]. In experimental settings, the etching of InGaAs displays pronounced anisotropy in dilute ferric chloride, with the <010> directions representing the fast etch directions [64]. In contrast, AlInAs is essentially isotropic [65].

Figure 3.12 presents an analysis of the crystalline planes revealed through the undercut process of W400-100 at room temperature, employing a 1:2 diluted ferric chloride. In this analysis, the undercut sample is cleaved perpendicular to the minor axis (Figure 3.12 a) and major axis (Figure 3.12 b and c) to expose the lattice planes $(01\bar{1})$, (011) and $(0\bar{1}\bar{1})$ respectively.

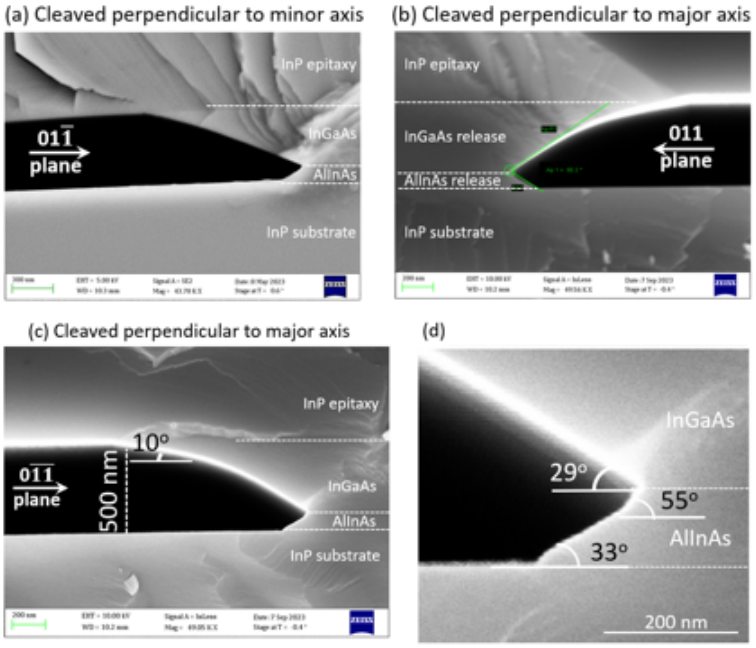


FIGURE 3.12: SEM cross section image of W400-100 wafer revealing slow etching planes (a) Cleaved across minor axis and (b) Cleaved across major axis (011), (c) Other side of major axis $(0\bar{1}\bar{1})$ and (d) Zoom in view of undercut for image (c).

It is evident from Figure 3.12 (c) and the zoom-in image of release layers in (d), that two angles are formed by AlInAs release layer with InP substrate, measuring approximately 33° and angle gradually evolving at around 55° [73]. At the junction, InGaAs forms an angle of approximately 29°, which decreases to about 10° with distance of around 1 μm from the junction. This trend is attributed to the slower vertical etch rate of InGaAs R3, which is 0.5 μm/min, causing an angle with the lateral etch rates. This delays the revelation of the slower etching planes in InGaAs. These angles consistently align within a deviation of ± 2° for both cleaves across the major and minor axes.

3.3.2.5 Selectivity comparison

Until now, the etch rate has been compared for different release layers, dilutions, along various lattice planes and for different etch duration. This section delves into the consequences of etch rate on selectivity to InP. In the context of wet etching, selectivity denotes the ratio of the lateral etch rate of the release layer to the vertical etch rate of InP, situated above the release layer. A higher selectivity is desirable, indicating that the release layer is undercut rapidly while only minimal InP material is etched. Faster etch rate accelerates the overall process time and higher selectivity enables to have a epitaxy design with a thin InP layer above release layer, saving cost.

Etch rate increases with raise in temperature while selectivity decreases, as at higher temperature chemical reactivity increases, leading to attack of unintended materials. Therefore, previous studies have typically employed lower temperatures for undercut processes to achieve higher selectivity, albeit with longer etch times. Table 3.4 compares the selectivity for different cases.

The vertical etch rate of InP is only a couple of nanometers per minute, making it difficult to measure the material etched during short etch duration. To determine the etch rate, InP samples with patterned dielectric hard masks are used. The etch depth of the samples is measured before wet etching. Then, the samples are immersed in a ferric chloride solution for three hours. After immersion, the etch depth is measured at the same spots on the samples. The difference in etch depth provides the vertical etch rate of InP. It is important to note that this is the average vertical etch rate of InP. The etch rate is not linear with time, it is high initially and gradually saturates, as discussed in earlier sections.

The undercut of the dual release layer (W400-100) with a 1:2 dilution demonstrates twice and thrice higher selectivity compared to individual AlInAs and individual InGaAs release layers respectively. This improvement is further enhanced with a more diluted solution of ferric chloride (1:5). At room temperature, the 1:5 dilution exhibits a vertical etch rate of InP at 0.88 nm/min, compared to the 2.28 nm/min observed with the 1:2 dilution. This highlights that the 1:5 dilution, containing more water, etches InP at half the speed of the 1:2 dilution. Consequently, the selectivity achieved using the 1:5 dilution of ferric chloride in dual release layers reaches the highest value of 5410.

TABLE 3.4: Comparison of selectivity at room temperature, using lateral etch rate (LER) of release layers and vertical etch rate (VER) of InP along <100>, where selectivity = LER/VER.

Wafers	**Etchant**	**LER of release layers**	**VER of InP**	**Selectivity**
InGaAs [64]	1:2	1500 nm/min	2 nm/min	750
AlInAs [65]	1:2	3300 nm/min	2.06 nm/min	1600
W400-100	1:2	4850 nm/min	2.28 nm/min	2127
W400-100	1:5	4760 nm/min	0.88 nm/min	5410

The key takeaways from the etch characterization are as follows:

- Dual release layers (W400-100 and W400-50) exhibits a threefold higher etch rate than InGaAs and 1.3 times higher than AlInAs individual layers, from earlier works [64] and [65].
- Almost isotropic etching is achieved, although with some minor variation in etch rates along different lattice planes.
- Etch rates depend on the dilution of ferric chloride wet etchant. An interesting anomaly is observed where 1:2 dilution yields similar etch characteristics as 1:5 due to saturation. Overall, 1:5 dilution offers similar etch rates, higher linearity and better selectivity compared to 1:2, enabling faster room temperature release.
- Changing the thickness of the AlInAs release layer from 100 nm to 50 nm does not affect the etch rate.
- Cross-section SEM analysis on cleaved samples reveals the evolution of slow etching planes along both parallel and perpendicular axes to the major axis.

Moving on from the etch characterization of release layers, we focus on the interface roughness of the coupons resulting from different release layers and the potential reasons behind it. Ensuring a high-quality coupon interface is crucial for achieving a high transfer print yield and successful direct bonding onto the target wafer. Any roughness or unevenness on the coupon interface could pose challenges for direct print to the target surface.

3.3.3 Interface characterization

To analyze the coupon interface, it is required to completely undercut the release layers as previously described in Figure 3.4. Generally direct bonding of coupons are preferred which can be achieved by extremely smooth interface.

The basic requirement for direct bonding is that both mating surfaces must be exhibiting sub-nanometer roughness over the bonding area. The smooth coupon interface directly adheres to the target surface through Van der Waals forces, eliminating the need for additional adhesives. Direct bonding is advantageous in optimizing optical coupling, aiding in heat dissipation and eliminates reliability and processing issues associated with adhesive usage. The adhesion strength can be further enhanced by plasma activation of the target surface. This section details how the smoothness of the lower interface of the InP coupon is influenced by the thickness of the InGaAs release layer. Finally, the required InGaAs thickness for achieving optimal direct bonding is illustrated.

3.3.3.1 AFM and WLI analysis

The InP lower interface, which is adhered to the tape in Figure 3.4 (h), is analyzed by White Light Interferometry (WLI) on a 150 μm x 50 μm and through AFM on 10 μm x 10 μm scale and the results are shown in Figure 3.13. The bow observed in the images arise from the flexible tape holding the coupons and not inherent to the coupon itself. The AFM scan reveals precise roughness values than WLI, though the same coupon interface is used for both. This is because AFM is a mechanical measurement where the probe scans across the interface surface in contrast to WLI being an optical measurement. Figure 3.13 (a and b) shows prominent hills and valleys for wafer with no InGaAs and only 500 nm AlInAs as release layer. These features are reduced comparatively in Figure 3.13 (c and d) for wafer with 20 nm InGaAs. Finally, an extremely smooth interface is obtained for wafer with 400 nm InGaAs on 100 nm AlInAs as

shown in Figure 3.13 (e and f). Thus it is noticed that the thicker InGaAs of 400 nm is required to achieve smooth interface. The wafer W400-50, with 400 nm InGaAs and 50 nm AlInAs has slightly higher roughness than W400-100 as seen in Table 3.5, but however both W400-50 and W400-100 have roughness less than 1 nm over 10 μm x 10 μm scan area.

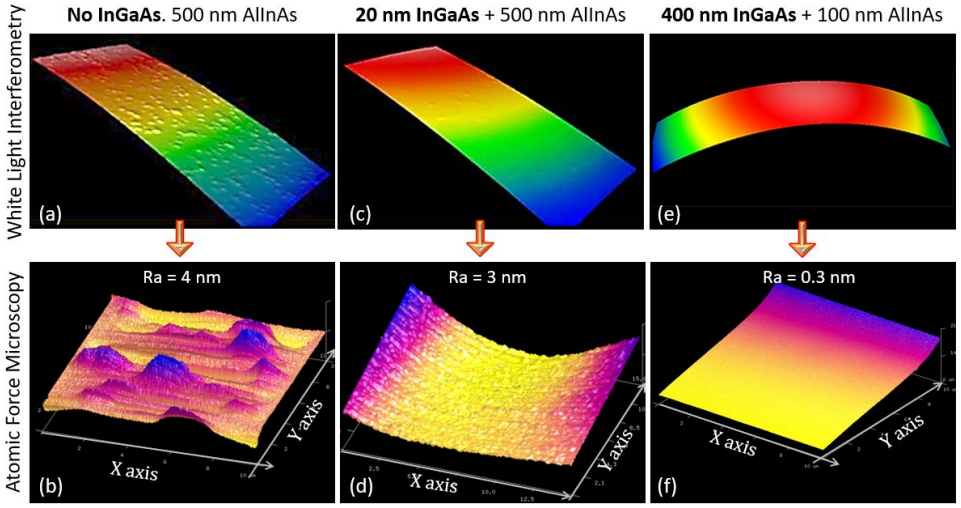


FIGURE 3.13: Coupon surface analysis for different release layer structure using white light interferometry over 150 μm x 50 μm (a, c and e) and Atomic force microscopy over 10 μm x 10 μm (b, d and f).

AFM scans are analyzed for varying thicknesses of InGaAs in the release layer, ranging from no InGaAs (W0-500) to 20 nm InGaAs (W20-500) and 400 nm InGaAs (W400-100), as detailed in Table 3.5. Here, Rq represents the root mean square average and Ra signifies the arithmetic average of roughness. The analysis reveals a consistent reduction in the average roughness Ra with increasing InGaAs thickness. For the W400-100 wafer, featuring a 400 nm InGaAs layer, the roughness is minimized to an impressive 0.3 nm.

A comprehensive understanding of roughness is obtained through a 2D section conducted across the AFM scan. The dimension of the hills or roughness is analyzed by measuring the hill length (L) along the X-axis and the hill width (W) along the Y axis as marked in Figure 3.13 (b, d and f). The results are summarized in Table 3.5.

TABLE 3.5: Roughness measurement details for AFM scan of 10 μm x 10 μm .

AFM scan	**Avg L (nm)**	**Avg W (nm)**	**Rq (nm)**	**Ra (nm)**
W0-500	2400	1500	5.53	4.01
W20-500	370	370	3.54	2.96
W400-100	None	None	0.37	0.29
W400-50	None	None	0.72	0.55

It is worth highlighting that no measurable roughness (hills) was detected for the W400-100 and W400-50 wafer. Consequently, the average length and average width are specified as "none". The final conclusion is that interface-related roughness issues are effectively solved by incorporating a 400 nm thick InGaAs layer in the release layer.

3.3.3.2 Raman analysis

Upon conducting AFM analysis of the interface, it becomes evident that wafers containing either solely AlInAs or a predominant amount of AlInAs in the release layer exhibit a roughness issue. This phenomenon stems from the formation of nanostructures during the transition of precursors from the AlInAs release layer to InP epitaxy, in the MOCVD growth process at Tyndall, as detailed in the work by Gocalinska et al [80]. This effect is particularly pronounced in the material combination of $Al_xIn_{1-x}As/InP$.

To gain better understand of interfaces, Raman spectroscopy was employed on the bare InP substrate (100) prior to any epitaxial growth, serving as a baseline reference (Figure 3.14). Subsequently, following the complete growth of the epitaxial stack, Raman measurements were taken on the top surface. Additionally, upon releasing the coupon, another measurement was conducted at the n-InP interface ($\bar{1}00$) just above the release layer. This investigation involved samples featuring 20 nm (from W20-500) and 400 nm (from W400-100) InGaAs release layers. The measurements employ a 514 nm laser at room temperature, with a penetration depth of less than 100 nm into InP ensured that surface region was probed. The resulting Raman plots are presented in Figure 3.15, after baseline correction and the data were smoothed using the adjacent averaging method in the Origin software.

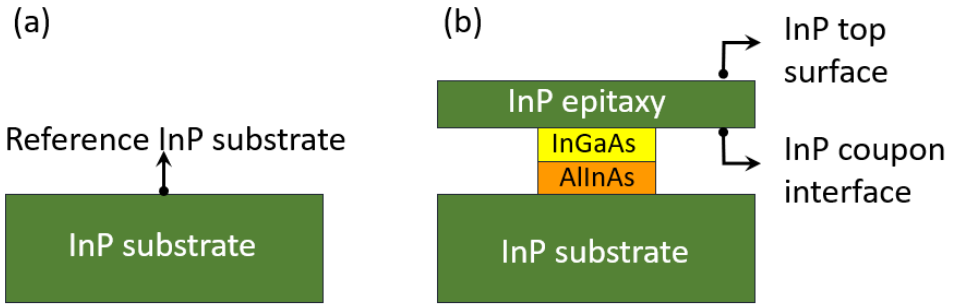


FIGURE 3.14: Locations of Raman measurements (a) Reference measurement on InP substrate before any epitaxial growth and (b) After coupon processing, measurement on coupon interface after release and top most surface of epitaxial stack.

The Raman spectra display extra peaks compared to the reference InP substrate [81]. Table 3.6 presents the Raman fingerprints of the InP transverse optical (TO), longitudinal optical (LO), and lattice vibrational (LV) phonon modes. The spectra of the InP interface with the W400-100 release structure show an extra peak at 226 cm^{-1}, possibly due to InAs from As overflow at the interface [82]. Additionally, a broad peak around 366 cm^{-1} is observed, attributed to the LO phonon-plasmon coupled modes in the n-doped InP [83]. The W20-500 released surface exhibits phonon-plasmon coupled modes closer to the LO peak, likely due to lower doping in this sample. All spectra include the forbidden TO phonon mode.

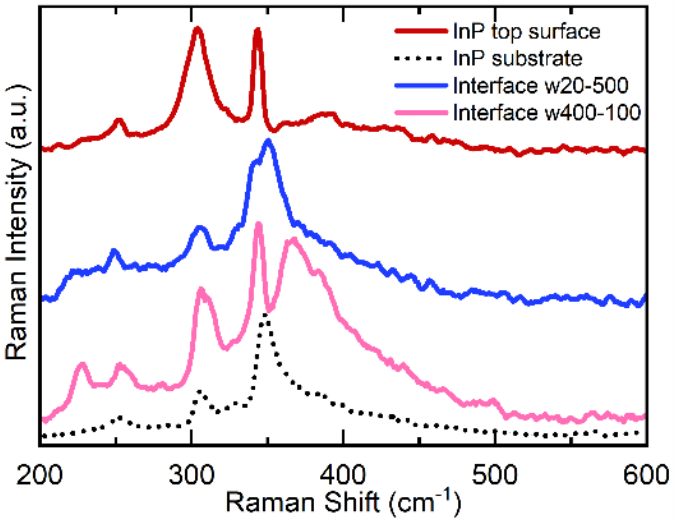


FIGURE 3.15: Results of the Raman measurements are presented with an offset for clarity. The InP substrate serves as the baseline, with additional plots obtained from the InP interface of wafers W20-500 and W400-100, as well as from the top surface of wafer W400-100.

TABLE 3.6: List of Raman shift observed along with reference literature.

Raman Shift	**Fingerprints**	**References**
253 cm^{-1}	InP (LV)	[81]
305 cm^{-1}	InP (TO)	[81]
348 cm^{-1}	InP (LO)	[81]
230 to 240 cm^{-1}	InAs (LO phonon-plasmon)	[83]

Overall, we think that roughness is more due to the disordered nature of the interface rather than the specific binary semiconductor. Although we cannot conclusively determine which element causes interface roughness in wafers with low InGaAs thickness and a majority of AlInAs in the release layer, it's worth noting that certain fingerprints are challenging to precisely decipher and attribute to specific semiconductors.

In future, quantitative techniques like X-ray photoelectron Spectroscopy (XPS) and Secondary Ion Mass Spectroscopy (SIMS) could be carried out to understand the elemental composition

of the interface surface and thus what causing the roughness.

3.4 Conclusion and discussion

This chapter details about dual sacrificial layer of InGaAs and AlInAs for InP based devices. It discusses various benefits in undercutting and transfer printing and compares with earlier individual release layers. A review of wet etchants is also presented along with experimentation of different dilutions of ferric chloride.

A thickness of 400 nm of InGaAs on top of 100 nm or 50 nm AlInAs proves most beneficial. This combination facilitates a fast etch rate, nearly isotropic etching behaviour and exceptionally smooth interfaces, thereby enabling direct bonding of coupons to target wafer. Notably, these advantages are achieved at room temperature, saving time, cost and energy. Furthermore, this study demonstrates that a 1:5 dilution of ferric chloride with water yields similar etch rates, greater selectivity and enhanced linearity compared to a 1:2 dilution. These contributions enhance the yield of transfer-printed devices and speeds up the undercut process for InP-based epitaxial stacks.

In the future, more investigations can be done through simulation and more experiments. However, due to time constraints, we could explore only limited wafers with varying thickness of dual release layer. An optimal approach would involve employing fluid mechanics-based simulations to comprehend the undercut process. Nevertheless, this is a complex task as it needs parameters such as the viscosity of the wet etchant, etch rates along all planes and the anisotropic nature of III-V wet etching, requiring 3D simulation. Despite the complexity involving detailed parameters, these simulations would provide a clear understanding of the coupon release process.

Chapter 4

Theory and performance of InGaAs photodetector

4.1 Introduction

Indium Gallium Arsenide is a commonly used III-V semiconductor material for photodetection, especially in the near-infrared (NIR) range. While germanium photodetectors integrated on SOI platforms are researched, they demand additional processing time and high thermal budgets [21]. Nonetheless, InGaAs maintains its popularity due to various advantageous factors.

Firstly, $In_{0.53}Ga_{0.47}As$ has a direct bandgap of ~ 0.75 eV, which ensures effective photon absorption across wavelength ranging from 0.9 μm to 1.7 μm [84]. Notably, this includes the crucial telecommunication wavelengths of 1.31 μm and 1.55 μm, widely employed for data transmission. The fiber dispersion loss is least at 1.31 μm, ensuring signal integrity over long distances. Additionally, both wavelengths benefit from minimal optical fiber loss and reduced attenuation due to minimized water absorption. This wavelength sensitivity positions InGaAs as an ideal choice for communication applications. Secondly, InGaAs photodetectors demonstrate high responsivity [85], efficiently converting incident photons into electrical signals which is essential for detecting weak optical signals. Thirdly, InGaAs photodetectors have low dark current [86], contributing to low noise and improved signal-to-noise ratios. The combination of these properties makes InGaAs a suitable material for high-performance photodetection in diverse applications.

III-V photodetectors have demonstrated exceptional performance [87], [88], offering the flexibility to detect various optical bands by adjusting the composition of the compound semiconductor. Several successful integrations of high-speed InGaAs photodetectors on SOI platforms have been showcased, employing methods such as epitaxial growth [89] and by wafer bonding [90]. An alternative approach is to integrate the PDs through micro-transfer printing, offering advantages such as highly efficient material usage and low process temperature. Recent advancements include the integration of InGaAs PDs onto silicon nitride (SiN) platforms, achieving a responsivity of 0.42 A/W at 1310 nm [91] and 0.3 A/W at 1550 nm, coupled with impressive bandwidth capabilities [92].

Earlier research aimed at enhancing the performance of PD by integrating them to SOI platform using a single coupling method. However, the different coupling strategy like diffractive coupling, evanescent coupling and adiabatic coupling from Si to different materials are illustrated [93]. A review article on high-speed photodetector on SOI platform highlights coupling methods including vertical coupling (normal incidence), edge coupling, waveguide evanescent coupling, waveguide bottom grating coupling, and butt coupling structures [94]. This chapter demonstrates the successful integration of photodetectors with the same footprint, onto the SOI platform through three effective coupling mechanisms facilitated by the transfer printing approach (More details of coupling mechanism were provided in Chapter 2, with SOI design, simulation of absorption and interface losses between silicon and PD, for each coupling mechanism).

This chapter details the heterogeneous integration of the ultra-thin InGaAs waveguide photodiode coupons to SOI platform via micro-transfer printing technique and further measurements of the high bandwidth performance. The coupling schemes employed are butt, grating and evanescent. The InGaAs device coupons have dimensions of 21 μm $\times$ 57 μm with 675 nm thickness. These are isolated from the InP source wafer using a dual-layer release structure as discussed in Chapter 3. These PD coupons are directly bonded to the Si, eliminating the need for adhesives. The ultra-small, ultra-thin design enables the use of the underlying oxide for dielectric isolation. These integrated PDs exhibit maximum responsivity up to 0.6 A/W with 48 nA dark current and 17.5 GHz bandwidth at 1550 nm for reverse bias of 0.6 V. Along with 50 Gb/s data transmission for non-return-to-zero on-off keying (NRZ-OOK) at 1550 nm while with pulse-amplitude modulation (PAM4) and post-processing with equalization, we accomplish back-to-back transmission rates of 100 Gb/s. The discussion on the design and fabrication

of these photodetectors is presented along with their detailed results in subsequent sections of this chapter, which was previously published in references [95] and [96].

4.2 Photodetector design

The entire epitaxial stack is grown using MOCVD at Tyndall National Institute. The epitaxial stack (see appendix Figure A.3 a) employed in this study is based on the work by Bach et al [97], with adjustments tailored for the transfer printing process. Notable modifications include the incorporation of release layers and the utilization of lattice-matched InP as the N contact. To facilitate the transfer print process, sacrificial layers are incorporated into the structure just above the substrate. Here a dual release layer consisting of 400 nm of InGaAs on top of 100 nm AlInAs is used. The total PD material above release layer is only 675 nm thick. This stack facilitates high-speed performance by majorly utilizing electrons as active carriers. This design mitigates the impact of hole transport mechanisms on the diode response and output saturation current [88].

The doping strategy for the absorption layer (150 nm P-InGaAs) involves introducing a p doping concentration on the order of 10^{17} cm^{-3} to mitigate the relaxation time effect. Simultaneously, the contact layers (P-InGaAs and N-InP) are heavily doped exceeding 2×10^{18} cm^{-3} to effectively minimize contact resistance [98]. To further enhance the internal quantum efficiency and reduce capacitance, a partially depleted absorber layer is incorporated [99].

The epitaxial stack includes a 400 nm thick InGaAs absorbing region divided into two parts. It comprises of 150 nm p-doped layer and a 250 nm not-intentionally-doped (nid) layer. 400 nm thick absorbing region is chosen for stronger absorption of light in InGaAs and optimize coupling to 500 nm SOI wafer. Carriers (electrons and holes) are generated in both the doped and nid absorber layers. The holes generated in p-doped layer are relaxed and they are immediately captured by P contact via graded p-doped layers. Whereas the holes generated in nid layer are moved by electric field in opposite direction and are collected from p-doped absorber.

Whereas the electrons created from each layer are collected through two distinct mechanisms. Electrons generated in p-doped region are hindered from reaching the P contact by the wider bandgap InGaAsP electron block layer. These electrons diffuse towards the undoped absorber and reaches the N contact. Conversely, electrons generated in the nid absorber layer are

accelerated and drifted by the reverse bias towards the N contact with the assistance of the electric field across it.

4.3 Photodetector fabrication

The fabrication of a fully testable photodetector involves three essential stages. Initially, the transfer-printable PD is manufactured on the native III-V source wafer. Simultaneously, the target wafer is patterned, which is the second step. Following this, the PD coupons from the source wafer are released from the substrate. The third step is to pick the released coupons and print on the target wafer using micro-transfer printing. This is followed by post-processing steps, resulting in integration of III-V PD to the SOI wafer. These steps are detailed in the following sections.

4.3.1 Source wafer fabrication

The fabrication process of PD coupons within the source wafer involves a 6-step lithography procedure, illustrated in a step-by-step fashion in Figure 4.1. These coupons are held in place, even after the removal of release layer via an anchoring system called tethers, which connects the coupon to the substrate. Different tether types are experimented in PD design which are detailed in appendix A.4 and A.5, along with more technical details of fabrication in A.6. The dual release layer is employed in the epitaxial stack. Consequently, the coupons are released rapidly (5 min) and exhibit an interface roughness of 0.2 nm over 10 μm $\times$ 10 μm, facilitating adhesive-free bonding to SOI target wafer.

4.3.2 Target wafer

The target SOI wafer was extensively described in Chapter 2, with SOI wafer designs and different coupling mechanism of PD depicted in Figure 2.2. Further details regarding the target SOI mask are provided in Appendix Figure A.7. The SOI wafer received from Cornerstone exhibits a roughness of 0.47 nm in an AFM scan covering an area of 10 $\mu m\times$ 10 μm. The same wafer is utilized for all three coupling mechanisms: co-planar butt coupling, grating coupling and evanescent coupling.

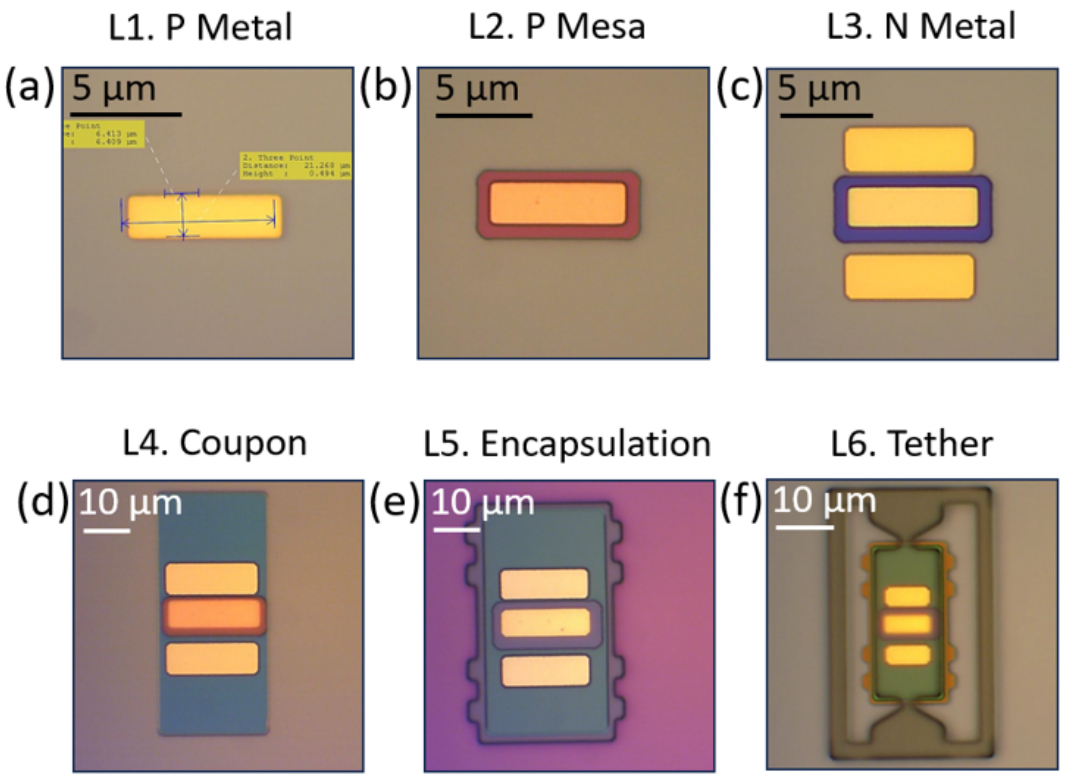


FIGURE 4.1: Top view of source wafer, with step by step fabrication levels (L): (a) P metallization, (b) P mesa etch, (c) N metallization, (d) Coupon formation, (e) SiN encapsulation and (f) Tether definition.

For butt-coupled integration, the target wafer undergoes additional preparation by etching a trench at the output taper. The etch depth is precisely controlled using endpoint detectors to achieve an accurate depth of 550 nm. This ensures that the PD absorber region aligns with the thickness of the silicon waveguide. Specifically, out of the 550 nm etch, the top 500 nm of silicon in SOI wafer is removed, along with a 50 nm etch into the SiO_2 layer. This etched area of the SOI wafer has a roughness of 1.02 nm in AFM scan over an area of 10 $\mu m \times$ 10 μm. The process of plasma etching has increased the roughness of the SOI wafer from 0.47 nm to 1.02 nm.

4.3.3 Micro-transfer printing

The PD coupons, fully released from the InP-based source wafer, are transfer printed onto a pre-patterned SOI wafer, at room temperature and ambient atmosphere. The PD coupon size measures 21 μm $\times$ 57 μm, for which a PDMS stamp, with a post of similar size to the PD coupon, 20 μm $\times$ 50 μm is utilized for printing. The initial state of the target wafer is illustrated in Figure 4.2 (a), featuring silicon taper on the output side designated for PD printing. The

stamp applies a downward acceleration of 0.75 g during the picking phase. The target region must be locally flat to accommodate the printed PD coupons and the smooth coupon surface enables adhesion through Van der Waals forces. A single pick-up and print cycle takes $\leq$ 40 s, provided printing parameters such as pick acceleration, overdrive distance and print speed are optimized. Large arrays of devices can be printed simultaneously using an appropriate multi-post stamp. The target locations exhibit sub-nanometer roughness enabling the printing process with no difficulties and almost 100 % yield.

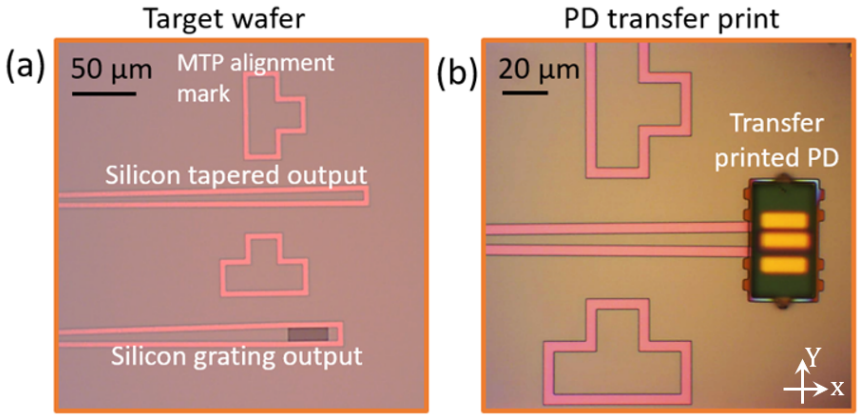


FIGURE 4.2: (a) Initial stage of patterned SOI target wafer and (b) Target wafer with PD printed to tapered end of silicon.

Alignment is achieved using software to adjust the horizontal (x-axis) and vertical (y-axis) positions of the PD coupon relative to the silicon taper end, as shown in Figure 4.2 (a). Typically, MTP alignment marks on the target silicon wafer are used for alignment. In this case, due to the small size of the PD coupons, the top right end of the silicon taper on the target wafer and the top left corner of the P metal on the PD coupon served as reference marks. The closest possible alignment achieved had a misalignment of $\pm$ 200 nm along the x-axis, measured using SEM. The output Si waveguide, tapered to a width of 7 μm, is aligned with the InGaAs mesa width of 10 μm during printing, as shown in Figure 4.2 (b). The alignment of the transfer-printed coupons is crucial for the subsequent integration lithography stages.

In typical scenarios, an adhesive layer like benzocyclobutene (BCB) is applied to the target wafer to securely hold the coupons in place. However, in this instance, no adhesives were utilized, instead, the PD coupons were directly bonded to the silicon dioxide in a co-planar coupling arrangement.

It is worth noting that while a layer of BCB can enhance high-speed performance by reducing capacitance, although its processing is not as straightforward as direct bonding. The breakdown

voltage for BCB and thermal SiO_2 falls within the range of 530 V/μm and 400 to 1000 V/μm, respectively [100]. The dielectric strength is approximately 3 x 10^6 V/cm for BCB and ranges from 6 to 9 x 10^6 V/cm for thermal SiO_2 [101].

4.3.4 Post-integration process

Subsequent to printing, the metal contacts in the PD coupon need to be opened to create bond pads for the final device, as illustrated in schematic Figure 4.3. This section will address the challenges encountered during this process and solution to them.

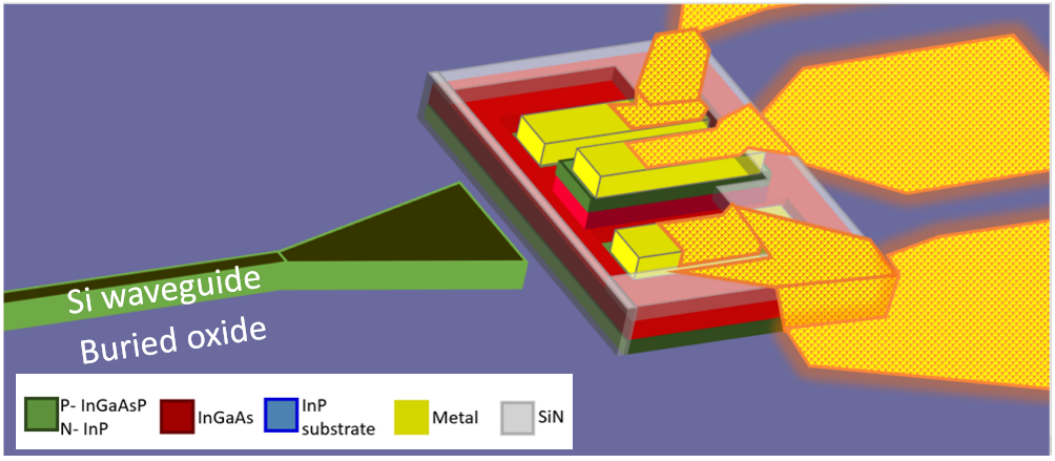


FIGURE 4.3: Schematic representation of final post processed PD on SOI wafer.

In Figure 4.4 (a), SEM image of a printed PD on a silicon sample is shown, covered with photoresist from tether patterning. Following printing, the coupons exhibit a flat profile, displaying good bonding to the silicon target sample. To proceed with further processing, the photoresist is removed using oxygen plasma treatment. This step exposes the SiN encapsulation layer covering the PD. Subsequently, the sample undergoes a 20-minute treatment with CF_4 plasma to strip the SiN and open the metal contacts, illustrated in SEM image in Figure 4.4 (b). Notably, upon removal of SiN, bowing of coupon is observed on either side of P mesa. And also, during this process, fluorine etches the silicon sample, resulting in a visibly rough silicon surface in SEM images. The schematic cross-sectional view of the transfer-printed PD, following the removal of the SiN hard mask, is illustrated in Figure 4.4 (c). Additionally, in some instances, delamination (spalling effect) of the undoped InGaAs layer is observed, leaving behind a 150 nm layer of N-InP on the silicon sample, as depicted in Figures 4.4 (d and e).

To address this challenge, immediately following the removal of photoresist, a 50 nm SiO_2 blanket deposition is performed on the target wafer with PD coupons. This SiO_2 layer serves

to stabilize the coupon and affix it to the target substrate. Following this step, instead of completely removing SiN, an additional lithography step is implemented to selectively eliminate SiN only from metal contacts and the region in front of the P Mesa, which connects to the silicon waveguide (Figure 4.4 f). This strategic approach ensures that the coupon remains flat even after the removal of SiN, simultaneously opening the metal contacts to establish probe pads.

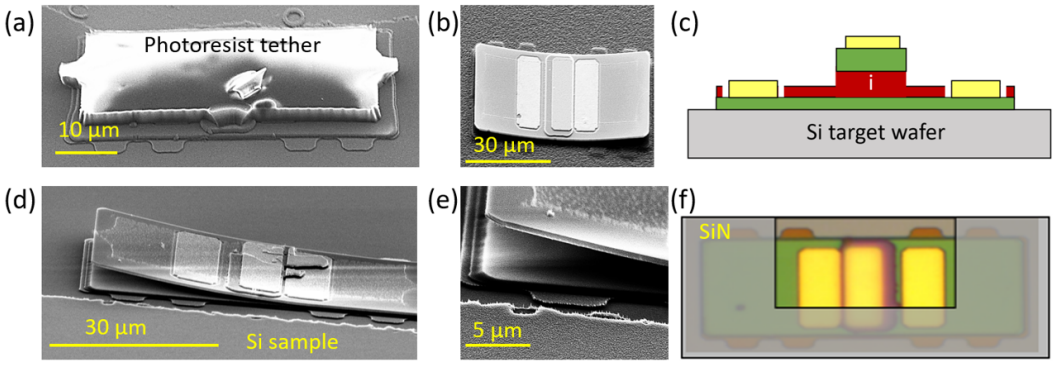


FIGURE 4.4: (a) Printed PD on target without any post processing, (b) PD bowing after removal of photoresist and SiN, (c) Schematic cross-section of PD after removal of SiN, (d) Coupon showing spalling of InGaAs layer from N-InP layer, (e) Zoomed image of spalling and (f) Schematic top view showing selective removal of SiN to overcome bowing.

The reason behind this bowing phenomenon is analyzed. We observe that prior to the removal of SiN, the coupons exhibited a flat profile. This observation indicates that the SiN layer played a compensatory role in managing the inherent strain within the epitaxial layers, preventing the coupons from bowing. The deposition of $\sim$ 700 nm of SiN was required at various stages of coupon fabrication process, contributing to stress during each deposition step (D), as illustrated in Figure 4.5 (a). We were aware that the deposition of SiN would induce stress, and therefore, we monitored the bow of the source wafer before and after each deposition step using a Tencor profilometer. Typically, stress in thin films of dielectric depositions is assessed by scanning across the entire wafer and calculating the stress from the bow measurements before and after deposition.

The bow was measured, over approximately a centimeter length. Subsequently, I inferred the stress for the final SiN film of thickness 690 nm, from the bow using the cantilever beam technique developed by G. Gerald Stoney for thin film stress measurement, as expressed by Equation 4.1. This approach allowed us to efficiently evaluate stress levels.

In this equation, $E/(1-\nu)$ represents the wafer elastic constant, σ signifies stress, t_f denotes film thickness (First deposition D1: 94 nm, second deposition D2: 300 nm, and third deposition

D3: 297 nm), t_s represents the InP wafer thickness (0.4 mm), R_s is the radius of curvature of the bare substrate before deposition, R_f is the radius of curvature of the substrate with the deposited film, E is the Young's modulus for the InP substrate (6.11×10^{10} pascal), and ν denotes the Poisson's ratio for InP, which is taken as 0.36, from Ioffe institute webpage (https://www.ioffe.ru/SVA/NSM/Semicond/InP/mechanic.html).

$$\sigma = \frac{1}{6}\frac{E}{(1-\nu)}\frac{t_s^2}{t_f}[\frac{1}{R_f} - \frac{1}{R_s}] \tag{4.1}$$

$$R_f = \frac{H_f}{2} + \frac{W^2}{8H} \tag{4.2}$$

Following each deposition (D1, D2 and D3), the sample undergoes a scanning process across the same length (W) of 6 mm, and the value of bow before deposition (H_s) and after deposition (H_f) are measured using a Tencor profilometer, as depicted in Figure 4.5 (a). The radius of curvatures, R_s and R_f, are calculated based on H_s and H_f using the Intersection Chords Theorem, outlined in Equation 4.2 for R_f. Stress values are determined after each deposition, culminating in a final compressive stress of 539 MPa attributed to the total thickness of SiN.

During the epitaxial growth process at Tyndall National Institute, lattice mismatch between InGaAs and an InP substrate was identified through repeated XRD measurements, conducted after selectively etching different layers from the epitaxial stack as shown in Figure 4.5 (b). The 'As grown' XRD measurement was performed on the complete epitaxial stack, revealed four peaks. The most intense peak corresponds to the InP substrate, with two tensile-strained peaks on its right and one compressive-strained peak on its left. Among the two peaks on the right, the one closest to the InP peak is the most dominant, leading to bowing.

To identify the compound semiconductor causing this peak, XRD measurements were taken after selectively removing each semiconductor layer in the epitaxial stack. When the InGaAsP layer was etched, the peak to the left of the InP substrate disappeared, as shown by the dotted circle in the purple plot of Figure 4.5 (b), confirming this peak was due to InGaAsP. After wet etching 400 nm of the absorber InGaAs layer, there was no observed reduction in the XRD peaks (red plot). However, once the n-InP and the release InGaAs layer was removed, the dominant peak on the right disappeared, as indicated by the black dotted line in the green plot. This confirmed that the dominant peak was due to the lattice mismatch between InGaAs and InP.

The bowing of the released coupons is attributed to the strained InGaAs layers, which is not a problem under normal circumstances. For proper lattice matching of InGaAs on an InP substrate, the composition of InGaAs should be Indium 0.53, Gallium 0.47, and Arsenide, where the InGaAs peak aligns with the InP peak in the XRD plot, but with lower intensity. Thus the bow of the coupon is expected to arise from lattice mismatch of InGaAs which is seen from profilometer and XRD in Figure 4.5.

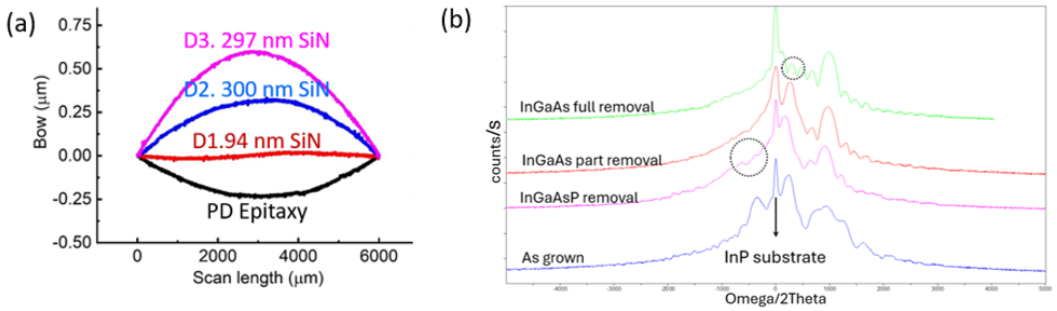


FIGURE 4.5: (a) Profilometer plots showing coupon bow on original epitaxy and after three sequential SiN depositions, and (b) Plot of XRD measurements on the PD epitaxial stack after sequential layer removal. The 'As grown' plot reveals a dominant InP substrate peak and three other peaks. The first peak to the right of the InP peak, identified through wet etching as due to InGaAs, causes bowing of the coupons due to tensile strain.

The SEM image of the final post-processed transfer-printed PD, with opened SiN, is presented for each coupling scenarios in Figure 4.6. The metal probe pads are situated on a 3 μm oxide layer in the edge-coupled scenario. The ground-signal-ground (GSG) pads have a pitch of 125 μm, with each pad measuring 100 μm by 100 μm and a gap of 25 μm between ground and signal. Metal evaporation of Ti/Au (50/300 nm) layers underwent a 360° rotation to fabricate probe pads, ensuring consistent metal coverage across the printed PD with a varying height profile.

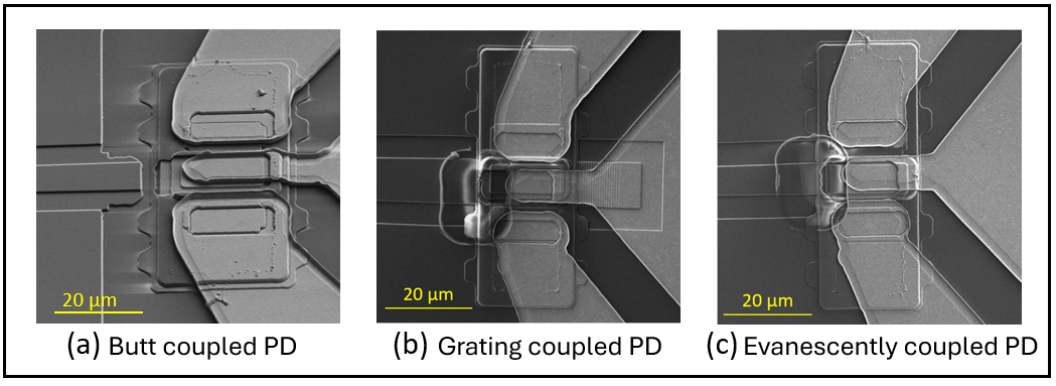


FIGURE 4.6: Final transfer-printed PD onto SOI after post integration process through (a) Butt coupling, (b) Grating coupling and (c) Evanescent coupling.

4.3.4.1 Challenges with in-fill process

After metallization of the probe pads, the final processing step involved amorphous silicon in-fill, for one of the target chips, which featured butt-coupled PDs. Although simulation was straight forward for co-planar coupling, executing this step proved highly intricate and demanding. Chapter 2 provides an in-depth discussion of the a-Si in-fill process (see Figures 2.12 and 2.15). A blanket deposition of a-Si is not feasible due to its refractive index of 3.1. This could cause leakage of the propagating mode from the silicon waveguide to a-Si at the interface, resulting in significant loss and reduced coupling to the PD. Hence selective removal using lift-off technique was tried.

In this section, we will discuss into the specific challenges faced during the in-fill process on the actual target SOI wafer with printed PDs. For the in-fill process, the samples are coated with a lift-off resist, followed by the evaporation of a-Si. Subsequently, the a-Si in unwanted areas is removed by immersing the sample in a solvent, facilitating the lift-off of a-Si from those regions.

Initially, a negative photoresist was utilized for the lift-off process, but it proved ineffective. After the lift-off process, the sample was expected to feature only a-Si measuring 10 μm^2 at the end of the waveguides. However, contrary to expectations, the target SOI sample was entirely covered with a-Si (depicted as shiny green color in Figure 4.7 a). A closer inspection of the sample in Figure 4.7 (b) revealed a-Si evaporated on top of the photoresist, which had curled during the evaporation process, complicating the lift-off.

To address this issue, we experimented with an alternative approach, employing a bi-layer lift-off photoresist. This new approach featured sufficient open areas on the chip, facilitating chemical access and simplifying the lift-off process. As a result, a clean sample was obtained successfully, as demonstrated in Figure 4.7 (c and d). It is evident that the use of bi-layer resist yielded satisfactory results, with the final sample devoid of any remaining resist. Additionally, in Figure 4.7 (c), the black rectangular region denotes the actual device location on the chip. A closer examination of this region in Figure 4.7 (d) highlights the stark difference between using negative resist and employing bi-layer lift-off resist, where a-Si is only present at the required spots while the rest of the areas are exposing silicon sample.

Even after using bi-layer resist, we had another issue. To selectively remove a-Si, a lithography step was introduced, (Figure 4.8 a) and the final sample after lift-off had 'rabbit ear' around

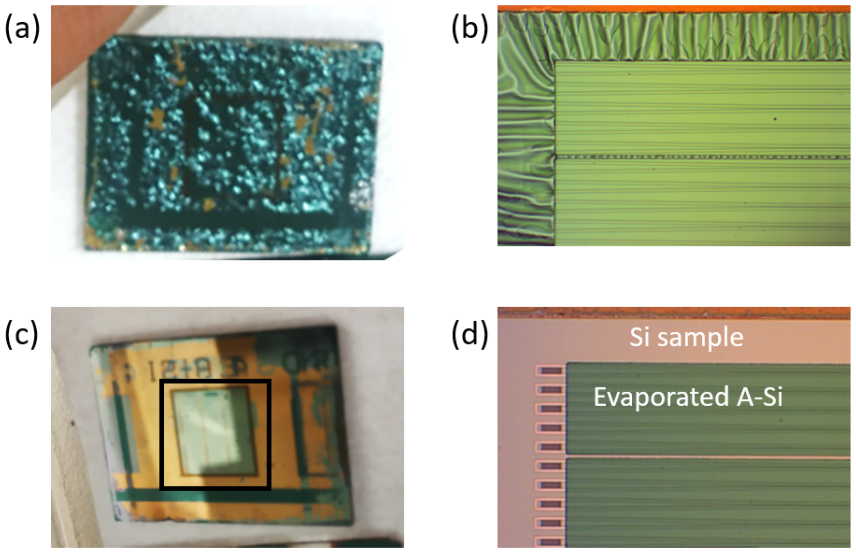


FIGURE 4.7: Target SOI wafers after a-Si inf-fill (a) Burned photoresist during evaporation of a-Si using negative photoresist and (b) it's zoomed section showing curled up a-Si in green colour, (c) Clean SOI sample as expected after evaporation and lift off process using bi-layer resist and (d) Its zoomed section comparing the same spot as in (b).

the a-Si in-fill region as shown (Figure 4.8 b). This phenomenon occurs due to evaporation of a-Si along the photoresist sidewalls. It is observed that in-fill pattern design in Figure 4.8

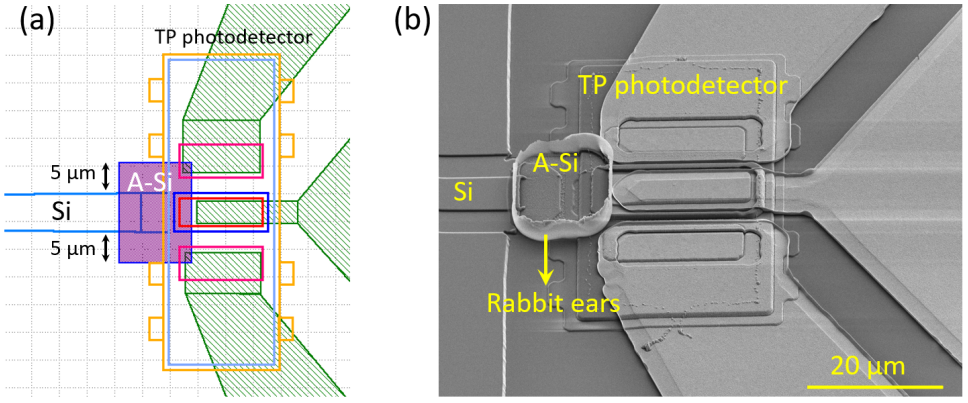


FIGURE 4.8: (a) The mask pattern showing a-Si infill patterning in purple shaded box at the interface and (b) SEM image of the PD, showing rabbit-ear feature after in-fill process.

(a) is widened by 5 μm on top and bottom of silicon taper as labelled. It results in mode loss and preventing from sufficient light coupling to the PD. To address this issue in future, a precise electron beam patterning is essential, connecting the silicon taper and PD mesa, to achieve efficient coupling. Additionally, it is crucial to perform a-Si evaporation without sample rotation inside the chamber to overcome rabbit-ear structures and ensure optimal results.

4.4 Results and discussion

4.4.1 Grating coupler measurements

Characterizing the photodetector starts with assessing the coupling efficiency of grating couplers. For every photodetector placed on chip, there is a reference grating coupler design with input and output couplers placed adjacently as shown in appendix Figure A.7. The experimental setup is illustrated in the block diagram (Figure 4.9) for these reference couplers measurement. The tunable laser source (TLS) emits light with wavelengths ranging from 1520 nm to 1580 nm, which is directed to polarization paddles. The light is then transmitted to the input optical fiber fixed to a goniometer, directed into the grating coupler, at a defined angle on the input end. The power meter measures the light coupled out of the grating coupler and the coupling is optimized at 1550 nm by adjusting the polarization control paddle to obtain the TE optical mode and simultaneously adjusting the angles of the input and output fibers in the goniometer. A microscope image during the testing of grating couplers is provided in Figure 4.10 (a).

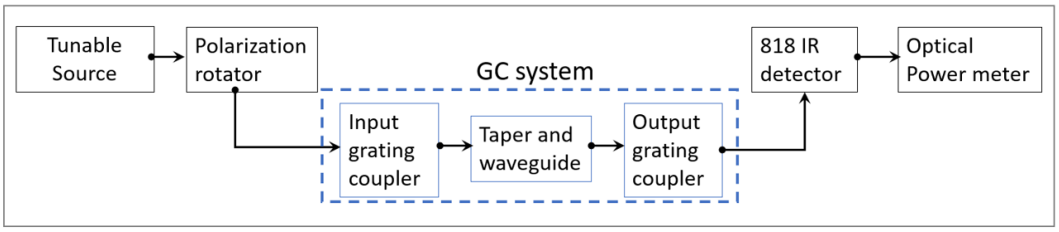


FIGURE 4.9: Block diagram of the grating coupler measurement setup.

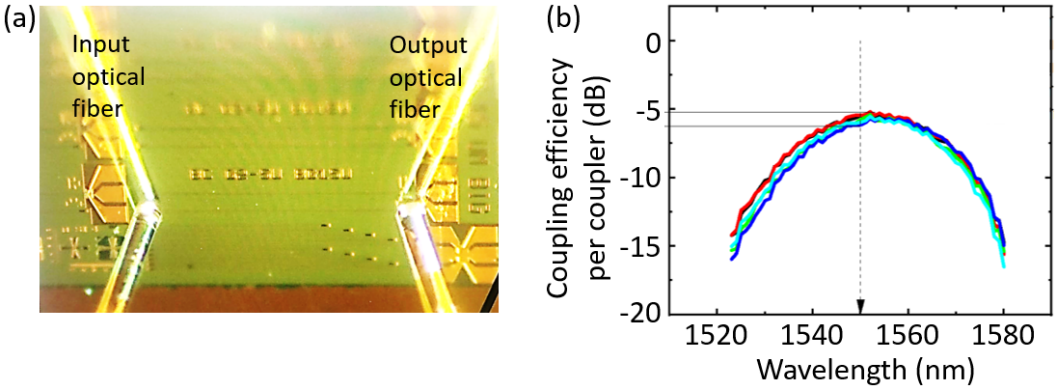


FIGURE 4.10: (a) Microscope image of device under test showing optical fibers on grating couplers and (b) Plot showing measured grating coupler efficiency for different waveguide lengths of 100 μm to 500 μm on unprocessed target wafer.

The same grating couplers are tested with five different waveguide lengths ranging from 100 μm to 500 μm, as depicted by different color plots in Figure 4.10 (b), with no significant

change observed due to these length variations. The maximum coupling efficiency per coupler is determined to be -5 dB, assuming negligible taper and waveguide loss. This is the result promised by Cornerstone as detailed in Chapter 2 Figure 2.3. The results remain same for all reference grating couplers at different locations on a chip.

4.4.2 Dark current measurements

Photodetector testing starts with current-voltage (I-V) measurement across p and n metal. These measurements are executed in dark environment, as provided in Figure 4.11. On reverse bias side the measurement is not done till breakdown in order to preserve the PDs and a value of -0.6 V is chosen for further measurements as its in the mid of linear regime, with a minimum contribution from the dark current. Series resistance of the PD is obtained from the I-V measurement as 83 Ω.

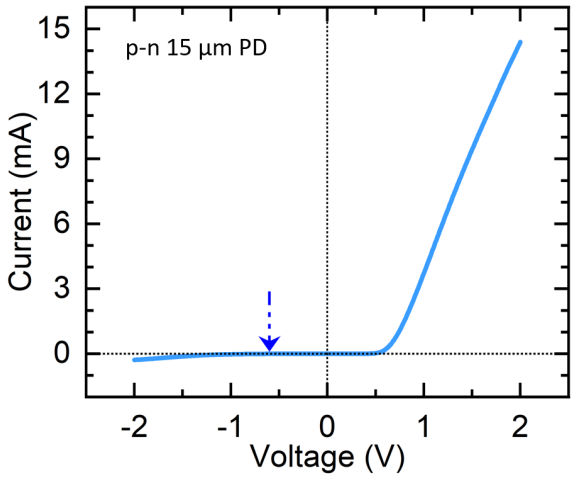


FIGURE 4.11: Plot of IV characteristics of transfer printed PD, dark measurement for 15 μm x 5 μm p and n metal.

Dark current measurements for transfer-printed photodetectors were conducted with no optical input, employing a reverse bias voltage of 0.6 V supplied using a Keithley 2602A source meter. The results, depicted in Figure 4.12, reveal distinct dark current values for evanescent, grating and edge-coupled photodetectors, registering 48 nA, 47 nA and 400 nA respectively.

Despite employing the same photodetector design for all coupling configurations, the edge-coupled photodetector surprisingly demonstrates nearly ten times higher dark current compared to its evanescent and grating counterparts. The process of opening dielectric from metal contacts also involves removing the SiN passivation from the front of the mesa to enable efficient light coupling from the silicon waveguide in the butt-coupled PD as shown in Figure 4.13.

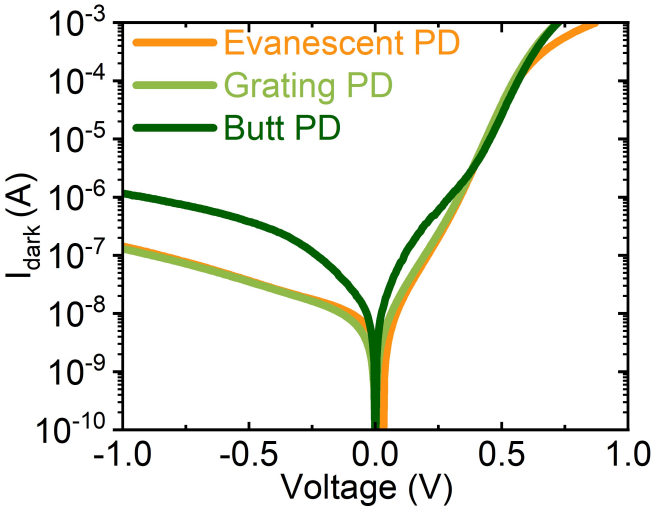


FIGURE 4.12: I-V plot with comparison of dark current for each PD coupling mechanism. Dark current is measured at 1550 nm for PD with 17 × 7 μm^2 mesa used in grating and evanescent coupling, along with 19 × 9 μm^2 mesa for butt coupling.

This removal exposes the mesa and its etched sidewalls, contributes to carrier recombination and a significant increase in dark current. Enhanced lithography alignments are proposed as a potential solution to mitigate and reduce dark current.

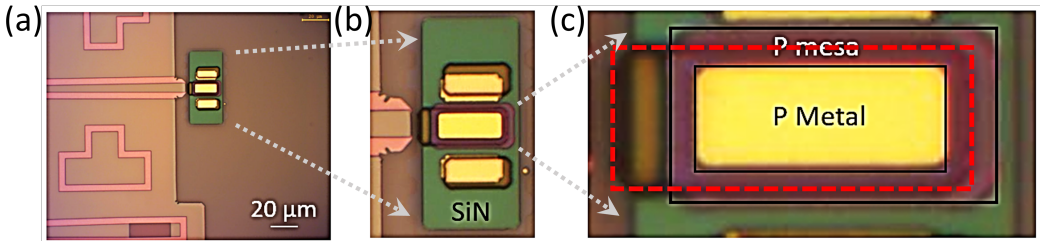


FIGURE 4.13: Metal opening process in post-processing. (a) PD transfer on SOI via edge coupling after exposing metal contacts. The green-colored region on PD indicates SiN deposition, (b) Close-up view of PD with three rectangular regions on top of metals where SiN is removed and (c) Enlarged view of P mesa, with the red-dotted line indicating the opened region exposing the mesa (purple), leading to an increase in dark current in the butt coupling scenario.

It is worth noting that the behavior of the photodetector before transfer printing was not assessed due to the small size of the metal contact (15 x 5 μm^2) and the presence of a SiN passivation layer covering the devices.

4.4.3 Responsivity measurements

Responsivity of a photodiode is a measure of its effectiveness in converting incident optical power (P) to electrical signals given by Equation 4.3 where R_λ is responsivity at the specific

wavelength λ and I_p is the photo-current generated. Higher responsivity indicates greater sensitivity of photo detection and depends on material of PD as well as wavelength of detection.

$$R_\lambda = \frac{I_p}{P}(A/W) \tag{4.3}$$

The responsivity of the photodetector is measured using a setup similar to that employed for grating coupler measurements, with the exception on the output side with transfer printed PD, as illustrated in Figure 4.14. Optical input is provided by a tunable light source (Agilent 8164B) and a polarization controller maintains TE optical input by directing light through a single-mode fiber at a 14-degree angle to couple with the grating coupler on the input side.

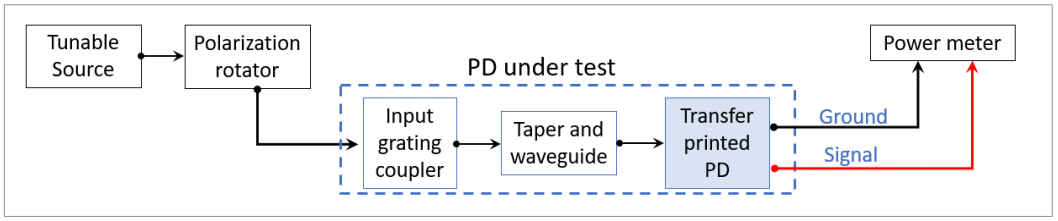


FIGURE 4.14: Block diagram showing experimental setup used for responsivity measurement of photodetectors.

The photodetectors are coupled to the waveguides in three distinct manners, and their responsivity is determined by applying a reverse bias voltage of 0.6 V. This bias is applied by probing the ground and signal pads and the resulting current is measured using a Keithley power meter. Three different optical input power (P_{in} to PD) 0.65 mW, 1 mW and 1.3 mW are supplied to the PDs, through the input grating coupler. The details of the power reaching the PD are provided in the appendix with the calculations (refer to Figure A.8 and A.9 for details). The photo-current generated for these optical input powers to the PD is illustrated in the current-voltage plot (Figure 4.15 a, b and c). The higher the optical input to PD, the more current generation. Each optical input is plotted for all three coupling mechanisms. For instance, the supplied optical input of 1.3 mW generates photo-current 0.2 mA for butt coupling type PD, 0.4 mA for grating coupling type PD and 0.8 mA for evanescent coupling type PD as in Figure 4.15 (c). Though the optical input calculated at the end of silicon taper is 1.3 mW for all three coupling, the difference in current generated arises from how efficient this light at silicon taper is absorbed by the PD in three different configurations.

There is a certain amount of loss before the light gets coupled to the PD. Unfortunately, the exact amount of loss cannot be directly measured and it varies based on the coupling

mechanism. Therefore, Ansys Lumerical FDTD software was utilized to estimate the interface loss through simulations (refer to Chapter 2, Figures 2.8, 2.9 and 2.10). We have calculated the responsivity based on the measured current generated and estimated optical power coupled to the PD. This optical power coupled could be lower in reality than in simulated values. Overall, the actual responsivity of the PD can be higher than what is presented.

The responsivity is calculated using Equation 4.3 as 0.13 A/W, 0.3 A/W, and 0.6 A/W for butt, grating, and evanescent coupling respectively for optical input of 1.3 mW.

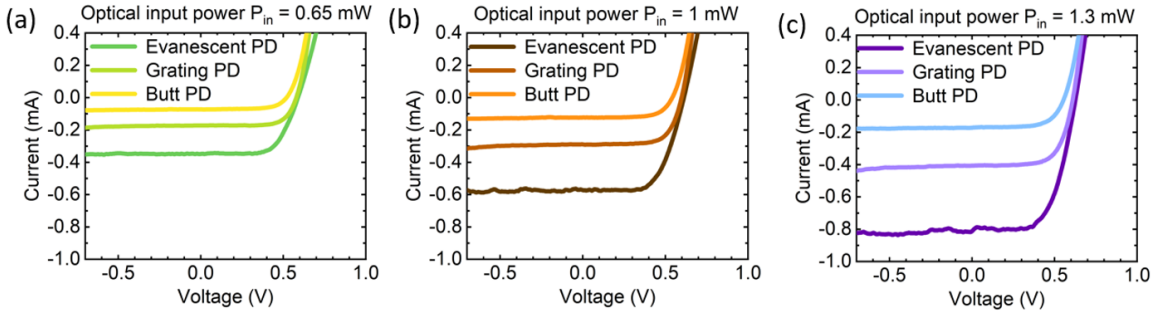


FIGURE 4.15: Current voltage plots for reverse bias of 0.6 V at 1550 nm, for following optical input supplied to PD (a) 0.65 mW, (b) 1 mW and (c) 1.3 mW.

The comparison between measured and simulated responsivity is presented in the Table 4.1 for an optical input of 0.65 mW. The measured values of current generated (-0.077 mA) and responsivity (0.13 A/W) are extracted from Figure 4.15 (a).

In simulations, it is found that only 40 % of the optical input is coupled to the PD in the edge-coupling scenario after considering interface losses. For the optical input of 0.65 mW, this corresponds to 0.26 mW (40 % of 0.65 mW) of optical power expected to be coupled to the PD. The simulated responsivity is obtained by dividing the measured current generated (-0.077 mA) by the simulated optical power input (0.26 mW), resulting in an expected responsivity from simulations as 0.3 A/W. Since there is no exact way of measuring the light coupled out of the waveguide to PD, and simulated values are obtained from 2D designs, there is a possibility of large error here.

TABLE 4.1: Table comparing calculated (Calc) and measured (Meas) responsivity (Resp), P_{in} being optical input power and I_{gen} being current generated.

Coupling	**Sim. P_{in} to PD**	**Calc. Resp**	I_{gen}	**Meas. Resp**
Edge	40 %	0.3 A/W	0.077 mA	0.13
Grating	62 %	0.45 A/W	0.18 mA	0.3
Evanescent	94 %	0.61 A/W	0.35 mA	0.54

4.4.4 Capacitance-voltage measurements

Capacitance-Voltage (C-V) measurements were performed on a 19 × 9 μm^2 mesa PD after transfer printing, as illustrated in Figure 4.16 (a and b). At a frequency of 2 MHz, the capacitance exhibited minor fluctuations with reverse bias voltage and reached saturation beyond -1 V at 100 fF, indicating complete depletion of the nid region. The observed increase in junction capacitance within the bias voltage range of 0.5 V to 2 V can be attributed, in part, to the presence of the p-doped InGaAs absorber. In the C-V measurement, the depletion region widens across doped layers with increasingly negative applied voltage, leading to a reduction in capacitance.

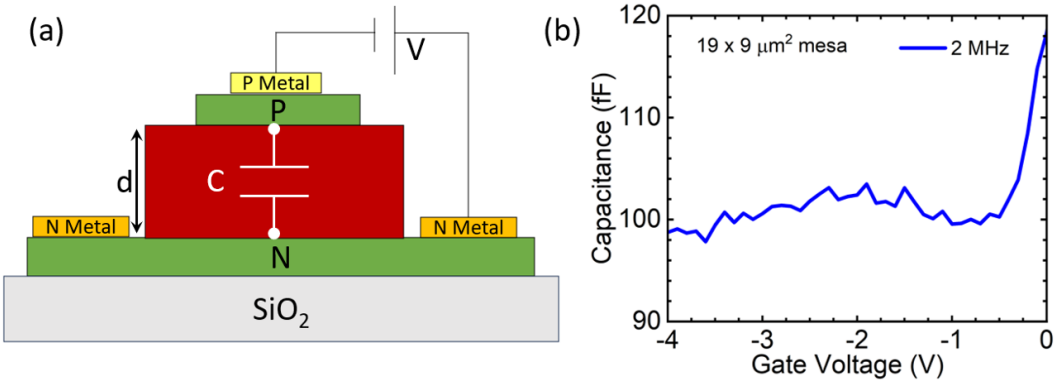


FIGURE 4.16: (a) Scheamtic cross-section of transfer printed butt-coupled PD with applied reverse bias for capacitance-voltage (C-V) measurement and (b) Plotted C-V result for 2 MHz.

4.4.5 Bandwidth measurements

The high-speed measurement setup, featuring a vertical optical fiber on the left and GSG probes connected to the right is displayed in Figure 4.17 (a). The setup is observed through a microscope, with illumination provided by a gooseneck lamp for visualization. In Figure 4.17 (b), the chip with an array of transfer-printed PDs is shown. Optical input is provided via a single-mode optical fiber (SMF, S/N: 03110005) positioned on a grating coupler on the left, while a GSG probe (FNU15) makes contact with the bond pads of the PD.

The experimental arrangement for the 3 dB bandwidth measurement is depicted in detail in Figure 4.18 (a). The optical signal at 1547 nm is generated by a diode laser (YE1430 from Eblana photonics) and further modulated through a high-speed 45 GHz Avanex SD40 Mach-Zehnder Modulator (MZM). Subsequent amplification is achieved using an Erbium-Doped Fiber Amplifier (EDFA, from Amonics, AEDFA-DWDM-23-B-FA), producing a 13 dBm output. To

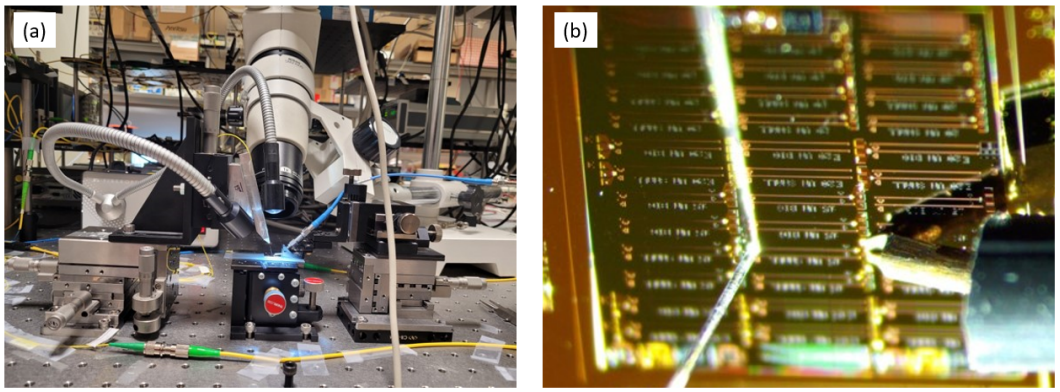


FIGURE 4.17: (a)Photo of experimental setup for high speed measurement and (b) Microscope image of chip with optical probing from left and electrical probe on right.

mitigate out-of-band amplified spontaneous emission noise, a 4 nm optical band-pass filter (OBF) from Santec (OTF-300-12S2) centered at 1547 nm is strategically placed in the optical path.

The filtered optical signal is then efficiently coupled to the Si waveguide via a grating coupler and directed towards the PD on the chip under test. The PD, connected through a GSG configuration, is linked to a 45 GHz bias tee, effectively splitting RF signals from DC components. A DC bias voltage of -0.6V is applied and the resulting current is precisely measured. The RF output from the PD is then detected using a 50 GHz network analyzer from Agilent (E8364C), with the entire setup meticulously calibrated using a reference 50 GHz photodetector from Anritsu (MN4765A). Initial electronic calibration of the network analyzer is carried out using Agilent's calibration module N4694-60001. As a next step, in the same setup shown in Figure 4.18 (a), a calibrated photodetector from Anritsu replaced the transfer-printed PD to calibrate other frequency components such as the MZM.

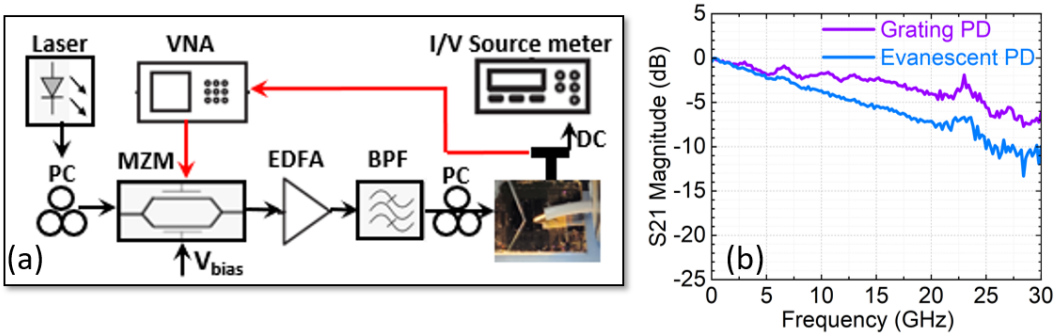


FIGURE 4.18: (a) Schematic diagram of bandwidth measurement and (b) S21 measurement for grating and evanescently coupled PD.

The input optical power, measured at 10.4 dBm between the polarizer and the fiber input to the grating coupler, is determined using an integrating sphere. This high input current is

expected to saturate the photodiode, although no direct experiments have been conducted to confirm this for the reported PDs.

The currents generated by the grating-coupled and evanescent-coupled PDs are recorded at -1.9 mA and -3.5 mA, respectively. Subsequently, their corresponding 3 dB bandwidths are calculated, yielding values of 17.5 GHz and 7.5 GHz, as visually represented in Figure 4.18 (b). Butt coupled devices was lossy at the interface and we could not couple sufficient light to generate a bandwidth response above the noise floor. Hence Figure 4.18 (b) does not include a plot for the butt coupled PD. Notably, despite both grating coupled and evanescent coupled PDs sharing identical bond pads and PD structures, the evanescent coupling configuration results in an open circuit between one of the ground and signal, leading to higher resistance. This discrepancy in resistance contributes to the observed differences in the 3 dB bandwidths of the two PD configurations [95]. Factors influencing PD bandwidth is analyzed further, to check the limiting factors in this process.

4.4.6 Bandwidth calculation

The final bandwidth of the photodetector is impacted by both the transit time limited bandwidth and the resistance-capacitance (RC) limited bandwidth as depicted in Equation 4.9 from [102].

Both electron and holes contribute to total transit time. However, it is to be noted that effective electron diffusion velocity is higher than the hole saturation velocity. In scenarios, where width of collector region dominates, the transit time limited bandwidth is provided by Equation 4.5 from [103], which depends majorly on electron transit time (τ_{tr}). This is the case with the epistack used in this PD, with collector region thickness dominates (250 nm). Transit time τ_{tr} is determined by Equation 4.4 from [104] where W_p is the width of the p-doped absorber (150 nm), W_i is the width of the nid region (250 nm), D_e is the diffusion of electrons in p-doped InGaAs ($\sim$ 200 cm^2/s), and v_p is the drift velocity of electrons in the nid region ($10^7 cm/s$). The calculated transit time for the PD is 1.7 ps, with a transit time bandwidth of 261 GHz using Equation 4.5.

$$\tau_{tr} = \frac{1}{W_p + W_i}\left(\frac{W_p^3}{3D_e} + \frac{W_i^2}{v_p}\right) \tag{4.4}$$

$$f_{tr} = \frac{2.8}{2\pi\tau_{tr}} \tag{4.5}$$

Figure 4.19, shows the trend of transit time for increase in intrinsic region thickness. For this graph, the total absorber thickness of PD is kept fixed at 400 nm, in which as the intrinsic region thickness increases, the thickness of p-doped absorber layer decreases. For example at 50 nm of intrinsic region, 350 nm of p-doped layer is considered, to obtain a total of 400 nm absorber.

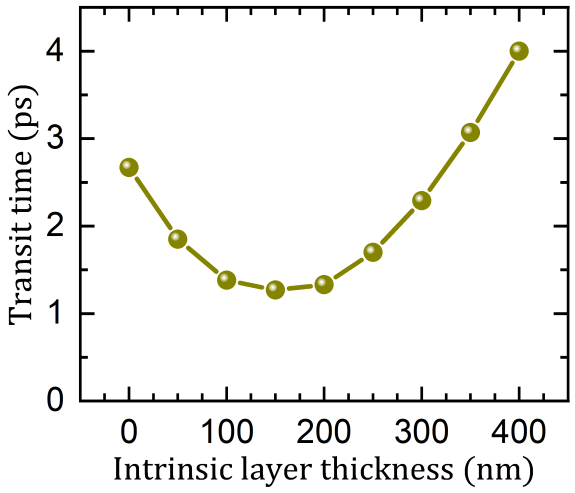


FIGURE 4.19: The transit time of electrons is plotted while keeping the total absorber thickness fixed at 400 nm. The variation in the intrinsic region thickness is plotted, while the remainder consists of the thickness of the p-doped absorber layer.

Generally electron drift in intrinsic region takes longer time which is seen by increase in transit time beyond 200 nm in the graph. In that case, below 200 nm of intrinsic layer thickness, the transit time is expected to reduce. On the contrary, it is seen increasing, which is due to the fact that, as the intrinsic thickness reduces, p-doped absorber layer thickness increases, thus diffusion of electrons takes a longer time below 200 nm. Thus we have chosen a thickness of 250 nm for nid absorber layer in the epistack, to take advantage of higher transit time.

Thus we notice that transit time limited bandwidth is not the limiting factor to the overall bandwidth of the photodetector.

4.4.6.1 RC limited bandwidth

There are many sources of resistance involved in a PD. There is contact resistance between p metal and p-contact layer, bulk resistance of the PD, p to n lateral resistance and n contact

resistance with N-InP.

It has been optimized earlier in the group for p metal (Ti/Pt/Au) on p-doped InGaAs and is expected to be in 10^{-4} to 10^{-5} Ωcm^2 range. n contact resistivity is measured during fabrication using TLM patterns and four probe measurement. The samples are annealed in a nitrogen atmosphere for 5 minutes at 350 $^{\circ}C$ in a tubular furnace. After which contact resistivity reduced from 6 x 10^{-4} Ωcm^2 to 5 x 10^{-5} Ωcm^2.

The lateral device resistance (R) is given by Equation 4.6, where ρ represents resistivity, n denotes the doping of N-InP (2 x 10^{18} cm^{-3}), e signifies the electronic charge (1.6 x 10^{-19} C) and μ represents the electron mobility in N-InP ($\sim$ 5000 $cm^2V^{-1}s^{-1}$). The length (L) is the distance between N and P metal contacts of the PD (5 μm), and the area (A) is calculated with W as the width of N metal (15 μm) and T being the thickness of N-InP (150 nm) as shown in Figure 4.20 (a).

$$R = \rho\frac{L}{A}(\Omega); \rho = \frac{1}{ne\mu}; A = T \times W \tag{4.6}$$

Given these values, the device resistance, arising from the distance between N and P metal contacts of the PD, is calculated to approximately $\sim$ 250 Ω. I-V measurement between n-n metals are provided in Figure 4.20 (b), (where the distance between n metals is 12 μm) with a resistance value of 461 Ω.

Thus we see that lateral resistance is the limiting factor to the overall bandwidth of the PD. This can be reduced by increasing the thickness of N-InP and minimizing the distance between the n and p contacts.

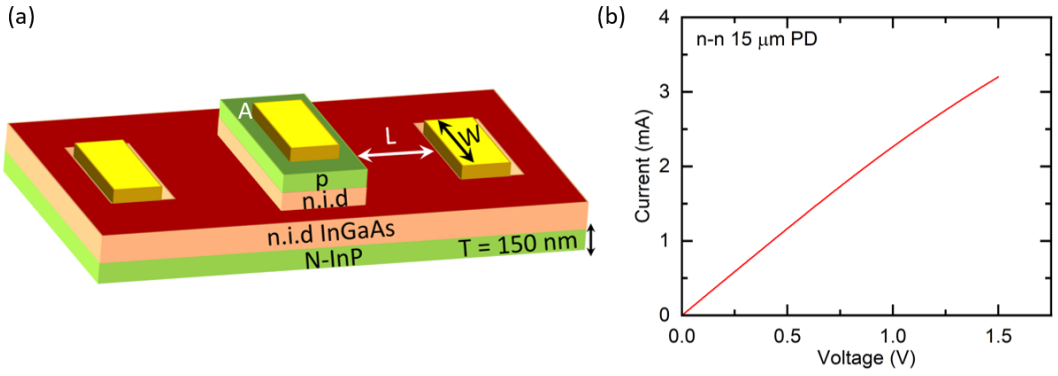


FIGURE 4.20: (a) Schematic of PD with terms involved for lateral resistance calculation and (b) Measured I-V characteristics between n to n metal contact for 15 μm by 6 μm n metal.

Having seen the resistance, this section focus on calculation of capacitance for increase in intrinsic region thickness using Equation 4.7. Where k represents the dielectric constant (approximately $\sim$ 11.6 for $In_{0.53}Ga_{0.47}As$), ϵ_o is the vacuum permittivity and A is the area of the p-mesa (19 $\times$ 9 μm^2) and d is the depletion depth. From the Equation 4.7, we see that capacitance depends on depletion depth. Figure 4.21 (a), shows a linear increase in RC limited bandwidth as the intrinsic thickness increases, due to linear reduction in capacitance and a fixed resistance R of 250 Ω.

$$C = \frac{k\epsilon_o A}{d} \tag{4.7}$$

$$f_{RC} = \frac{1}{2\pi RC} \tag{4.8}$$

$$f = (\frac{1}{f_{RC}^2} + \frac{1}{f_{tr}^2})^{-\frac{1}{2}} \tag{4.9}$$

Despite the low calculated transit time of 1.7 ps as in Figure 4.19 with a transit time bandwidth is 261 GHz, and the low measured capacitance 100 fF from Figure 4.16 (b), the overall device bandwidth is affected by the high lateral resistance of 250 Ω. The final bandwidth of the PD is constrained by the RC bandwidth as in Equation 4.8 and as shown in Figure 4.21. There is no transit time limitation in the PD. To address this RC limitation, one potential solution is to enhance the doping and/or thickness of the n-layer while concurrently reducing the separation between the n-metal and p-mesa. These adjustments aim to mitigate the impact of the high lateral resistance and thereby improve the device's performance.

4.4.7 Data-transmission measurements

The setup, analysis and data processing for the transmission measurements (shown in Figure 4.22) are executed by Cleitus Antony from systems lab at Tyndall National Institute where all high speed measurements are done. My part was to build optical coupler setup and optimize fiber probing to the chip.

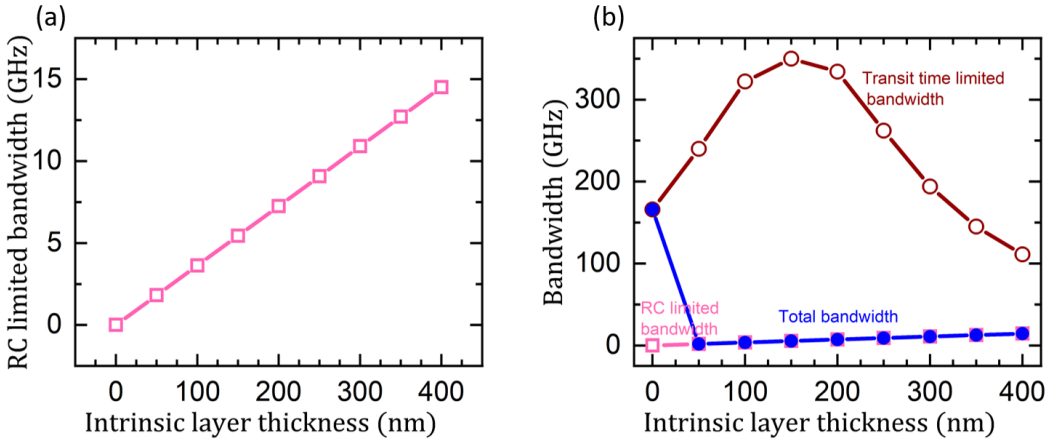


FIGURE 4.21: (a) RC limited bandwidth is plotted for varying intrinsic region thickness and (b) Graph showing transit time limited bandwidth, RC limited bandwidth and total bandwidth of the PD as a function intrinsic region thickness.

For the purpose of data transmission measurements, a digitally pre-compensated 50 GBaud Non-Return to Zero (NRZ)/Pulse Amplitude Modulation 4 (PAM4) pseudorandom binary sequence 15 (PRBS15) signal is utilized. This signal is generated through a 44 GHz Micram digital-to-analog converter (DAC) and serves to modulate an optical carrier at a wavelength of 1550 nm. The modulated optical signal undergoes amplification and filtering stages, facilitated by an Erbium-Doped Fiber Amplifier (EDFA) and an optical band-pass filter (OBF) respectively.

Subsequently, the modulated signal is directed to the on-chip PD through a polarization controller and grating coupler, while maintaining a reverse bias. The resulting output is then meticulously recorded using a high-performance sampling oscilloscope. Figure 4.22 provides a visual representation of the measured open eye diagrams for different data rates, including 25 Gb/s and 50 Gb/s in Non-Return to Zero (NRZ) and 50 Gb/s and 100 Gb/s in PAM4.

It is noteworthy that the 100 Gb/s PAM4 clear eye diagrams presented in Figure 4.22 (e and j) have undergone digital post-processing. This involved the application of a symbol-spaced 12-tap linear feed-forward equalizer to enhance the quality of the open eyes.

4.5 Conclusion and discussion

Successful demonstration of an ultra-thin InGaAs PD with three different coupling mechanisms were shown, via direct bonding using dual sacrificial layer. The best performance of the PD is

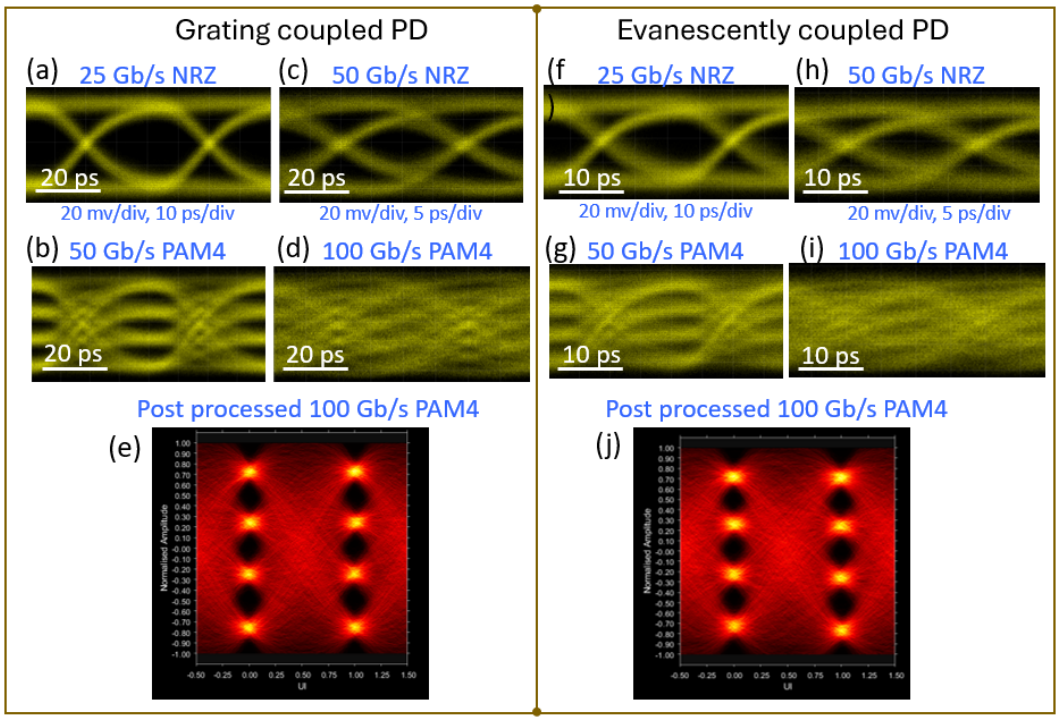


FIGURE 4.22: Eye diagram measured for grating coupled PD at (a) 25 Gb/s and (c) 50 Gb/s NRZ; (b) 50 Gb/s and (d) 100 Gb/s PAM4; (e) post processed 100 Gb/s PAM 4 with equalizers. Eye diagram measured for evanescently coupled PD at (f) 25Gb/s and (h) 50 Gb/s NRZ; (g) 50 Gb/s and (i) 100 Gb/s PAM4 and (j) post processed 100 Gb/s PAM4 with equalizers.

responsivity of 0.6 A/W, a dark current of 48 nA, a 3 dB bandwidth of 17.5 GHz and an open eye at 100 Gb/s post-processing.

The major issue in this work is high device resistance and coupling loss in co-planar butt coupled PD, which lowers the device bandwidth and responsivity. The learnings to overcome these issues are listed below.

To increase bandwidth

Epitaxial stack modifications include increasing the thickness of N-InP to reduce lateral resistance and simulation optimization for the thickness of p-doped and n-i.d absorber layers, aiming for lower capacitance simultaneously low transit time.

However, increasing the thickness of InP can impact optical mode coupling from silicon waveguides to photodetector. For butt coupling mechanisms, achieving co-planar integration between the Si and InGaAs absorber would require more oxide etching to accommodate the increased thickness of InP. In grating and evanescent coupling mechanisms, the optical mode would need to propagate through a thicker layer of InP when transferring from silicon to InGaAs, lowering mode absorption in the PD.

Therefore, simulations are necessary to optimize the thickness of InP that reduces lateral resistance without significantly affecting mode absorption during coupling from silicon to the PD.

Regarding PD design, the lateral distance between the p and n metal contacts should be reduced to decrease device resistance. However, caution must be taken to ensure that bringing the n metal too close to the p mesa does not result in the n metal absorbing light from the p mesa. Therefore, cross-sectional simulations of the PD are necessary to determine the optimal proximity of the n metal to reduce resistance without absorbing the optical mode.

Incorporating this, shall shrink the overall PD dimension as well. Along with making P mesa wider by couple of μm than silicon taper end width, to couple maximum light and robust to misalignments during TP.

To increase responsivity

Regarding butt coupling in-fill method, major loss is at the interface which reduces the responsivity of the PD. To overcome that, the a-Si infill requires e-beam patterning technique to guide light efficiently from silicon taper to wider P mesa.

All these modifications would enable lower RC values which leads to higher bandwidth, efficient coupling leads to increase responsivity and the shrinking PD device size lowers dark current.

Chapter 5

Conclusion and future work

5.1 Results overview

Demand for PICs is ever increasing with growing data centres and telecom industry. The aim of the thesis was to develop a method towards compact PIC through micro-transfer printing technology. A compact PIC is crucial as it has low footprint saving expensive wafer space, power efficient and reduces cost of manufacturing and packaging with enhanced performance. To achieve compact PIC, a co-planar in-fill method of integration was aimed for thin active devices. This thesis successfully demonstrates integration of same InGaAs photodetectors via co-planar, grating and evanescent coupling mechanism to SOI platform, as a step towards compact PIC.

Various coupling mechanisms for integrating PDs into SOI platform are detailed in Chapter 2. It begins with introducing the patterned SOI wafer received from Cornerstone MPW run. The way in which PD coupling is achieved by three different fashions to this SOI wafer was elaborated. Each coupling mechanism from silicon waveguide to the PD is described via simulations. Grating coupler theory is explained with simulation optimization for 1550 nm grating coupler, achieving coupling efficiencies of 66 %. Evanescent coupling is also explored, leveraging a trench in silicon to scatter light upwards to the III-V device without tapering. Apart from simulations, processing of co-planar coupling is also detailed with its challenges and solutions. For this butt-coupling, in-fill with a s-Si was experimented using PECVD and evaporation methods. The selective removal of a-Si was tried using CMP and photoresist lift-off techniques. Finally, evaporation of a-Si with lift-off technique is opted.

Despite the challenges posed by the butt coupling approach, further process optimization such as patterning the a-Si can enhance the coupling between silicon and PD. This could potentially achieve up to 98 % power coupling. Grating and evanescent coupling mechanisms emerge as being relatively straightforward, albeit grating couplers exhibit sensitivity to wavelength and polarization, limiting the operational range of the PD. Addressing issues like substrate leakage is crucial, with proposed solutions including grating teeth apodization. Meanwhile, the evanescent approach, while showing minimal loss, would benefit from a taper down design in silicon. Overall, these optimized mechanisms play a pivotal role in PD integration onto the SOI platform and their performance, as further discussed in subsequent chapters.

With the coupling mechanism for integrating the PD sorted, next we discussed optimizing the sacrificial layer for efficient undercut and transfer printing of PD coupons in Chapter 3. It established a combination of two sacrificial layer instead of individual release layers used previously along with experimentation on dilution of ferric chloride wet etchant. A novel dual release layer, comprising of InGaAs on top of AlInAs is introduced and extensively studied for its impact on interface smoothness, etch crystallinity, etch rate and selectivity.

The chapter includes a review of wet etchants for InGaAs and AlInAs and compares how ferric chloride is better in etch rate than others. Optimal results are achieved with a 400 nm InGaAs release layer atop 100 nm or 50 nm AlInAs, facilitating fast, nearly isotropic etching and smooth interfaces, allowing direct bonding of coupons to the target wafer. Notably, these benefits are achieved at room temperature, saving time, cost and energy.

Additionally, the study demonstrated that a 1:5 dilution of ferric chloride with water offers similar etch rates, improved selectivity and enhanced linearity compared to a 1:2 dilution. These advancements enhance the yield of transfer-printed devices and improves the undercut process for coupons on InP-based epitaxial stacks. Although time constraints limited wafer exploration, future investigations could involve fluid mechanics-based simulations to better understand the undercut process's complexity.

Using the coupling mechanisms discussed in Chapter 2 and dual sacrificial layer in Chapter 3, a successful demonstration of an ultra-thin InGaAs PD via direct bonding is showcased in chapter 4. It emphasizes the significance of the PD uni-traveling carrier epitaxial structure for high-speed photodetection. The PDs exhibit notable performance metrics, including a responsivity of 0.6 A/W, a dark current of 48 nA, a 3 dB bandwidth of 17.5 GHz and an open eye at 100 Gb/s after processing.

However, challenges such as high device resistance and coupling loss in co-planar butt-coupled PDs are identified, which diminishes device bandwidth and responsivity. Strategies to address these issues include modifying the epitaxial stack to increase the thickness of N-InP and reducing the lateral distance between p and n metal contacts for reduced lateral resistance. Optimizing the thickness of p-doped and n.i.d absorber layers for lower capacitance and transit time, can increase device bandwidth further. Additionally, widening the P mesa compared to the silicon taper end width is proposed to enhance light coupling and resilience to misalignment during transfer printing.

To enhance responsivity, modifications to the butt coupling in-fill method are suggested, particularly focusing on reducing interface losses through e-beam patterning of the a-Si infill to efficiently guide light from the silicon taper to the wider P mesa. These proposed modifications aim to lower RC values, increase absorption and shrink the PD device size, ultimately leading to higher bandwidth, improved responsivity and lower dark current.

We have successfully developed a high-speed photodetector, which has been directly bonded to the SOI wafer facilitated by the newly optimized dual sacrificial layer. Furthermore, utilizing transfer printing technology, we have integrated the same photodetector employing three distinct coupling mechanisms on the target wafer. Key insights gained from the co-planar infill process are also presented, with details of encountered challenges and proposed potential solutions to address them.

5.2 Future work

Thus we have shown a step forward towards compact PIC, by integrating such tiny high performance photodetector to SOI, with extremely prominent results for first run. Moving ahead the plan is to continue in the same direction by integrating thin laser to SOI. To reduce laser size, we need high optical confinement in thin quantum well stack, which increase gain. The challenge here is to overcome the optical loss from metal contacts which are close to quantum well due to reduced thickness. This section presents initial simulation done for laser, however, lot more optimization and process are required for successful integration of laser to PIC in future.

Figure 5.1 (a) shows a 3D schematic view of a thin ridge laser integrated in co-planar fashion to silicon ridge waveguide. Laser consists of SiO_2 on the bottom, InP on top of it, with active

quantum well stacks above InP as depicted in cross-section from Fimmwave software (Figure 5.1 b). To keep the metal contacts apart from quantum wells, ridge structure is employed. Ridge has a shoulder and a rib part on top of it. The metal is deposited over the rib part which is at a higher thickness compared to active quantum well, giving some distance for the mode to expand without being absorbed by the metal. The result of simulations carried out are shown in Figure 5.2.

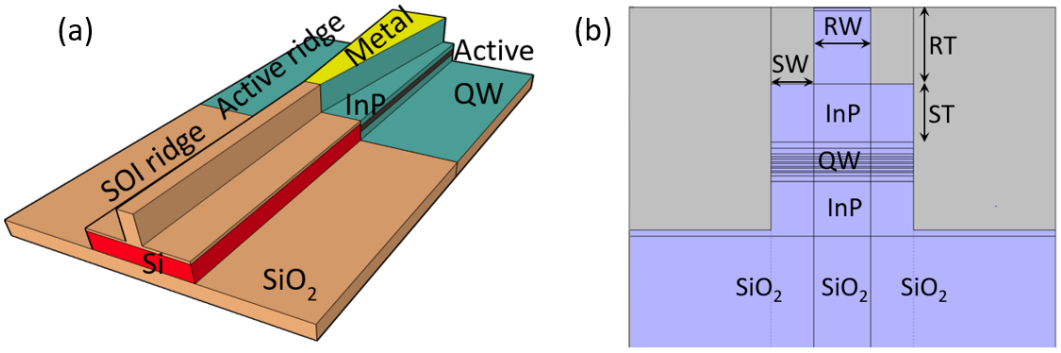


FIGURE 5.1: (a) Schematic of thin laser integrated in co-planar fashion with silicon waveguide and (b) Cross-section of laser from Fimmwave simulation software, showing the position of quantum wells in the ridge, where RW is Ridge Width, SW is Shoulder Width, RT is Rib Thickness and ST is Shoulder Thickness.

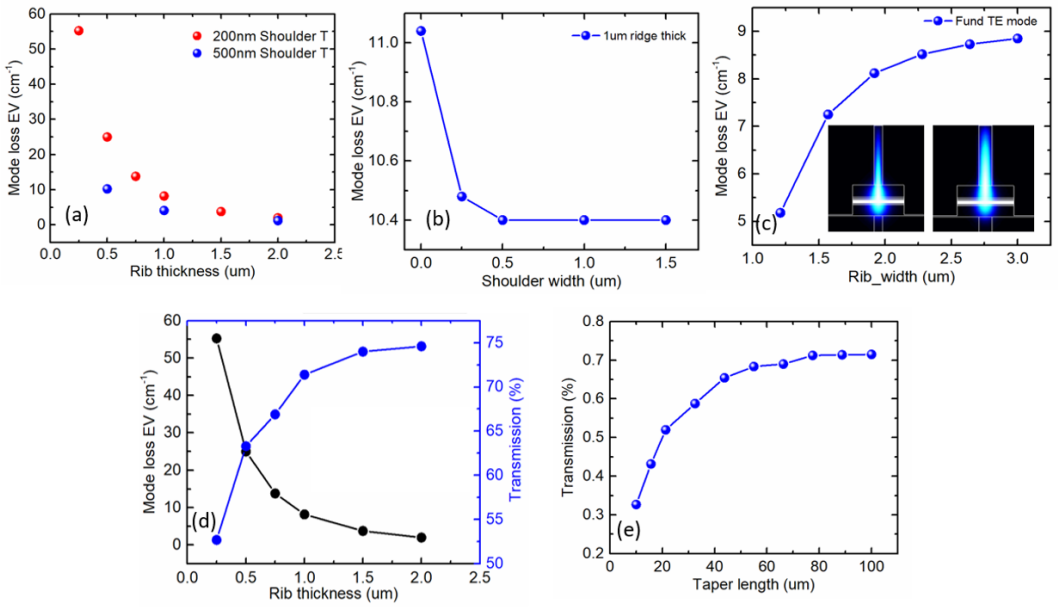


FIGURE 5.2: Mode loss is plotted for variation in (a) Shoulder thickness, (b) Shoulder width, (c) Rib width, with inset showing 2 μm and 3 μm mode confinement, (d) Spectra showing the impact of rib thickness on mode loss and transmission of optical mode out of the active taper and (e) The transmission of fundamental TE mode for different taper length in active device is plotted.

In this structure, lot of parameter sweeps were carried out to check the required Ridge Width (RW), Shoulder Width (SW), Rib Thickness (RT) and Shoulder Thickness (ST) to confine the

mode tightly in quantum well region with least absorption in metal. The taper length of the laser is adjusted to obtain maximum light transmitted from laser to silicon waveguide. All these are shown in Figure 5.2. It is observed that to have least mode loss it is better to have higher rib thickness around 1.5 μm and wider shoulder width of around 0.5 μm along with narrow rib width. And transmission gets saturated beyond 60 μm of taper length. Further more optimizations are required to confine mode without loss within a thin 500 nm.

5.3 Conclusion

The photodetectors presented in the thesis are well-suited for integration into photonic integrated circuits, potentially allowing the production of almost 1 million devices per 75 mm InP wafer, including the transfer printing area (90 μm x 50 μm) of the photodetector.

We have successfully demonstrated PD integration, moving forward, the same can be shown for laser and modulator integration as well. Overall idea is to build a compact photonic circuit integrating all components using the same technique. Benefit of our approach is that it can be integrated with CMOS foundries via transfer printing and onto Si or SOI platform which are commonly used. Thus, our process is economical and mass produced with replicable nature.

Appendix A

Appendix

A.1 Summary of etch rates

Summary of wet etches for InP, InGaAs and InGaAsP is provided in Table A.1. Details of dry etches used for fabrication process in this thesis are given in Tables A.2 and A.3. The etch rates can vary by couple of nm from time to time.

TABLE A.1: Table containing wet etches for III-V materials used.

Material	**Etchant**	**Etch rate**	**Selective to**
InP (100)	HCl	10 μm/min	InGaAs
InP	HCl:H_3PO_4 (1:4)	240 nm/min	InGaAs
InGaAs	H_3PO_4:H_2O_2:H_2O (1:1:8)	400 nm/min	InP

TABLE A.2: Table containing etch rates for Si, SiO_2, SiN, InP and photoresist (PR) used in chlorine based chemistry, with ratio of gases (sccm).

Material	**Etch rate**	H_2	Cl_2	CH_4	N_2
Si	50 nm/min	-	20	-	40
SiO_2	7 nm/min	-	20	-	40
Chrome	2 nm/min	-	20	-	40
AZ5214E (PR)	50 nm/min	-	20	-	40
ZEP (PR)	38.5 nm/min	-	20	-	40
SiO_2	30 nm/min	13.5	23	19	-
SiN	60 nm/min	13.5	23	19	-
InP	300 nm/min	13.5	23	19	-

TABLE A.3: Table containing etch rates for Si, SiO_2, SiN and photoresist (PR) used in Fluorine based chemistry, with ratio of gases (sccm).

Material	**Etch rate**	SF_6	C_4F_8	H_2	**He**
Si	772 nm/min	30	-	-	-
SiO_2	50 nm/min	30	-	-	-
SiN	273 nm/min	30	-	-	-
SiO_2	186 nm/min	55	75	-	-
SiN	250 nm/min	55	75	-	-
Si	400 nm/min	75	55	-	-
SiO_2	220 nm/min	75	55	-	-
S1813 (PR)	80-100 nm/min	75	55	-	-
AZ5214E (PR)	80-100 nm/min	75	55	-	-
Si	13.5 nm/min	-	10	15	175
SiO_2	220 nm/min	-	10	15	175
S1813 (PR)	210 nm/min	-	10	15	175
AZ5214E (PR)	20 nm/min	-	10	15	175

A.2 Mask design for dual release layer testing

The mask employed for analyzing the samples with dual release layer is displayed in Figure A.1. Purple regions in mask, shall be covered with hard mask for protection, while the white

background regions undergo etching, during the fabrication process. The design features three wagon wheels with varying spoke angles, along with other shapes to assess etch rates across different lattice planes.

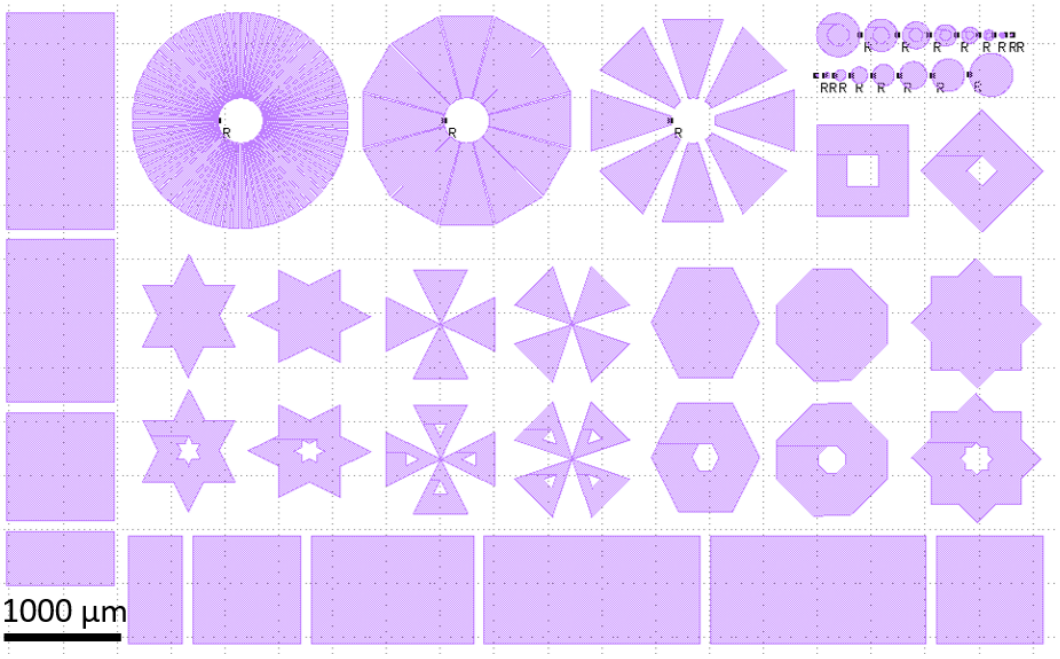


FIGURE A.1: Various shapes, in different sizes used in mask for experimenting etch rate of dual release layer.

A.3 Reason for separate samples for linearity measurement

In chapter 3, for linearity measurement, individual samples were used for each data point. Reasons for the same is discussed here.

In this process, samples devoid of tethers are partially undercut to a length (X) and then removed from the wet etchant. During microscopic observation of these coupons, two distinct boundaries become apparent. The first is a white boundary located 8 μm inside the coupon edge and the second is a black inner boundary positioned at 24.5 μm inside the coupon edge, as illustrated in Figure A.2 (a). While the presence of only the black inner boundary is anticipated due to undercut and absence of release materials. The SEM analysis reveals that due to the partial removal of the release layer and the absence of tethers, the portion of the coupon above the removed release layer lacks support, leading it to bow and flap over a certain length (Y) towards the substrate, as indicated in the schematic cross-section with black dotted squares in Figure A.2 (b). Due to gravity, this flapped section touches the substrate, resulting in a length (Y) between the coupon edge and the region where the flapped coupon contacts the substrate.

In SEM measurements, this length (Y) is determined to be 10 μm, while the length from the coupon edge to the undercut (X) is measured as 25.05 μm. Comparing these SEM values with the microscope values, it is deduced that the white boundary corresponds to the length of flapped coupon touching the substrate (Y). Whereas, the inner black boundary is arising from the actual undercut of release layer (X), as illustrated in Figure A.2 (d). This verification also affirms that the microscope-measured values of undercut fall within an error range of $\pm$ 2 μm.

This is main reason to use separate sample pieces for each data point in the measurements presented in Figure 3.10. Initially, the same sample was used for different times, for instance, immersing it in the wet etchant for 10 minutes, removing it for microscope measurement and repeating the process for 20 minutes, 30 minutes and so forth—yielded inconsistent and non-sensical data points. Subsequent SEM analysis on cleaved coupons revealed that the issue lay with the flapped coupons. When the sample without a tether was partially released and removed from the wet etchant, the coupon flaps, which Upon re-immersion, altered the way the wet etchant accessed the release layer. This acts as barriers, hindering a smooth inflow and created trouble in undercut rate. Consequently, employing individual samples for each wet etch measurement became imperative to ensure consistent and reliable results.

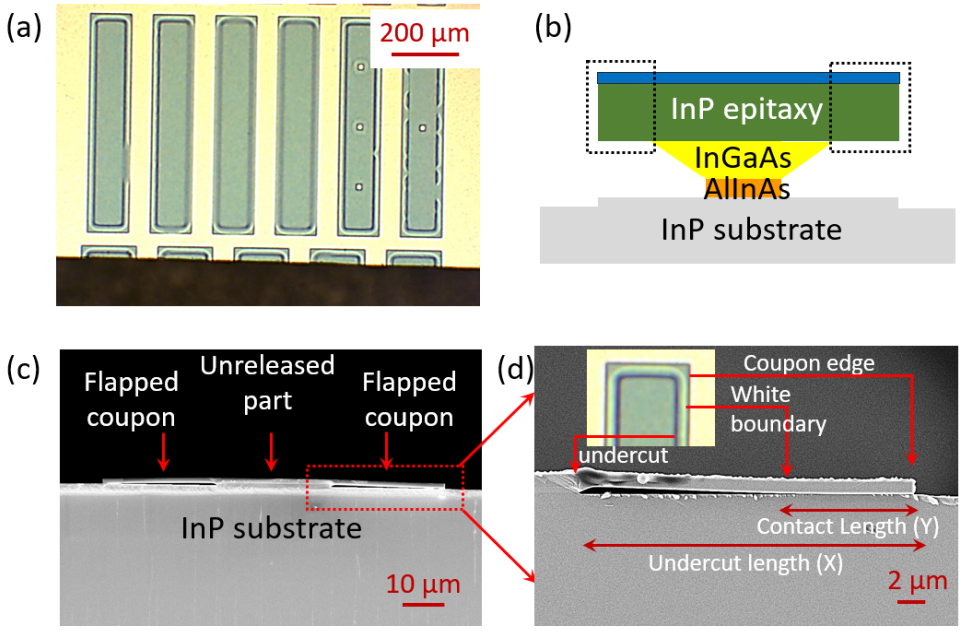


FIGURE A.2: (a) Microscope image of partially released coupon showing white and dark boundaries, (b) Schematic showing partial release and the black dotted region of coupon flap due to absence of tether, (c) Cross section SEM of the cleaved coupons showing flapped coupons on either side and (d) Zoom-in image showing part of the coupon flapping touches the substrates creating white boundary.

A.4 PD Epitaxial stack

The photodetector epitaxial stack (A3488) is grown on a nominally lattice-matched (100) oriented n-InP substrate using MOCVD at Tyndall, as illustrated in Figure A.3 (a and b). Top view of PD design obtained from KLayout software provides various lithographic steps and details of spacing between each level as in Figure A.3 (c).

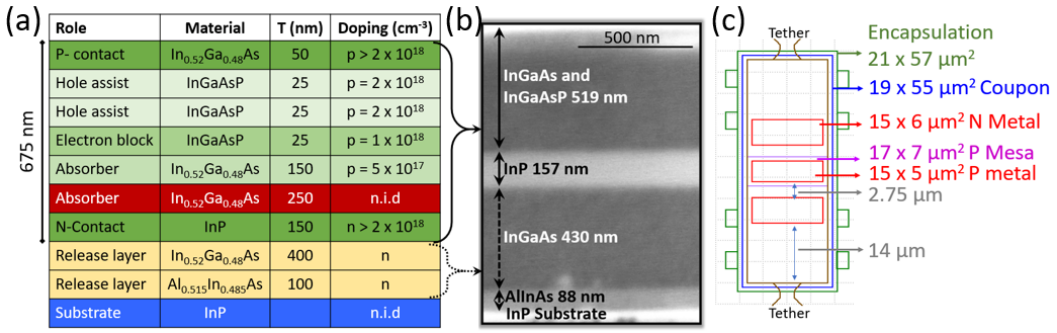


FIGURE A.3: (a) Epitaxial stack used for high speed PD grown on InP sustrate with dual release layer for transfer printing, (b) SEM cross-sectional depiction of the as-grown III-V material and (c) Dimensional specifications of PD coupons for each lithography level.

A.5 PD Tether design and placement

The source wafer fabrication involves optical lithography, with mask designs created using KLayout software. Figure A.4 shows the graphic design system (GDS) displaying three tether types employed. The neck, with widths of 2.5 μm and 3 μm, represents the point where the tether breaks during coupon retrieval. Meanwhile, the foot of the tether, depicted in Figure A.4 (a, b and c) prevents coupon from collapsing, post-release. All these variations are done approximately as simulating these features involves lot of variable related to material and dimensions.

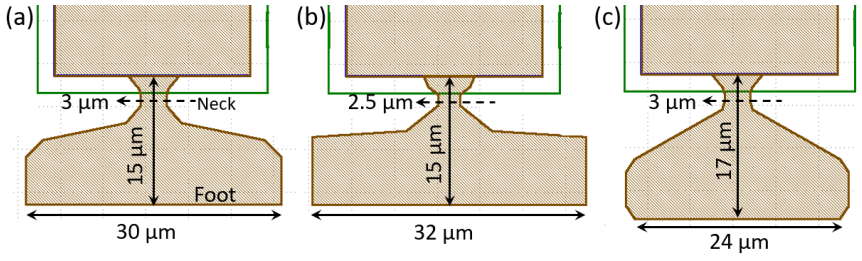


FIGURE A.4: Design showing different type of tethers used for PD coupons with variation in foot length, width and neck width.

Every single tether type has four variations in their placement around the PD coupon as shown in Figure A.5. There are no tethers along one of the lengths of the PD, to facilitate intact transfer printing of PD to silicon waveguides in butt coupled scenarios. So far PD with two and three tethers as shown in Figure A.5 (c and d), are picked and printed successfully, for all three different tether designs.

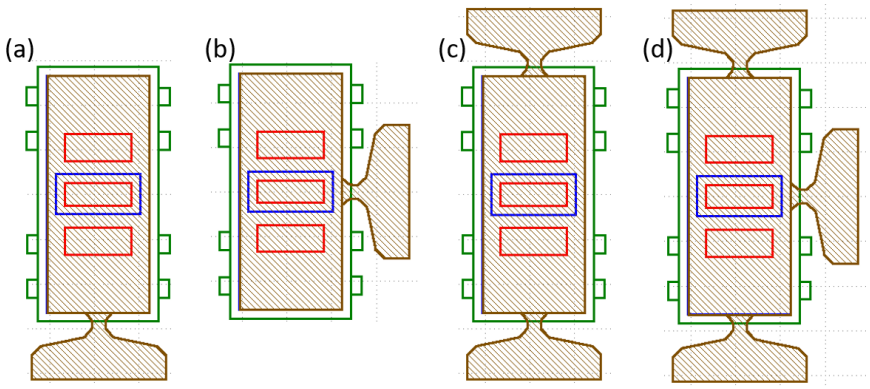


FIGURE A.5: PD source coupon with tether variations (a) Single tether along coupon length, (b) Single tether along coupon width, (c) Two tethers on either side of its length and (d) Three tethers around the coupon except the front side allowing for close transfer printing to silicon waveguide.

A.6 PD Source wafer fabrication

The PD coupons measuring 21 μm x 57 μm, were fabricated following the processing sequence depicted in Figure A.6, on the epitaxial wafer as shown in Figure A.3 (a). Initially, an anode metallization composed of Titanium, Platinum and Gold (Ti/Pt/Au:30/50/200 nm) is deposited through lift-off lithography onto the P contact layer, as illustrated in Figure A.6 (a).

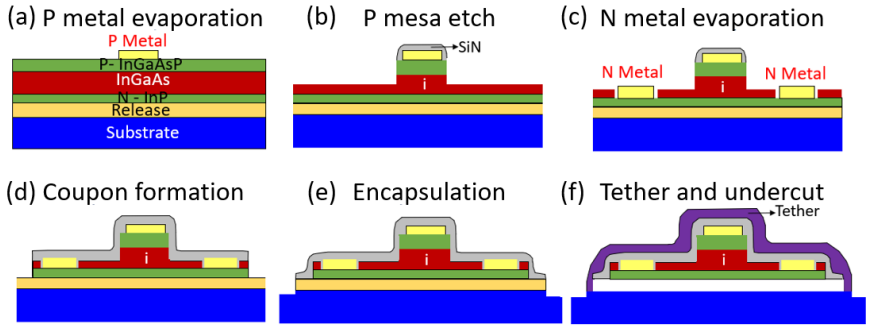


FIGURE A.6: Fabrication process of the PD coupon on the source wafer: (a) Deposition of P metal on the P-contact layer, (b) Etching of P mesa to define the active area of the PD, (c) Evaporation of N metal on the N-contact InP layer, (d) Etching to create the PD coupon, (e) Protection of the coupon through SiN encapsulation and substrate etching to facilitate the undercut process and (f) Patterning of tethers followed by the undercut process, removing the release layer and separating the PD coupon from the substrate.

Subsequently, a mesa etch is performed into the n.i.d InGaAs absorber, utilizing SiN as a hardmask (Figure A.6 b). This is a dry etch process involving chlorine, methane and hydrogen gases which also etches InP. Hence it is difficult to stop the etch exactly on top of N-InP and also cannot afford etching of N-InP as its very thin (150 nm). Thus using an end point detector, this dry etch etch step is stopped in n.i.d InGaAs absorber layer. The process continues with N metal lithography and wet etching of the exposed InGaAs using a phosphoric acid and peroxide mixture, halting at the N-InP layer for the N metallization of Gold, Germanium and Nickel (Au/Ge/Au/Ni/Au: 14/14/14/11/250 nm) as shown in Figure A.6 (c). A 5 minute annealing at 350° C in a nitrogen atmosphere establishes ohmic contact. Employing SiN as a mask, the coupons are defined through wet etching the remaining InGaAs and the entire N-InP layer (figure A.6 d). A subsequent dielectric deposition serves as encapsulation, safeguarding the active material during the release etch. This dielectric also covers N-InP from all sides, preventing potential shorting between the P metal bond pad and N-InP during post-processing. The coupon is etched through the release layer into 200 nm of the substrate (Figure A.6 e), exposing the release layer for the undercut process. Finally, photoresist tethers with a thickness of 2.2 μm are established to connect the PD to the substrate, securing the coupon in place after the removal of sacrificial layer (Figure A.6 f). The PD coupons are released from the substrate through wet etching of dual sacrificial layers, utilizing a ferric chloride and water mixture (1:2) for 5 minutes at room temperature.

A.7 SOI target wafer design

Design of target chip received from cornerstone is given in Figure A.7 (a) measuring 4.5 mm by 5.5 mm. The zoomed section of one waveguide pattern is shown in Figure A.7 (b) after transfer printing of PD and post processing. It shows the reference grating coupler system with input and output couplers on the bottom and the top waveguide has only input coupler with PD transfer printed on output.

A.8 Calculation of optical power reaching photodetector

The SOI samples were equipped with a reference grating coupler system designed for the 1550 nm fundamental TE mode, as illustrated in Figure A.8 (a). Equivalent structures were employed to couple light to the PD (Figure A.8 b), with the distinction that they featured only

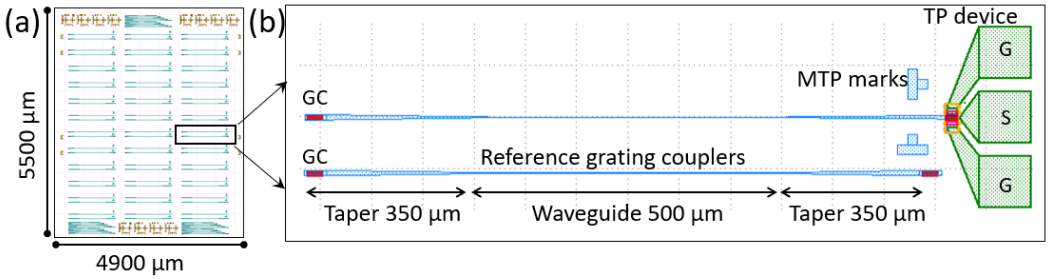


FIGURE A.7: (a) Starting stage of SOI target chip received from Cornerstone and (b) Zoom of one of the waveguide patterns after transfer printing of PD and post processing.

input couplers and the PD was transfer printed at the output end of the silicon taper. The optical power coupled to the PD was determined by measuring the reference grating coupler system using the schematic setup depicted in Figure A.8 (c). A tunable laser source (TLS) provided a specific optical power directed to an input single-mode fiber (SMF) through a polarization controller (PC) and the light from the output coupler was measured by an optical power meter.

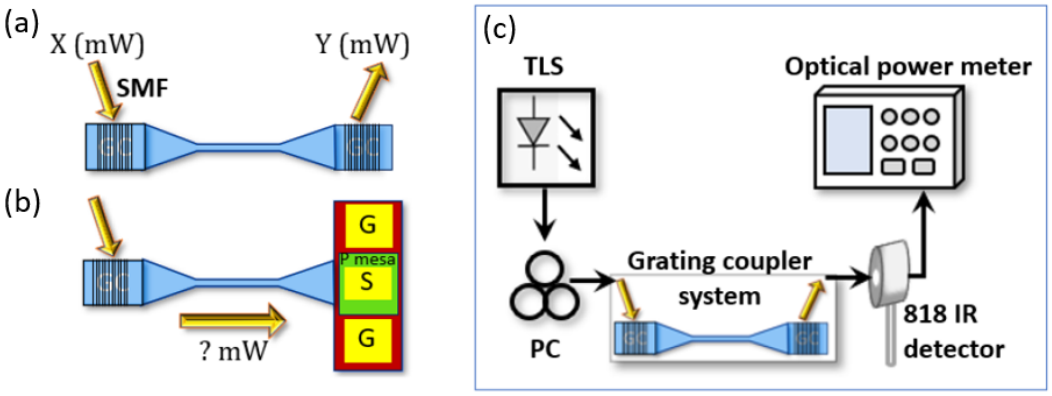


FIGURE A.8: (a) Reference grating coupler system with X (mW) optical power supplied to the input grating coupler and Y (mW) optical power measured from the output coupler, (b) Similar system with the transfer printed PD at the output, for which the supplied optical power needs to be determined and (c) Block diagram illustrating the vertical fiber-to-chip grating coupler test setup for measuring coupling efficiency

Image of Table A.9 outlines the step-by-step calculation of the coupled power, beginning with the optical power set at the tunable laser source (TLS). The power supplied to the input vertical fiber is denoted as X mW and is measured after passing through the polarization controller. The optical power diffracted from the output grating coupler is measured through the output vertical fiber (Y mW) using an optical power meter. The power lost due to both grating couplers, tapers and the waveguide is determined as X-Y mW. Assuming negligible loss from the silicon tapers and waveguide, the entire loss is attributed to the input and output grating couplers. Since they share similar designs, the loss contributed by each grating coupler

is considered equal. Consequently, the power lost solely due to the input grating coupler is calculated as (X-Y)/2 mW. The power reaching the photodetector is the difference between the optical power supplied to the input vertical fiber and the power lost due to the input grating coupler. This represents the power at the silicon taper end where the PD is transfer printed.

TLS Power (mW)	**P_{in} GC_{in} (X mW)**	**P_{out} GC_{out} (Y mW)**	**Loss due to both GC: (X-Y) mW**	**Loss due to GC_{in}: (X-Y)/2 mW**	**Power before PD: X-[(X-Y)/2] mW**
3	1.20	0.11	1.09	0.54	0.65
5	1.77	0.15	1.62	0.81	0.96
7	2.46	0.22	2.24	1.12	1.34

FIGURE A.9: Calculation of power at silicon taper end just before PD is provided in step by step manner. P_{in} GC_{in} is the power supplied to the input grating coupler. This GC_{in} is measured after the polarization controller just before the input GC. P_{out} GC_{out} is the output power measured from output grating coupler at 1550 nm for fundamental TE mode.

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