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# A simulation-based design method to transfer surface mount RF system to flip-chip die implementation

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**Abstract**

The flip-chip technology is a high chip density solution to meet the demand for very large scale integration design. For wireless sensor node or some similar RF applications, due to the growing requirements for the wearable and implantable implementations, flip-chip appears to be a leading technology to realize the integration and miniaturization. In this paper, flip-chip is considered as part of the whole system to affect the RF performance. A simulation based design is presented to transfer the surface mount PCB board to the flip-chip die package for the RF applications. Models are built by Q3D Extractor to extract the equivalent circuit based on the parasitic parameters of the interconnections, for both bare die and wire-bonding technologies. All the parameters and the PCB layout and stack-up are then modeled in the essential parts' design of the flip-chip RF circuit. By implementing simulation and optimization, a flip-chip package is re-designed by the parameters given by simulation sweep. Experimental results fit the simulation well for the comparison between pre-optimization and post-optimization of the bare die package's return loss performance. This design method could generally be used to transfer any surface mount PCB to flip-chip package for the RF systems or to predict the RF specifications of a RF system using the flip-chip technology.

**Introduction**

Flip chip is a promising technology that has several advantages over wire-bonding, such as short electrical interconnection, low cost, and high reliability. Lots of efforts were spent to characterize the performance of flip-chip [1][2], to build its equivalent model [3][4] and to investigate the packaging effects [5]. Some applications such as flip-chip transition [6] were developed based on the knowledge and understanding of the flip-chip interconnection to make good use of flip-chip's advantages. However, very little attention was paid to perform the system analysis for the electrical applications, wireless communication system for example, adopting the flip-chip technology.

For the wireless communication systems, the impedance matching is so critical that the change of interconnect and the related PCB track modification might affect the RF performance greatly. There is no straightforward guarantee that the same circuit running on surface mount PCB board can work well with the flip-chip technology. Thus it is worth to investigate converting the surface mount electrical system to a flip-chip version. The main objective of this paper is to find a reliable way to transfer surface mount PCB RF circuit to the flip-chip technology design. The proposed method tries to model, simulate and optimize the system in the concern of RF impedance matching with the help of the simulation software, instead of dealing with the complex transmission line or parasitic calculation. During the process of modelling, circuit components, PCB layout and stack-up, flip-chip interconnect parasitic and other impacts are studied and converted to passive network to achieve a complete simulation of the RF circuit. Based on the modelling and simulation, a parameter sweep procedure is carried out to obtain optimized return loss performance.

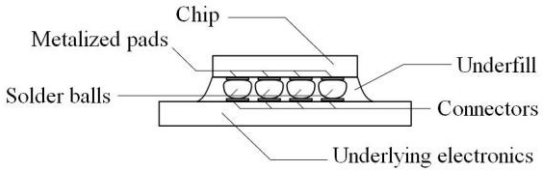



Figure 1. Side-view of a typical flip chip mounting

**System overview**

Based on the reference design from the ADF7020 evaluation board datasheet, a credit card shape flat mote with flip chip bare die of ADF7020 is developed with the same circuit connection. Figure 1 shows the chip die flip-chip mounted on the PCB board by applying solder balls between the chip and the PCB.

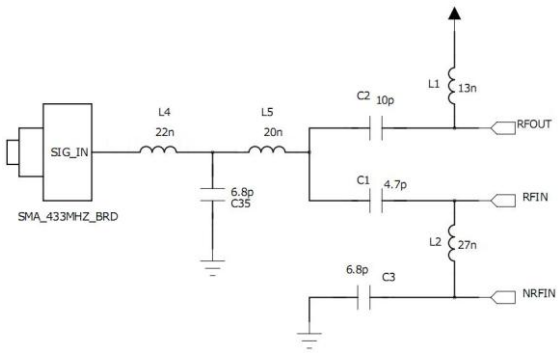



Figure 2. The balun circuit of the transceiver

The RF circuit, shown in Figure 2, between the ADF7020 chip and the antenna is targeted. The RFIN and NRFIN are the differential ports for receiving, while the RFOUT is for transmitting data. A balun circuit matches the chip ports with the SMA antenna connector "SMA_433MHZ_BRD". The balun consists of L1, L2, L4, L5, C1, C2, C3 and C35.

**The Proposed Method**

Figure 3 shows the design flow used during the modelling and optimization process.

The first step of the procedure is designing the RF circuit layout, following the reference design from the manufacture. Modelling of the PCB tracks, the substrate stack-up and the discrete components is carried out based on the RF circuit layout. Meanwhile, the Ansoft Q3D Extractor is used to extract parasitic parameters of the interconnection. Following that, an electrical model of the balun subsection is developed in order to accurately predict the RF performance of the balun. The simulation tool employed is the Ansoft Designer.

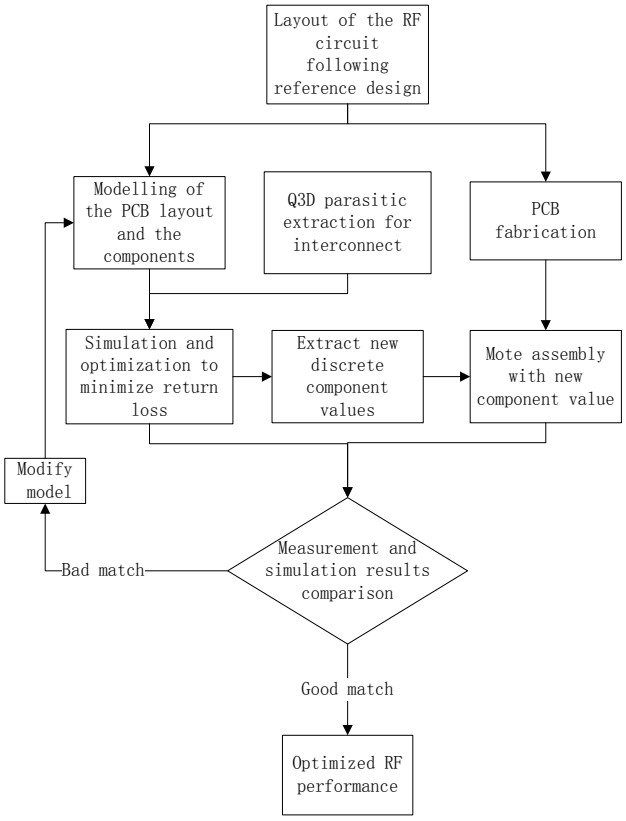



Figure 3. Design flow

By importing the finished balun layout and Q3D parasitic, the accurate model is developed. The values of the discrete components are optimized by parameter sweep in simulation. Minimizing the return loss at the antenna port can help to achieve good RF performance.

The new component values are applied to the assembly of the PCB boards. Commercial, high quality components are then sourced with nominal values as close to optimal as possible. Measurement and simulation results are compared to see the improvement brought by this method. For an accurate circuit model, the simulated and measured results should correlate very closely, and after optimization, should lead to a balun with optimal performance.

**Interconnect Simulation**

The parasitic of the wire-bonding and flip-chip interconnection are extracted by Ansoft Q3D Extractor simulation.

Figure 4 shows the geometry of the wire-bonding interconnection inside the ADF7020 chip packaging. The structure "A" is the pad of the die, while "B" is the pad of the quad flat nonlead (QFN) package. The metal used for the wire-bonding is gold, with a height of 0.5mm and length of 2.4mm, which is the average length of all the wire-bondings. The metal composition, area and height of the pads A and B are listed in the Table 1.

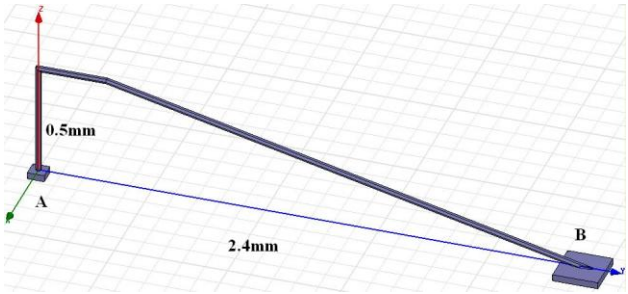



Figure 4. The 3D structure of wire-bonding

| | Metal | Area | Height |
|---|---|---|---|
| A | 98.5%Al, 1% Si, 0.5% Cu | 75μm* 75μm | 10μm |
| B | 98.5%Al, 1% Si, 0.5% Cu | 200μm*200μm | 10μm |

Table 1. Parameters of the pads A and B

The purpose of wire-bonding simulation is to have a comparison with the result of flip-chip. Since the convert method is to be investigated, the differences between wire-bonding and flip-chip, no matter in interconnect parasitic or in PCB layout, are essential to predict the system performance.

Figure 5 shows the geometry of the flip-chip interconnection. The solder ball, conducting the die and the board, is made of gold, with a height of 40 μm. The structure "D" is the pad of the die, while "C" is the pad of the PCB board for flip chip. The metal composition, area and height of the pads C and D are listed in the Table 2.

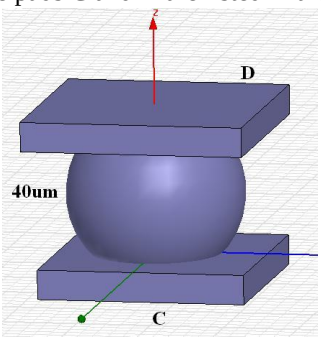



Figure 5. The 3D structure of flip-chip

| | Metal | Area | Height |
|---|---|---|---|
| C | Electroless Ni/ Au | 75µm* 75µm | 10µm |
| D | 98.5%Al, 1% Si, 0.5% Cu | 75µm* 75µm | 10µm |

Table 2. Parameters of the pads C and D

The parasitic parameters are extracted by simulation and the equivalent circuits of the wire-bonding and flip-chip are expressed by the same form of circuit shown in Figure 6. However, the values of the components, shown in Table 3, differ between two simulation results. It is clear that the flip-chip technology has very low parasitic property. The equivalent circuit is presented by a sub-circuit in PSpice or Ansoft Designer.

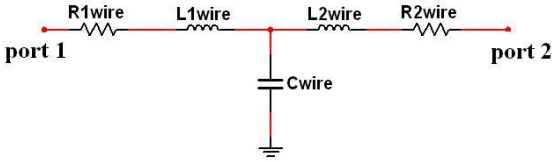



Figure 6. The equivalent circuit
for both interconnect technologies.

| | R1wire | L1wire | Cwire | L2wire | R2wire |
|---|---|---|---|---|---|
| Wire bonding | 0.057Ω | 1.28nH | 35.8fF | 1.28nH | 0.057Ω |
| Flip chip | 0.001Ω | 8.33pH | 5.9fF | 8.33pH | 0.001Ω |

Table 3. Parasitic parameters of the equivalent circuit

**Modelling of passives, ports, PCB substrate and tracks**

The discrete passives in Figure 2 can be modelled as ideal or real components, depending on the accuracy requirement. The real components have parasitic like ESR and ESL, which could be obtained from the manufacturer or Ansoft Designer vendor library. The pads of the surface mount components are treated as micro-stripe transmission lines.

Not only the discrete components, but also the PCB tracks and substrate should be modelled. Figure 7 gives the schematic of the substrate and the micro-stripe line. All the PCB tracks are modelled as micro-stripe lines.

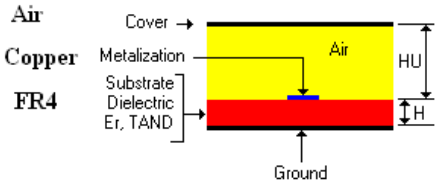



Figure 7. Schematic of the substrate stack-up

| Parameter | Value |
|---|---|
| H | 0.154mm |
| HU | 100mm |
| $\varepsilon_r$ (FR4) | 4.5 |
| tanδ | 0.002 |
| Copper thickness | 35µm |

Table 3. PCB and cover material properties

Once the stack-up has been defined, individual transmission line sections are modelled by specifying the trace width and physical length of each section. Interconnect features such as corners and bends, whose effects can be significant at high frequencies, and are modelled for accuracy.

Special modelling of the following 50µm PCB tracks, in red colour in Figure 8, to the RF die ports should be made. These tracks play the same role of the wire-bonding to connect the die with the outside PCB. Thus the parasitic of the 50µm width PCB tracks, which is normally omitted by the characterization study of flip-chip, degrades the flip-chip low parasitic performance. The three red PCB tracks correspond to the ports NRFIN, RFIN and RFOUT. The lengths of the three tracks, from top to bottom, are 1.39mm, 1.37mm and 2.3mm.

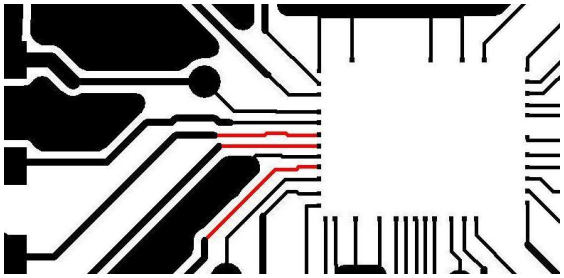


Figure 8. The 50µm width PCB tracks
of the flip-chip interconnect

The three RF ports are quite essential for modelling as passive components because it is difficult to simulate the circuit with some active components. The lumped element models of the ports, presented in Figure 9, are given by [7]. The values of the passive components are also listed in [7], or can be obtained by impedance measurements of the ports.

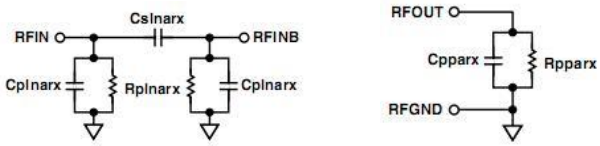



Figure 9. The LNA (left) and PA (right) models

**Simulation and Measurement**

By putting all the parts, including the interconnect parasitic, the passive value and parasitic, the PCB substrate and tracks, LNA and PA lumped-element models, into the Ansoft Designer circuit, simulation results of return loss at the SMA antenna connector can be obtained.

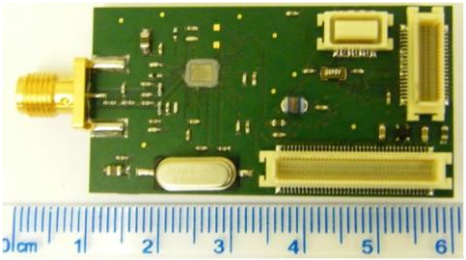


Figure 10. The wireless mote with a flip-chip bare

Following the design flow in Figure 3, sweep of passive components' values was performed to get an optimized return loss simulation result. The reason to sweep the passives is that replacing the passives with new values is much easier than replacing all other parameters.

Finally the new values of the passives were applied for PCB assembly. Measurements were compared with the simulation results until a good match was achieved. The optimization procedure was ended at this step.

In our case, optimization suggested changing the value of C2 from 10pF to 39pF and C1 from 4.7pF to 10pF.

The measurement of return loss was carried out on the mote shown in Figure 10. The mote had an ADF7020 die flip-chip mounted on the left part of the board.

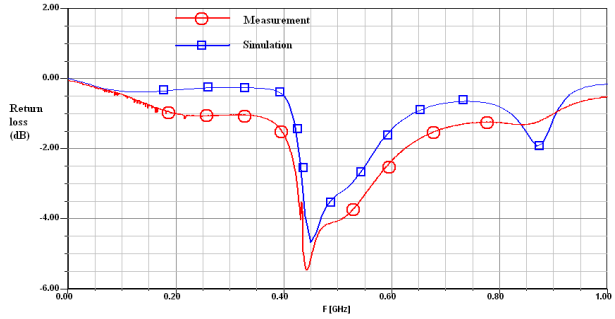



Figure 11. Simulation and measurement of the return loss with the recommended values of the passives

Firstly, return loss measurement was performed by VNA for the circuit with the recommended values from the datasheet. Results in Figure 11, both simulation and measurement, give the conclusion that the impedance matching is rather bad since the return loss is only at the level of around -5dB. Note that the ADF7020 was programmed to operate at the frequency of 433MHz.

This is basically because the changes of PCB layout, substrate stack-up, interconnect parasitic and other effects affect the impedance matching in a negative way.

The result in Figure 11 partly explained the necessity to do simulation and optimization for the wireless mote using new interconnect technology or different substrate stack-up or PCB layout.

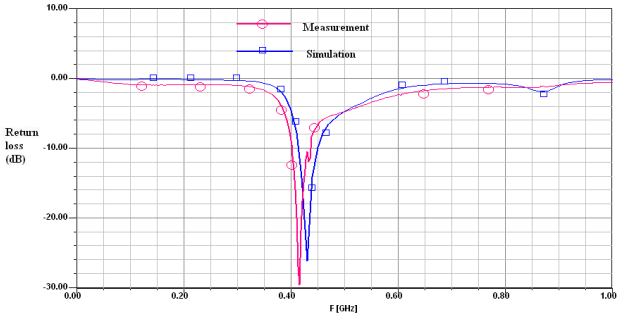



Figure 12. Simulation and measurement of the return loss with the optimized values of the passives

As mentioned before, the value of C2 was changed from 10pF to 39pF, and C1 from 4.7pF to 10pF. Simulation and measurement of the return loss, shown in Figure 12, were carried out again. The return loss at 433MHz improved to -25dB for both simulation and measurement results. This level of return loss meant good impedance matching of the balun circuit.

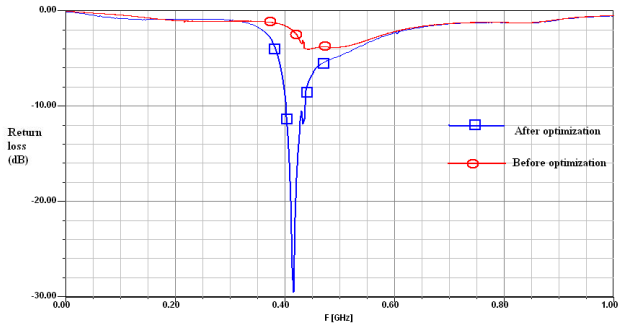



Figure 13. Measurements of the return loss before and after optimization

It can be seen from Figure 13 that the return loss of the optimized board is significantly better than the un-optimized case, with a greater than 20dB improvement. It is clear that in this particular application, using the nominal component values from the reference design leads to a very poor performance. When substrate stack-up, interconnect and PCB layout changes are made to the reference design, it can no longer be expected that the design remains optimized and the resulting balun performance can be significantly degraded.

## Conclusions

This paper presented a methodology to transfer and optimize PCB balun circuits to flip-chip design systems. The modelling of the balun circuit reqired flip-chip interconnects parasitic extraction, PCB layout and substrate stack-up build-up and equivalent circuit construction. The methodology allowed the optimization of an ADF7020 wireless node with good correlation between simulation and measurement. New passives components' values were given to achieve optimized return loss performance of the antenna port. This method enabled fast and reliable transfer of surface mount PCB designs to some systems using advanced packaging technologies(such as flip-chip) and thus avoided extensive lab testing or numerous and costly PCB re-spins. The optimization process led to a 20dB improvement in return loss.

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