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Low Power ADC Buffer: A Python Based g_m/I_D Design Methodology

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***Abstract*—Low-power Analog-to-Digital Converters (ADCs) are critical for energy-constrained applications such as portable and biomedical systems. However, the input buffers required to drive large ADC sampling capacitors, neglected in ADC Figure of Merit (FoM) calculations, can dominate power consumption. This paper addresses the challenge of designing stable, low-power unity gain buffers capable of driving large sampling capacitors across a wide output swing. The sampling capacitor itself is leveraged to set the dominant pole, enabling a power-efficient pole placement strategy in a two-stage buffer configuration. We show how older technologies present an obstacle in stabilizing a two stage OTA while maintaining reasonable power consumption, and propose a more suitable architecture to enable energy efficiency – achieving better PM with a quarter of the power.**

***Index Terms*—ADC, SAR ADC, SAR, ADC input buffer, input buffer, amplifiers, high output swing amplifiers, g_m/I_D**

I. Introduction

Successive Approximation Register (SAR) ADCs are currently the most popular ADC architecture for low-power applications, because their building blocks are well-suited to modern CMOS technologies. SAR ADC efficiency, measured by the Walden and Schreier Figures of Merit (FoM), has improved significantly, as shown in Murmann's ADC Survey [2]. However, the input buffers required to drive such ADCs often consume a considerable portion of the power budget, a cost frequently excluded when calculating the ADC's FoM.

The energy efficiency of the input buffer is often compromised to achieve rail-to-rail output swing, necessary to utilize the full ADC input range. Additionally, short settling times are required since a significant portion of the conversion cycle is allocated to the SAR comparisons and settling, leaving limited time for the input buffer to drive the signal to the sampling capacitor.

In Bindra et al. [1], the ADC input range is equally divided between two unity gain buffers: a NMOS buffer handles the upper half, while a PMOS buffer handles the lower half. The polarity of the buffer configuration is dynamically "swapped" by sensing the polarity of the differential input signal with a comparator. A "SWAP" bit, indicating polarity, is appended to the digitised signal for later reconstruction. This is illustrated in Fig. 1. For two stage buffers with common source output stages, this enables undistorted digitisation of an input signal within $[V_{SS}+V_{DSAT}; V_{DD}-V_{DSAT}]$. Provided the effects of DC offsets of the buffers are mitigated, this scheme produces good results.

In this work we highlight that the design of two stage OTAs can be hard for older technologies, due to stability issues, and propose a modified architecture.

The designed buffers target a 400 kS/s 10 bit ADC, with a sampling time of $0.5\,\mu s$. Designing a buffer with less than 1 bit offset would require large devices to remove offset. Therefore, it is assumed that a DC offset scheme will be implemented to complement the amplifier design.

This paper is structured as follows: section II introduces the design equations for the two stage unity gain buffer. Technology plots (for 65nm and 180nm) are shown in section III, based on the g_m/I_D methodology [3], [4], [5].

II. Theoretical Background

A two stage amplifier, shown in Fig. 2, will be designed – aiming for an open loop gain of at least 60dB (resulting in $0.1\,\%$ closed loop error) and big output swing. Cascoding the load in the second stage increases the gain by $\approx 6\,\mathrm{dB}$ without affecting the output range. This is optional and it should be included only if the additional gain is required.

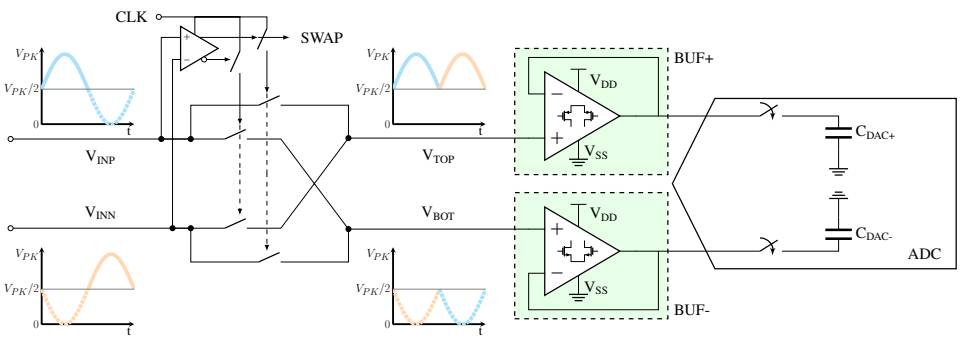


Fig. 1: ADC input buffer scheme block diagram. Remastered from [1].

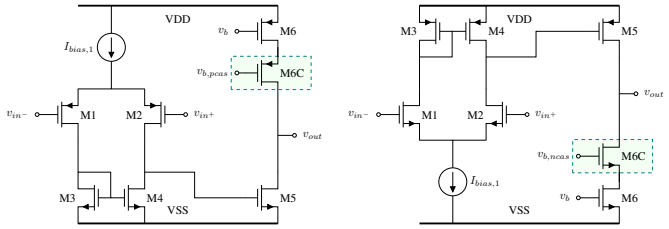


Fig. 2: Two stage OTA with a differential pair input stage and a common source output stage: (a) PMOS input (b) NMOS input

A. Settling and slewing characteristics

Large input signal steps could lead to slewing. The amplifier should be designed to guarantee that, even under these conditions, the buffer output settles to the input voltage, with a maximum error (ε), within the sampling period (T_{sample}). Part of the design procedure consists in choosing what portion of T_{sample} should be allocated to slewing and linear settling, as shown in (1). This ratio sets minimum conditions for the output stage current (I_{out}) and unity gain crossover frequency (ω_u).

$$T_{\text{sample}} = \underbrace{T_{\text{sample}}\,\alpha}_{\text{T}_{\text{linear}}} + \underbrace{T_{\text{sample}}(1-\alpha)}_{\text{T}_{\text{slew}}} \tag{1}$$

$$I_{\text{out}} \geq \frac{V_{\text{step}} - V_{\text{dsat},1}}{T_{\text{slew}}} C_L \tag{2}$$

$$\omega_u \geq \frac{-\ln(\varepsilon)}{T_{\text{linear}}}, \quad \varepsilon \leq \frac{1}{2^N} \tag{3}$$

where "N" is the resolution of the downstream ADC.

(3) is derived from the analysis of the linear settling of a 1st order system and assumes that the system has its non-dominant pole ($\omega_{p,2}$) with higher frequency than ω_u. Using the same assumption, a minimum condition for the dominant pole ($\omega_{p,1}$) position to ensure settling can be extracted:

$$\omega_{p,1} \geq \frac{\omega_u}{A_0} \tag{4}$$

where A_0 is the open loop gain.

B. Stability considerations

Considering dominant pole behaviour, minimum placement of $\omega_{p,2}$, as a multiple of $\omega_{p,1}$, in order to guarantee a specific phase margin, **PM** (°), is given by:

$$\frac{\omega_{p,2}}{\omega_{p,1}} \geq A_0 \cot\left(90 - \mathbf{PM}(^\circ)\right) \tag{5}$$

Yang et al. [6] showed that a phase margin of 70° corresponds to an optimal settling condition. This provides a simplified equation that effectively illustrates the essential condition for stability:

$$\omega_{p,2} \geq 3\,\omega_{p,1}\,A_0 \tag{6}$$

To satisfy (6) while minimizing power consumption, A_0 should be no larger than necessary. This is especially important in older technologies, where high intrinsic gain can cause the overall gain to overshoot the desired value.

Two stage amplifiers commonly use Miller compensation to ensure stability, placing the dominant pole in the first stage. However, this approach is not power-efficient, as pushing the second stage pole beyond $3\,\omega_u$ often demands significant current due to the large load capacitance. In this work, an alternative approach is adopted: the dominant pole is placed in the output stage.

C. Two stage buffer design equations

(7), (8), (9), show the total DC gain of the architecture and the approximated expressions of $\omega_{p,1}$ (output node) and $\omega_{p,2}$ (output of the first stage) poles.

$$A_0 = \frac{g_{m,2}}{G_{o,S1}}\frac{g_{m,5}}{G_{o,S2}} = \underbrace{\frac{g_{m,2}}{g_{ds,2}+g_{ds,4}}}_{\text{Gain 1}^{\text{st}}\text{ Stage}} \cdot \underbrace{\frac{g_{m,5}}{g_{ds,5}+\frac{g_{ds,6C}}{g_{m,6C}}g_{ds,6}}}_{\text{Gain 2}^{\text{nd}}\text{ Stage}} \tag{7}$$

$$\omega_{p,1} \approx \frac{G_{o,S2}}{C_{dd,5}+C_{dd,6C}+C_L} \approx \frac{G_{o,S2}}{C_L} \tag{8}$$

$$\omega_{p,2} \approx \frac{g_{ds,2}+g_{ds,4}}{C_{dd,2}+C_{dd,4}+C_{gd,5}\left(\frac{g_{m,5}}{G_{o,S2}}\right)+C_{gs,5}} \tag{9}$$

$\omega_{p,2}$ is maximised when a considerable amount of power is used in the first stage. This scenario increases the dimensions of the transistors to the point where the capacitance in the node is dominated by the extrinsic parasitic capacitances of M_2 and M_4. This results in a maximum frequency of:

$$\omega_{p,2} \approx \frac{g_{ds,2}+g_{ds,4}}{C_{dd,2}+C_{dd,4}} \approx \frac{g_{ds}}{C_{dd}} = \frac{g_m}{\boldsymbol{C_{dd}}}\frac{\boldsymbol{g_{ds}}}{g_m} \tag{10}$$

$\omega_{p,2}$ is limited to approximately the transit frequency ($\frac{g_m}{C_{dd}} \approx 2\frac{g_m}{C_{gg}}$) divided by the intrinsic gain (g_m/g_{ds}). In addition to being an inefficient way to stabilize the architecture, it shows an intrinsic limitation: ω_u of the amplifier cannot be larger than g_{ds}/C_{dd}, which can be small for older technologies.

The proposed solution to this problem consists of changing the input stage topology to a symmetrical differential pair, as shown in Fig. 3, which has a low output impedance.

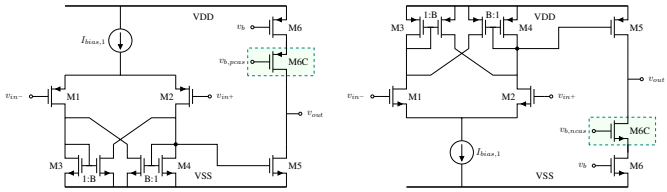


Fig. 3: Two stage OTA with a symmetrical differential pair input stage and a common source output stage: (a) PMOS input (b) NMOS input

The DC gain of the symmetrical differential pair is:

$$A_{0,S1} = \frac{\frac{1}{2}\left(g_{m,1}\frac{g_{m,3M}}{g_{m,3}}+g_{m,2}\right)}{g_{m,4}\left(\frac{1}{g_{m,4}}\left[g_{ds,2}+g_{ds,3M}\right]+1-\frac{g_{m,3M}}{g_{m,3}}\frac{g_{m,4M}}{g_{m,4}}\right)} = \frac{\frac{1}{2}g_{m,2}\left(B+1\right)}{g_{m,4}\left(\frac{1}{g_{m,4}}\left[g_{ds,2}+g_{ds,3M}\right]+1-B^2\right)} \tag{11}$$

where B corresponds to the current mirror ratios. $B = 1$ is undesired, since the gain would simplify to that of a differential pair. For $B \neq 1$ the gain is approximately:

$$A_{0,S1} = \frac{g_{m,\text{effective}}}{G_{o,S1}} \approx \frac{\frac{1}{2} g_{m,2} (B+1)}{g_{m,4} (1-B^2)} \tag{12}$$

Transistors $M_{3B,4B}$ behave as negative resistances that cancel the positive resistances associated with $M_{3,4}$, decreasing the output impedance [7]. $B \geq 1$ should be avoided, since it results in an overall negative output resistance, leading to a right half plane pole, and consequently unstable system. $B \leq 0.9$ is preferred due to mismatch considerations. (13) shows the approximated expression of the non-dominant pole (output of the first stage).

$$\omega_{p,2} \approx \frac{g_{m,4} \left(1 - B^2\right)}{C_{dd,2} + C_{dd,4} + C_{gd,5} \left(\frac{g_{m,5}}{G_{o,S2}}\right) + C_{gs,5}} \tag{13}$$

III. Design Procedure

The design procedure is initialised by ensuring that settling and slewing conditions of the OTA are met. These conditions, extracted from equations 2 and 3, are represented in Fig. 4, for a sampling time of 500 ns. A $1.6V_{P-P}$ differential input (short of the $2V_{P-P}$ reported in [1]) was considered, leading to $V_{Step} = 0.4V$ condition for I_{out}. This design utilizes a loading capacitor of 1 pF.

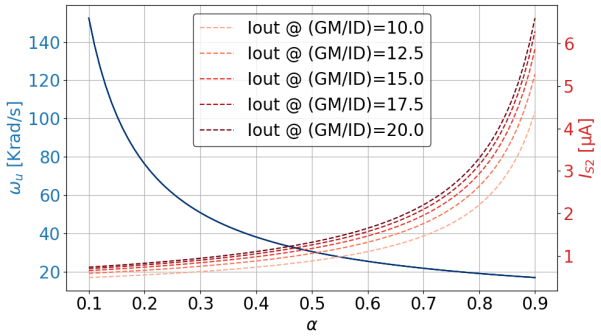


Fig. 4: Slewing (I_{S2}) and settling (ω_u) conditions for multiple sampling time proportions (α).

From a power efficiency point of view, minimizing $(g_m/I_D)_{1,2}$ would be beneficial for two reasons: 1) according to Fig. 4, smaller second stage current (I_{S2}) is necessary to achieve the slewing condition (as predicted in (2), due to the impact in $V_{\text{dsat},1}$); 2) leads to transistors with smaller areas, resulting in a smaller loading capacitance on the first stage. Conversely, small $(g_m/I_D)_{1,2}$ leads to a small voltage headroom for the current source of the differential pair, which makes it less robust to variations in the input common mode. For this reason, $(g_m/I_D)_{1,2} = 18$ is chosen in this design.

In DC steady state, the gates of the load devices in the first stage have the same voltage as the gate of the active device of the second stage. For this reason $(g_m/I_D)_{3,4} = (g_m/I_D)_5$.

Reducing $(g_m/I_D)_5$ results in a smaller device and commensurately smaller miller capacitance. This requires less power to achieve stability. However, small $(g_m/I_D)_5$ would results in large V_{dsat}, which would significantly reduce the undistorted output range of the Buffer, limiting the input range of the ADC. For this reason, $(g_m/I_D)_5 = 19$ is chosen in this design.

Fig. 5a, 5b and 5c show the contour plots of the maximum achievable **PM** and the respective gain. These plots were produced by trying to numerically solve for the maximum achievable **PM**. Fig. 5a, 5b show how the theoretical limit shown in (10) is affected by the technology node: older technologies cannot achieve high non-dominant pole frequencies, resulting in a smaller maximum **PM**. Fig. 5b, 5c show how the effect of reducing the first stage output impedance of the symmetrical-load differential pair results in higher maximum pole frequency. Consequently, this provides a higher maximum **PM** while simultaneously meeting the closed loop error specification.

However, as stated in Section II, to achieve the maximum first stage pole frequency relatively large bias currents are required to increase the transistors sizes in such a way that their capacitance dominates over the Miller capacitance. The numerical solver needed currents of hundreds of mA in most cases, which is unreasonably high for a low power application. Fig. 6a, 6b and 6c show what is realistically achievable in a low power scenario. For 65 nm, it is possible to achieve the desired gain and **PM**, with a total current consumption of 10 µA (without accounting for layout extraction), as shown in Fig. 6a. The same cannot be said for the 180nm technology. Fig. 6b and 6c show that tens of microamperes are necessary to achieve a reasonable **PM**. Furthermore, these results highlight the proposed architecture's ability to enable stability of the OTA with lower power consumption.

IV. Simulated Results

To demonstrate the proposed design methodology two NMOS buffer designs were implemented in a 180 nm process with VDD=1.2 V. *Design 1* is a conventional two-stage OTA. *Design 2* is a symmetric load two-stage OTA. The target input range is 600 mV to 1 V. Both architectures were designed to achieve a DC gain of 60 dB under the worst case condition ($V_{in} = 1$ V). A 1 pF MIM capacitor was used to model the input of the ADC. Layouts for both designs were carefully routed to minimize parasitics at the non-dominant pole node. The corresponding design parameters and simulation results are summarized in Tables I and II. The low **PM** observed in *Design 1* illustrates the challenge of achieving high pole ratios with low currents, which is alleviated in *Design 2*. The parasitic capacitance that defines the non-dominant pole is correlated with its impedance across process corners, resulting in a phase margin that primarily depends on variations of the dominant pole. Design 2 enables higher output stage impedances, reducing the excessively high GBW of the conventional OTA. The total current consumption of both designs supports the argument that, in older technology nodes, a symmetric-load architecture can outperform a conventional two-stage OTA in efficiency.

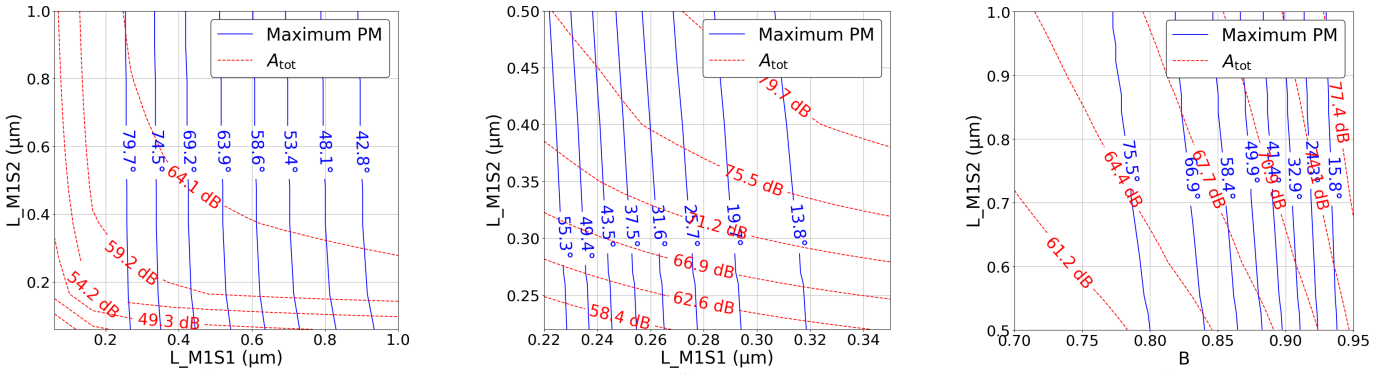


Fig. 5: Contour plots of the maximum achievable PM and A_0, sweeping $L_{1,2}$ and L_5 for (a) 65 nm, two stage OTA (b) 180 nm, two stage OTA (c) 180 nm symmetric OTA.

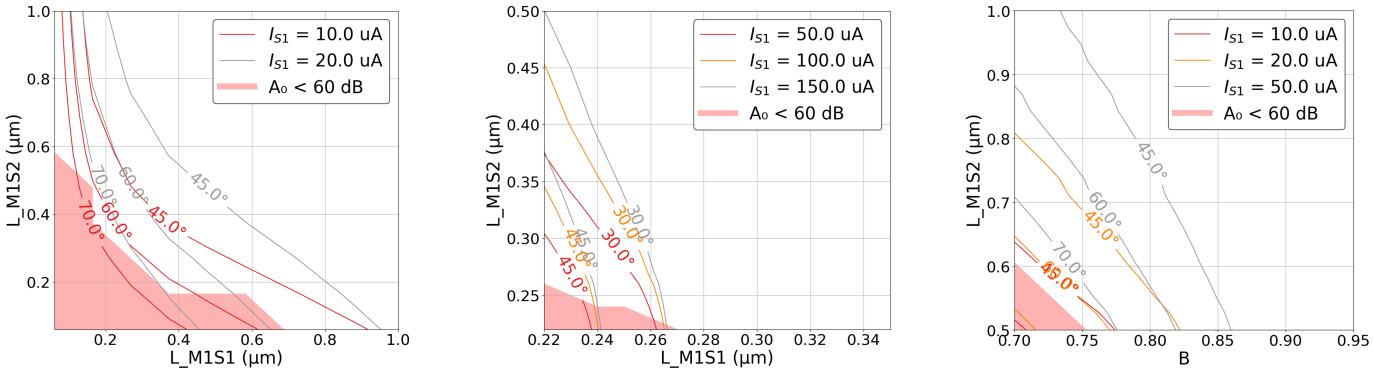


Fig. 6: Contour plots of A_0 and the PM for multiple I_{S1} values, sweeping $L_{1,2}$ and L_5 for (a) 65 nm, two stage OTA (b) 180 nm, two stage OTA (c) 180 nm symmetric OTA.

TABLE I: Transistor-level design parameters.

Design	Device	W/L [µm/µm]	NF	M	I_D [µA]
Design 1: Conventional Two-Stage OTA	M0	1.5/0.8	1	10	87.5
	M1,2	4/0.25	4	4	43.75
	M3,4	6/0.25	6	7	43.75
	M5	1.4/0.3	2	1	1
	M6,6C	0.4/0.5	1	4	1
Design 2: Symmetric Load Two-Stage OTA (Proposed)	M0	0.5/1	1	20	20.0
	M1,2	2.2/0.6	2	4	10.0
	M3,4	4.6/0.6	4	5	5.55
	M3B,4B	4.6/0.6	4	4	4.44
	M5	6.9/0.8	6	1	1.25
	M6,6C	0.25/1	1	5	1.25

TABLE II: Simulated small-signal and transient performance.

Parameter	Design 1		Design 2	
	Schematic	PEX	Schematic	PEX
I_{tot} [µA]	88.5	88.5	21.25	21.25
A_0 [dB] [a]	68.3 / 60.6	68.3 / 60.6	65.8 / 59.3	65.8 / 59.3
GBW [MHz]	61.3	47.8	12.5	11.6
PM [°] [c]	44.3 / 36.9	32.1 / 26.8	56.4 / 48.4	51.4 / 43.9
$T_{settling}$ [ns] [b,c]	382 / 432	401 / 453	397 / 459	447 / 504

[a] Measured at $V_{in} = 0.6$ V and 1.0 V (reported as "0.6 V / 1 V").
[b] 0.05 % criterion (final value), step from 1 V to 0.6 V.
[c] Reported as "Typical / Worst Corner" - Process and Temp. ([-40, 100]°C)

V. Conclusion

ADC input buffers tend to consume a considerable amount of power. Bindra et al. [1] proposed an energy efficient solution, where two high output swing OTAs are necessary (a PMOS input, and a NMOS input). Their proposed architecture considered a two stage OTA with a differential pair input stage and a common emitter output stage. This work shows that fast settling with low power consumption is hard to achieve for older technologies. An alternative architecture, with a symmetrical-load differential pair, is shown to have better energy efficiency.

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