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ARTICLE

Access resistance reduction in Ge nanowires and substrates based on non-destructive gas-source dopant in-diffusion

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To maintain semiconductor device scaling, in recent years industry has been forced to move from planar to non-planar device architectures. This alone has created the need to develop a radically new, non-destructive method for doping. Doping alters the electrical properties of a semiconductor, related to the access resistance. Low access resistance is necessary for high performance technology and reduced power consumption. In this work the authors reduced access resistance in top-down patterned Ge nanowires and Ge substrates by a non-destructive dopant in-diffusion process. Furthermore, an innovative electrical characterisation methodology is developed for nanowire and fin-based test structures to extract important parameters that are related to access resistance such as nanowire resistivity, sheet resistance, and active doping levels. Phosphine or arsine was flowed in a Metalorganic Vapour Phase Epitaxy reactor over heated Ge samples in the range of 650-700 °C. Dopants were incorporated and activated in this single step. No Ge growth accompanied this process. Active doping levels were determined by Electrochemical Capacitance-Voltage free carrier profiling to be in the range of 10^{19} cm^{-3}. The nanowires were patterned in an array of widths from 20-1000 nm. Cross-sectional Transmission Electron Microscopy of the doped nanowires showed minimal crystal damage. Electrical characterisation of the Ge nanowires was performed to contrast doping activation in thin-body structures with that in bulk substrates. Despite the high As dose incorporation on unpatterned samples, the nanowire analysis determined that the P - based process was the better choice for scaled features.

Introduction

With the billions of handheld portable electronic devices globally in use, scaling power consumption of electronic components and transistor devices can directly reduce the global demand for energy, addressing a primary grand-challenge of the modern world. Power consumption control for handheld devices and other mobile Information Communication Technology systems, is the fastest, cheapest, and cleanest way to address energy usage issues.

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The computing heart of these mobile electronic devices is the microprocessor, the state-of-the-art contains close to 1 billion transistor devices therein. Due to the performance and economic value obtained by scaling, future semiconductor electron devices for logic functions will progress toward ultra-thin-body channels. The benefit is that small devices can be made that yield higher performance and greater energy-efficiency. However, in order to continue scaling trends, new high mobility channel materials, along with thin-body device architectures such as ultra-thin semiconductor-on-insulator, double or tri-gate multi-gates, or nanowires will have to be introduced. Over the last couple of years fin field-effect-transistors (FinFETs) have become mainstream but still comprise of Si and SiGe channels. The next large steps that are foreseen are the introduction of III-V and Ge channel materials.

In simple terms, higher electron and hole mobilities could lead to performance gain or power saving in digital applications. High carrier mobility materials can enable increased integrated circuit functionality or reduced power consumption by delivering a fixed drive current and circuit speed at a reduced power supply voltage, therefore enabling standby and dynamic power reduction. Considering how large

the hand-held portable consumer electronics market has become, the impact could be very wide-reaching.

One of the biggest challenges for future logic device technologies involves material and process solutions such as novel contact and doping techniques for low access resistance. These devices will not be technologically relevant if the high-mobility benefit is swamped by losses due to access resistances. Basic understanding of the physics and chemistry behind advanced high-mobility non-Si materials is in an embryonic stage compared to that of Si, due in the main to the relatively short research and development time these materials have seen compared to over four decades of Si research.

The novelty of our work lies in the use of in-diffusion for doping non-planar Ge devices. To date Ge FinFETs have relied on ion-implantation for highly-doped regions. Furthermore we develop an electrical characterisation methodology for nanowire and fin-based test structures to extract important parameters that are related to access resistance such as nanowire resistivity, sheet resistance, and active doping levels. From a dopant diffusion standpoint in-diffusion can be considered analogous to the chemical predeposition doping techniques of the past. Well-established theory is used to extract diffusion coefficients of the in-diffused P and As, and are compared to intrinsic diffusivities.

With the trend towards non-planar FETs using nanowire or fin-based architectures, there has been an emphasis in the community to achieve conformal doping. Unlike ion implantation where ions are extremely mono-directional, conformal doping aims to coat the surface of the target structure uniformly with a dopant-enriched layer, from which the dopant can be evenly redistributed during a thermal anneal. Should one place a high concentration of dopant equally successfully on all surfaces, then a uniform or conformal dopant profile is a realistic outcome. Gas-phase and solid-source doping technologies have been around for many years, but there have been recent developments in molecular monolayer doping (MLD) of Si,[1,2] which would be compatible with highly scaled wires and fins with aggressively scaled pitches. Very recently Kong et al. proposed MLD doping for InGaAs nMOSFETs.[3]

Regarding in-diffusion of dopants into Ge from a surface, Takenaka et al. used a Metalorganic Vapour Phase Epitaxy (MOVPE) system to in-diffuse As into Ge at 500-700 °C, using tertiarybutylarsine.[4] Maximum active concentrations were 10^{19} cm^{-3}, and the profiles were 0.5-1.5 µm deep due to 60 min anneals. The same group demonstrated diode performance that beat their ion implant baseline, correlated with the reduction in crystal defects from the MOVPE approach.[5] Maeda et al. used a Sb-doped silicate glass solid source for the in-diffusion of Sb into Ge at 700 °C.[6] Maximum chemical concentrations were 5×10^{18} cm^{-3}, and the doping profile was 4 µm deep. Excellent diode performance with an I_{ON}/I_{OFF} ratio of 1.5×10^{5} was demonstrated. Further solid-source work was proposed by Jamil et al, as P in-diffusion from a spin-on-dopant source into Ge was verified at 650-750 °C.[7] Maximum active concentrations were approximately 7×10^{19} cm^{-3} with a junction depth close to 0.5 µm. Again improved diode performance shows the advantage of this approach, as diode ideality factor was 1.03 for the spin-on-dopant process, compared to 1.45 for their ion implanted baseline.

Ge FinFET devices have been limited to p-type channels, with ion implantation used for source/drain doping. The smallest fin width reported to date is 20 nm. Feng et al. fabricated Ge p-channel FinFETs with fin widths (W_{fin}) of 130-350 nm.[8] Van Dal et al. reported scaled p-channel Ge FinFET devices with W_{fin} of 40 nm, fabricated on a Si bulk wafer using the Aspect-Ratio-Trapping technique.[9,10] Liu et al. reported p-type Ge FinFET devices with W_{fin} = 60-100 nm.[11] Furthermore Ikeda et al. fabricated p-type Ge nanowire FET devices with W_{fin} = 20 nm.[12]

Nanowire resistor devices are based on top-down lithography and patterning. They are similar to multi-gate-field-effect-transistor (MugFET) devices, except the gate stack is omitted. These test structures are excellent diagnostic tools for evaluating the effectiveness and quality of a specific doping process in terms of access resistance characterisation. Resistance versus fin width can be used to calculate doping concentrations, Ge resistivity, and crystal quality. Si fin resistors have been demonstrated by a number of groups for this purpose.[13,14,15] To the best of our knowledge this is the first report of Ge fin resistors formed by top-down patterning.

Note, total access resistance is partly metal-semiconductor contact resistance, and partly resistance of the doped semiconductor layer. By the design of our test structure we have filtered out the contact resistance element of the access resistance, so we could target our study on the resistance associated with the doped regions of the Ge. It is beyond the scope of this work to evaluate contact resistance. Metal-semiconductor contact resistance in Ge has been studied by our group recently based on nickel-germanide contact formation using rapid thermal anneal[16] and laser thermal anneal.[17]

Finally a note on terminology; depending on who you talk to, academics or industrialists, or indeed which company or which university, the terms "*fin*" and "*nanowire*" are somewhat interchangeable. In this paper we use both terms, but they effectively refer to the same thing in this context, namely a thin-body structure patterned by top-down lithography.

Experimental

Unpatterned sample processing

The first part of this work was carried out on unpatterned (100) Ge substrates, with p-type doping concentration in the range of $5\text{-}9\times10^{16}$ cm^{-3} according to the supplier information. Unpatterned substrate processing is a key part to the work, as we develop the methodology and optimise parameters associated with cleaning, MOVPE processing and characterisation. Many of the important material characterisation techniques that are necessary for impurity doping analysis, such as Atomic Force Microscopy, Secondary Ion Mass Spectrometry, and Electrochemical Capacitance Voltage profiling require unpatterned substrates.

Prior to MOVPE processing the Ge surfaces were cleaned by performing a 10 min dip in hydrochloric acid (37%) : deionised water in the ratio 27:73. This was followed by immediately drying with N_2 and loading onto a graphite susceptor within an AIX200-AIX200/4 MOVPE horizontal reactor which, using double purification of the highest commercially available purity precursors, which has achieved near Molecular Beam Epitaxy quality III-V material by MOVPE.[18] The samples were heated under a flow of N_2 carrier gas at 80 mbar to 250 °C at which point purified AsH_3 (or PH_3) was also introduced at a flow rate of 50 sccm. The sample temperature was then ramped to the process temperature[19] over 10 min, whilst linearly increasing the flow rate of AsH_3 (or PH_3) into the reactor to 250 sccm, and held at the process temperature for a further 20 min under a flow of 250 sccm AsH_3 (or PH_3) and N_2 carrier gas. The heating was then switched off and the sample allowed to cool under 100 sccm AsH_3 (or PH_3). The AsH_3 was switched out at 450 °C and the PH_3 was switched out at 250 °C and

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the sample allowed to cool under N_2 to below 60 °C before unloading from the reactor.

Nanowire processing

The process evaluation was then extended to nanowire structures patterned by top-down lithography. Undoped (100) germanium-on-insulator (GeOI) substrates were used, with a Ge thickness of 50 nm, and SiO_2 thickness of 145 nm.. Often doping studies are performed on unpatterned substrates, the relevance of which is questionable when applied to the appropriate device structure. i.e. a non-planar structure of some sort. Furthermore it will be demonstrated from our data how misleading optimising a process based only on unpatterned samples can be, when the application is a FinFET or nanowire-based FET device.

For the nanowire processing the GeOI substrates were patterned using the Raith e-Line Plus electron beam lithography (EBL) system and high resolution EBL resist known as hydrogen silsesquioxane (HSQ). Post EBL exposure, the HSQ resist is developed using an aqueous developer followed by deionised (DI) water rinse. If the HSQ resist is placed directly on the Ge oxides, which are soluble in water, there is possibility of the exposed HSQ resist to be rinsed away together with the underlying oxides. In order to avoid this, a surface passivation method is inserted in addition to the routine HSQ resist deposition.[20] The substrates were firstly degreased by ultrasonicating them consequently in acetone and isopropylalcohol (IPA) solvents. They were then blown dry with N_2 gun and immersed in 1-2% hydrofluoric (HF) acid for 30-40 s and rinsed under flowing DI water. This step ensured the removal of water insoluble Ge oxides. Subsequently, they were dipped in 4.5 M HNO_3 for 20 s, rinsed under DI water and immediately submerged in a solution of 7.5 M HCl for 10 min. This step provided Cl-terminated Ge surfaces. The substrates were then dried thoroughly under flowing N_2 and 1:2 concentration solution of HSQ in methylisobutyl ketone (MIBK) was spun on the substrates with 2000 rpm for 33 s (lid closed). This gives approximately 50 nm thick HSQ film on any substrate. The substrates were then baked at 120 °C for 3 min prior to EBL exposure.

The EBL exposure was a two-step process where the first lithography step was used to expose only the high resolution fin structures. In the second step the contact pads for the four probes were exposed. To attain a highly focused beam for the first step, 10 kV beam voltage and 100 µm write-field was chosen. To avoid the large exposure time, the low resolution contact pads were written with 1 kV beam voltage and 400 µm write-field. After the EBL exposures, the substrates were developed in 0.25 M NaOH and 0.7 M NaCl solution mixture for 15 s followed by 60 s rinse in DI water and 15 s immersion in IPA. For the second lithography the substrates were Cl terminated as before excluding the HF dip and developed using the same method. To transfer the HSQ pattern into the top Ge layer of the GeOI substrates, they were subjected to reactive ion etch (RIE) using Cl2 chemistry in Oxford Instruments Plasmalab 100 system.

Characterisation methodology

Inspection was first done by top-down scanning electron microscopy (SEM) was performed on an FEI 650 FEG SEM. Atomic Force Microscopy (AFM) was implemented in tapping/non-contact mode at room temperature on 5×5 µm scanning area. Cross-sectional Transmission Electron Microscopy (XTEM) was carried out using JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were obtained by using FEI's Dual Beam Helios Nanolab system. For electrical characterization the KEITHLEY 37100 and KEITHLEY 2602 were used. Secondary Ion Mass Spectrometry (SIMS) was done to obtain the concentration of the dopants. SIMS analysis typically has a standard error of 20 % in concentration, and 10 % relative error from sample to sample. Electrochemical Capacitance Voltage (ECV) profiling was also performed to determine active carrier concentration using thiron as the etchant. ECV profilers extract an error with every data point in the curve. For the data presented here the errors don't exceed 20 %. As doping concentration axes are plotted in log-scale, these errors are relatively small and do not affect the overall conclusions of this work. XPS was carried out with a VG Scientific Escalab MKII system using Mg X-rays at 1253 eV. Survey scans were performed using a pass energy of 200 eV and core level scans at a pass energy of 20 eV.

Results and Discussion

Total impurity doses and diffusion coefficients

Figure 1 shows the ECV carrier concentration profile from the P and As doped unpatterned samples. The As has diffused in faster than the P as expected, as has been reported in ion implanted studies.[21,22] The As profile has diffused to a depth of approximately 550 nm for the 700 °C process, and approximately 400 nm for the 650 °C process. The flat-topped nature of the As profiles is consistent with concentration enhanced diffusion.[23] In all the samples the peak carrier profiles are approximately 10^{19} cm^{-3}. Integrating the profiles to extract total active dose yield 3.70×10^{14} and 6.41×10^{14} cm^{-2} for As in the 650 and 700 °C processes respectively, and total active P doses of 4.91×10^{12} and 1.81×10^{13} cm^{-2} for the 650 and 700 °C processes respectively. This data is tabulated in Table I, along with other extracted parameters.

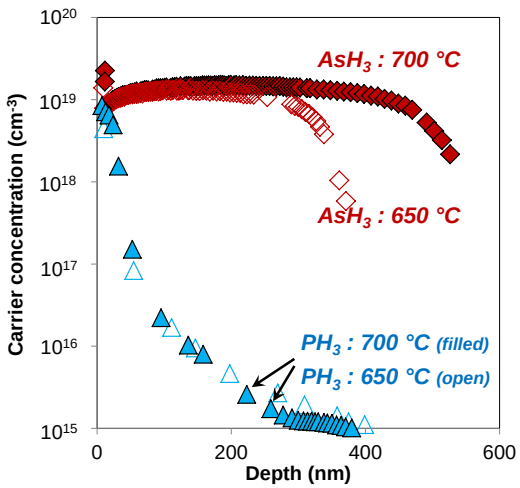


Fig 1 Carrier concentration vs depth profiles extracted by ECV profiling for the unpatterned Ge samples in this work. The As-based process shows greater dopant incorporated dose than the P-based process.

Using standard values for concentration-dependent electron mobility,[24] sheet resistance was calculated according to the equation

$$R_{sheet} = \int_0^{\infty} \frac{1}{q.\mu.N.dx}$$

The R_{sheet} values based on the ECV data are 55.8 and 34.5 Ohm/sq for the As samples, and 3323 and 973 Ohm/sq for the P samples. R_{sheet} is relatively low for the As cases due to the relatively deep carrier concentration profiles. Note four-point-probe measurements can experimentally measure R_{sheet}, these

calculated values here are merely a guideline for those interested in this parameter.

The SIMS data are shown in Fig. 2. The concentration versus depth profiles are only shown for the As samples, with maximum chemical concentrations of approximately 5×10^{19} cm^{-3}, ignoring the surface peak artefact. Note, we did perform SIMS analysis on the P-doped samples which showed a signal close to the surface, much like that of the ECV profiles, but the SIMS provider considered it unwise to put faith in the data, due to the apparent similarity to a SIMS surface artefact. For the As profiles, the SIMS data match the ECV well in terms of depth. In terms of total dose the SIMS shows a higher amount of chemical As than the electrically active As. This is somewhat surprising as if the dopant is diffusing in from the surface, one might expect complete activation of that dopant. Integrating the profiles to extract total chemical dose yield 6.77×10^{14} and 1.19×10^{15} cm^{-3} for the 650 and 700 °C processes respectively, which are approximately double the electrically active As doses.

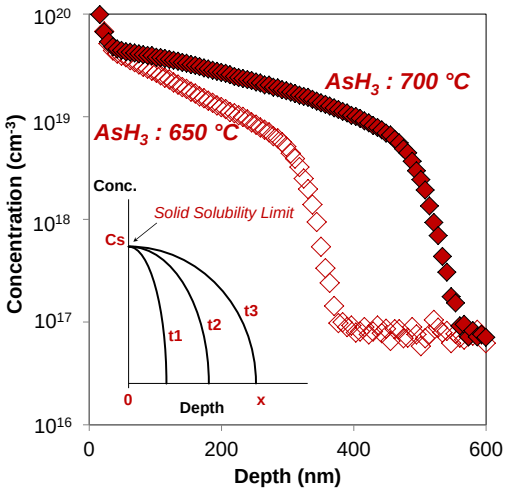


Fig 2 Chemical concentration vs depth profiles extracted by SIMS analysis for the unpatterned Ge samples processed using an AsH_3-based method. The higher temperature of processing is more effective at incorporating As, however there is greater diffusion. The inset shows a schematic representation of the time evolution of impurity incorporation in a semiconductor using a chemical predeposition process. The peak concentration is capped by the solid solubility limit at the processing temperature. The profiles get deeper with increasing time.

Sample	Active dose (at/cm^2)	Diffusivity (cm^2/s)	SIMS dose (at/cm^2)	Diffusivity (cm^2/s)
As 650 °C	3.70×10^{14}	8.93×10^{-13}	6.77×10^{14}	8.31×10^{-14}
As 700 °C	6.41×10^{14}	2.68×10^{-12}	1.19×10^{15}	2.57×10^{-13}
P 650 °C	4.91×10^{12}	6.29×10^{-16}	n/a	n/a
P 700 °C	1.81×10^{13}	8.55×10^{-15}	n/a	n/a

Table I Extracted data for the unpatterned samples in this work, showing total active dose and diffusivity all extracted from the ECV profiles in Fig. 1, as well as total chemical dose and diffusivity extracted from the SIMS profiles in Fig. 2.

The surface quality of the Ge surfaces was checked post-doping by AFM. In all cases the root-mean-square roughness was in the order of 0.1-0.2 nm which is close to the roughness of as-received wafers. From this data we conclude that this method of doping does not attack or corrode Ge surfaces.

Let us now consider the diffusion of dopant from the semiconductor surface. This experimental system is equivalent to the "chemical predeposition" process described in traditional silicon technology textbooks. The relevant theory is now briefly summarised. The impurity concentration (C) profile for the chemical predeposition process has the form

$$C_{(x,t)} = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$

where x is the distance from the surface, t is time, C_s is the impurity surface concentration, and D is the impurity diffusivity. The evolution of the doping profile with time is shown schematically in the inset of Fig. 2, assuming a constant processing temperature. If D is constant the depth of the profile depends only on time, and the surface concentration remains fixed, as this is limited by solid solubility limit at that processing temperature. If the total quantity of dopant is defined as dose, Q, then this can be described as

$$Q_{(t)} = \int_0^\infty C_{(x,t)} dx$$

Using these two equations, the total incorporated dose can be simplified thus

$$Q_{(t)} = \frac{2}{\sqrt{\pi}} C_s \sqrt{Dt}$$

Experimentally the doping profile can be characterised by ECV profiling and by SIMS analysis, and from those Q and C_s can be extracted. Knowing the experimental processing time, t, means D is the only unknown above, and thus can be calculated. This is now demonstrated for our experimental data, and the values are listed in Table I.

In general, constant diffusion occurs when the dopant concentration is below the intrinsic carrier concentration (n_i) for that processing temperature. Below n_i the diffusion is dominated by the intrinsic diffusivity, while above n_i the diffusion is dominated by the extrinsic diffusivity. The extracted diffusivities are plotted in Fig. 3 versus 1000/T, where T is in Kelvin, and are compared to the intrinsic diffusivities.[25] The experimental P diffusion coefficients in this work lie on the intrinsic diffusivity trend-line. The As diffusivities extracted from the SIMS data do the same, however if the active concentrations are considered, with C_s and Q taken from the ECV profiles, then the diffusion coefficients are extrinsic. Considering n_i at 650-700 °C is in the $3\text{-}4\times10^{18}$ cm^{-3} range,[25] it is understandable that extrinsic diffusivity rates are observed here, as the As concentrations are above this level in Figs. 1 and 2.

Figure 4 shows an XPS survey spectra of Ge cleaned by in-situ ion etching, a Ge wafer post MOVPE reaction (inset is a core level spectrum in the As 2p region post MOVPE reaction). The survey spectrum of Ge after MOVPE shows large O (532 eV) and C (285 eV) peaks and are due to the native oxide and ambient contamination respectively. These levels are similar to those that you would find in an as-received Ge wafer that has not undergone a cleaning step. Core level examination of the As 2p core region of the spectrum indicates the presence of a small As peak (~0.6 at %). The presence of As on the surface of the wafer after the MOVPE reaction is indicative of the fact that there is a constant renewed supply of As during the reaction that stops diffusing in as the temperature of the reactor decreases. It was not possible to positively identify the presence of P due to it being masked by larger Ge peaks that occur at similar binding energies.

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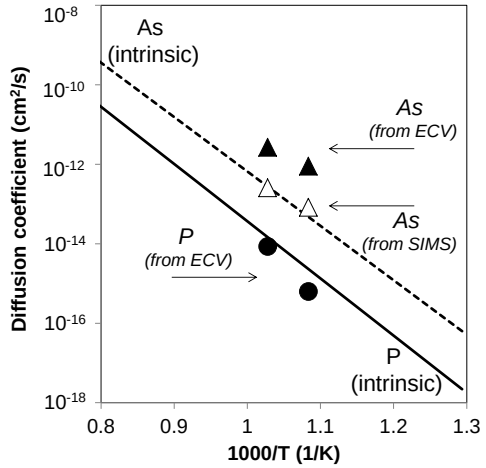


Fig 3 Diffusion coefficients vs 1000/T, where T is in Kelvin. The solid trend-line shows the intrinsic P diffusivity, and the dotted trend-line shows the intrinsic As diffusivity. The experimental data from our work is shown as the symbols. Both ECV and SIMS data were used to extract diffusion coefficients here.

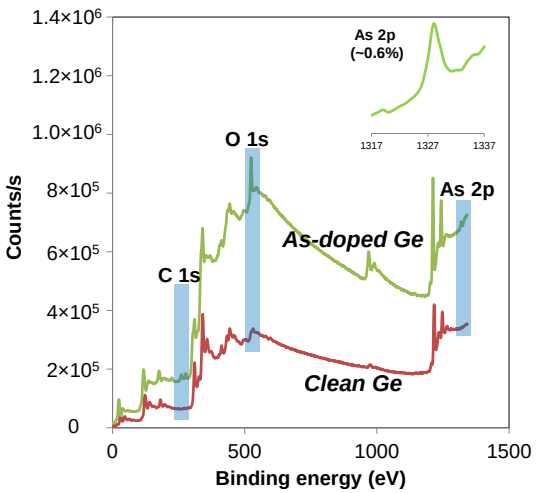


Fig 4 An XPS survey spectra of Ge cleaned by in-situ ion etching, and a Ge wafer post MOVPE doping using AsH_3. The inset is a core level spectrum in the As 2p region post MOVPE reaction.

Ge nanowire access resistance modification

In order to properly evaluate the MOVPE based doping process for fine features we fabricated top-down patterned Ge nanowires (or fins) in a range of widths, namely 20-1000 nm. The nanowire process is summarised in Fig. 5(a), and was described in detail in the *Experimental* section. The test structure used to electrically characterise the access resistance modification is shown in a representative SEM image in Fig. 5(b). The test structure is a 4 probe structure, with a user-defined current forced through the outer 2 electrodes, and the inner 2 electrodes "sense" the voltage drop across the nanowire. There may be a voltage drop at the force contact pads, however because of the design of the test structure, that is filtered out by the sense inner electrodes. There is no current flow into the sense electrodes so there should be no voltage drop at those pads, and thus the voltage drop across the nanowire only is extracted.

We exposed the nanowires to PH_3 at 650 or 700 °C, or to AsH_3 at 650 °C by MOVPE as described previously for unpatterned samples. Based on the unpatterned sample analysis of the AsH_3 at 700 °C, this process was considered too coarse for the small nanowires, hence was not further evaluated.

Representative current versus voltage characteristics are shown in Fig. 6 for Ge nanowires in a range of widths. The current is well behaved, linearly dependent on voltage and passing through the origin. As the nanowire width is scaled the current level drops, as expected.

The oxide layer underneath the Ge should not contribute to the conductivity of the nanowire devices, as it is an insulator even if it has incorporated some P and As atoms. Silicon dioxide electrical resistivity is typically quoted to be in the 10^{16} Ω•cm range, one of the highest values for materials used in semiconductor device processing.

In the case the P or As has diffused through the oxide and then into the Ge substrate, this should not have an effect on the nanowire device as the substrate is held at 0 V during the measurement, and thus should not influence the current conduction.

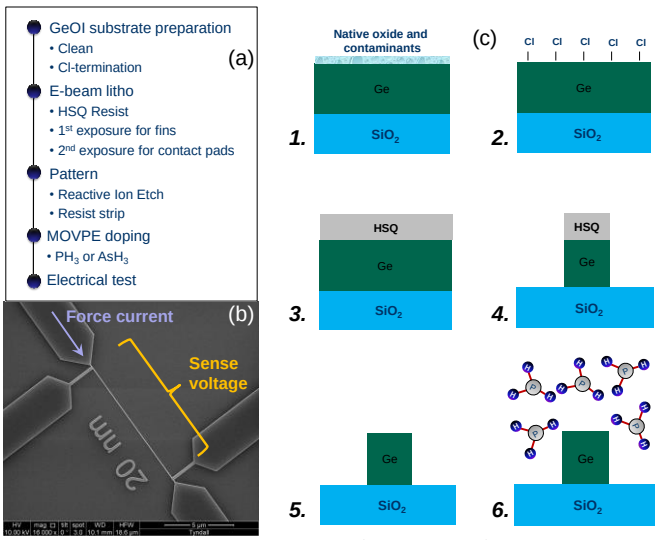


Fig 5 (a) A schematic representation of the process flow used to process the Ge nanowires on GeOI substrates. After cleaning, the test structures were patterned by a combination of e-beam lithography and reactive ion etch. MOVPE-based doping was then performed to alter the resistance of the nanowire resistor structures. (b) A representative top view SEM image of the test structure under evaluation in this work. It is a 4 point probe test structure where a current is forced by the outer electrodes and the voltage drop across the nanowire is sensed by the inner 2 electrodes. From this current-voltage relationship resistance is extracted. In this image a 20 nm wide structure is shown. (c) A schematic illustration of the process.

Further analysis of the current-voltage was performed in two ways, depending on the assumption of where the current flows in the cross-section of the nanowires. The first possibility is that the current flows primarily along the edges of the nanowires, valid for a condition where active doping is highest there (see ECV profiles for P-doped samples especially), say like that in a gated device such as a MugFET or FinFET. In this case the electrical width of the device is then calculated according to the equation :

$$W_{electrical} = 2H_{fin} + W_{fin}$$

where H_{fin} is the height of the fin, and corresponds to the thickness of the Ge on the GeOI wafer. W_{fin} is the width of the fin. The resistance of the fin is calculated according to

$$R_{fin} = \frac{V}{(I/W_{electrical})} = \frac{V}{I}(2H_{fin} + W_{fin})$$

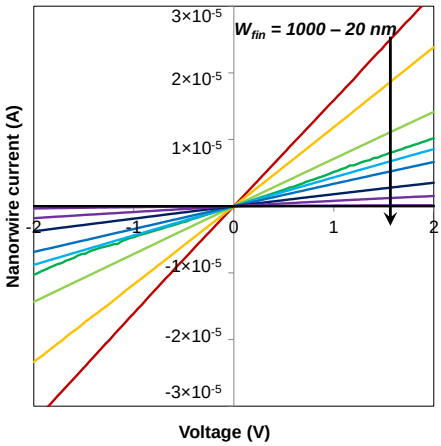


Fig 6 Representative current-voltage characteristics of the Ge nanowires post-doping. The current obeys Ohms law, is symmetrical around the origin, and scales with reduced fin width. The voltage in this plot is the voltage drop across the inner sense electrodes.

This type of electrical parameter extraction is shown in Fig. 7. Immediately it is obvious that the MOVPE-based process has successfully doped the nanowires as the access resistance has dropped about 4-5 orders of magnitude from the undoped case, where the current-voltage characteristics were measured before the MOVPE-based process was done. It is perhaps surprising to see that the P and As based processes give similar results in the wide nanowires despite the large differences in the unpatterned substrates. 650 °C does not seem to be a high enough temperature for the P-based process, as the resistance is significantly lowered by increasing the process temperature to 700 °C. The higher temperature process works best for the PH_3 process, and that is matched by the 650 °C AsH_3 process. As we scale the Ge nanowire widths the resistance is expected to rise, as has been shown many time for Si nanowires and FinFETs. In this regard the AsH_3 based process performs the worst as the resistance increases sharply around W_{fin} = 40 nm. In contrast, the PH_3 doped nanowires can be scaled beyond this point, and the resistance does not sharply increase, making this process a better choice for scaled features.

The second possibility for electrical parameter extraction is if we consider the current flows uniformly throughout the cross-section of the nanowire, say like that of a metal track. From metal interconnect theory we know that

$$R = \rho\frac{L}{A}$$

and

$$\rho = R\frac{A}{L}$$

where ρ is the material resistivity, A is the cross-sectional area, L is the track length, and R is V/I. Furthermore

$$R_{sheet} = \frac{\rho}{t}$$

where R_{sheet} is sheet resistance, and t is the thickness of the layer. This type of electrical parameter extraction is shown in Figs. 8. The trends are similar to the previous analysis in Fig. 7, where surface conduction was assumed. Once again 700 °C is better for the P doping process, the two dopant species produce similar results for wide devices, and the P-based process is a better choice for scaled features. This is a significant result considering the ECV and SIMS data back in Figs. 1 and 2. Bearing in mind only the unpatterned samples, one might think that the AsH_3 based process would be a better choice, due to the greater dose incorporation. However As may also exhibit greater likelihood of dopant clustering, evident is the differences between the SIMS and ECV data, and may even trap at surfaces more readily, a feature that is observed in As-doped Si.[26]

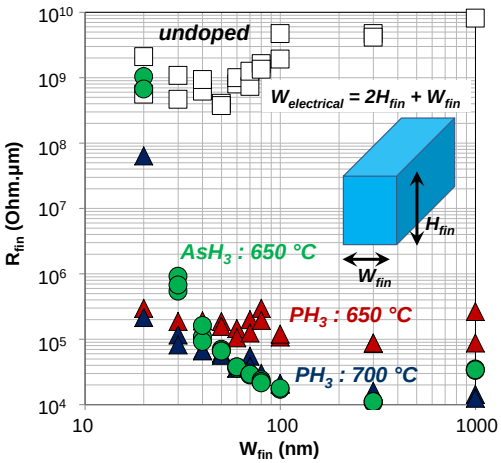


Fig 7 R_{fin} vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3.

At this point we ought to consider which of the two parameter extraction approaches is more suitable for scaled nanowires and FinFETs. As we scale down to very small dimensions (sub-30 nm) the doping profiles from all sides will tend to overlap, and we are likely to have a *uniformly* doped structure in cross-section. There comes a point where the device is so small that the volume is essentially uniformly doped and the current flow is throughout the entire cross section of the doped region. Thus in that case it is more appropriate to use the second model for electrical parameter extraction above.

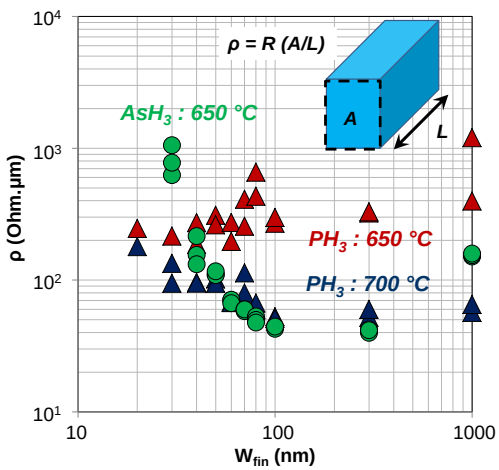


Fig 8 ρ vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3.

Furthermore, assuming a uniformly doped fin, resistance of the nanowire can be theoretically calculated according to the equations

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$$R = \rho \frac{L}{A}$$

$$= R_{sheet} . t . \frac{L}{A}$$

$$= \frac{1}{q . \mu . N . t} . t . \frac{L}{A}$$

$$= \frac{L}{q . \mu . N . A}$$

assuming published values for carrier concentration-dependent mobility, μ.[24] From these values theoretical expectations for R were calculated and are plotted as isolines of constant active concentration alongside the experimental data (simply R=V/I) in Fig. 9. From this plot we can see that the 700 °C PH_3 process and the AsH_3 process touch the 3×10^{18} cm^{-3} isoline, while the 650 °C PH_3 process can only touch the 3×10^{17} cm^{-3} isoline. In all cases the active doping levels appear to degrade as the nanowires are scaled. This effect is most dramatic for the As-doped structures.

From Fig. 9 it appears surfaces are bad for low resistance as W_{fin} is scled down. The proximity to the surface impedes dopant activation, presumably because the crystal structure is not ideal in the first few nanometres close to the surface. As the nanowire is scaled then the surface to volume ratio increases, surfaces become more influential, and hence we see the trend in Fig. 9.

Furthermore one might think that the overlapping doping profiles originating from left and right surfaces would lead to greater active concentration and lower resistance. In this case we are probably limited by solid solubility limits of P and As in Ge. In other words even though the chemical concentration is increased we have a ceiling in terms of activation, based on the equilibrium solubility of the material. A method to beat this trend could be the use of advanced annealing, say, such as laser of flash lamp annealing, which are known to boost dopant activation levels under certain processing conditions.

Finally, XTEM analysis of the As-doped nanowires was undertaken to determine if crystal defects had been introduced by this process. Traditional problems doping thin body semiconductors are stacking faults and {111} twin boundary defects formation, often by the ion implantation process which causes semiconductor amorphisation and subsequent recrystallisation during anneal. These defects are usually are easily visible in this form of TEM imaging. Shown in Fig. 10 are representative images of the Ge nanowires test structures. On the right-side we show the problem associated with the traditional ion implantation approach where defects are clearly visible.[27] In contrast, on the left-side of Fig. 10 for the MOVPE-based doping process, no visible crystal defects of this type were observed, which is consistent with the non-destructive nature of the process. Furthermore as the sample temperatures are 650-700 °C during the dopant in-diffusion one would expect a great deal of dynamic annealing, and thus no crystal damage build-up that could cause the formation of defects. This is in contrast to ion implanted thin-body structures where crystal damage, {111} defects, and poly-crystalline transformation can be a problem with decreasing W_{fin}.[28,29]

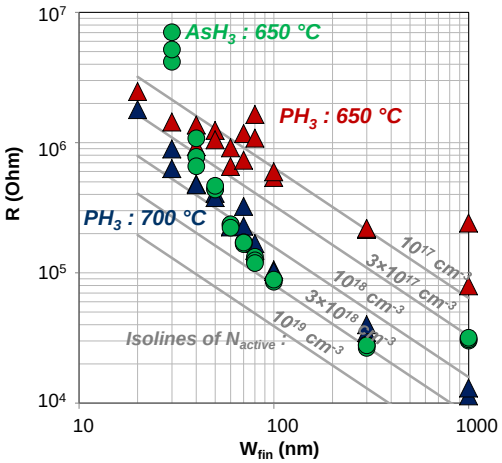


Fig 9 R vs W_{fin} for Ge nanowires doped at 650 or 700 °C using PH_3, or doped at 650 °C using AsH_3. R is also calculated based on the assumptions for uniformly doped concentration levels, and carrier concentration dependent mobilities. These calculations are plotted in the form of isoline of constant carrier concentrations, in grey.

Note, from Fig. 10 we can see that the Ge nanowires are not perfectly rectangular shaped, thus introducing a systematic error in our assumptions for W_{fin} and calculations of $W_{electrical}$ and A. This systematic error is the same from sample to sample, as the same lithography and etch process was applied to all samples in this work. The overall conclusions regarding the advantages/disadvantages of the P-based versus As-based processes remain the same, as in essence we are comparing "like with like" across the samples.

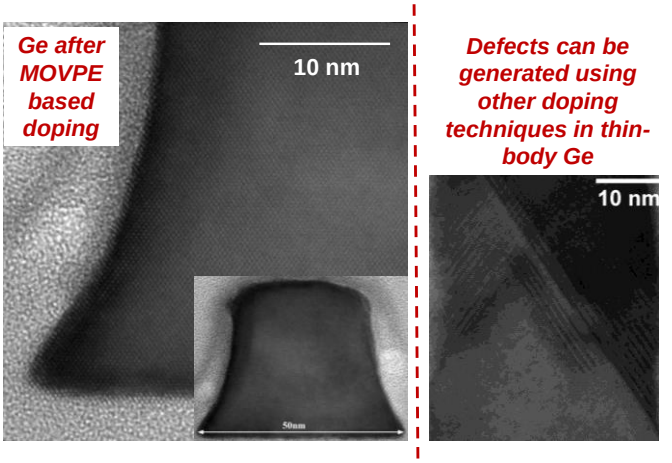


Fig 10 Left side : Representative XTEM images of a 50 nm wide Ge nanowire structure post MOVPE-doping and post electrical characterisation. No visible crystal defects appear to be present. Right side : typical {111} defects visible in thin-body Ge formed during doping by ion implantation and thermal anneal.[27]

Ion implantation is the industry standard for semiconductor doping because it can generate a single ion species with a single energy in an industrially friendly highly controlled fashion. The problems associated with it are crystal damage of the semiconductor as the energetic atoms strike the target and the extremely directional nature of the process, leading to a lack of conformality in non-planar structures. Plasma doping, under development, has the advantage of generating more conformal doping profiles than ion implantation but it causes damage to the target as ions strike. It also suffers from implanting multiple

species with multiple energies in a single process which can be a problem when a high level of control is required.[30,31] Our MOVPE approach is presented as an alternative methodology, based on surface in-diffusion, providing a conformal and non-destructive solution for semiconductor doping of non-planar structures and devices.

Conclusions

Doping thin-body features is a difficult challenge, in order to get the impurity atoms into the structure, activate and prevent them escaping during thermal treatments, all while preserving crystalline integrity of the semiconductor crystal. Conformal doping techniques such as plasma doping may evolve as the ultimate choice for MugFETs and nanowire FETs.[32,33] However, a major cause for concern for thin-body FET optimisation is the trade-off between parasitic access resistance and W_{fin}. Fins and nanowires must be narrow to control short channel effects and thus enable scaled devices. High access resistance and variability in Si devices has been correlated with poor crystal quality of thin-body Si regions. Moreover, Ge is more likely to amorphise than Si,[34] as many standard implants will amorphise Ge at room temperature. Consequently a non-destructive doping methodology for Ge thin-body structures is highly desirable.

In this work we have demonstrated a non-destructive dopant in-diffusion process, by means of flowing PH_3 or AsH_3 in a MOVPE system above heated substrates. Crystal damage was avoided, access resistance was reduced many orders of magnitude compared to the undoped case. The usual resistance degradation from scaled dimensions (W_{fin}) was very effectively suppressed using a PH_3–based process.

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