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Authors	Caruso, Enrico;Lin, Jun;Monaghan, Scott;Cherkaoui, Karim;Floyd, Liam;Gity, Farzan;Palestri, Pierpaolo;Esseni, David;Selmi, Luca;Hurley, Paul K.
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University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

On the Interpretation of MOS Impedance Data in Both Series and Parallel Circuit Topologies

E. Caruso[1,4], J. Lin[1], S. Monaghan[1], K. Cherkaoui[1], L. Floyd[1], F. Gity[1],
P. Palestri[2], D. Esseni[2], L. Selmi[3], P. K. Hurley[1]

[1] Tyndall National Institute University College Cork, Cork, Ireland, email: paul.hurley@tyndall.ie
[2] DPIA, University of Udine, Via delle Scienze 206, 33100, Udine, Italy ,
[3] DIEF, University of Modena and Reggio Emilia, Via P. Vivarelli 10/1, 41125, Modena, Italy,
[4] Infineon Technologies Villach, Austria

1. Abstract

We investigate the interplay between the series (S) and parallel (P) equivalent circuit representations of the MOS system conductance (G) and capacitance (C) in inversion. Experimental and simulated data for Si and InGaAs MOSCAPs are firstly analyzed mathematically. It is found that by interpreting the measured data in both the series and parallel mode, five independent values are obtained for the magnitude and frequency of the maxima and minima points of the $-\omega dC_{S,P}/d\omega$ and $G_{S,P}/\omega$ functions versus angular frequency (ω). The significance and application of the approach is presented and discussed.

2. Introduction

Measuring and analyzing the impedance of the metal-oxide-semiconductor (MOS) system has played a central role in the development of MOS structures. The *ac* impedance/admittance of the MOS structure at a given voltage (V) is typically represented via its frequency-dependent capacitive (C) and conductive (G) elements according to *either* a series *or* a parallel equivalent circuit. The resulting C (ω,V) and G (ω,V) data are used to characterize the basic MOS structure and its electrically active defect parameters [1]. For MOS structures the measured impedance are typically converted to C (ω,V) and G (ω,V) data using a parallel equivalent circuit model, even if not explicitly stated. The objective of this contribution is to investigate the impact and significance of using *both* series *and* parallel equivalent circuit representations for the case of an MOS system in inversion. Our study comprises, mathematical analysis, physics based simulations and experimental data for the impedance of Si and InGaAs MOSCAPs.

3. Equivalent Circuit Representations

Figure 1(a) shows a generic three-element equivalent circuit for a two-terminal MOS structure in inversion. when interactions between electrons and holes in the semiconductor and oxide traps (so-called border traps) are neglected. **Plots (b) and (c)** illustrate the corresponding two-element representations, in the parallel [$C_P(\omega)$, $G_P(\omega)$] and series [$C_S(\omega)$, $G_S(\omega)$] modes respectively. Based on the expression for the admittance of the three-element structure in **Figure 1(a),** expressions for $C_P(\omega)$, $G_P(\omega)$, $C_S(\omega)$, $G_S(\omega)$ can be derived in terms of the oxide capacitance (C_{OX}), the semiconductor capacitance (C_{SC}) and the semiconductor conductance (G_{SC}). Of course the $C_S(\omega)$, $G_S(\omega)$ curves are not independent of the corresponding $C_P(\omega)$, $G_P(\omega)$ curves because they are different interpretations of the same three-element structure in **Figure 1(a).**

It was recently shown that both G_P/ω and $-dC_P/d\log_e(\omega)$ ($\equiv -\omega dC_P/d\omega$) exhibit a maximum value of equal magnitude at the transition frequency (f_1) [2]. This relationship is true for all bias regions of the MOS [3]. Simplified analytical expressions for the magnitude and frequency of the maximum and minimum of G_P/ω and $-\omega dC_P/d\omega$ are shown in **Figure 2(a)**. These solutions are obtained by assuming G_{SC} and C_{SC} are frequency independent at the maxima, f_1, of G_P/ω and $-\omega dC_P/d\omega$. The validity of this assumption will be investigated in Section 4. The results obtained in **Figure 2(a),** from the parallel equivalent circuit model are replicated from physics-based *ac* simulations and also observed in experimental MOS structures in inversion [2, 3].

When the impedance of the three element equivalent circuit in **Figure 1(a)** is interpreted in a series C_S, G_S circuit, G_S/ω exhibits a minimum, not a maximum. Moreover, the maximum of $-\omega dC_S/d\omega$ does not occur at the same frequency as the minimum in G_S/ω. This is significant, as interpretation of the impedance data in both the series and parallel mode yields five separate features in the minima/maxima of the $-\omega dC/d\omega$ and G/ω functions. For the series circuit representation, the magnitude of the functions at the extremes is determined uniquely by C_{OX} and C_{SC}, with G_{SC} only appearing in the frequency of the maxima/minima (f_2 and f_3, respectively). A significant observation from the series mode representation in **Figure 2(a),** is that the minima in the G_S/ω function depends solely on the depletion capacitance in inversion. Consequently, N_D can be evaluated before extracting the oxide capacitance, C_{OX}. This allows C_{OX} evaluation from the maximum of the $-\omega dC_S/d\omega$, or from either maxima of the parallel circuit.
To verify the assumption that C_{SC} and G_{SC} are frequency independent around the transition frequencies, we extract them from the simulations where there is no uncertainty on the C_{OX} value. Simulations provides Cp and Gp (**Figure 1(a)**), which are used in combination with C_{OX} to extract C_{SC} and G_{SC} (**Figure 1(b)**). From this analysis it emerged that the assumption is not strictly correct at f_1 (parallel mode, **Figure 3(a)**), but it is much more accurate at f_2 and f_3, series mode, **Figure 3(b).** From inspection of the analytic expressions for the transitions frequencies in inversion, it is also noted that $f_3 > f_2 > f_1$ is generally true. By calculating the extremes of the $-\omega dC/d\omega$ and G/ω functions using the analytic expressions (**Figure 2**), and comparing to exact solution from TCAD, we obtain an error of ≈10% for the extremes of $-\omega dC_P/d\omega$ and G_P/ω, an error of ≈5% for $-\omega dC_S/d\omega$ and < 1% error for G_S/ω (not shown). The error is reducing because $f_3 > f_2 > f_1$, and thus the assumption that C_{SC} and G_{SC} are independent of frequency is more accurate for the series mode, which has then to be preferred for parameter extraction purposes. To overcome completely these errors, this work uses the analytical expressions shown in **Figure 2** to provide initial estimates for C_{OX}, N_D, C_{SC}, G_{SC}, and the precise parameters are extracted by reproducing the experimental characteristics using TCAD simulations.

4. Experimental Results and Simulations for Si and InGaAs MOS structures:

To examine these relationships in the parallel and series mode equivalent circuit, we take the experimental cases of a Si MOS and an InGaAs MOS. For the case of a silicon MOS in inversion, an *ac* response in inversion is not typically measured at frequencies above 1Hz. A minority carrier inversion response can be achieved by the intentional incorporation of elements which induce states near mid gap in silicon (e.g., Au), or by increasing the temperature, as the minority carrier generation increases as n_i^2/τ_g (where n_i is the intrinsic carrier concentration and τ_g is the minority carrier generation lifetime). In [4], an experimental minority carrier inversion response was achieved by increasing the temperature to 80ºC. Using the C (ω,V) and G (ω,V) data in [4], the $\omega dC_{P,S}/d\omega$ and $G_{P,S}/\omega$ functions for a Si MOS at 80ºC were constructed and are shown in **Figure 4.** The experimental data for the $-\omega dC_P/d\omega$, G_P/ω and $-\omega dC_S/d\omega$, G_S/ω functions exhibit the form predicted in **Figure 2**, where the minima of the G_S/ω and the maxima of $-\omega dC_S/d\omega$ now occur at different frequencies.

Figure 4 also shows *ac* simulations [5, 6], including Fermi-Dirac statistics, multi-valley band structure with non-parabolic corrections and SRH generation/recombination. The value of the silicon doping concentration (from $G_S/\omega = 2C_{SC}$ minima) is determined as $4x10^{15}$ cm^{-3}, in line with the value quoted in [4]. Then, the values of C_{OX} and τ_g can be determined from the peak frequency and peak magnitude in the parallel model ($-\omega dC_P/d\omega$ and G_P/ω) and the frequency of the $-\omega dC/d\omega$ in the series mode, using *ac* device simulations. Moreover, the doping concentration expression obtained directly from the G_S/ω minima is confirmed as correct based on the simulated multi-frequency CV/GV response.

Experimental multi-frequency C_P-V and G_P-V responses measured for Ni/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$/InP stacks, [7], are shown in **Figure 5.** The $In_{0.53}Ga_{0.47}As$ layer in 2μm in thickness and Si doping in the InGaAs layer is determined to have a mean value of $4x10^{17}cm^{-3}$ by electrochemical CV (ECV) depth profiling. The Al_2O_3 thickness is 6.3 nm from cross sectional TEM analysis. The experimental and simulated (without oxide traps) $G_{S,P}/\omega$ and $-\omega dC_{S,P}/d\omega$ functions are shown in **Figure 6**; they exhibit excellent agreement. From the minimum value of $G_{S,P}/\omega = 2C_{SC}$, a doping concentration $N_D=4.6x10^{17}$ cm^{-3} is determined in the InGaAs, which is in agreement with the value obtained from ECV. Excellent agreement between the simulated and experimental data is obtained using $C_{OX}=0.098$ F/m^2 (consistent with TEM thickness of 6.3 nm and ε_{ox} of 7 for Al_2O_3), $\tau g=$ 80 ps and $N_D=4.6x10^{17}$ cm^{-3} as inputs for the *ac* simulations.

It is noted that despite the presence of a high density of oxide (border) traps which are known to be present in Al_2O_3/InGaAs MOS structures [7], the simulated $-\omega dC_{S,P}/d\omega$ and $G_{S,P}/\omega$ functions, without oxide traps, are still in very good agreement with the experimental data. An agreement between the experimental data (with oxide traps) and *ac* simulations (without oxide traps) occurs because oxide defects distributed in energy and space do not generate extra peaks in the $G_{S,P}/\omega$ or $-\omega dC_{S,P}/d\omega$ functions. For peaks to occur in the functions G/ω and $-\omega dC/d\omega$, it is necessary that the physical mechanism controlling the *ac* response, at a given bias point, is associated to a specific time constant (in our case, the minority carrier generation rate in the depletion region). Interface states (not considered here) also generate peaks in the $G_{S,P}/\omega$ and $-\omega dC_{S,P}/d\omega$ functions, as a fixed surface potential relates to a specific capture/emission rate. In the case of oxide traps distributed at different position x along the oxide, at a given bias point, there is an exponential range of time constants resulting from the tunneling expression $\tau(x) = \tau_0 \exp(2kx)$ [8]. This produces no peaks in the G/ω or $-\omega dC/d\omega$ functions but leads to approximately linear increase of G/ω or $-\omega dC/d\omega$ with reducing frequency.

5. Conclusions

It is well established that for an MOS system in inversion, which demonstrates a measureable *ac* minority carrier response, G_P/ω plotted versus ω demonstrates a peak value. The peak occurs due to the time constant associated with the minority carrier generation rate. The corresponding function $-\omega dC_{,P}/d\omega$ also demonstrates a peak value at the same frequency and the same magnitude. In this work we have demonstrated that when the impedance data are interpreted as a series equivalent circuit, a minimum appears in the G_S/ω versus ω plots in the inversion region. The corresponding capacitance function $-\omega dC_{S,P}/d\omega$ exhibits a maximum value, and importantly, this occurs at a different frequency than the minima in G_S/ω. As a consequence, by interpreting the measured data in both the series and parallel mode, five independent values are obtained for the magnitude and frequency of the maxima and minima points of the $-\omega dC_{S,P}/d\omega$ and $G_{S,P}/\omega$ versus angular frequency ω.

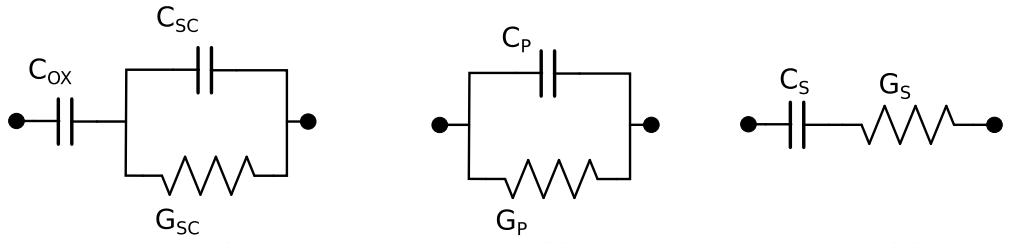
Analytic expressions obtained from the equivalent circuit representation are replicated from physics-based *ac* simulations and by experimental results for a close to ideal Si MOS and a non-ideal InGaAs MOS structure. An important finding, is that in the series mode interpretation, the analytic expression for the minima in the

G_S/ω function depends solely on the minimum depletion capacitance in inversion, leading to a direct evaluation of the semiconductor doping concentration without prior knowledge of the oxide capacitance. This allows unique evaluation of C_{OX} from either maxima in the parallel mode or from the maximum value of $-\omega dC_S/d\omega$ in the series mode. The minority carrier generation lifetime in the semiconductor (τ_g) is obtained from simulations, by matching the simulated frequencies of the maxima/minima to the experimental data, where three frequency values are available for minimization of errors. The approach described is applicable to any MOS system where an inversion response is detected over the bias, frequency and temperature range of the measurements.

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(a)	(b)	(c)
$Y = \frac{j\omega C_{ox}(G_{SC} + j\omega C_{SC})}{G_{SC} + j\omega(C_{ox} + C_{SC})}$	$C_p = C_{ox}\left[1 - \frac{\omega^2 C_{ox}(C_{ox} + C_{SC})}{{G_{SC}}^2 + (C_{ox} + C_{SC})^2\omega^2}\right]$ $G_p = \frac{\omega^2 {C_{ox}}^2 G_{SC}}{{G_{SC}}^2 + (C_{ox} + C_{SC})^2\omega^2}$	$C_S = \frac{C_{ox}({G_{SC}}^2 + {C_{SC}}^2\omega^2)}{{G_{SC}}^2 + C_{SC}(C_{ox} + C_{SC})\omega^2}$ $G_S = G_{SC} + \frac{{C_{SC}}^2\omega^2}{G_{SC}}$

Figure 1: (a) The generic representation of the MOS system in inversion, **(b)** the parallel interpretation and corresponding G_P and C_P functions in terms of the circuit elements appearing in **Figure 1(a)**, and **(c)**, the series representation and the corresponding G_S and C_S functions.

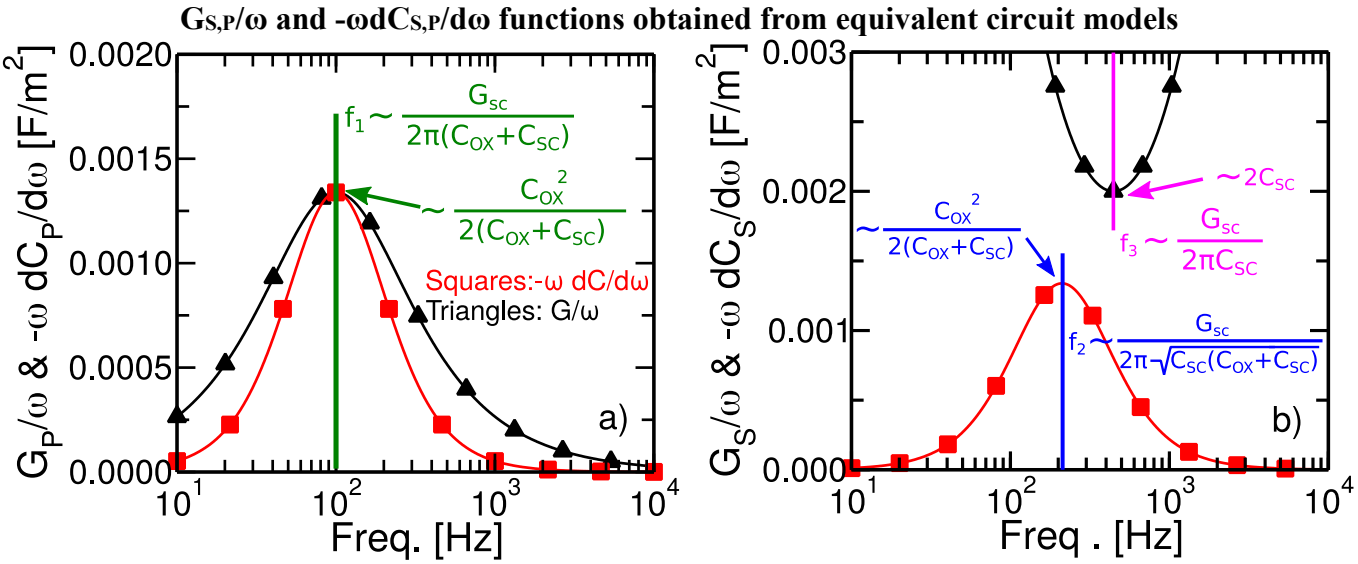


Figure 2: G/ω (triangles) and -ωdC/dω (squares) functions obtained directly from the simplified analytic solutions of the **(a)** parallel and **(b)** series RC equivalent circuit representations, for the case of an MOS structure with T_{ox}=10 nm, relative permittivity 3.9, and a doping concentration of N_D=5x10^{16} cm^{-3}. The transition frequency is selected as 100Hz, which fixes G_{SC} = 2 S/m^2. The corresponding expressions for the maxima/minima and transition frequencies are shown inset in the figure, assuming G_{SC} and C_{SC} are frequency independent at the maxima/minima.

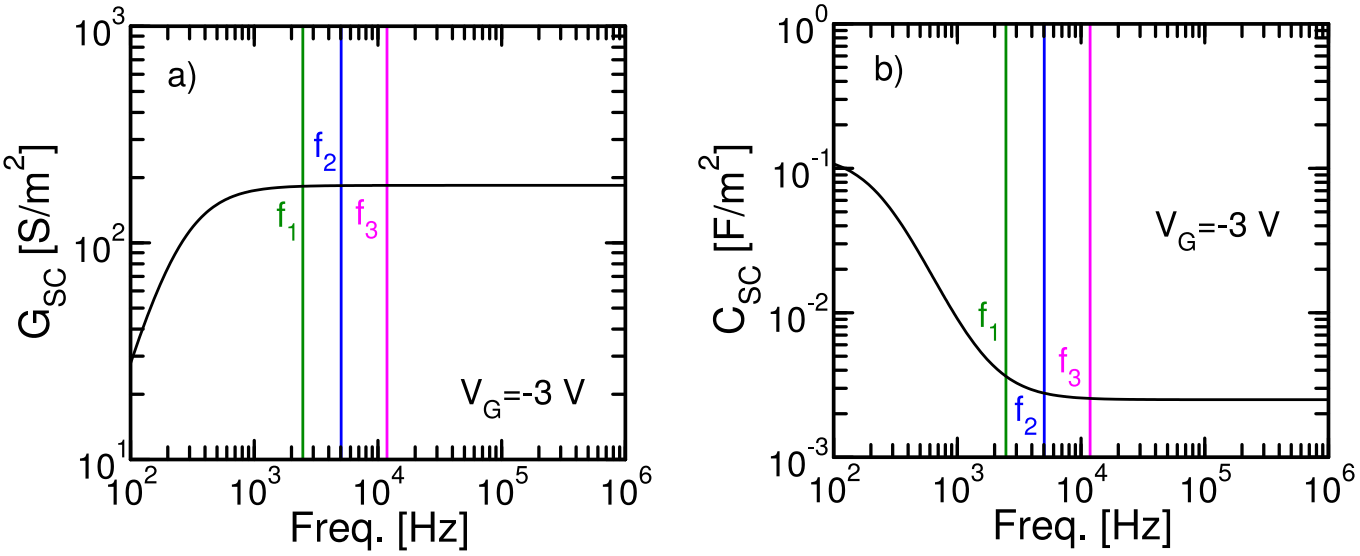


Figure 3: (a) G_{SC} and **(b)** C_{SC} extracted from the simulated data in **Figure 6** by assuming the equivalent circuit shown in **Figure 1(a)**. G_{SC} and C_{SC} show some frequency dependence; however, G_{SC} is essentially constant around all the transition frequencies, while C_{SC} is essentially constant only around f_2 and, to an even higher extent around f_3. This means that our assumptions on the frequency independence of G_{SC} and C_{SC} is much better verified for the series mode than for the parallel one. The frequency dispersion at low frequency is due to the minority carrier response time of the MOSCAP in inversion.

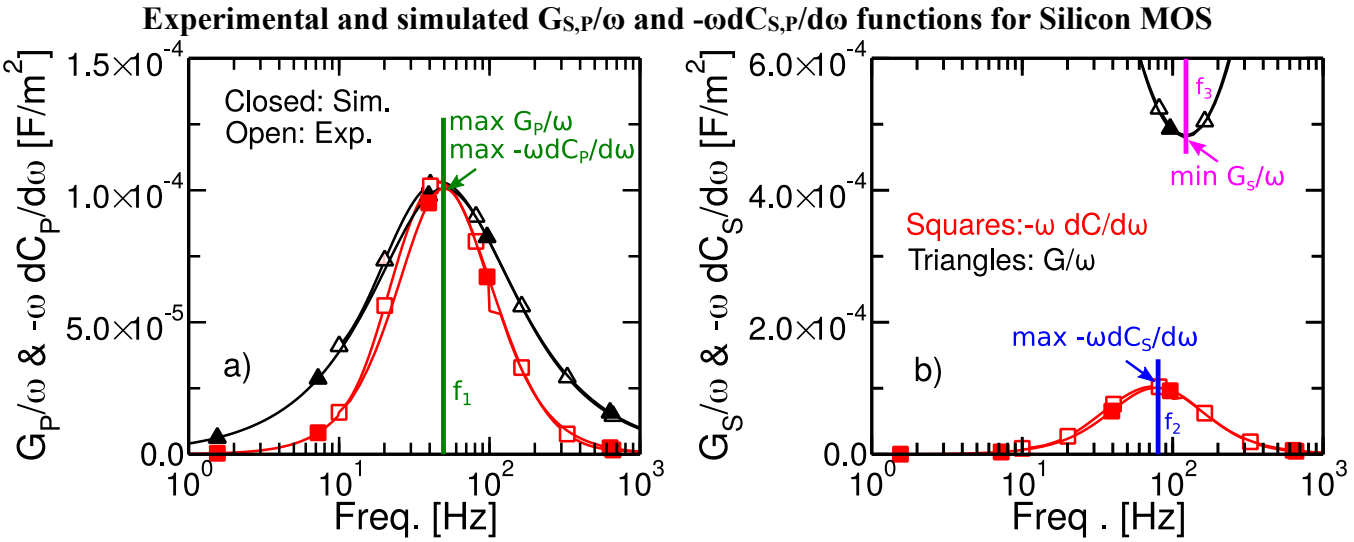


Figure 4: (a) G_P/ω (triangles) and $-\omega dC_P/d\omega$ (squares) functions constructed from the experimental (open symbols) *n*-Si MOS data in inversion (V_G = -7V, 80°C) [4], and **(b)** the corresponding G_S/ω and $-\omega dC_S/d\omega$ functions. The experimental sample is 100nm SiO_2 on Si with nominal N_D=1x10^{15} cm^{-3}. The graphs show both measurements (open symbols) and device simulations (closed symbols). Excellent agreement is obtained using N_D= 4x10^{15} cm^{-3} and a minority carrier generation lifetime τ_g = 1ms. For the parameter extraction, it is important to highlight that min G_S/ω depends only on N_D, max $-\omega dC_S/d\omega$, max G_P/ω and max $-\omega dC_P/d\omega$ depends on N_D and C_{OX}, f_3 depends on N_D and τ_g, f_2 and f_1 depends on τ_g, N_D and C_{OX}.

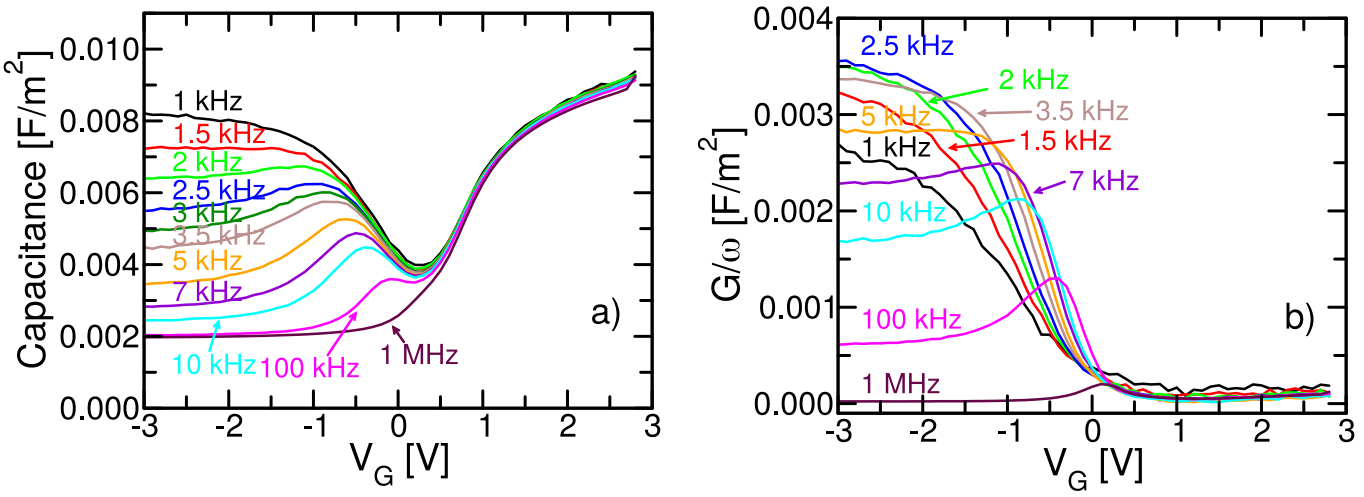


Figure 5. Experimental (a) C_P-V and (b) G_P-V responses at 25ºC for an InGaAs MOS structure. (Ni/Al_2O_3 (6.3nm)/*n*-$In_{0.53}Ga_{0.47}As$/InP) [7]. Si n-type doping in the InGaAs layer is nominally $4x10^{17}cm^{-3}$. The gate leakage is negligible over the CV/GV bias range.

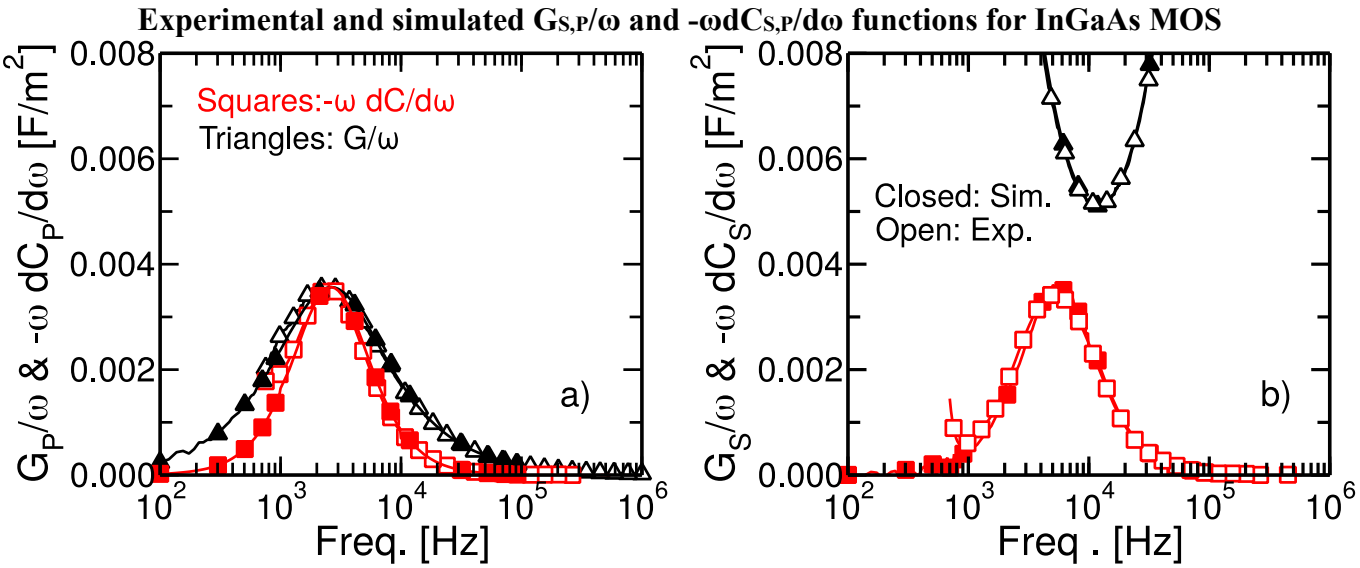


Figure 6. (a) G_P/ω (triangles) and $-\omega dC_P/d\omega$ (squares) functions constructed from the InGaAs MOS C (ω,V)/G (ω,V) responses shown in **Figure 5** (V_G=-3V)**, (b)** corresponding G_S/ω and $-\omega dC_S/d\omega$. Simulations based on C_{OX}=0.098 F/m^2 τ_g= 80 ps and N_D=$4.6x10^{17}$ cm^{-3} are in excellent agreement with the measurements for both circuit modes; the extracted N_D is in agreement with ECV measurements.