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Use of Semiconductor Optical Amplifiers in Signal Processing Applications

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Abstract: We describe a 42.6 Gbit/s all-optical pattern recognition system which uses semiconductor optical amplifiers (SOAs). A circuit with three SOA-based logic gates is used to identify the presence of specific port numbers in an optical packet header.
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OCIS codes: (200.4660) optical logic; (190.4390) nonlinear optics, integrated optics; (060.1155) all-optical networks.

1. Introduction

We illustrate the use of semiconductor optical amplifiers (SOAs) in signal processing by describing a photonic firewall that has been developed as part of the European FP6 project WISDOM [1]. An initial screening of incoming packets is performed using a novel logic circuit that requires only three gates for any length of target pattern [2]. Here we demonstrate experimentally the recognition and location of 16-bit port numbers in a 32-byte packet header.

2. Operating principle

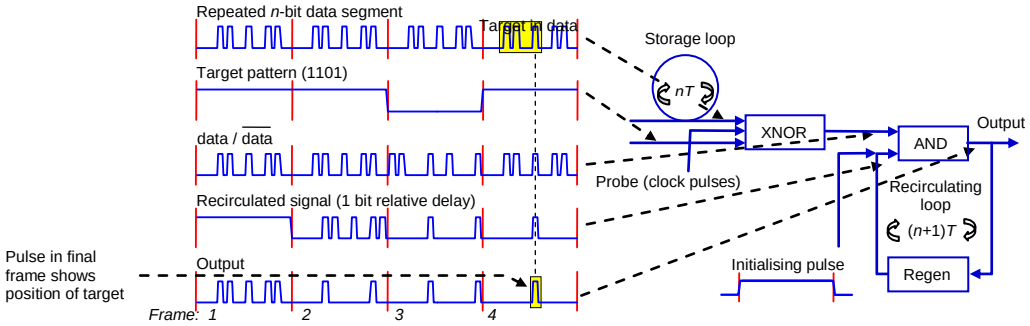


Fig. 1 Schematic of pattern recognition system with example waveforms.

The complete pattern matching system (Fig. 1) holds data in an n-bit storage loop to permit interaction between adjacent bits without the need for an unfeasibly short feedback loop [3]. A segment of input data $\{a_1 \ldots a_n\}$ is selected as the search field by switching it into the storage loop. The loop repeats the data segment into N output frames, where N is the number of bits in the target binary pattern being sought. The low-speed target pattern is generated at the rate of one bit per frame and is compared to the repeated high-speed data using an XNOR gate that gives a high-speed true output when its inputs are equal. Thus, during the first frame, the XNOR gate gives a binary output vector, Y^1, that is true for all the data bits a_i that match the first bit of the target, b_1:

$$y_i^1 = (a_i = b_1), \text{ for } i = 1 \ldots n. \quad (1)$$

An initialising pulse opens an AND gate to allow the first frame of Y to enter a second recirculating loop n+1 bit periods long. This loop includes a regenerator to suppress noise accumulation.

During the second frame, the XNOR gate compares all the a_i with the second bit of the target and, because the recirculating loop is one bit period longer than the storage loop, the results of this comparison are aligned at the AND gate with the first frame, Y^1, with a 1-bit relative delay. The output of the AND gate, Y^2, now becomes:

$$y_i^2 = y_{i-1}^1 \bullet (\text{ai} = b_2) = (a_{i-1} = b_1) \bullet (a_i = b_2) \quad (2)$$

After each circulation, the data in the recirculating loop is gated with the results of the comparison of the a_i with the next target bit, until after N circulations the output, Y^N, is given by:

$$y_i^N = (a_{i-N+1} = b_1) \bullet (a_{i-N+2} = b_2) \bullet \ldots \bullet (a_{i-1} = b_{N-1}) \bullet (a_i = b_N) \quad (3)$$

A true bit in the final frame, therefore, indicates an occurrence of the complete target pattern in the data. Because the output pulse is aligned with the final bit of the target pattern, it also indicates the position of the target in the data segment and could be used for synchronisation purposes. The system can search for targets of any length with the same number of gates, though to avoid contention the processing time should not exceed the total packet length.

3. Experimental system

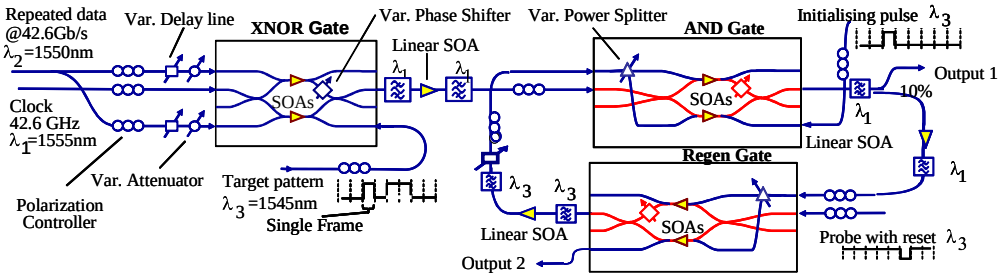


Figure 2. Final experimental arrangement of the pattern matching circuit

The three gates were hybrid-integrated Mach-Zehnder interferometers with SOAs in each arm (Fig. 2) [4]. "Push" and "pull" inputs enabled differential operation. The XNOR gate had an extra input to enable the target pattern to invert the output of the interferometer by inducing a phase change in one arm. The storage loop was simulated using a repeated 256-bit data pattern at 42.6Gbit/s which was searched for a 16 bit port number (25). The clock was a 42.6GHz train of 2ps pulses. Additional fibre-tailed components set the minimum loop length, and hence frame length, to 144.23ns (24 x 256-bit data). This frame was repeated 16 times. Target patterns and initial pulse were generated with a bit period equal to the frame length. At the end of the recognition process, the CW probe to the regenerator was interrupted for a frame to clear the loop.

4. Results and discussion

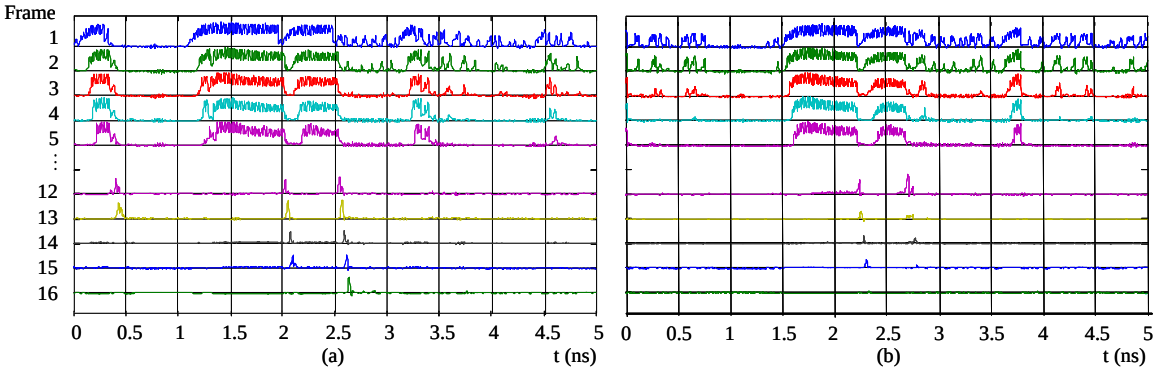


Figure 3. Experimental frame-by-frame output. (a) A pulse in the 16th frame indicates the presence of port number 25 in the packet. (b) The lack of a pulse in the final frame indicates that the port number is not present.

The system was tested with a set of packet headers, each of which had a port address to be assessed against the target address. Each successive frame of the output (Fig. 3) showed matches in the data to the sequence of target bits so far presented. When the port number was present in the data, a pulse appeared in the final frame aligned with the last bit of the target. The contrast of the output pulses was >10dB. Further photonic integration should substantially reduce the latency and allow the length of the recirculating loop to fit the data segment being searched.

5. Conclusions

An all-optical pattern recognition system that both identifies and locates occurrences of a port number in a data segment has been demonstrated at 42.6Gbit/s. The system requires only three gates for any length of target and is suitable for recognition and synchronisation tasks in packet-based optical transmission systems.

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