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Properties of latent interface-trap buildup in irradiated metal–oxide–semiconductor transistors determined by switched bias isothermal annealing experiments

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Isothermal annealing experiments with switched gate bias have been performed to determine the properties of the latent interface-trap buildup during postirradiation annealing of metal–oxide–semiconductor transistors. It has been found that a bias-independent process occurs until the start of the latent interface-trap buildup. During the buildup itself, oxide-trap charge is not permanently neutralized, but is temporarily compensated. © *2000 American Institute of Physics.* [S0003-6951(01)02601-8]

Regardless of many years of extensive research,[1] there are still gaps in understanding of postirradiation effects in metal–oxide–semiconductor (MOS) devices. One of the most controversial postirradiation phenomena certainly is the so-called latent interface-trap buildup (LITB).[2] The LITB is defined as a large sudden increase in interface traps during postirradiation annealing, after apparent saturation of the interface-trap density immediately following the irradiation.[2] It can have significant implications on performance and long-term reliability of MOS devices in radiation environments. The LITB has been observed in several different MOS device types and previous investigations have clarified some details pertinent to this process.[2–5] Namely, it has a much longer time scale than normal, conventional interface trap buildup,[6] which occurs during and immediately following the irradiation (several hours for normal buildup[6] versus several thousand hours for LITB at room temperature).[5] During the LITB, the increase in interface traps is accompanied by the decrease in oxide-trap charge. The LITB is a thermally activated process, with an activation energy of 0.47 eV.[2] The LITB is also a radiation-induced effect, enhanced by radiation dose and positive gate bias.[2,5] We have recently performed a detailed study aimed at elucidating additional details of the LITB. Here, we report and discuss the results of switched bias isothermal annealing experiments that have revealed some important properties of this phenomenon.

Commercial *n*-channel power vertical double-diffused MOS field-effect transistors (VDMOSFETs) EFL1N10,[5] known to exhibit the LITB, were irradiated at room temperature with Co-60 gamma rays to a total dose of 200 Gy at a dose rate of 0.03 Gy(Si)/s. The gate bias (V_{GS}) during irradiation was +10 V. Irradiated devices were subjected to isothermal annealing, during which time the gate bias was switched from positive to negative or vice versa at some characteristic points. The first data points in the figures were measured immediately after irradiation, and the second points immediately before annealing. Transistors were characterized for the densities of radiation-induced oxide-trap charge [$\Delta N_{ot}(\mathrm{cm}^{-2})$] and interface traps [$\Delta N_{it}(\mathrm{cm}^{-2})$], using the midgap (MG) technique of McWhorter and Winokur.[7] The modified charge-pumping (CP) technique for power VDMOSFETs (Ref. 8) was also used. Only MG data will be shown here, CP data in all cases confirm the trends of MG data.

Figure 1 shows ΔN_{ot} and ΔN_{it} during annealing for the case when the bias switch was made immediately before the start of LITB, i.e., at the end of phase 1 of annealing.[9] It can be concluded that the ΔN_{it} and ΔN_{ot} behaviors are independent of the bias sign during phase 1. Moreover, the bias sign during this phase does not affect device response at later annealing times. It is the bias sign in the period after the start of the LITB that determines the defects' behavior. The LITB is observed for both positive and negative V_{GS}, but is largely suppressed in the latter case.

Figure 2 shows the effect of bias switch from positive to negative at some characteristic points during annealing.

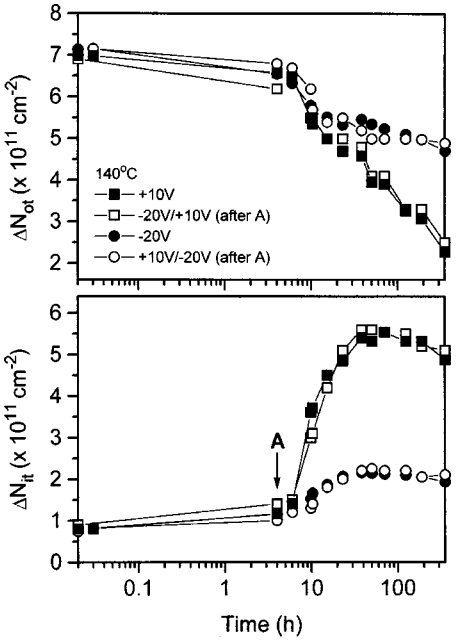


FIG. 1. ΔN_{ot} and ΔN_{it} during switched bias isothermal annealing at 140 °C. The bias was switched at point A (4 h).

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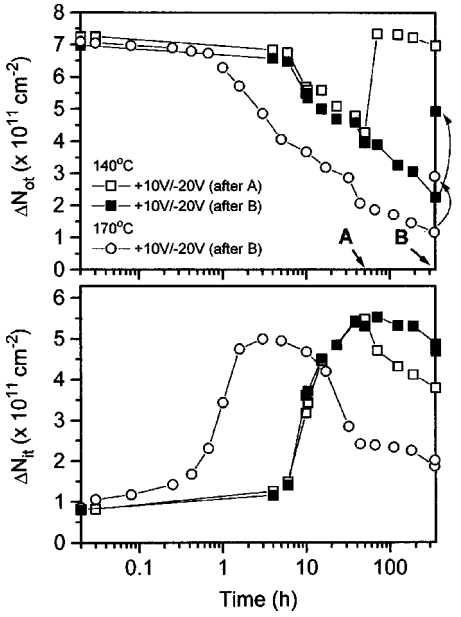


FIG. 2. ΔN_{ot} and ΔN_{it} during switched bias isothermal annealing at 140 and 170 °C. The bias was switched from positive to negative at point A (50 h) or B (340 h) at 140 °C and at point B (340 h) at 170 °C. Arrows point to ΔN_{ot} values after the bias switch at 340 h.

When the switch is made at the point of maximum ΔN_{it} (140 °C data), ΔN_{ot} ''rebounds'' to its preannealing value and the ΔN_{it} decrease is enhanced. The first postswitch data point in Fig. 2 was measured some 20 h after the switch; however, it takes only several minutes, if not even less, for dramatic changes in ΔN_{ot} to occur.[10] These changes are shown to be reversible: switching the bias to positive again leads to ΔN_{ot} values close to the values before the first bias switch.[10] It can be concluded that during phase 2 of annealing, the oxide-trap charge is not permanently neutralized, but rather temporarily compensated by the electrons tunneling from Si under the positive bias.[11] When the bias is switched at later annealing times, i.e., at the end of phase 3 (140 and 170 °C data), ΔN_{ot} also rebounds, but not quite to its preannealing value, while ΔN_{it} changes are almost negligible. This implies that at later annealing times there is permanent neutralization of a portion of the oxide-trap charge. Since this portion is more significant in both absolute and relative terms at the higher annealing temperature, the permanent neutralization is most probably caused by thermal emission of electrons from the oxide valence band to traps in the oxide.[12]

The presented experimental results have serious implications for the understanding of processes underlying the LITB, which will be briefly discussed below. It is clear from Fig. 1 that some bias-independent process occurs during phase 1 of annealing. This is inconsistent with the LITB model involving bias-assisted tunneling of electrons from Si and the assumption of a peaked hole-trap distribution further from the Si/SiO_2 interface than is typical.[2]

An interesting possibility is to attribute the LITB to retarded H^+ transport through SiO_2 and Si and its interactions at or near the Si/SiO_2 interface[3] and/or in the Si surface layer.[4] Commercially processed oxides, as is our case, are plausible candidates for retarded H^+ transport, during which the H^+ is captured at traps associated with O vacancies, and released at later annealing times.[3,4] If we take the scenario of interface-trap formation by H^+ reaction at the interface, we would have essentially the same mechanism as for conventional interface-trap buildup,[6] but slowed down. A particularly intriguing possibility is that H^+-induced passivation of dopants in the Si surface layer may lead to a switch from buried to surface channel conduction.[4] In such a case, the latent increase in ΔN_{it} would not necessarily have to come as a consequence of the increase in the actual number of interface traps, but as a result of their increased influence on conduction in the *p*-channel region of our devices, as the current would move closer to the Si/SiO_2 interface. The reversible exchange of H^+ between near-interfacial SiO_2 and Si, along with the reversible oxide-trap charge compensation by electrons,[11] may be responsible for rebound in ΔN_{ot} after the bias switch in Fig. 2 and also for the reversible ΔN_{ot} changes in subsequent bias switches.[10] However, the bias-independent behavior during phase 1 of annealing is more difficult to account for. It might be that the H^+ ions are, during this period, so deeply trapped that the bias sign has no influence on their transport. On the other hand, for the retarded H^+ transport concept to be consistent with experimental data in Fig. 2, almost 45% of ΔN_{ot} after irradiation should be due to hydrogen ions, and not due to trapped holes. This is not very likely, since it has been established that the majority of the radiation-induced oxide-trap charge is from holes trapped at E' centers.[13]

The data in Fig. 1 are in accordance with the so-called hydrogen cracking models,[1,4,5] as they assume as a first step diffusion to the Si/SiO_2 interface of radiolytic H_2 released in the gate oxide and/or adjacent structures (poly-Si gate, chemical-vapor-deposited oxide).[14] In addition, these models have been shown to be consistent with other previously known details of the LITB as well.[5] The crucial step in these models is the H_2 cracking reaction at the positive charge centers in the vicinity of the interface.[14] However, the cracking reaction would lead to permanent neutralization of the oxide-trap charge during the LITB, i.e., phase 2 of annealing, which is in contrast to the data in Fig. 2.

It is clear that additional work is required to elucidate all the details of the LITB. It might be that an explanation should be sought in non-P_b like nature of most of electrically observable interface traps.[15] This assumption is in contrast to the vast majority of work on radiation effects[1] and is still to be verified.[16] Finally, within the context of the P_b approach, and not necessarily in direct connection with the LITB, we would like to stress the importance of taking into account the concurrent running of interface-trap formation and passivation processes.[5] This fact has often been neglected in analysis of the postirradiation response of MOSFETs.[1] It depends on experimental conditions, such as gate bias and temperature, which process (formation or passivation of interface traps) will dominate; and it is the balance between formation and passivation kinetics that determines ΔN_{it} postirradiation behavior.[5,10] Data in Fig. 2 reinforce this approach. Passivation of interface traps during long-term postirradiation annealing has been attributed to the reaction of slowly diffusing H_2O at the interface and is bias independent and enhanced by temperature,[5] while the formation is largely enhanced by positive bias.[5,6] Thus, suppression of interface-trap formation by negative bias during phase 3 of annealing leads to pre-

dominant passivation at earlier times than in the case when both processes are enabled to occur (140 °C data). On the other hand, increased temperature also leads to predominant passivation at earlier times (140 °C vs 170 °C data).

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