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GeSn semiconductor for micro nanoelectronic applications

Thesis presented by

Emmanuele Galluccio

for the degree of

Doctor of Philosophy

University College Cork

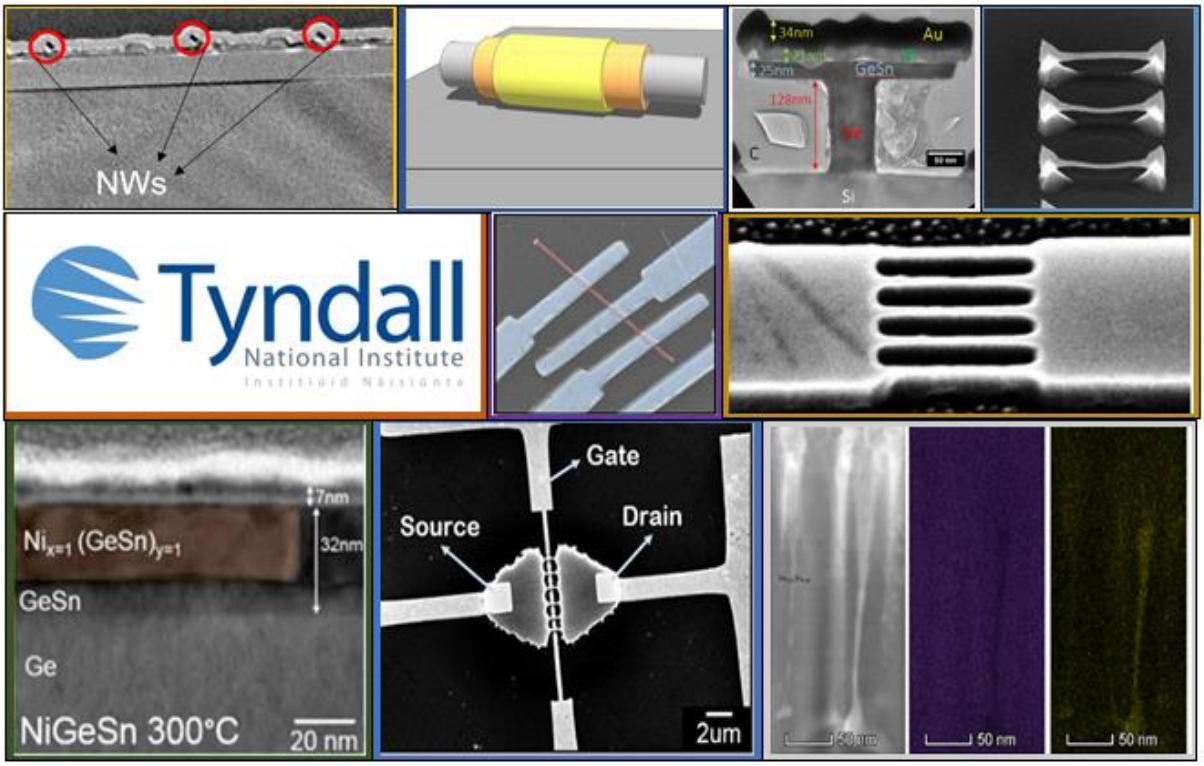
Department of Electrical and Electronic Engineering

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April 2020



University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

GeSn semiconductor for micro nanoelectronic applications

Emmanuele Galluccio,
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Declaration

I Emmanuele Galluccio certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents.

Emmanuele Galluccio

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This project was not realizable without the help and the contributions of many individuals that I would like to genuinely express my gratitude.

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List of Publications

Based on results presented in this thesis

(1) **Galluccio E**., Petkov N., Mirabelli G., Doherty J., Shih-Va L., Fang-Liang L., Chee Wee L., Holmes J., Duffy R., *Formation and characterization of Ni, Pt, and Ti stanogermanide contacts on Ge0. 92Sn0. 08.* Thin Solid Films, 2019. **690**: p. 137568.

(2) **Galluccio E**., Petkov N., Mirabelli G., Doherty J., Shih-Va L., Fang-Liang L., Chee Wee L., Holmes J., Duffy R...*, Ni, Pt, and Ti stanogermanide formation on Ge0.92Sn0.08,* 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Grenoble, France, 2019, pp. 1-4

(3) Doherty J., Biswas S., **Galluccio E.**, Broderick C., Garcia A., Duffy R., O'Reilly E., Holmes J., *Progress on Germanium-tin Nanoscale Alloys, ACS Chem. Mater. 2020, 32, 11, 4383–4408*

(4) **Galluccio E**., Doherty J., Biswas S., Holmes J., Duffy R., *Field-Effect Transistor Figures of merit for VLS grown* $Ge_{1-x}Sn_x$ (x=0.03-0.09) *Nanowire devices,* ACS Applied Electronic Materials doi.org/10.1021/acsaelm.0c00036. 2020.

(5) Galluccio E., Mirabelli G., Harvey A., Conroy M., Napolitani, E., Duffy, R., *Cell formation in stanogermanides using pulsed laser thermal annealing on* $Ge_{0.91}Sn_{0.09}$. Materials Science in Semiconductor Processing, 105399¸2020

Conference contributions and talks

- **E. Galluccio**, J. Holmes, R. Duffy., *Modelling Ge(1-x)Sn(x) junctionless nanowire transistors through the study of the bandgap and effective mass in the alloy*. E-MRS fall meeting, September 18-21, 2017, Symposium L, Warsaw, Poland.
- **E. Galluccio**; Petkov, N., Mirabelli, G., Doherty, J.,Shih-Va, L., Fang-Liang, L., Chee Wee, L., Holmes, J., Duffy, R...*, Ni, Pt, and Ti stanogermanide formation on Ge0.92Sn0.08,* 2019, EUROSOIULIS 2019, Grenoble, France.

Other contributions that are not discussed in this thesis

(6) Duffy R., Kennedy N., Mirabelli G., **Galluccio E.**, Hurley P.K., Holmes J.D. and Long B., 2018, March. *Monolayer doping and other strategies in high surface-to-volume ratio silicon devices*. In 2018 18th International Workshop on Junction Technology (IWJT) (pp. 1-6). IEEE.

(7) Duffy R., Thomas K., **Galluccio E.**, Mirabelli G., Sultan M., Kennedy N., Petkov N., Maxwell G., Hydes A., O'Connell D. and Lyons C., 2018. *AsH3 gas-phase ex situ doping 3D silicon structures*. Journal of Applied Physics, 124(4), p.045703.

(8) Duffy R., Meaney F. and **Galluccio E**., 2020. *Doping Considerations for Finfet, Gate-All-Around, and Nanosheet Based Devices.* 237th ECS Meeting with the 18th International Meeting on Chemical Sensors (IMCS 2020) (May 10-14, 2020)

(9) Biswas S., Doherty J., **Galluccio E**., Manning H., Conroy M., Bangert U., Duffy R., Boland J. and Holmes J. D., *Stretching the Equilibrium limit of Sn Incorporation (x > 0.3) in Ge1-xSnx nanowires under High Pressure*. (in-preparation).

“As with people, it’s the defects that make materials interesting.”

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List of abbreviations

α-Sn	Gray-Tin
β-Sn	White-Tin
$\mathcal{E}_{ox}$	Dielectric constant oxide
$\mathcal{E}$si	Dielectric constant Silicon
ρ_C	Contact Resistivity
4PP	Four Point Probe
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
Al_2O_3	Aluminum oxide
AMAT	Applied Materials
As	Arsenic
Au	Gold
B	Boron
BCC	Body Centre Cubic
B_g	Bandgap
BOE	Buffered oxide etching
BTBT	Band to Band Tunneling
C	Carbon
C_B	Conduction Band
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical vapour deposition
DFT	Density Functional Theory
DI	Deionised
DIBL	Drain Induced Barrier Lowering
DOS	Density Of State
EBL	Electron beam lithography
EDX	Electron Dispersive X-ray
Ed	Energy Displacement
EF	Energy Fermi level
Eg	Energy gap
EPM	Empirical pseudopotential method

E_{VAC}	Vacuum Energy level
eSBH	electron Schottky Barrier Height
F	Fluorine
FA	Furnace Annealing
FCC	Face-Centered Cubic
FET	Filed Effect Transistor
FFT	Fast-Fourier-Transformation
FLA	Flash Lamp Annealing
GAA	Gate all around
Ga	Gallium
Ge	Germanium
$Ge_{1-x}Sn_x$	Germanium-Tin alloy
HAADF	High Angle Annular Dark Filed
HCl	Hydrogen chloride
HF	Hydrogen fluoride
HFO_2	Hafnium dioxide
high-K	high dielectric constant
hSBH	hole Schottky Barrier Height
HSQ	Hydrogen Silsesquioxane
IC	Integrated Circuit
ICP	Inductive Coupled Plasma
ICT	Information & communication technology
I_{leak}	Leakage current
I_{off}	Off current
I_{on}	On current
IPA	Isopropyl Alcohol
IRDS	International Roadmap Device and System
ITRS	International Technology Roadmap for Semiconductors
JNT	Junctionless transistor
LN_2T	Liquid nitrogen temperature
LTA	Laser Thermal annealing
MBE	Molecular Beam Epitaxy
MLD	Molecular Monolayer Deposition

MLDA	Modified-Local-Density-Approximation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUGFET	Multiple Gate Field Effect Transistor
MS	Metal-semiconductor
MWA	Microwave Annealing
N	Nitrogen
N_2	Di-Nitrogen
Ni	Nickel
NiGe	Nickel-Germanide
NiGeSn	Nickel-Stanogermanide
NiSi	Nickel-Silicide
NMOS	Negative channel Metal Oxide Semiconductor
NWs	Nanowires
O	Oxygen
PECVD	Plasma Enhanced Chemical Vapour Deposition
PMMA	Poly Methyl Methacrylate
PMOS	Positive channel Metal Oxide Semiconductor
PLM	Pulsed laser melting
Pt	Platinum
PtGe	Platinum-Germanide
PtGeSn	Platinum-Stanogermanide
PVD	Physical Vapour Deposition
R_C	Contact Resistance
RIE	Reactive Ion Etching
RMS	Root Mean Square
Rp	Projected Range
R_{sh}	Sheet Resistance
RT	Room Temperature
RTA	Rapid Thermal annealing
SCE	Short Channel Effects
S/D	Source/Drain
SEM	Scanning Electron Microscopy
Si	Silicon

SIMS	Secondary ion mass spectroscopy
SiN	Silicon Nitride
Sn	Tin
SiO_2	Silicon Oxide
SOI	Silicon on Insulator
SPER	Solid Phase Epitaxial Regrowth
SRIM	Stopping and Range of Ions in Matter
SS	Subthreshold Slope
T	Temperature
TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscopy
TFET	Tunnel field effect transistor
TLM	Transfer Length Methodology
Ti	Titanium
TiGe	Titanium-Germanide
TiGeSn	Titanium-Stanogermanide
TiSi	Titanium-Silicide
TMD	Transition Metal Dichalcogenides
TRIM	Transport of Ions In Matter
tox	Thickness oxide
ULSI	Ultra Large Scale Integration
V_B	Valence Band
VCA	Virtual Crystal Approximation
V_{ds}	Drain-Source Voltage
V_{th}	Threshold Voltage
VLS	Vapor-Liquid-Solid
VS	Virtual Substrate
WF	Work Function
XTEM	Cross-sectional Transmission Electron Microscopy

Abstract

Within the last few years the steady electronic evolution lead the semiconductor world to study innovative device architectures and new materials able to replace Si platforms. In this scenario $Ge_{1-x}Sn_x$ alloy attracts the interest of the scientific community due to its ability to tune the material bandgap as a function of Sn content and its extreme compatibility with Si processing. Although the enhanced optical properties of $Ge_{1-x}Sn_x$ are evident, the augmented electrical properties such as the higher electron and holes mobility are also beneficial for metal oxide semiconductor. Therefore the alloy is expected to be a potential solution to integrate both electrical and optical devices.

On one hand, several theoretical and experimental works depict the $Ge_{1-x}Sn_x$ alloy as a novel and fascinating solution to replace Si; on the other hand the material novelty forces us to enhance the knowledge of its fundamental physical and chemical properties, re-adapting the processing steps necessary to develop electronic and optical devices.

In this dissertation a comprehensive study on $Ge_{1-x}Sn_x$ has been undertaken and discussed analysing a wide range of topics. The first chapter provides a detailed theoretical study on the electronic properties of the GeSn performed using first principle methods; subsequently the data obtained have been inserted into a TCAD software in order to create and calibrate a library used to simulate electrical devices. It is important to note, that at the beginning of this PhD GeSn was not an available material in the Synopsys device software, and thus it had to be defined from scratch

As a next point, since the ever decreasing device size push toward the definition of Ohmic contacts, different stanogermanide films have been thoroughly analysed using various metals (Ni, Pt and Ti) annealed with two distinct methodologies (Rapid Thermal Annealing and Laser Thermal Annealing).

Subsequently, considering the material limitation such as the limited thermal budget and the Sn segregation, an exhaustive study on the material doping has been firstly discussed theoretically and after experimentally characterized using both classical ion implantation and layer deposition techniques.

The different building blocks of Field Effect Transistors have been investigated and tuned individually with the aim to develop FET devices with bottom up approach. Then, Field Effect Transistor devices using GeSn NWs grown by a VLS methodology with Sn composition ranging from (0.03-0.09 at.%) have been developed and extensively characterized with the state of the art present in literature.

Finally the analysis of highly selective etch recipes lead to the development of sub-nm device configuration such as Gate-All-Around (GAA) structure obtained using classical top down lithography approach. The innovative structure was electrically characterized highlighting the possibility to obtain decananometer device architecture with this innovative alloy.

Lastly thesis summary and final outlooks were reported with the aim to outline the thesis contribution and the future material investigations.

1 | Introduction

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This chapter is adapted from the following publication:

(1) Doherty, J.; Biswas, S.; **Galluccio, E.**; Broderick, C.; Garcia, A.; Duffy, R.; O'Reilly, E.; Holmes, J. *Progress on Germanium-tin Nanoscale Alloys ACS Chem. Mater. 2020, 32, 11, 4383–4408*

1 | Introduction

In this section the conventional CMOS scaling process is extensively discussed pointing out the importance of using new semiconductor materials and alternative device architectures to overcome the technology limits. In the first part the miniaturization process is broadly debated focusing mostly on the challenges and the opportunities in relation to scaled dimensions. Thereafter, a brief literature review of the $Ge_{1-x}Sn_x$ alloy is made focusing on three key points: modelling work to estimate the material features, the creation of reliable substrates with high enough Sn content, and lastly on the development of electronic and optical devices. Finally, a manuscript overview has been outlined to introduce the reader into this dissertation.

1.1 The Scaling of CMOS technology

Down the years the disruptive semiconductor innovations set the pace for the steady progress of the *Information & Communication Technology (ICT)*. Considering the growing number of electronic devices in daily life, the transistor device had a breakthrough impact on modern society in several sectors such as telecommunication, medical, financial and environmental. *Germanium (Ge)* had always played an active and important role in the outstanding electronics history; as a matter of fact the first transistor was manufactured with Ge in the Bell labs on 1947 by W. Shockley, W. Brattain and J. Bardeen [1].

Nevertheless, the difficulty in handling Ge, in conjunction with superb *Silicon oxide (SiO_2)*, favoured *Silicon (Si)* development over the years [2]. From the birth of the first functional *Metal-Oxide-Semiconductor-Field-Effect-Transistor MOSFET* (1959, D. Kang and J. Atalla) up to the modern microprocessors, giant steps have been made in circuitry manufacturing [3]. The scientific proposal described by G. Moore in 1965 has been followed for generations by semiconductor companies as the driving force for endless innovations.

For a long period scaling followed the Dennard scaling rules [4] even though considerable efforts have been made to meet the Moore's law criteria. In the last 50 years the semiconductor companies focused relentless on Moore's law [5] to reduce the transistor device size passing from 10 µm channel length to 7 nm nowadays. Indeed Fig. 1.1 shows both the actual status and the predicted miniaturization

process according to the IRDS international roadmap and *International Technology Roadmap for Semiconductors (ITRS)* [6].

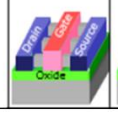
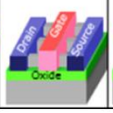
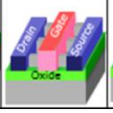
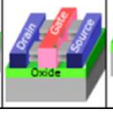
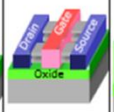
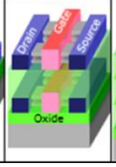
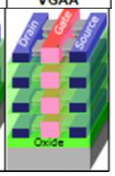
YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
							

Figure 1.1: *Evolution of MOSFET gate length in integrated circuit where area listed the "node range", the architecture used and the representative device image. (adapted from [7]).*

Nowadays the electrical scaling trend has become a significant challenge to sustain for the semiconductor companies due to the onset of physical restrictions and bottlenecks [8]. Essentially for a long time the scaling rules were based on the constant electrical field paradigm, in order that only the gate was able to control the current flow. Nevertheless, the continuous device reduction led to a constant *gate oxide thickness (tox)* thinning, with the inset of *high dielectric constant materials (high-k),* used to reduce the tunneling effects and gate leakage current. Nonetheless as the technology node passed 130 nm, *CMOS* scaling had to think of alternative solutions to improve the device performance. In the beginning, the introduction of tensile or compressive strain respectively in negative channel MOS (*N-MOS*) and in positive channel MOS (*P-MOS*) allowed the continuation of the conventional scaling route. Although the application of stress lead to performance boosting [9-12], the progressive device reduction induced to a steady electrical degradation due to two bottlenecks; namely *short channel effects (SCE)* and the increment of the *leakage current (I_{leak}).* Therefore to go beyond the 32 nm technology node the *multiple gate (MUGFETs)* device architecture has been proposed [13, 14]. The main idea was to make the transistor more efficient against SCE by improving the gate electrostatic control. For many years numerous studies on physical properties [15-17] and process variability [16, 17] have been performed, while new devices architectures with channel lengths in the decananometer range have already been manufactured and commercially used [18-21].

However as the logic device scaling approached 10 nm the semiconductor companies had to address both the historical scaling challenges (SCE, mobility) as

well as new demands associated with the extreme gate length shrinkage (quantum effects).

Figure 1.2 summarizes all the insights used to overcome the scaling limits as a function of the technology node released. Each area highlighted with a different colour emphasizes the intuition used to address the challenges. According to the *International Roadmap Device and System* (IRDS) [7] and Nereid roadmaps [22] the next steps would be the development of vertical hybrid structure.

Therefore new technology and alternative materials are required to go beyond the limits. Then in this scenario, Ge and its alloy seems to show the potentiality to replace Si due to the higher carrier mobility, the ability to tune the *bandgap* (B_g), and the extreme compatibility with existing Si manufacturing processes.

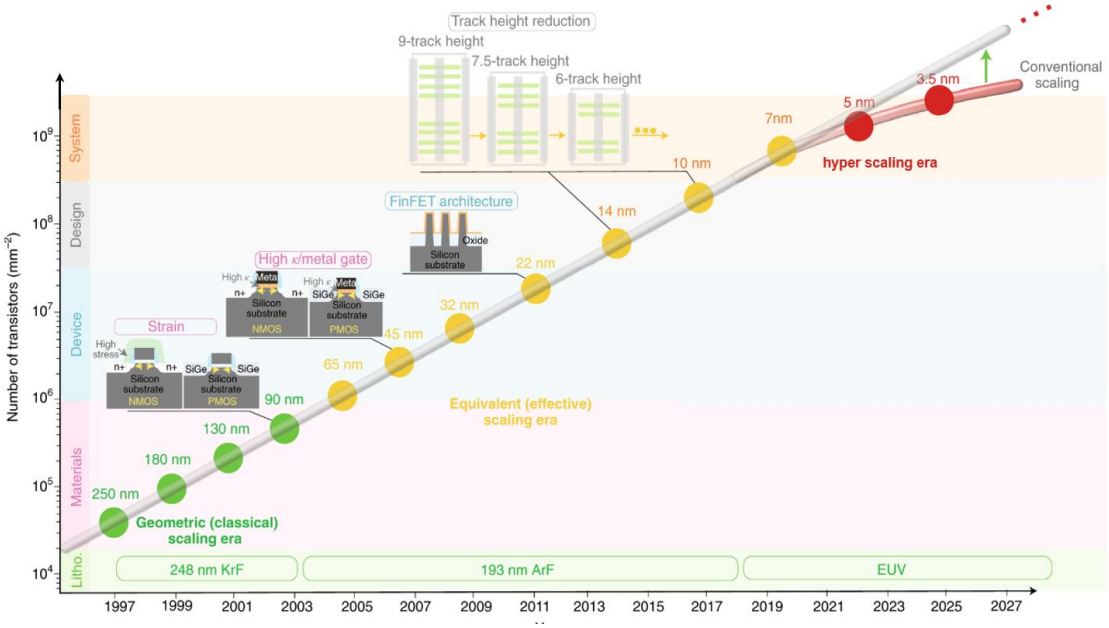


Figure 1.2: *Generic overview on the scaling evolution divided into three different scaling areas: geometrical equivalent and hyper scaling, adapted from* [23].

1.1.1 Transistor shrinking challenges

The main driving force that lead the semiconductor company to reduce the transistor size was increasing device speed coupled with reduced manufacture costs. Indeed, smaller circuits in the same time increased operating speed, while allowing more die in one wafer, cutting the total cost.

However to have a comprehensive view, before exploring the major challenges faced by the scaling process, it is important review some basic MOSFET equations and performance benchmark parameters.

Figure 1.3 shows the typical planar MOSFET I_{ds}-V_{gs} characteristics in its different region of operation. Starting from off status *(I_{off})*, where no voltage is applied on the gate, the drain current is equal to zero, see Fig. 1.3.(a). Increasing the gate voltage the device reaches the threshold voltage (V_{th}) condition, defined as the point where the minority carriers start to be attracted from the channel forming an inversion layer underneath the gate. At this stage as the drain voltage increases the device enters in triode mode, see Fig. 1.3.(b).

Furthermore, increasing V_{ds} the channel starts to saturate due to the enhancement of the depletion regions. In this situation the channel is partially truncated, but the strong electrical field around the drain region allow the carrier to pass the truncated region, see Fig. 1.3.(c). In saturation regime, as pointed out by the equation, the current is almost independent of the drain voltage, it is primarily controlled by the gate source voltage. [24]

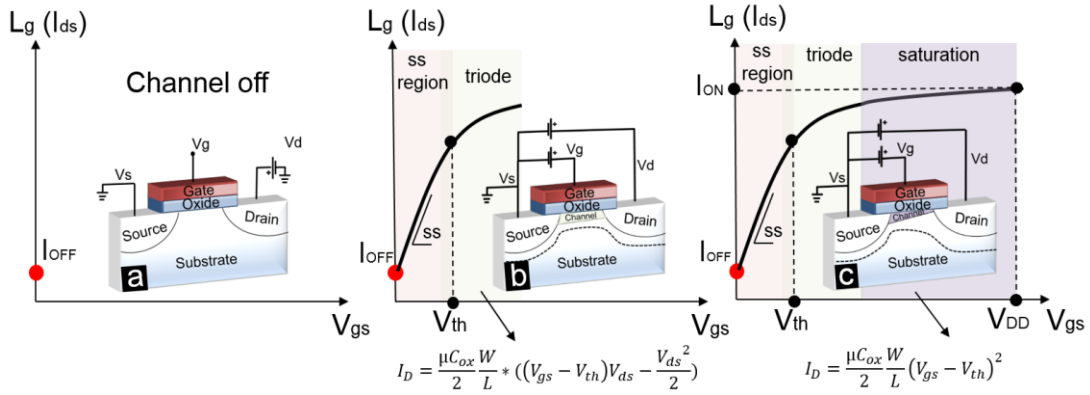


Figure 1.3: *Id-Vg characteristics in log scale for a MOSFET transistor with the representative device schematic. (a) shows the device when it is off, while (b) and (c) show respectively the characteristics in triode and saturation region with the current output equation.*

Beside the typical working region of MOSFETs other important parameters to take into account for the evaluation of the fundamental transistor performance are the intrinsic speed (3); namely the time required for the input to be propagated to the output to drive a second similar inverter; the switching energy (4), composed by two parameters; P_{ACTIVE} and $P_{PASSIVE}$ respectively related to the charging and the discharging of capacitance and to the power dissipation when the device is in sleep mode. Finally the *subthreshold slope SS* (5) that express the velocity transition between I_{off} and I_{on}.

$$\tau = C_{GATE} * V_{DD}/I_d \quad (3)$$

$$P_{TOT} = P_{ACTIVE} + P_{PASSIVE} = C * {V_{DD}}^2 f + I_{leakage} * V_{DD} \quad (4)$$

$$SS = \left(\frac{KT}{q}\right) * \ln 10 * (1 + \frac{C_{bulk}}{C_{gate}}) \quad (5)$$

where f denotes the frequency, *K* the Boltzmann constant, *T* the temperature, *q* the electron charge, V_{DD} is the supply voltage, I_d the drain current and $I_{leakage}$ represent the leakage current; while $C_{bulk} = \varepsilon_{Si}/W_d$ and $C_{gate} = \varepsilon_{ox}/t_{ox}$ are respectively bulk and gate capacitances. Looking at all the equations, the basic ideology that drove MOS device scaling was to keep I_d as large as possible while V_{DD} and $I_{leakage}$ as small as possible in order to have fast switching without energy waste.

Nevertheless, as the device size pushed towards nanodecanometer technological nodes, numerous issues, revealed in the form of unwanted side effects, started to be considered.

As a regards of *Short Channel Effects (SCEs)* [15] several aspects have to be contemplated due to the strong influence on the electrical device performance.

1. *Drain Induced Barrier Lowering (DIBL)* leads to undermine the gate control due to the channel potential barrier reduction. As the gate size decreases the current into the device tends to be strongly influenced by the drain depletion region extension leading to a degradation of SS and V_{th} [8].
2. *Punchthrough* occurs if the drain and source are enough close, the formation of a unique depletion region may happen under the gate due to the junction depletion regions spreading. This is essentially equivalent to reducing the transistor threshold voltage V_{th} *roll-off* because the drain is able to partially control the channel [8].
3. *Velocity saturation* caused by the strong electrical field in the channel that leads to increase the level of interaction with the lattice encouraging scattering [8].

Another relevant aspect to scrutinize is the tunneling current evolution as scaling increases. Basically by reducing the channel size two tunneling effects might contribute in I_{off} degradation. *Band to Band Tunneling (BTBT)* occurs when the potential barriers between the drain and the gate are thin enough that the carriers

might be able to travel from the *valence band (V_B)* to the *conduction band (C_B)* and vice versa; while the second effect derives directly from the t_{ox} reduction; as the channel was shrunk, a remarkable gate quantum mechanical tunneling contribution can occur. In addition as the gate length was shrunk down to decananometer scale (gate length < 20 nm) source to drain tunneling might become a substantial factor.

Overall the major outcome, coming from the SCE and tunneling effects, is the high leakage current in the SS region. As a matter of the fact, increasing the scaling the $P_{PASSIVE}$, SS and the gate overdrive worsen dramatically [25, 26] then the only way to potentially reduce the negative effects is the use of novel semiconductor with higher mobility, new high-k materials and the formation of new multigate device architectures with higher electrostatic control [13, 17, 27].

Moreover, as MOS technology scales further, processing aspects also have to be taken into account because the reliability drastically impacts on the device accuracy [28]. Then the processing variations can be categorized in two classes [29]; the first one, historically regrouped patterning effects [30], line edge and line width roughness [31], variations in gate dielectric (thickness variations [32], defects and traps [33]). While the second one includes variations that have emerged according to the scaling pace; such as the random dopant fluctuations [34, 35] or the innovative doping technologies as the *molecular monolayer doping (*MLD*)* [36] through the optimization of the annealing recipes [37] or finally variations associated with the strain in the material [38].

Therefore to push beyond the nanometer nodes it is essential to face all the challenges that have arisen over the years to continue the astonishing electronics progress toward atomistic scale.

1.1.2 New device architecture

The necessity of developing a new disruptive device architecture able to replace the planar configuration came from the bottlenecks that arose during the continuous transistor scaling. Fig. 1.4 shows the transistor evolution according to the technology node. Basically, the transformation process can be grouped in three main areas according to the technology booster carried out to follow the scaling paradigm (classical scaling, stress and high-k introduction and finally new device architectures).

The first refinement for the planar structure was the introduction of the *Silicon*

on insulator (SOI) substrate. It is well established that SOI improved the SCE control compared with traditional bulk transistor architecture because it enabled smaller source/drain to substrate capacitance, faster switching and the ability to run at lower voltages [17]. However the necessity to fabricate very thin semiconductor layers generates process variability and physical problems such as thickness targeting and quantum confinement.

As the device reduction approached the 130 nm technological node the necessity to improve the electrical behaviour due to ever worsening SCE control lead to the debut of the strain concept to boost the channel mobility (tensile for n-type and compressive for p-type). The strain technique, extensively studied in literature [39-41], relies on the equilibrium lattice constant alteration resulting in superior electrical properties. In addition, the continuous device reduction caused severe current limitations; then, both the necessity to decrease the gate leakage and to increase the electrical performance motivated to use high-k material in the 45 nm technology node [42].

Although the application of strain and high-k material did not result in a substantial MOS configuration diversity, it established the emergence of new concepts that motivated the research of new materials and ingenious device architectures. According to the idea to restrict the SCE, the multigate structure has been used for the first time in the 22 nm technology node. The definitive switch from new device architecture enabled the industry to address the SCE and go beyond what was possible with the conventional miniaturization process.[17]

Though new processing challenges emerged, with the switch to new device architectures (fabrication of high aspect ratio structures) the integration of multigate structures enabled advantages both from the electrical point of view, achieving higher performance, that from the topology, decreasing the device area [43-45]. The extraordinary electrostatic advantage over the conventional planar structure achieved led towards a reduction of SCE due to the development of device with more than two gates such as TriGate architectures [46, 47] that provide higher performance considering the similar processing challenges.

The ultimate CMOS device is likely to be a nanowire channel with surrounded gate. The *gate all around (GAA)*- FET geometry was designed with the aim of reducing SCE, however scaling has a massive effect on electrical performance.

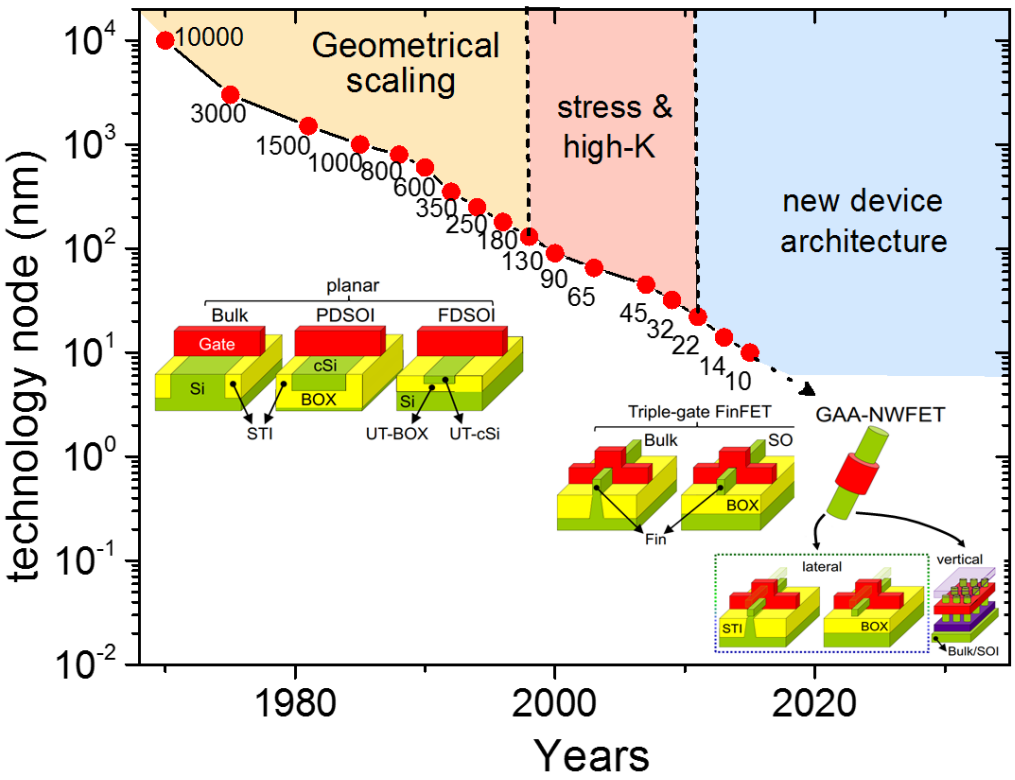


Figure 1.4: *Electronic device evolution as a function of the technology node, and device architecture used to enable CMOS scaling starting from the planar device up to the extremely scaled GAA-NWFET which can be implemented both in lateral and in vertical orientation (adapted from* [48] *and* [49]).

The last exotic architecture predicted sees the development of vertical structure (skyscraper approach) interconnected through specific vias to go beyond the physical restriction (shorter wires with lower latency problems) and increase the device density [50].

Therefore in this context, the need to research and study new materials to improve the performance of these new fascinating architectures, seems to be a key point to address the new challenges proposed by the device scaling.

1.1.3 New semiconductor materials

Over the last few decades new concepts as the material strain [51, 52], high-k adoption [10, 53] and new device configuration [54-57] (FinFET, GAA, *Junctionless transistor (JNT)*) have been extensively researched to continue the scaling process. The most intriguing challenge to improve the electrical device performance and go beyond physical limits consist of emerging semiconductor materials [7].

Actually to enhance the device performance there is the argument to replace Si with higher carrier mobility semiconductors such as III-V compounds [58], Ge and

its alloy [59, 60], Graphene [61], and *transition metal dichalcogenides* (TMDs) [62]. Table 1.1 details all the major semiconductor materials investigated to date. Among all the materials inspected, III-V semiconductors provide the higher electron mobility exploitable for n-MOS while Ge has superior hole mobility usable for p-MOS. In addition, Group IV semiconductors, such as Ge and its alloys, seems to be the most favourable candidates to replace Si in the future CMOS devices due to the extreme process compatibility. Beyond the compatibility with Si, Ge looks to be interesting opportunity because it exhibits several benefits as higher carrier mobility (electron (2×), hole (4×)), lower lattice constant mismatch with Si substrate and the extreme compatibility with Si processing.

Although the several advantages offered by Ge and its application as a channel booster, the semiconductor is still under research. Recent investigations on $Ge_{1-x}Sn_x$ gained a lot of interest due to its distinctiveness. Semiconducting GeSn alloys offer higher carrier mobility, high compatibility with the already well-established Si processing and last but not least the possibility to tune the B_g as a function of the Sn content [63, 64]. Nevertheless, even considering the remarkable properties of $Ge_{1-x}Sn_x$ alloy and the unequivocal straightforward integration with the well-established Si platform, all the steps needed to fabricate $Ge_{1-x}Sn_x$ circuitry need to be further optimized. Nonetheless, the introduction of alternative materials into FET architectures is fraught with several difficulties such as the fabrication of high quality substrates without defects, the lattice mismatch with the substrate, the processing and fabrication challenge due to the possible contamination; therefore it is essential to re-adapt the fabrication line of the well-established Si process.

	Group IV		Group III-V			
Semiconductors	Si	Ge	GaAs	InP	InAs	InSb
Electron mobility (cm^2/Vs)	1600	3900	9200	5400	40000	77000
Hole mobility (cm^2/Vs)	430	1900	400	200	500	850
Bandgap (eV)	1.12	0.66	1.42	1.34	0.36	0.14
Electron effective mass ($/m_0$)	m_t:0.19 m_l:0.91	m_t:0.082 m_l:1.46	0.067	0.08	0.026	0.013
Hole effective mass($/m_0$)	m_{HH}:0.49 m_{LH}:0.16	m_{HH}:0.28 m_{LH}:0.04	m_{HH}:0.45 m_{LH}:0.08	m_{HH}:0.45 m_{LH}:0.12	m_{HH}:0.57 m_{LH}:0.35	m_{HH}:0.44 m_{LH}:0.01

Table 1.1: *Semiconductor material properties categorized as a function of group belongs adapted from* [65].

Therefore, despite several challenges have to be addressed to make the transition possible, undoubtedly $Ge_{1-x}Sn_x$ represents a valid alternative to the integration and to the scaling of both optoelectronics and logic device in one chip.

1.2 $Ge_{1-x}Sn_x$ alloy challenge and opportunities

Over the years the continual evolution of *ICT* lead to an enhancement of networked devices and data traffic in modern society [66]. Nowadays electronics apparatus are everywhere and they are part of our daily routine. Nevertheless, the conventional CMOS transistor miniaturization approach has arrived at the point where dramatic power consumption triggers materials and device architecture innovations.

Intriguing alternatives to settle the miniaturization problem includes the application of massless photons instead of electrons for the data transfer, or the usage of new semiconductors material that enables both higher speed and less power consumption devices. Therefore, for the scientific community, the ultimate insight to reduce the power consumption might be represented by the adoption of one semiconductor material able to integrate both electronic and photonic devices.

According to outstanding manuscripts by Cohen and Sau [67] and other fundamental works [68-71], the $Ge_{1-x}Sn_x$ alloy platform exhibits higher mobility channel and direct B_g nature. Hence the material characteristics turn in set the route for MOSFET performance enhancement by merging photonics with Si-CMOS technology.

Figure 1.5 shows the increasing interest in the material according to data found on [72]; Fig 1.5.(a) reports the popularity increase in the last 20 years while Fig.1.5.(b) outlines the relative area of interest.

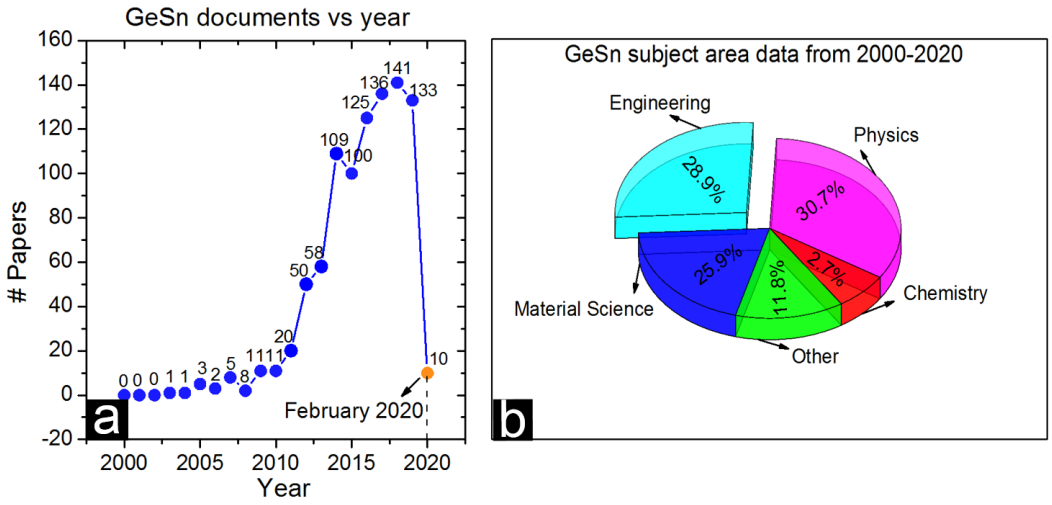


Figure 1.5: *(a). GeSn manuscript evolution in scientific community with its relative areas of interest (b). Data extracted from* [72].

Although the material represents a valid alternative to Silicon, the implementation route is still full of obstacles because many processing aspects need to be addressed. Hence to have a comprehensive vision about $Ge_{1-x}Sn_x$ a literature review on three key points listed below have been made:

(1) $Ge_{1-x}Sn_x$ band structure.

(2) Thin film formation and growth challenges.

(3) Transistor and optoelectronic applications.

The three milestones chronologically represent the most important advances for the material obtained in research. The coming sections detail, as far as our knowledge in literature, challenges tackled and the future perspectives.

1.2.1 Theoretical perspective of $Ge_{1-x}Sn_x$ Band structure

$Ge_{1-x}Sn_x$ alloy investigation started more than three decades ago with the aim to improve Ge device electrical performance. The first studies [73, 74] predicted large electron and hole mobility and the B_g modification considering a very large Sn atomic percentage (at. %) window (26%<Sn<74%). Then, for long time, the transition point between a direct B_g and indirect B_g material was not determined experimentally due to the fabrication process challenges. Nonetheless, according to more elaborate simulation models to calculate the band structure, a remarkable reduction in the Sn composition has been proposed attracting the interest of the scientific community.

Basically Sn is an element belonging to group IV of the periodic table and in nature it exists in two allotropic forms. α-Sn, also known as grey tin, with diamond

cubic lattice structure and β-Sn, known as white tin, which has body centred lattice structure. Then the vision to alter the Ge band structure was born from the fact that Ge shows an indirect B_g of 0.66 eV while α-Sn has a negative direct B_g of -0.41eV[75]; therefore merging the two materials in an alloy was expected to create the indirect to direct bandgap transition.

Figure 1.6 shows the band structure of Si, Ge and α-Sn. Essentially Ge is an indirect semiconductor with its lowest conduction band at the L point while α-Sn is a semi-metal with direct and negative B_g. Then mixing the two materials it is possible tune the B_g as a function of the Sn content because the Γ- valley is going to decrease faster than the L-valley, transforming the material into a direct semiconductor.

In addition, due to the large lattice mismatch between the materials, many theoretical works also include the strain influence in the calculations showing how this effect might influence electrical and optical performance. Gupta et al. [69] demonstrated that compressive strain, obtained by alloying Ge and Sn, lead to a remarkable shift of the direct B_g transition towards higher Sn content. Then the stronger the compressive strain the higher Sn content is needed to the onset of direct gap, as experimentally demonstrated in [76].

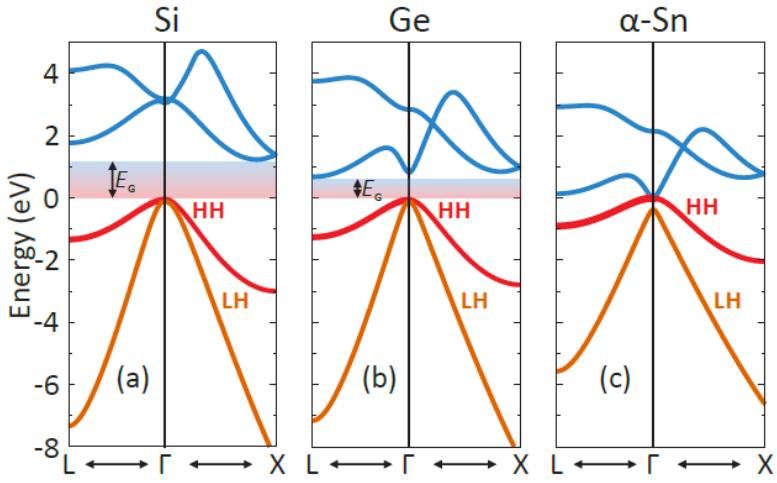


Figure 1.6: *(a-c) Band structure of Si, Ge and α-Sn reprinted from [77]. Whereas Si and Ge shows indirect B_g, α-Sn exhibits a negative and direct gap.*

Historically, the Sn content required to obtain the direct B_g drastically reduced due to the different strategies used to extract the data. In 1987 Jenkins et al. [78] predicted using the *virtual crystal approximation (VCA)* the direct B_g onset with > 20% Sn content; after that, in 2007, Moontragoon et al. [77] exploiting the atomistic

methodology (super cell mixing) to foresee the direct indirect to direct transition with 17% of Sn. Subsequently in 2008 Yin et al. [79] used *density functional theory (DFT)* to predict the transition at 6.3% of Sn.

Although most of the early theoretical reports return quite a wide Sn range to achieve the B_g transition; recent experimental studies [80, 81], based on photoluminescence investigations, suggest the onset of a direct gap around 7-8% of Sn. Once the Sn window has been defined atomistic analysis to explore and predict the band mixing effects influence were made [82, 83]. Recent works show the prominent effects of band mixing for $Ge_{1-x}Sn_x$ alloy with Sn content lower than 10% due to the small Ge B_g and the hybridized mixture of L and Γ states.

As the material knowledge evolves, $Ge_{1-x}Sn_x$ turns into a reality for future electric and photons devices, therefore it becomes essential take into account secondary effects as the band mixing or the Sn atom position within the lattice, to understand and predict electrical and optical features.

1.2.2 Growth and challenges of $Ge_{1-x}Sn_x$ material

$Ge_{1-x}Sn_x$ growth established new perspectives in the semiconductor sector and the material knowledge has been improved over the year. From the first reported growth of microcrystalline $Ge_{1-x}Sn_x$ [84] a lot of challenges have been addressed. Essentially two reasons hampered and delayed the material growth; (1) the low solid solubility of Sn into Ge (2) the high compressive strain.

According to Olesinki et al [85] the maximum solid solubility of Sn in Ge is 1.1% at 400 °C; in addition it tends to degrade as the temperature reduces expecting it to be 0.52% at room temperature. Therefore basing on theoretical and experimental previsions, listed above in the previous paragraph, the Sn content necessary to obtain the direct transition was bigger compared to the equilibrium limit. Then to obtain higher Sn integration, optimized non-equilibrium and low temperature techniques have been developed.

Secondly, the $Ge_{1-x}Sn_x$ alloy has to be grown on Si or Ge substrate that both present higher lattice mismatch. Therefore the high difference among the materials lattice constant leads to large amounts of compressive strain and in some cases, to the formation of defects, such as threading dislocations, in the lattice due to partial relaxation [86]. Therefore to tackle the two aforementioned issues several techniques with different substrates, Ge [87] and $In_yGa_{1-y}P$ [88] have been investigated.

The growth of thin films has been reported using various fabrication methodologies such as, the *molecular beam epitaxy (MBE)* [84, 89, 90] mainly exploited up to the year 2000 due to the lack of Sn precursors to shift toward the *chemical vapour deposition (CVD)* [91-94]. $Ge_{1-x}Sn_x$ layers grown by CVD showed remarkable results [95] thanks to the precursor improvement made by Vincent et al. [96] which details the higher stability of $SnCl_4$ compared to SnH_4.

The ultimate revolutionary methodology used to obtain $Ge_{1-x}Sn_x$ layers involved the combination of cryogenic ion implantation and *pulsed laser melting* (PLM) annealing [97]. The fabrication methodology used ion implantation to incorporate Sn atoms into the Ge followed by a non-equilibrium regrowth process such as PLM. Due to the quick annealing time all the laser energy is absorbed only from the surface while the entire substrate is still at room temperature promoting the solid epitaxial regrowth. Therefore during the re-solidification process the melting surface tends to form $Ge_{1-x}Sn_x$ alloy using the underlying crystalline substrate.[98, 99]

Furthermore recently $Ge_{1-x}Sn_x$ nanowire growths, though *vapour-liquid-solid (VLS)* processes, have been investigated showing interesting results [100-102]. Nevertheless, it is noteworthy that the research in this field is still immature due to several problems such as the process variability, the NWs size and Sn dispersion control. Therefore further study is needed to address the challenges, and to extend the knowledge in order to arrange $Ge_{1-x}Sn_x$ NWs platforms for future sensors, electrical or optical devices.

1.2.3 Field effect transistor and optoelectronic applications

Considering both the exponential growth of the communication data and the increased devices velocity, the future trends expect to see an increasing integration of optoelectronic and electronic circuitries. Then, $Ge_{1-x}Sn_x$ might represent an interesting solution due to the possibility to tune the $B_{g.}$.To prove the higher electrical performance of $Ge_{1-x}Sn_x$ compared to Ge, the first FETs developed were planar even if also a multitude of structure such as FinFET and GAA-FET have been manufactured. Although the remarkable properties of $Ge_{1-x}Sn_x$ alloys and the unequivocal straightforward integration with the well-established Si platform, all the steps needed to fabricate $Ge_{1-x}Sn_x$ circuitry need to be adapted and specifically developed, such as lithography, etching, cleaning, doping, etc.

The first $Ge_{1-x}Sn_x$ p-MOSFFET was introduced in 2011 [63, 103] outlining the material supremacy compared with Ge counterpart (hole mobility 60% higher compared with the Ge counterpart). After the outstanding innovations, several investigations showed the ability to fabricate $Ge_{1-x}Sn_x$ p-MOSFET with higher performances [104-107]. Gong et al. [108] studied the hole mobility dependencies as a function of the wafer orientation showing a mobility enhancement of 18% using a Ge (111) wafer orientation compared with Ge (001). Guo et al [109] examined the surface passivation technology to reduce Sn segregation on the surface to increase the material mobility. As a regard the n-MOSFET several works have been developed due to the ability to introduce the tensile strain; the strain benefit aimed to improve the electron mobility and n-FET platform have been studied to date [110-112]. Along with the typical planar configuration also tunneling FETs (TFETs) and Negative capacitance FETs (NC-FETs) have been extensively explored to produce steep SS.

Zhou et al. [113-115] investigated the negative differential resistance using the $HfZrO_x$ on $Ge_{1-x}Sn_x$ showing the ability to go beyond the theoretical limit of 60 mV/dec. Concerning Tunnel FET studies Liu et al. [116] designed a heterojunction n-channel tunneling FET with an I_{on} enhancement more than 300% ($Ge_{0.92}Sn_{0.08}/Ge_{0.94}Sn_{0.06}$) compared to $Ge_{0.92}Sn_{0.08}$; while Yang et al. [117] simulated and developed a 4 µm channel length TFET device with high I_{on} within the voltage range of ±1V.

Furthermore in parallel, new device architectures such as FinFET and GAA architectures were developed due to wide and comprehensive studies on processing aspects, such as the etching [118-120], doping [121] and metal contact formation [122, 123]. $Ge_{1-x}Sn_x$ FinFETs with fin in decananometer scale were fabricated by Wang et al. [124] and Lei at al. [125] showing respectively a SS of 93 mV/dec and 79 mV/dec. Recently GAA structures were developed by Y-S-Huang et al. [126, 127] that report the formation of 2 and 3 stacked $Ge_{1-x}Sn_x$ channel with higher I_{on} (2000 µA/µm) achieved for channel length (60 nm) and Gong et al. [128] that describes the highest peak transconductance of 573 µS/µm obtained in $Ge_{1-x}Sn_x$ GAA.

With regard optoelectronic devices the ability to tune the band gap as a function of Sn at.% represent an additional point for the alloy. $Ge_{1-x}Sn_x$ thin films are

expected to have greater photoconductivity compared with Ge, so they become more attractive for the development of photodetectors [129-133] photodiodes [134, 135]. Nevertheless the increasing interest lead to the development of lasing devices [136] exploiting the direct gap features. Wirths et al. developed a Fabry–Perot cavity to explore the optical pumping [76]. Von den Driesch et al. investigated lasing capability of different heterostructures and quantum wells with varying geometries [137]. Stange et al. [138] tried to improve the lasing temperature analysing the features of $Ge_{1-x}Sn_x$ microdisks develop on a Ge buffered layer. The microdisk structure lead to increase the optical properties due to the large refractive index contrast between the air and the material and it produced the possibility to laser up to 130 K. In addition, the ability to develop nanostructures lead to the development and investigation of quantum structures usable both for the nanophotonics and nanoelectronics future applications [139, 140].

Therefore the tunable B_g, combined with the higher carrier mobility, good optical response and realisable process integration, provide several opportunities for $Ge_{1-x}Sn_x$ in future devices.

1.3 Thesis structure

The dissertation explores several challenges about $Ge_{1-x}Sn_x$ with the aim to outline and benchmark the alloy capabilities as a novel and useful semiconductor material. In the last years the incredible advances on $Ge_{1-x}Sn_x$ research drastically enhance the possibilities of the material use; therefore the thesis has the intention to represent the contribution carried out for the advancement of $Ge_{1-x}Sn_x$ in future applications.

In Chapter 1 a literature review on MOSFET scaling and on $Ge_{1-x}Sn_x$ has been outlined to introduce the reader to the challenge and the state-of-the-art present in literature so far.

Chapter 2 reports TCAD analysis using continuum-based device modelling. Since GeSn was not available on the software the alloy has been firstly characterized through the extraction of physical parameters such as the B_g and electron and hole mass and subsequently the values obtained have been used to create a parameter library further used to simulate double gate FET devices. The results have been tuned according to experimental results and the final parameter library developed in this work also take into account tunneling and quantization effects.

Chapter 3 details the investigation of the electrical contact on $Ge_{1-x}Sn_x$ with the aim to improve the access resistance of the material through the formation of stanogermanide layers. Two different experiments, respectively using rapid thermal annealing and laser thermal annealing, have been carried out to understand and point out the best metal candidate both morphologically and electrically for future $Ge_{1-x}Sn_x$ devices.

Chapter 4 explores the doping challenges for the alloy. $Ge_{1-x}Sn_x$ is a metastable material that can withstand only an extremely low thermal budget. Then the need to create shallow doped regions lead to the investigation of several doping methodologies to find the most suitable and reliable technique. Different doping methodologies, ion implantation and layer deposition, have been extensively analysed during the internship made at Applied Materials in MA, USA.

Chapter 5 is a comprehensive analysis on the electrical performance of $Ge_{1-x}Sn_x$ nanowire devices, with nanowires grown through a VLS process. NWs with 3 different Sn content (3, 6, and 9%) were processed with a bottom up approach, electrically characterized and benchmarked with other FET works found in literature in order to extract trends for GeSn NWs.

Chapter 6 describes the formation of a GAA device obtained through a top down approach. The device has been developed through an accurate control of the processing steps and subsequently it was electrically characterized and benchmarked versus literature.

Finally, Chapter 7 details the thesis conclusion and the future outlooks for $Ge_{1-x}Sn_x$.

2|TCAD analysis and simulation on $Ge_{1-x}Sn_x$ semiconductor devices

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Conference presentation associated with this Chapter:

(1) **E. Galluccio**, J. Holmes, R. Duffy., *Modelling Ge(1-x)Sn(x) junctionless nanowire transistors through the study of the bandgap and effective mass in the alloy*. E-MRS fall meeting, September 18-21, 2017, Symposium L, Warsaw, Poland.

2 |TCAD analysis and simulation on $Ge_{1-x}Sn_x$ semiconductor devices

2.1 Introduction

In the last years, *Technology Computer-Aided Design (TCAD)* software has become essential for semiconductor companies and research due to the extreme difficulties in developing sub-nanometer electrical device technologies. TCAD plays a key role in the new technologies evolution because it represents the interface between the research and the industry. In addition with the approach to new semiconductor materials, the simulation concept becomes indispensable to predict the possible electrical performance considering the even more complex physics.

In this chapter fundamental properties of the $Ge_{1-x}Sn_x$ semiconductor material have been extracted using Synopsys TCAD software. Firstly $Ge_{1-x}Sn_x$ physical properties, such as B_g and effective carrier mass, have been calculated to create a tailored model. Subsequently the double gate *JNT* as a function of Sn incorporation, channel size and doping have been analysed. Finally, according on experimental results obtained, models have been calibrated and the study was repeated to report the electrical behaviour variations.

It is important to note, that at the beginning of this PhD GeSn was not an available material in the Synopsys device software, and thus had to be defined entirely from scratch.

2.2 TCAD Potential

According to Moore's law, electrical devices have become even smaller and integrated circuit design had to face several issues related to scaling. Therefore the simulations were used as a bridge to link the broad range of underlying material physics and the electrical behaviour expected.

Essentially the main concept of TCAD is to use simulations, based on fundamental physics, to fully understand and predict both electrical features and processing steps for new device configurations. Nevertheless, over time, TCAD had to improve and to address the new challenges that arose, because the transistor characteristics had to be tailored according to new predictions and paradigms. Indeed, as the technology became more complex the first device modelling software as SUPREM [141], PISCES [142] were replaced by more powerful programs such as SILVACO [143] and SYNOPSYS[144].

The actual commercial software are composed of several tools in order to simulate, characterize, and predict the electrical behaviour of devices according to the underlying fundamental physics effects [145]. Based on ITRS predictions, TCAD can reduce more than 40% of the fabrication costs as well as speeding up the development process. Therefore the semiconductor industry and research both rely increasingly more on this approach both for the physical/electronic analysis of the new semiconductor materials.

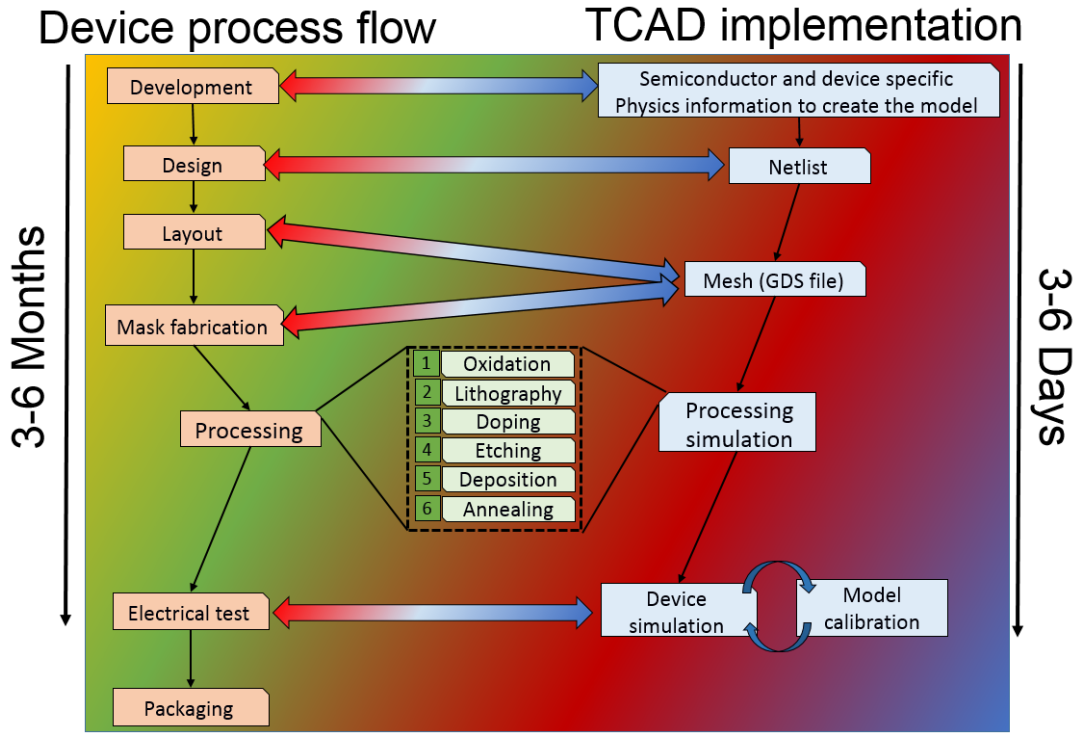


Figure 2.1: *Schematic of the main processing steps in the semiconductor manufacturing versus the TCAD implementation process flow and representative expected timeline in both.*

Figure 2.1 summarizes and compares the process chain in semiconductor manufacturing against the TCAD implementation. The plot points out the extreme time advantage in using the simulation approach compared with the fabrication process. According to Figure 2.1, TCAD simulations consists of two main branches: the process and the device simulations. In process simulation material/device is discretised and represented as a finite element structure. Then the processing steps are simulated taking into account two important parameters, namely the physical equations that govern the process, and the mesh developed to predict the possible behaviour. While device simulations can be thought as a virtual measurement of electrical behaviour in order to obtain prediction of any semiconductor device.

Similarly as in the previous case, the device is represented as a meshed finite-element structure where each node has specific properties associated with it. Therefore the device simulator solves several equations, in accordance with the models activated, in order to extract the electrical features.

In this work Synopsys commercial software and its tools have been comprehensively used to characterize the $Ge_{1-x}Sn_x$ alloy, both physically and electrically.

2.3 MATERIAL BACKGROUND

Recently the scientific community interest is increased exponentially towards the research of new semiconductor materials for electrical and optoelectronic purposes. In this context the $Ge_{1-x}Sn_x$ alloy, due to its peculiarity as 1) the ability to tune the B_g according to the Sn content, 2) the higher mobility compared with other group IV material and 3) the easier integration with Si processing, attracts the attention of several research groups. Basically in nature Sn is present in two allotropic forms: grey/α-Sn, which has a diamond cubic lattice structure as Ge or Si, and white/β-Sn, characterised by a tetragonal lattice structure. α-Sn is a semi-metal with a direct but negative B_g (-0.4 eV) [75] while Ge is an indirect semiconductor (0.66 eV) with lowest conduction band minima at L point [146]. Therefore alloying Sn with Ge lead to a B_g decrease that allows to obtain the indirect to direct semiconductor transition as a function of the Sn content in the alloy.

The possibility to obtain a direct B_g material with enhanced mobility was first proposed by Goodman et al.[73] in 1982 but at that time it was still not clear if it was possible to synthetize the material; in addition the knowledge that $Ge_{1-x}Sn_x$ alloys exhibit a direct B_g was predicted also before the experimental data [74]. During the past few decades several works on $Ge_{1-x}Sn_x$ growth and physical material characterisation took place; the first report on crystalline $Ge_{1-x}Sn_x$ has been published by S. Shah et al in 1987.[90] Starting from this point, which represents a sort of milestone, an extensive and detailed study has been made on the material exhibiting the ability to grow $Ge_{1-x}Sn_x$ thin films using several fabrication techniques as the *CVD* [91, 93, 94], *MBE* [84, 89], and *physical vapour deposition(PVD)* [96, 147, 148]. Nevertheless remarkable challenges in epitaxial growth such as the low solid solubility of Sn in Ge (<1%) or the Sn tendency to diffuse, segregate and precipitate during the growth process and the thermal

treatments [131] have hampered the development of the alloy.

The second critical point to overcome was the strain due to the large lattice mismatch between Ge (5.658Å) and α-Sn (6.493Å); in the case of high Sn incorporation, the lattice mismatch leads to high compressive strain that shifts the change from indirect to direct semiconductor [138, 149]. Since it has also been demonstrated that the higher the compressive strain, the higher Sn content is necessary to reach the indirect to direct change [69], two approaches to counteract the strain limitation have been introduced: 1) The inclusion of a Ge buffer layer as *virtual substrate* (VS) in order to decrease the strain [76] and 2) thickness increment that leads to a gradual strain reduction [150]. Anyhow to obtain a thin film with high Sn incorporation, a low temperature and non-equilibrium technique has to be used.

Parallel to the growth process optimisation, in recent times comprehensive studies on the $Ge_{1-x}Sn_x$ band structure, including effective mass calculations, have been made to electrically characterize the alloy. One interesting and challenging aspect was the definition of the point at which the material changes from indirect to direct semiconductor.

Initially the prediction coming from the linear interpolation between the L and Γ valley of $Ge_{1-x}Sn_x$ set the transition over 20% Sn content [69]. Nevertheless with the technological improvement more complicated and accurate models have been developed to extract the precise Sn % required to obtain the indirect-direct change. For example tight binding calculations predict the change using a Sn content >20% [78], while first principle band structure calculations point out the transition at much lower Sn content (6%) [79].

Moreover experimental studies [80] suggest the onset of direct gap roughly around 7-8%. Fig. 2.2 reports the state of the art literature [68, 77-81, 151-154]; highlighting the point at which the transition from indirect to direct semiconductor has been predicted; while Figure 2.2.b shows the procedure used to extract both the physical parameters needed to develop the material library and device electrical simulations. Despite the massive work made, the material system is still in a relatively immature phase then it is difficult to form a single model for commercial TCAD able to predict all the material features. Nonetheless nowadays the commonly accepted value of Sn content to reach the direct B_g is no less than 6.5% and it represents an important breakthrough for the future works.

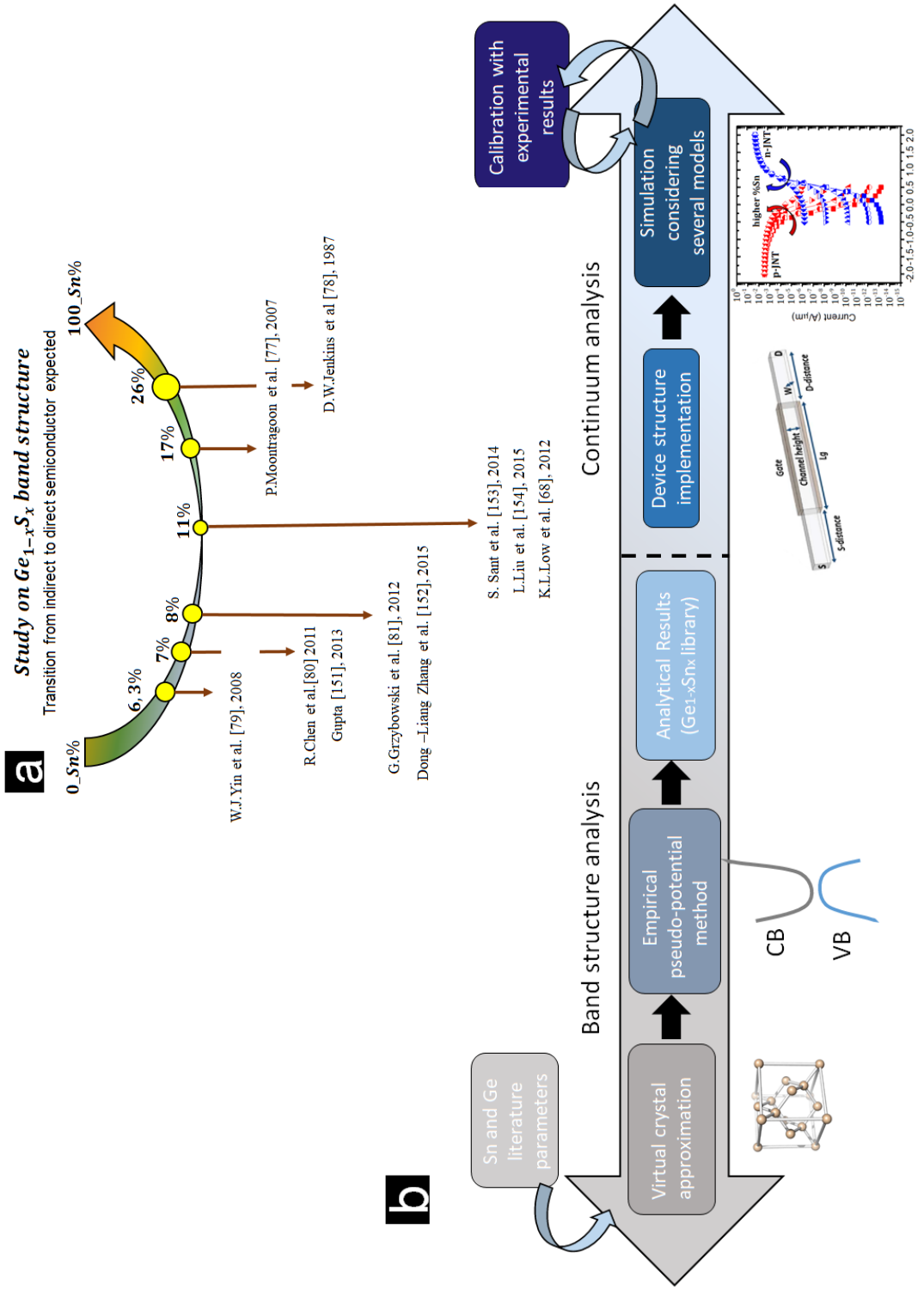


Figure 2.2: (a) *Summary of all the transition points from indirect to direct semiconductor for the $Ge_{1-x}Sn_x$ alloy found in literature;(b)specific steps considered in the modelling activity; from the B_g calibration to the electrical device simulations.*

2.4 $Ge_{1-x}Sn_x$ physical features

Since $Ge_{1-x}Sn_x$ was not available in Synopsys the material has to defined entirely from the scratch then in this section the methodology used to extract material band structure and effective mass using Synopsys software will be briefly explained. Firstly the correct crystal configuration has been identified and subsequently the *virtual crystal approximation* (*VCA)* has been used to represent the atoms within the basic lattice. Afterwards the *empirical pseudo-potential methodology* (*EPM)*, in which effective potential are used to replace the more complicated inner core electrons motion, has been adopted to extract the band structure and finally the derived features have been extracted.

2.4.1 Crystal structure

The study of the $Ge_{1-x}Sn_x$ semiconductor starts with the identification of the crystalline structure to outline the electronic material performance. A crystalline lattice is defined as an infinite and ordered arrangement of atoms described by the Bravais lattice as shown in equation 2.1.

$$R_n = n_1a_1+n_2a_2+n_3a_3 \tag{2.1}$$

Where R_n is a vector, $n_i \in N$ (natural numbers) and a_i is the base that indicates the physical location of the atoms within the structure. α-Sn, as Si and Ge, has a diamond structure with a *face centered cubic (FCC)* crystal lattice and the base is composed by two atoms, respectively placed at $a_o(0,0,0)$ and $a_o(\hat{x}+\hat{y}+\hat{z})/4$; where a_o indicates the lattice constant of the material.

The primitive cell of the FCC structure is shown in Fig.2.3.(a) where the two base atoms are indicated respectively by black and white dots within the blue zone [24]. The respective reciprocal lattice for a FCC structure results in the *Body Centre Cubic (BCC)* configuration represented in Fig. 2.3.(b); while the Wigner-Seitz cell of the reciprocal lattice, referred as the Brillouin zone, is shown in Fig. 2.3.(c). Inside the first Brillouin zone there are symmetrical points and directions indicated with capital letters; nevertheless for the calculations carried out in this work the directions (Λ) (Δ), highlighted in red, will be considered to extract the band structure [155]. Physical features of the $Ge_{1-x}Sn_x$ alloy can be evaluated, either with the VCA, in which the atoms of the crystalline unit cell have identical average composition or by populating individual lattice sites with pure element atoms, proportionally to the

alloy composition (mixed-method atoms). The latter approach is more realistic because it takes into account the disorder effects and the composition fluctuations in the cell [83], nevertheless it becomes computationally very expensive as the super-cell increases in size [77, 156] therefore in this study the VCA methodology has been used to simulate the $Ge_{1-x}Sn_x$ alloy atoms within the lattice structure.

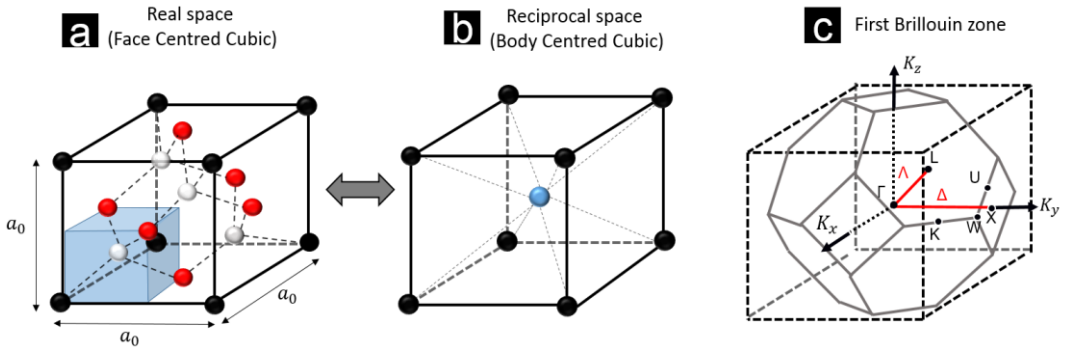


Figure 2.3: *(a) Diamond structure of α-Sn with its primitive cell highlighted in transparency; (b) Body centre cubic configuration in reciprocal space, (c) first Brillouin zone with the most important symmetrical point and directions.*

2.4.2 Empirical pseudo-potential methodology

The band structure calculation is important because it characterizes the material. Indeed, many properties exploited by electronic devices, such as the *valence band* (VB) and *conduction band* (CB) levels, the B_g and the carrier masses derive directly from it. In literature several techniques for calculating the band structure of a semiconductor material, such as $K \cdot p$, the *EPM* or *DFT*, are described and the main difference among them relies on the accuracy required.

In particular, in this work the EPM method was used to extract the $Ge_{1-x}Sn_x$ band diagram since in literature this approach has been already used successfully to extract the electronic band structure of other group IV semiconductor as Si, Ge and $Si_{1-x}Ge_x$ alloys.[157] Essentially EPM needs few parameters to obtain the material band structure and conceptually it is reliable and simple.

In substance the band structure estimation is facilitated because during the calculation of the Schröedinger equations the core states of the electrons, strongly bound to the nucleus, can be omitted by substituting the potential of the crystal with a pseudo-potential that represents the overall effect of the electrons. According to the remarkable Chelikowsky and Cohen work [158], without going into the details of this calculation, the single electron pseudo-potential equation can be summarised by equation 2.2

$$H = -\frac{\hbar^2}{2m_0}\nabla^2 + V_{loc} + V_{nloc} + V_{so} \quad (2.2)$$

Where the first term corresponds to the kinetic energy while V_{loc}, V_{nloc} and V_{so} represent respectively the local, non-local and spin orbit contributions to the equation. The first two terms of Equation 2.2 describe the local crystal variation but to obtain a more comprehensive approximation about the real crystal potential, the third and fourth terms have been introduced. V_{nloc} will capture the angular momentum dependence of the pseudo-potential while V_{so} will take into consideration the spin-orbit iteration.

In this work EPM calculations have been carried out by the Synopsys SBAND tool and the variable parameters are listed and described in Table 2.1; however for a more extensive explanation one should refer to [158, 159] or to the Synopsys manual [160].

Parameter	Unit	Ge[153]	Sn[153]	Description[160]
$V_{loc}\sqrt{3}$	Ry	-0.2378	-0.21	Local form factor $\|\|q\|\|^2 = 3(2\pi/a_0)^2$
$V_{loc}\sqrt{8}$	Ry	0.02852	0.02359	Local form factor $\|\|q\|\|^2 = 8(2\pi/a_0)^2$
$V_{loc}\sqrt{11}$	Ry	0.0469	0.01737	Local form factor $\|\|q\|\|^2 = 11(2\pi/a_0)^2$
a_0	Å	5.658	6.493	Lattice constant
μ	Ry	0.00096	0.00239	Spin-Orbit splitting strength
R_0	Å	0.0	1.0	Nonlocal well radius ($l = 0$)
α_0	Ry	0.0	0.0	Nonlocal well depth ($l = 0$)
β_0	-	0.0	0.365	Energy dependence correction for α_0
R_2	Å	1.2788	1.453	Nonlocal well radius ($l = 2$)
α_2	Ry	0.309	0.71	Nonlocal well depth ($l = 2$)
Non-Local-Well	-	Square	Square	Nonlocal well shape
ζ	-	0.45	0.50	Internal strain parameter
Q^2 cutoff	$(\frac{2\pi}{a_0})^2$	12.44	15.25	Cut-off for local pseudo-potential form actor

Table 2.1. *EPM parameters used and the respective description for the values present in Synopsys SBAND[160].*

The default values present in the software were inherent to Si and Ge therefore a careful research in the literature has been carried out in order to identify the

parameters necessary for the implementation [68, 77, 151, 153, 154, 161]. The values used for the $Ge_{1-x}Sn_x$ B_g extraction were summarized in Table 2.1.

2.4.3 Band structure calculation

In this section the $Ge_{1-x}Sn_x$ band structure and its variation as a function of the Sn content will be introduced. Sentaurus band structure (SBAND) extracts the band diagrams by constructing the crystalline structure through VCA and implementing the calculation via EPM. Each element present in the software is identified by a parameter file, nevertheless α-Sn was not available; therefore, according to the manual [160], a specific file was created from scratch, in this PhD work, in order to complete the analysis. Nevertheless it is mandatory to provide K vectors as input, according to the desired dispersion relation, and then the software provides output of 3 and 4 eigenvalues respectively for VB and for CB. Before extracting the alloy band-structure as a function of Sn percentage, the script developed was first tested and sanity-checked on Ge and α-Sn bulk, using the parameterisation values in [153]. The results achieved are in accordance with previous works reported in literature [77, 162] and are summarised in Table 2.2.

Valley	Unit	Ge[77]	αSn[162]	Ge	αSn
$\Gamma(CB)-\Gamma(VB)$	eV	0.800	-0.475	0.812	- 0.465
$L(CB)-\Gamma(VB)$	eV	0.660	-1.35	0.659	- 1.34

Table 2.2: *Comparison of Ge and α-Sn energy difference between Γ-Γ and L-Γ. Values are expressed always in eV and the data are extracted considering the highest valence band and lowest conduction band for both materials*

Subsequently, the $Ge_{1-x}Sn_x$ dispersion relation was performed. Firstly a new atomic species was defined using the SBAND tool according to the alloy composition and after the lattice constant variation as a function of the Sn percentage was considered by using Equation 2.3. Where a_{Sn} and a_{Ge} are respectively the lattice constants of α-Sn and Ge while xSn represents the Sn content and Θ is the bowing parameter (0.166Å) [163].

$$a_{GeSn}(\mathrm{xSn}) = a_{Sn}xSn + a_{Ge}(1-xSn) + \Theta_{GeSn}xSn(1-xSn) \qquad (2.3)$$

Finally when the crystal structure is created, the EPM calculation has been performed and in this work the transition from indirect to direct semiconductor occurs around 7.0%; a value in good agreement with literature data [151-153].

Figure 2.4 shows $Ge_{1-x}Sn_x$ band structure as a function of Sn content and the aim is to highlight the different nature of the semiconductor material. In all the images Ge band structure is highlighted with solid black line in background and overlapped on it, with red scattered line, $Ge_{0.97}Sn_{0.03}$, $Ge_{0.92}Sn_{0.08}$ and $Ge_{0.80}Sn_{0.20}$ band structure are presented respectively in Figure 2.4.(a), 2.4.(b) and 2.4.(c). Basically from Figure 2.3 is possible to clearly observe the B_g variation as a function of the Sn in the alloy thanks to the delimited area between the VB and the CB highlighted in light grey. Fig. 2.4.(a) shows the $Ge_{1-x}Sn_x$ band structure with CB minima in L valley, then the material is still an indirect semiconductor; while Fig.2.4.(b) shows the transition from indirect to direct semiconductor and finally Fig.2.4.(c) shows the semimetal behaviour.

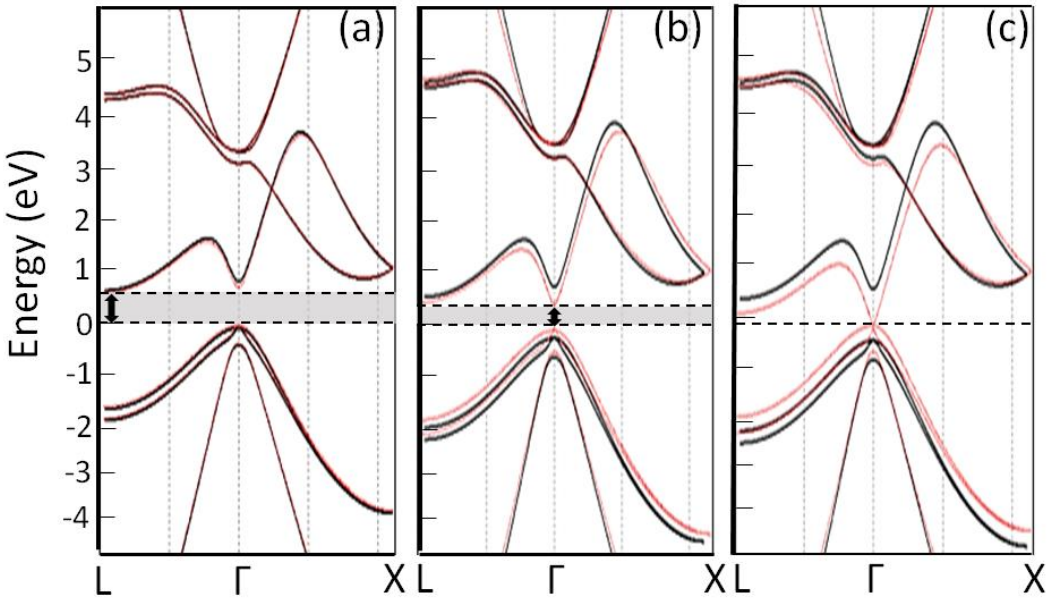


Figure 2.4: *Band structure of $Ge_{1-x}Sn_x$ alloy; with black solid line in background there is the Ge band structure instead with red dot line is highlighted the $Ge_{1-x}Sn_x$ outcomes obtained with different Sn content; (a) 3% Sn, (b) 8% Sn and (c) 20% Sn.*

2.4.4 Mass extraction

Effective mass is an important parameter that has significant effect on the transport properties in a semiconductor material since carrier mobility and valley occupation are dependent on it. Therefore, based on the previous analysis on $Ge_{1-x}Sn_x$ alloy, the effective mass calculation for electrons and holes has been carried out through SBAND according to equation 2.4.

$$m = \hbar^2 * \left(\frac{1}{\delta^2 E / \delta K^2}\right) \tag{2.4}$$

Where ħ is the reduced Planck's constant, E is the energy and K is the wave vector.

With respect to holes, the heavy and light values were extracted in three different directions, respectively <100>, <110> and <111> and the outcomes achieved are in accordance with the trends obtained in previous work [68, 154], in which a more thorough analysis has been developed. Basically the heavy holes values remained constant as the Sn percentage increased, whereas the light hole values decrease with increasing Sn concentration as showed in Figure 2.5 where the data obtained by Synopsys simulation were reported in blue while the literature comparison data ([68, 154]) where reported in black and red.

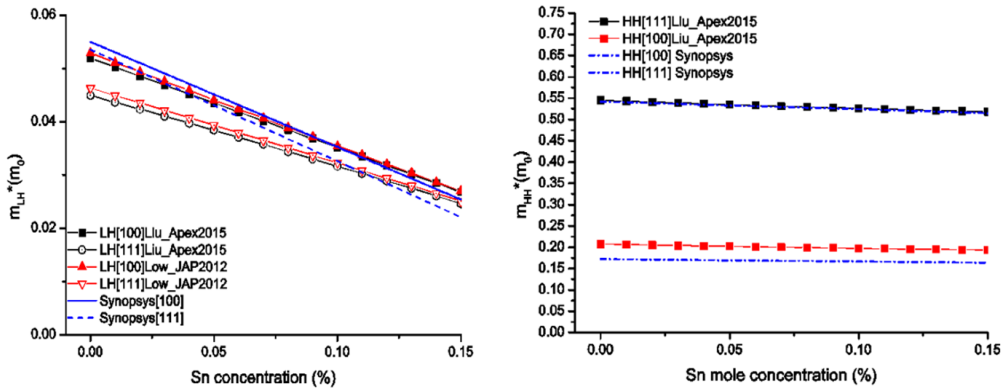


Figure 2.5 *Light and heavy holes mass as a function of the Sn content. Blue lines show the data extracted while black and red depict the comparison literature data*

Subsequently, the electron masses were extracted in L and Γ valleys and the values obtained are summarised in Table 2.3. It is noteworthy that in Γ-point the electron mass decreases as Sn content increases; instead, the transverse and longitudinal mass in the L-point remained roughly the same as the Sn % is varied.

Sn%	$m_{et}^{\Gamma}[m_0]$	$m_{et}^{L}[m_0]$	$m_{el}^{L}[m_0]$	$E_g^L[ev]$	$E_{eg}^{\Gamma}[ev]$
0.00	0.0416	0.0914	1.6745	0.700	0.852
0.01	0.0401	0.0909	1.6769	0.690	0.819
0.03	0.0356	0.0900	1.6823	0.630	0.640
0.05	0.0311	0.0892	1.6875	0.554	0.534
0.07	0.0266	0.0884	1.6926	0.461	0.431
0.09	0.0222	0.0875	1.6976	0.391	0.314
0.11	0.0179	0.0868	1.7024	0.325	0.202
0.13	0.0135	0.0860	1.7070	0.262	0.098
0.15	0.0115	0.0852	1.7116	0.204	0.000

Table 2.3: *Bg and electron mass in Γ and in L valley (longitudinal and transverse).*

Overall a clear decreasing trend for the mass as the Sn content increases was observed, both in Γ and L-point. Equation 2.5 depicts the correlation between the mobility and the mass

$$v_n = \frac{-q\tau_n E}{m_n} = -\mu_n E \tag{2.5}$$

where v is the drift velocity, q is the electron charge, τ_n is the average collision time, E is the electrical field applied and μ_n the electron mobility. The mass reduction highlights the possibility for $Ge_{1-x}Sn_x$ to become a high-mobility material; however the most interesting change occurs after the transition from indirect to direct because there is a wide variation between the mass took into account.

2.5 Device physics of Junctionless transistor (JNT)

Typically all metal-oxide-semiconductor (MOS) transistors are made using two p-n junctions, nevertheless as the future technological trends are projected towards a continuous size reduction, the manufacturing problems become more and more relevant.

The formation of well-confined doped areas has become more difficult due to the extreme sharp control required in the process; resulting in poor short channel effect control and thus deterioration of the MOS electrical performance. The JNT has been proposed as possible solution to overcome the problems related to the shrinkage effects [164, 165].

The JNT basically is multi-gate FET without the usual p-n junctions, and the doping concentration is uniform along the device, ranging typically from 10^{18} and 10^{20} atoms/cm^3. The device is essentially a resistor in which the current flow can be modulated by the gate and it can be tuned off choosing a proper *work function (WF)* [166]. The JNT is turned off by fully depleting the highly doped channel as shown in Figure 2.6.

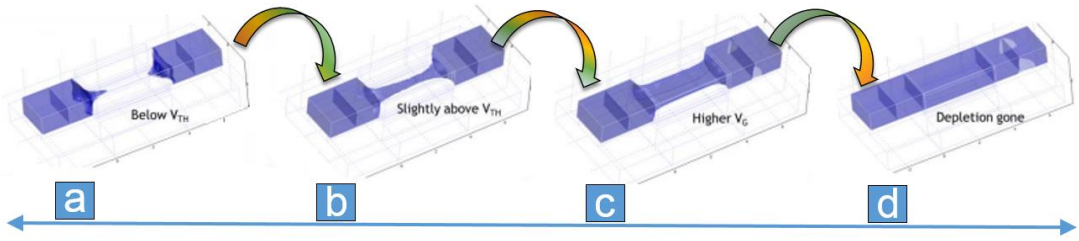


Figure 2.6: *Operating principle of JNT as a function of the gate voltage applied adapted from [165]. The structure is in OFF mode due to the carrier depletion effect*

in the channel (a); applying the gate bias, moving towards (d), the channel is starting to form allowing the current to flow before in the middle of the device (b) up to the point where the depletion region is gone.

The JNT device presents several advantages compared with the common MOSFET configuration; they provide an improved SCE control due to the lack of p-n junctions, as well as a relaxation of the vertical electrical field since the operating principle is completely different compared with "inversion" mode device.

Basically when the JNT is in OFF state and a large electrical field is required to completely deplete the channel region; conversely when it is ON, the field drops to zero allowing the carriers to flow inside the device. Nevertheless the JNT architecture also has drawbacks, as the high V_{th} variation due to the doping and thickness variation that might lead to unacceptable performance, as well as the channel mobility degradation due to the high doping concentration.

Hence considering the limitations and the issue related to the conventional MOSFET, the JNT is a promising configuration to outperform MOSFET electrical performance [167].

2.6 Simulation of $Ge_{1-x}Sn_x$ JNT

Synopsys TCAD software has a modular structure which allows to compare physical features with electrical device structures. Then all the simulations have been carried out using Synopsys SDEVICE tool that is able to link the physical parameters extracted in the previous sections with the electrical device characterisation.

2.6.1 Device structure & model

Since the research aim towards the formation of ever smaller devices with a better electrostatic control all the simulations have been performed by considering a double gate configuration as shown in Figure 2.7.

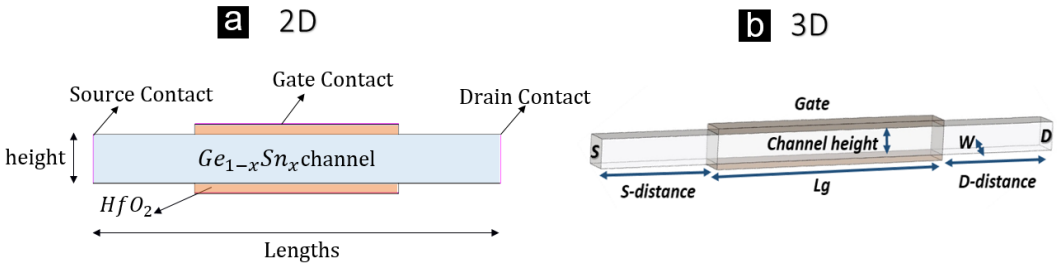


Figure 2.7: *Double gate 2D (a) and 3D (b) structure considered in this work. The structure has been developed through the Synopsys SEDITOR tool and 5 different channel lengths have been considered ranging from 100 nm to 20 nm. Source and*

Drain contacts have been placed always at the extremity of the structure that was developed considering half gate channel length extension in both directions (lengths). In addition the height was set to 10 nm in order to emphasize the JNT effects while the HfO_2 has a thickness of 2 nm in both directions top and bottom.

Basically the structure is formed by $Ge_{1-x}Sn_x$ thin layer uniformly doped (lengths) covered in the central section, in both directions, with 2 nm of HfO_2 (channel length).

The first part of the design was focused on choosing the correct WF and channel size in order to guarantee the proper functionality of the JNT. From literature, it is known that JNT device is less sensitive to SCE compared with typical inversion-mode MOSFETs due to the lack of junctions; moreover the I_{off} is determined solely by the electrostatic control of the gate and not by the leakage current of a reverse biased diode [165]. Nevertheless the bottleneck is the mobility degradation owing to the highly doped channel even if the JNT is able to achieve attractive device behaviour such as steep SS and I_{on}/I_{off} ratio of 10^3 considering both low supply voltage and tiny gate lengths ranging from 100 nm to 20 nm.

Different JNTs, both n and p-type, were simulated to extract the electrical trends. Self-consistent device simulations have been performed using several models as the Fermi-Dirac statistics, the drift-diffusion carrier transport, a doping dependent mobility model, the Auger, Shockley-Read-Hall generation/recombination and impact ionisation models, always taking into account B_g and multivalley variation previously extracted. Moreover since the channel lengths used for the devices developed ranged from 100 to 20 nm, the quantum effects and the tunnelling contributions cannot be neglected.

Then, to obtain a comprehensive analysis two specific models such as *Modified-Local-Density-Approximation (MLDA)* and *BTBT* were used to take into account the device variation for the quantum and the tunnelling effects respectively.

MLDA is a fast and robust quantum mechanical model used to calculate the quantisation effect in 3D structures. It is based on an extension of the more comprehensive work [168]; it uses all the mass and the valley defined in the parameter file to compute the numeric integration of both Fermi-Dirac and Boltzmann statistics in order to take the quantisation effects into account. Basically it mimics the carrier distribution to the gate-oxide/semiconductor interface due the application of gate voltage and the new carrier distribution has been used by the self-consistent Poisson solver.

While a non-local tunnelling model has been used to take into account the BTBT effects, it exploits the equations coming from exhaustive literature works [169, 170]. The model is based on the definition of a special purpose non-local mesh in the area desired and it assumes a trapezoidal barrier shape, includes carrier heating terms, and allows the description of tunnelling between the valence and the conduction band.

The model used requires several band structure quantities such as the effective mass in L and Γ valley, the band gap offset and the degeneracy pre-factor g_c and g_v defined respectively for conduction and valence band. For GeSn the most dominating tunnelling rate derives from the direct contribution and has been already shown in literature [171, 172]; therefore all the parameters used in the model have been extracted from the previous band structure calculation using parabolic approach that return estimated values especially for the CB in Γ valley; moreover the pre-factor is set to 1 for both values according to [161, 173, 174]. However almost all the models developed do not take into account the strain and the sub-band formation that lead to an increase of the effective B_g in the channel and a modification of the DOS in the valley. Indeed the model might underestimate or overestimate the overall conclusions, so given the lack of literature comparison work also the outcomes without the MLDA and the BTBT tunnelling will be presented.

Unless otherwise specified the n and p-JNT were highly doped, respectively with As ($N_D = 10^{19}$ cm^{-3}) for n-JNT or B ($N_A = 10^{19}$ cm^{-3}) for p-JNT and the lengths of the source and drain regions are halved with respect to the channel lengths. Yet, considering the minimum channel length, the two regions are equal to 10 nm each; then the effect of the abnormal drain reduction saturation does not affect the final results [175]. In addition, high-k material HfO_2 is used as the gate dielectric with an equivalent oxide thickness of 2.0 nm and the gate metal electrode WF in all the simulations is set equal to 4.0 eV and 5.0 eV respectively for p and n-type device. Moreover the supply voltage (V_{DD}) was set to 1 V, which is reasonable considering the future application field of the JNT.

2.6.2 Electrical characterisation before mobility calibration

The aim of the investigation in this section is to characterize the $Ge_{1-x}Sn_x$ alloy device behaviour as a function of Sn content. From previous physical analysis it was determined that when exceeding 15% of Sn in the alloy, the material becomes incompatible for typical MOSFET applications due to the B_g reduction (E_g < 100

meV). Thus only the results up to 15% of Sn will be presented and analysed here. All the simulations for n and p-JNT were obtained by considering the 3D structure depicted in Fig.2.7.(b) and as a starting point the mobility values of Ge has been used due to the small amount of Sn in the alloy and the lack of experimental data present in literature. Therefore all the outcomes are qualitative in nature, nevertheless qualitative analysis is still very useful for process and device design, and for aiding future experimental definition.

Fig. 2.8 shows a representative characteristic for device with channel length of 60 nm varying the Sn percentage from 3% up to 15%.

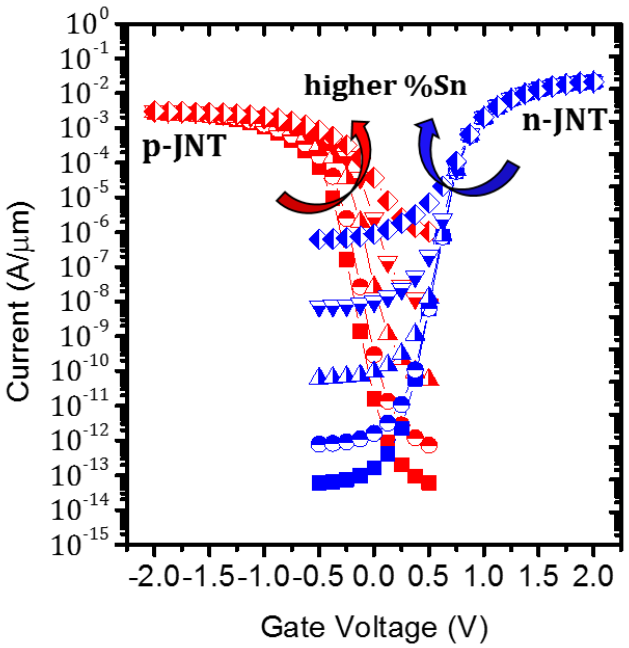


Figure 2.8: *Representative I_d versus V_g characteristic for n and p-JNT as a function of different Sn content (3, 6, 9, 12, 15%) for JNT device with L_{gate}=60nm and channel carrier concentration of 1×10^{19} atoms/cm^3.*

To characterize and compare the different devices, electrical figures of merit SS and I_{on}/I_{off} ratio have been calculated. As a regards of Sn variation, for all the devices simulated, a small variation for SS, I_{off}, and I_{on} currents occurred up to 10% Sn and this behaviour can be explained by the fact that the dominating transport is due to the L valley even when the device becomes a direct B_g [154]. Conversely for Sn concentration above 10% a drastic worsening of electrical performance occurs due to B_g reduction that can raise the leakage current.

While concerning the channel length, it was found that the electrical characteristics degraded rapidly as the gate size decreases. SS values have been extracted considering one decade (10^{-7} - 10^{-6}A/μm) change in drive current.

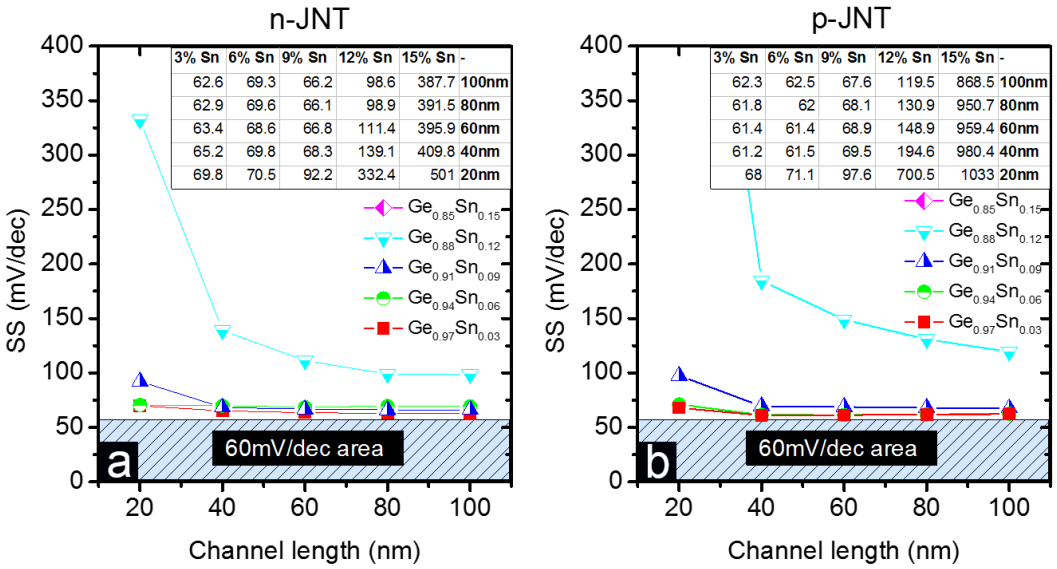


Figure 2.9: *SS for n and p-JNT device, respectively in configuration (a) and (b), as a function of gate length and 5 different Sn percentages. The inset table shows the SS values obtained as a function of different Sn content and the channel lengths used for both configurations.*

Figure 2.9. shows SS data and table respectively for n (2.9.(a)) and p-JNT (2.9.(b)) that were simulated. These data allow us to obtain a clear prediction for the JNT device using $Ge_{1-x}Sn_x$ alloys and to point out the dependence of the electrical characteristics both on device dimension that on Sn content. It is noteworthy that values close to the theoretical limit of 60 mV/dec has been obtained in both configurations only for alloys with Sn content up to 6%; even if device with 9% of Sn still shows results never higher than 100 mV/dec. Moreover, as it is possible to see from Fig. 2.9. the $Ge_{0.85}Sn_{0.15}$ curve has been omitted in both configurations because the values obtained are really huge then not usable for electronic purposes.

After, the current ratio for both device configurations p (Fig. 2.10.(b)) and n-JNT (Fig. 2.10.(a)) are illustrated below; the values have been extracted after normalizing I_{off} to 10^{-9}A and the I_{on} was extracted at $V_{gate}=V_{Ion}=V_{Ioff}+0.5V$.

The I_{on}/I_{off} current ratios for both devices exhibited higher variability as a function of Sn % compared with gate length variation. These trends were expected due to the big B_g modification that leads to higher leakage current in the off state. Nevertheless all the curves with 12% and 15% Sn were not able to reach the standard value suggested by the ITRS then the I_{off} has been set to the lowest current value, while the I_{on} has been taken at the same overdrive voltage range previously used such as $V_{gate}=V_{Ion}=V_{Ioff}+0.5V$.

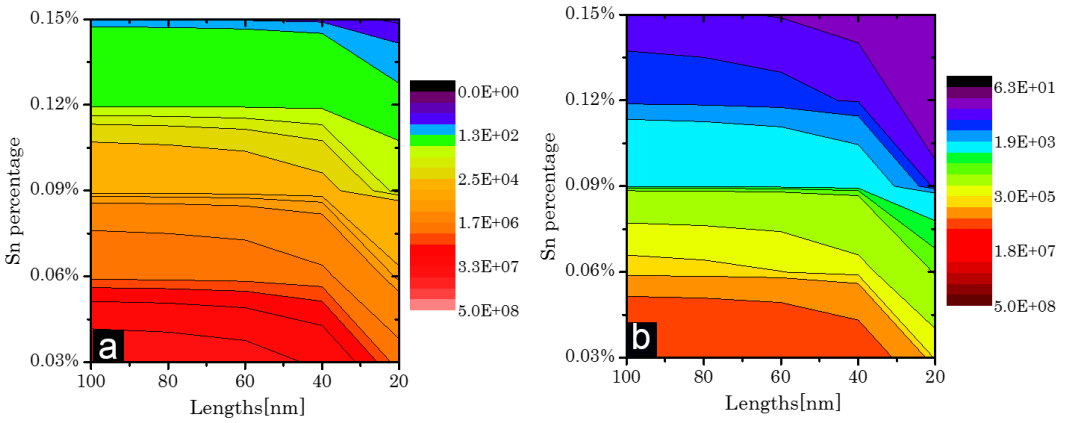


Figure 2.10: *I_{on}/I_{off} ratio respectively for n-JNT (a) and p-JNT (b) as a function of gate length and Sn percentage in the alloy for a device with doping concentration equal to10^{19} cm^{-3}.*

Furthermore, to have a comprehensive work, the analysis has been repeated as a function of doping concentration. The investigation allows us to explore the performance of n and p-JNT, and it was noticed that reducing the doping concentration the current ratio increases even if the spatial charge region increases; however there is always a trade-off among carrier density, mobility and doping concentration to respect, in order to obtain the higher overall performance.

The best performance of SS for both devices, is obtained for Sn concentration up to 9%. Data extracted are quite similar for n and p-type configuration, for the same Sn concentration, even if the best slope is achieved by device with 10^{18} cm^{-3} doping concentration. Above 11% of Sn the I_{off} increases due to the generation/recombination processes in the smaller B_g then the slope decreases. Furthermore electrical performance degradation occurs when the channel length goes below 40 nm; therefore the selection of a specific configuration is important to accurately evaluate the electrical features.

With regards to the quantisation phenomena in the perpendicular direction to the transport, Synopsys provides the MLDA model which is able to predict reliable results [173, 176]. Hence, all the analysis previously shown have been replicated in order to extract the trends also considering the quantum effects. Fig. 2.11 shows the data obtained and as it is possible to see the effect of the quantisation model, in both cases, is to effectively slightly increase the on current and decrease the off current, affecting consequently also the SS and the I_{on}-I_{off} ratio.

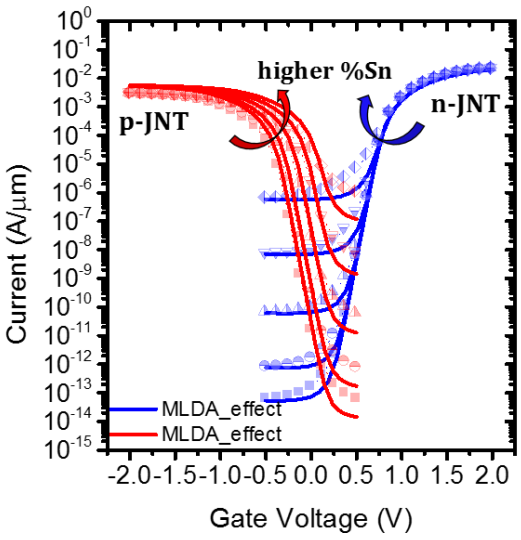


Figure 2.11: *Comparison with and without the quantisation effects; in transparency there are the I_d-V_{gs} characteristics obtained previously for different Sn percentage in the alloy (3, 6, 9, 12, 15%) of device with L_{gate}=60nm and height of channel=10 nm; overlapped on with solid line there are the curves obtained considering the MLDA model.*

3% Sn	***6% Sn***	***9% Sn***	***12% Sn***	***15% Sn***	***nm***	***3% Sn***	***6% Sn***	***9% Sn***	***12% Sn***	***15% Sn***
60.58 *mV/dec*	61.87 *mV/dec*	60.69 *mV/dec*	76.76 *mV/dec*	346.10 *mV/dec*	***100***	60.54 *mV/dec*	60.86 *mV/dec*	60.62 *mV/dec*	75.65 *mV/dec*	455.5 *mV/dec*
60.77 *mV/dec*	62.09 *mV/dec*	60.85 *mV/dec*	80.27 *mV/dec*	334.60 *mV/dec*	***80***	61.03 *mV/dec*	60.89 *mV/dec*	60.87 *mV/dec*	82.99 *mV/dec*	531.99 *mV/dec*
60.72 *mV/dec*	61.15 *mV/dec*	61.42 *mV/dec*	80.38 *mV/dec*	382.72 *mV/dec*	***60***	61.15 *mV/dec*	61.39 *mV/dec*	61.39 *mV/dec*	91.73 *mV/dec*	814.17 *mV/dec*
61.88 *mV/dec*	61.46 *mV/dec*	63.61 *mV/dec*	106.40 *mV/dec*	384.75 *mV/dec*	***40***	61.88 *mV/dec*	63.84 *mV/dec*	63.84 *mV/dec*	111.81 *mV/dec*	979.67 *mV/dec*
67.77 *mV/dec*	67.30 *mV/dec*	73.34 *mV/dec*	305.63 *mV/dec*	389.60 *mV/dec*	***20***	67.43 *mV/dec*	67.43 *mV/dec*	74.78 *mV/dec*	409.41 *mV/dec*	1061.1 *mV/dec*

Table 2.4: *SS values expressed in mV/dec considering the MLDA effect for both p and n-JNT. Values have been reported as a function of gate lengths, highlighted in the central column without colour, and Sn concentrations, reported on top of the table. The red part highlights the results obtained for p-JNT while the blue one highlights the outcomes for the n-JNT.*

Table 2.4 shows the SS value achieved considering the quantisation effects for both p –JNT (red section) and n-JNT (blue section). It is remarkable that the MLDA model has a very minor influence on both configuration with Sn contents up to 9% either on device with channel lengths greater than 60 nm.

Conversely for channel lengths lower than 60 nm and for Sn contents higher than 10% the effect is more emphasised leading to a SS decrease.

Subsequently, always considering the MLDA effect, further analysis to compare the previously presented I_{on}/I_{off} ratio values was performed. With respect to the Sn percentages in the device up to 6% there is an average increase of the 3% of current ratio, while for Sn content higher than 6% a current reduction of 4% has been achieved. Whereas concerning the channel length, devices with gate size less than 40 nm shows an average worsening of 5% due to the confinement effects. So it is possible to state that there are no large significant changes in the SS and I_{on}/I_{off} ratio, as long as the alloy does not become a direct B_g; however, even when the Sn content in the alloy exceeds the 7% the improvements obtained are really small.

Regarding the tunnelling effect there are mainly two contributions, BTBT and Source-Drain Tunnelling. BTBT is expected to be significant compared with the counterpart since the device channel lengths are greater than 15 nm [176]. Therefore the tunnelling effects have been taken into account using the BTBT model present in the Synopsys software. As previously shown in literature [177] tunnelling effects strongly influence the leakage current of the device to the point of drastically reducing the electrical performance. This aspect has been addressed and discussed in many literature works on the tunnel field effect transistors [117]. Nevertheless a tunnelling investigation have been made and as expected increasing the Sn percentage the B_g reduction occurs limiting the possible application of $Ge_{1-x}Sn_x$ in low power applications. Synopsys BTBT model used in combination with multivalley model allow to consider multiple tunneling process; tunneling between all valleys of the CB to all valleys of VB is accounted for; while no tunnelling between different valleys is taken into account. Indeed for 15% of Sn the I_d-V_{gs}, for both p and n-JNT configurations, seem to be quite flat and not usable for electrical purpose.

In relation to the SS due to the small on/off variability, the SS extraction has been made in the middle point of the characteristics. The values found show a SS degradation of 30% and 25% respectively for p-JNT and n-JNT. The SS aggravation might come from the B_g reduction as well as from both CB and VB bending imposed by the bias voltage applied that allow to create a tunnelling window between the channel and the drain [177]. Furthermore, the tunnelling effect tends to become more sensitive as the channel decrease because the source to channel barrier reduction that leads to I_{off} gains even without tunnelling effects.

Figure 2.12 reports the BTBT effects as a function of Sn concentration in device with channel length of 60 nm. It is noteworthy that the tunnelling effect becomes a serious problem for device with short channel lengths as already reported in literature [177] for other material systems, nevertheless in this study besides the aspect inherent to the short channel length also the low B_g belonging intrinsically to the alloy has to be taken into account.

Therefore since the material is innovative and did not exist a comprehensive model in the TCAD one future option might be the optimisation of the SS and I_{on}/I_{off} ratio parameters in order to use this new semiconductor material to create hetero Tunnel FET device that has a capability to exceed the planar MOSFET performance.

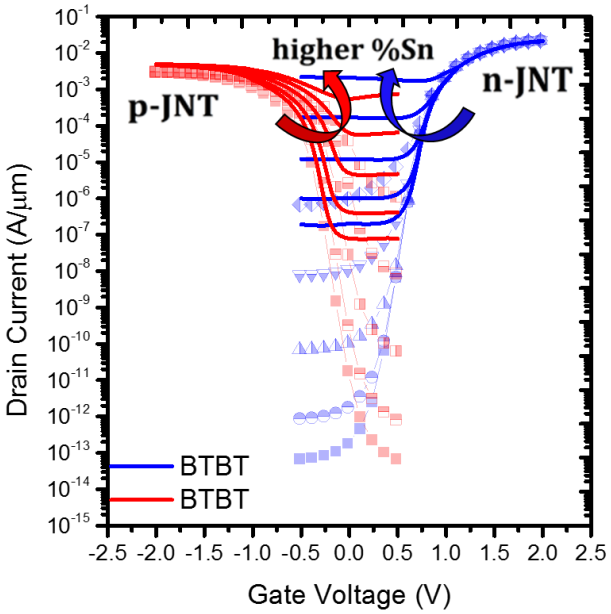


Figure 2.12: *Representative I_d-V_{gs} characteristics as a function of Sn content for p and n-JNT with a channel length of 60nm. In the I_d-V_{gs} characteristics in transparency there are the characteristics obtained without the considering the tunnelling effect while overlapped on it with red and blue there are the respectively the p and the n-JNT characteristics obtained with BTBT take into account.*

2.6.3 Mobility calibration

Since Synopsys TCAD uses a modular approach for the description of physical effects and accessible parameters that can be adjusted by the user, the models used might be improved adapting the software parameters to the more realistic outcomes coming from experimental results. Then, the aforementioned peculiarity has been exploited to calibrate the mobility. To calibrate the mobility basing on experimental data, the parameters of a specific mobility model (University of Bologna) have been modified for three different Sn concentration (3% , 6% and 9%). The default model

takes into account the mobility variation as a function of the temperature considering only the phonon scattering. Nevertheless for doped and alloy materials, the carrier scattering has to be turned on because these effects lead to a mobility degradation.

The University of Bologna bulk and surface models were used both to characterize the alloy mobility and they are based on the Masetti approach [178, 179]. The bulk model was able to take into account the mobility temperature dependence according to Equation 2.6.

$$\mu(T) = \mu_{max}\left(\frac{T}{300K}\right)^{-\gamma+c\left(\frac{T}{300K}\right)} \tag{2.6}$$

where μ_{max} denotes the lattice mobility at room temperature (27 °C), γ is a constant value and c is a corrective factor to handle high temperature analysis. While the surface mobility model considers the Coulomb, the surface phonons, and roughness scattering effects combined by Mathiessen's rule, showed in Equation 2.7.

$$\frac{1}{\mu} = \frac{1}{\mu_{bsc}} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \tag{2.7}$$

It means that the 3 degradation effects have been addressed separately and each of them will contribute in a different way; μ_{bsc} is a term associated with the substrate impurity and carrier concentration, D is a geometrical factor that takes into account the distance between the place where the carrier will flow and the interface, while μ_{ac} and μ_{sr} are the main scattering mechanisms related to the acoustic and surface scattering factors. A complete and more comprehensive analysis of the model is performed in the manual and it is reported in literature [180]. Equations 2.8; 2.9; and 2.10 govern the process and they respectively represent the Coulomb scattering, surface phonons and surface scattering contribution.

$$\mu_{bsc}{}^{-1} = \mu_b{}^{-1}(D(1 - f_{sc}{}^{\tau})^{-\frac{1}{\tau}} + (1 - D)) \tag{2.8}$$

$$\mu_{ac} = C(T) * \left(\frac{N_A + N_D}{N_2}\right)^{a} * \frac{1}{F_{\perp}^{\delta}} \tag{2.9}$$

$$\mu_{sr} = B(T) * \left(\frac{N_A + N_D + N_3}{N_4}\right)^{b} * \frac{1}{F_{\perp}^{\lambda}} \tag{2.10}$$

Furthermore, below in Table 2.5 there are the default and the calibrated values used in this PhD work. It is possible to see that the main change was made in order to decrease the fit factors; indeed l_{crit}, B and C parameters have been respectively tuned

with the aim to improve the surface, phonons and alloy scattering as a function of the Sn content.

Symbol	Parameter name	Default		$Ge_{0.97}Sn_{0.03}$		$Ge_{0.94}Sn_{0.06}$		$Ge_{0.91}Sn_{0.09}$		Unit
		Electrons	Holes	Electrons	Holes	Electrons	Holes	Electrons	Holes	
N1	N1	$2.34 * 10^{16}$	$2.02 * 10^{16}$	$2.34 * 10^{16}$	$2.02 * 10^{16}$	$2.34 * 10^{16}$	$2.02 * 10^{16}$	$2.34 * 10^{12}$	$2.02 * 10^{12}$	cm^{-3}
N2	N2	$4.0 * 10^{15}$	$7.8 * 10^{15}$	$4.0 * 10^{15}$	$7.8 * 10^{15}$	$4.0 * 10^{16}$	$7.8 * 10^{16}$	$4.0 * 10^{18}$	$7.8 * 10^{18}$	cm^{-3}
N3	N3	$1.00 * 10^{17}$	$2.00 * 10^{15}$	$1.00 * 10^{17}$	$2.00 * 10^{15}$	$1.00 * 10^{17}$	$2.00 * 10^{12}$	$1.00 * 10^{15}$	$2.00 * 10^{8}$	cm^{-3}
N4	N4	$2.4 * 10^{18}$	$6.6 * 10^{17}$	$2.4 * 10^{18}$	$6.6 * 10^{17}$	$2.4 * 10^{18}$	$6.6 * 10^{18}$	$2.4 * 10^{20}$	$6.6 * 10^{19}$	cm^{-3}
B	B	$2.4 * 10^{18}\gamma_B$	$7.8 * 10^{15}\gamma_B$	$5.8 * 10^{10}\gamma_B$	$7.8 * 10^{7}\gamma_B$	$5.8 * 10^{7}\gamma_B$	$7.8 * 10^{10}\gamma_B$	$5.8 * 10^{8}\gamma_B$	$7.8 * 10^{15}\gamma_B$	cm^{-2}/Vs
C	C	$1.8 * 10^{4}T^{-\gamma_C}$	$5.7 * 10^{3}T^{-\gamma_C}$	$1.8 * 10^{4}T^{-\gamma_C}$	$5.7 * 10^{3}T^{-\gamma_C}$	$1.8 * 10^{4}T^{-\gamma_C}$	$5.7 * 10^{3}T^{-\gamma_C}$	$1.8 * 10^{3}T^{-\gamma_C}$	$5.7 * 10^{3}T^{-\gamma_C}$	cm^{-2}/Vs
γ_B	B_exp	0	1.4	0	1.4	0	1.4	0	1.4	1
γ_C	C_exp	2.1	1.3	2.1	1.3	2.1	1.3	2.1	1.3	1
τ	tau	1	3	1	3	1	3	1	3	1
η	eta	0.3	0.5	0.3	0.5	0.3	0.5	0.3	0.5	1
a	ac_exp	0.026	-0.02	0.026	-0.002	0.05	-0.002	0.05	-0.002	1
b	sr_exp	0.11	0.08	0.11	0.08	0.11	0.09	0.11	0.10	1
l_{crit}	L_crit	$1.0 * 10^{-6}$	$1.0 * 10^{-6}$	$1.0 * 10^{-9}$	$1.0 * 10^{-9}$	$1.0 * 10^{-9}$	$1.0 * 10^{-9}$	$1.0 * 10^{-9}$	$1.0 * 10^{-9}$	cm
δ	Delta	0.29	0.3	0.29	0.3	$0.29 * 10^{-1}$	0.3	$0.29 * 10^{-1}$	0.3	1
λ	lambda	2.64	2.24	2.64	2.24	$2.64 * 10^{-1}$	2.24	$8.64 * 10^{-1}$	2.24	1

Table 2.5: *Table with default and calibrated values used in UniBoEnormalDependence Synopsys TCAD as a function of different Sn content.*

Moreover Synopsys TCAD permits modelling of the traps defect effect that might enhance the recombination process consequently increasing the leakage current. Therefore to obtain a proper calibration it was needed to insert an acceptor density trap layer near the conduction band according to previous literature works [181, 182]. Then the final model was able to take into account also the effect of the traps for all Sn concentrations considered. In the model $Ge_{0.97}Sn_{0.03}$ and $Ge_{0.91}Sn_{0.09}$ have a donor concentration of 1×10^{12} cm^{-3} shifted of 0.15 eV from the middle of the gap towards the CB while $Ge_{0.94}Sn_{0.06}$ has a donor concentration of 1×10^{12} cm^{-3} shifted of 0.25 eV from the middle of the gap towards the CB.

Figure 2.13 shows both 2D, 3D nanowire structure used for the calibration of $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ alloy. In all the image in black there is the experimental I-V curve coming from experimental data further discussed in Chapter 5 and overlapped on it, in red, there are the fit achieved.

Since the experimental data obtained show high variability the average I_d-V_{bg} curves were selected for all the Sn contents investigated; furthermore, the device was specifically tailored according to the real design. In addition for the simulation purposes also other models as the high-field velocity saturation model and the Shockley–Read–Hall generation-recombination models, with Ge parameters included.

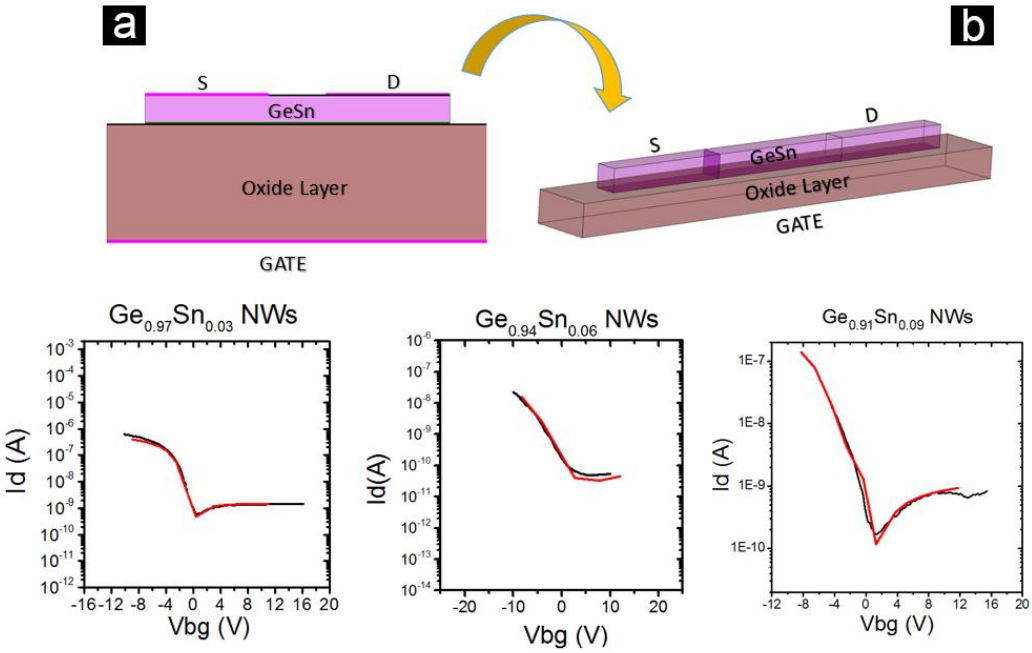


Figure 2.13: *2D (a) and 3D (b) structure used for the calibration and further below in the graph there are the results obtained as a function of the Sn content, highlighted in black in background there are the experimetntal results and overlapped in red there are the simulation data.*

2.6.4 Electrical characterisation after calibration

After the mobility calibration the simulations have been iterated again on both double gate p and n-JNT structure used in Section 2.6.2. The aim was to point out the electrical performance as a function of the Sn content, channel lengths and doping concentration in order to compare the results before and after the mobility calibration. Figure 2.14 shows the results obtained in the simulations without consider MLDA and BTBT models.

Accordingly to previous data, the characteristics are going to deteriorate as the Sn content will increase due to the B_g reduction. The study reports the I_{on}/I_{off} ratio and SS electrical benchmark for each curve and the results was firstly examined without taking into account the quantum confinement effects.

Concerning the channel length variation, despite the electrostatic control of the gate increases, the characteristics seems to change only slightly. As a regard of p-JNT, $Ge_{0.97}Sn_{0.03}$ shows a ratio of ~10^4, $Ge_{0.94}Sn_{0.06}$ of ~10^3 and $Ge_{0.91}Sn_{0.09}$ a I_{on}/I_{off} ratio of ~10^2; instead for the n-JNT, $Ge_{0.97}Sn_{0.03,}$ $Ge_{0.94}Sn_{0.06,}$ $Ge_{0.91}Sn_{0.09}$ show respectively a ratio of 10^3, 10^2, 10^1. Then compared with the results reported in Fig.2.9 a reduction of roughly 40%, and 75% occur individually for p-JNT and n-JNT.

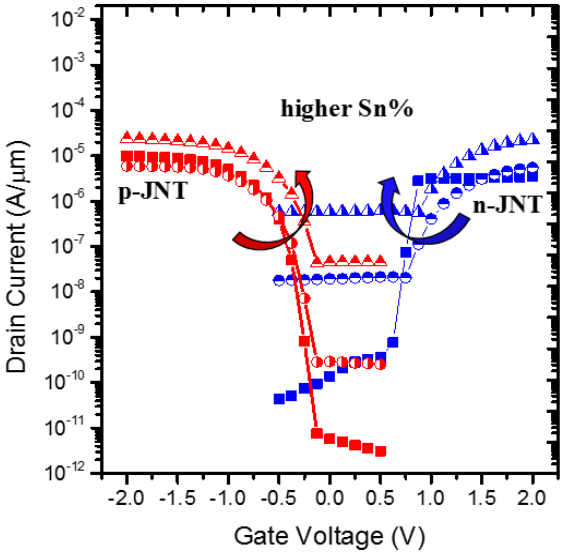


Figure 2.14: *Representative I_d-V_{gs} characteristics as a function of Sn content (3, 6 and 9%) for p (red curves) and n-JNT (blue curves) with a channel length of 100nm and doping concentration of 1×10^{19} atoms/cm^3 after mobility calibration.*

Relating to SS, the values have been extracted considering one decade variation and data have been inserted in the Table 2.6. As expected the values worsened due to the scattering effects. The output obtained from the simulations, even if the trend is always the same, show the decline of SS compared with the previous data obtained without calibration, and demonstrate the importance of experimental benchmarking. In p-JNT configuration the minimum value obtained is 74.2 mV/dec and the data are worsen in average of 22.5%, 32.5% and 110% respectively for Sn content of 3%, 6% and 9%; while for n-JNT the minimum value is 65.2 mV/dec and the data are deteriorated in average of 15%, 250% and 450% in relation to 3%, 6% and 9% Sn content in the alloy. Basically decreasing the channel size, the gate electrostatic control increases, leading to a better SS, these results were obtained without considering the tunnelling and the quantum confinement models.

3%Sn (mV/dec)	*6%Sn (mV/dec)*	*9%Sn (mV/dec)*	*(nm)*	*3%Sn (mV/dec)*	*6%Sn (mV/dec)*	*9%Sn (mV/dec)*
62.6→82.7	69.3→100.4	66.2→171.1	***100***	62.3→90.7	62.5→300.5	67.6→370.7
62.9→80.3	69.6→98.5	66.5→168.2	***80***	61.8→85.4	62.1→268.3	68.1→350.5
63.4→80.7	68.6→87.3	66.8→165.4	***60***	61.4→75.7	61.4→230.5	68.9→338.6
65.2→74.2	69.8→85.8	68.3→163.6	***40***	61.2→70.5	61.5→180.9	68.7→300.2
69.8→79.5	70.5→85.3	92.3→150.5	***20***	68.1→65.2	70.1→175.1	97.6→250.7

Table 2.6: *SS values expressed in mV/dec considering the new calibration model for both p and n-JNT. Values have been reported as a function of gate lengths, highlighted in the central column, and Sn concentrations, reported on top of the table. The red and blue section respectively report the results of p-JNT and n-JNT.*

As a regard of the doping concentration the analysis have been repeated and as expected, decreasing the doping concentration the space charge region will increase leading to an improvement of electrical performance. Overall as regards the I_{on}/I_{off} ratio there is roughly an improvement along the different doping concentration while a remarkable SS drop has been observed. Essentially the SS slope decreases in average of 20% and 40% respectively for p and n-JNT reaching minimum values of 85 mV/dec and 90 mV/dec.

Finally to have an exhaustive analysis the simulations have been repeated considering the quantum and the tunnelling effects. Concerning the MLDA simulations, a representative result using device with different channel length and doping concentration of 1×10^{19} atoms/cm^3 has been shown in Figure 2.15. The output coming from the simulations that include the MLDA model has been seen that the model slightly influences the electrical performance without leading to a remarkable difference.

Whilst for the tunnelling aspects, the model turned on was not able to convergence then further refinement, both on the physical material that for device geometry, are required to analyse the tunnelling contribution to the electrical performance.

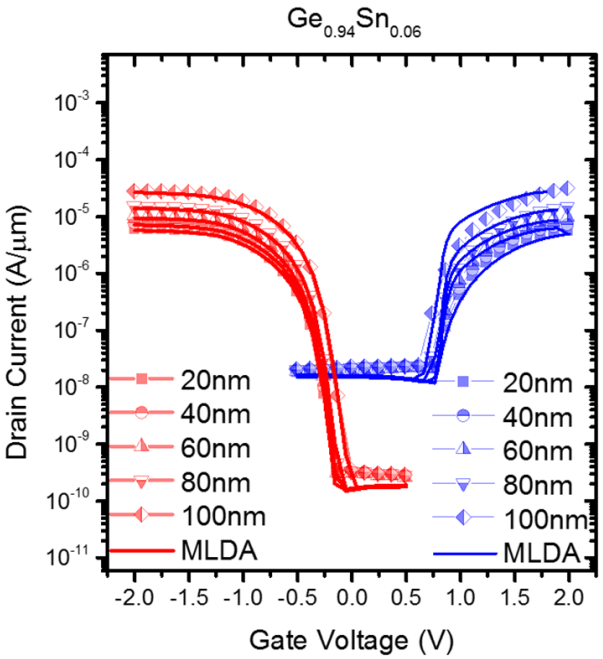


Figure 2.15: *Shows the transfer characteristics with MLDA model active. In transparency there are the curves without the model and overlapped on it there are the curve obtained considering the quantum confinement. Red and blue curves in the plot respectively indicate the p and the n-JNT data.*

2.7 Conclusion

In this Chapter $Ge_{1-x}Sn_x$ dual gate p and n-JNT with Sn concentration up to 15% were examined and calibrated basing on experimental results. The model was built starting from the scratch with Synopsys TCAD, and through it a systematic analysis has been made considering the physical device parameters variables, as a function of the Sn concentration.

Firstly, alloy B_g variations have been extracted using the EPM in the SBAND tool; afterward electron and hole masses have been extracted by Synopsys software and subsequently the outcomes have been used to simulate and predict the electrical performance of a double gate $Ge_{1-x}Sn_x$ JNT. Nevertheless, considering both, (1) the lack in literature about experimental data of $Ge_{1-x}Sn_x$ nm-devices and (2) the many physical effects involved into the system; the results report the underlying electrical characterisation of the material in a practical sense.

The parameter file developed, tried to be as comprehensive and reliable as possible considering several aspects as the B_g variation, the electron hole mass, mobility models, tunnelling effects and quantum confinement as a function of different Sn concentration, channel length and doping variations.

From the analysis of the $Ge_{1-x}Sn_x$ alloy, it has been shown that as a regard of digital purposes, despite physical model limitations, as long as the percentage of Sn does not exceed 9% the alloy has the ability to work as switch; while if the Sn percentage exceeds 10% the alloy is unusable for low power devices but the alloy could be used for optoelectronics purposes or to create hetero-structure device like TFET. Furthermore for the $Ge_{1-x}Sn_x$ JNT has also been seen that devices with Sn over 15% turn out to be unsuitable for all electrical purposes due to poor SS and I_{on}/I_{off} ratio. Overall the modified models and parameters, despite some limitations as the CB or VB offset, the sub-band formation, and the strain variation, are able to predict reliable electrical results even if further refinement basing on the experimental data are still necessary to tune the models. Data outlined must be interpreted qualitatively and not quantitatively due to limited experimental feedback. Therefore in future might be interesting to deepen the effect of the discreteness of the dopant ions, the mobility, the quantum effects and the tunnelling, because making comparison between the experimental data and simulation will be possible develop a global model able to take into account several physical effects.

3|Contacts on $Ge_{1-x}Sn_x$ devices

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This chapter is adapted from the following publications:

(1) **Galluccio, E.**, Petkov, N., Mirabelli, G., Doherty, J.,Shih-Va, L., Fang-Liang, L., Chee Wee, L., Holmes, J., Duffy, R., *Formation and characterization of Ni, Pt, and Ti stanogermanide contacts on Ge0. 92Sn0. 08.* Thin Solid Films, 2019. **690**: p. 137568.

(2) **Galluccio. E**, Petkov, N., Mirabelli, G., Doherty, J.,Shih-Va, L., Fang-Liang, L., Chee Wee, L., Holmes, J., Duffy, R., *Ni, Pt, and Ti stanogermanide formation on Ge0.92Sn0.08,* 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Grenoble, France, 2019, pp. 1-4.

(3) **Galluccio, E.**, et al., *Cell formation in stanogermanides using pulsed laser thermal annealing on $Ge_{0.91}Sn_{0.09}$* Materials Science in Semiconductor Processing, 105399,2020.

3 Contacts on $Ge_{1-x}Sn_x$ devices

3.1 Introduction

Metal-semiconductor (MS) contact formation is one of the essential processes required to connect any semiconductor based device to the external circuitry. In theory two contact types exist and the crucial difference mainly consists in the potential barrier formed between the interfaces of the two materials. MS contacts can be categorized as Rectifying Schottky Diodes, which are used in several electrical applications such as power devices, and non-Rectifying Ohmic contact, used to connect the transistor outward in the integrated circuit. Ideally the contact should present negligible resistance compared to the device resistance and linear Current-Voltage characteristics in order to not significantly affect the electrical performance.

Therefore, in the first part of this chapter is a brief introduction on the MS contacts, followed by the state-of-the-art, presented to report and address the issues observed so far for this new semiconductor material. Subsequently, a comprehensive study of the low resistance stanogermanide alloys, obtained by *Rapid Thermal Annealing (RTA)* and *Laser Thermal Annealing (LTA)*, is illustrated with the purpose of identifying both, the most promising metals and annealing technique candidates, for future stanogermanide contacts. These experiment would not have been possible without the collaborations with Taiwan National University and IQE that provided the substrates and the University of Padova that execute the LTA.

3.2 Theory

The principle of forming different types of MS contact is due by the difference in the *Fermi energy* (EF) level between metal and semiconductor material. The study of the MS contact starts from the understanding of material band diagram involved in absence of any interface/surface anomalies.

Figure 3.1 illustrates the band diagram for metal and semiconductor (Fig. 3.1.a n-type Semiconductor, Fig. 3.1.b p-type semiconductor) when the two materials are not in contact. *Work function (WF)* parameters, defined as $q\Phi_M$ and $q\Phi_S$ for metal and semiconductor respectively, delineates the energy required to extract one electron from the EF level to the *vacuum energy level* (E_{VAC}) for both elements. It must be said that WF is an intrinsic property of the material; it is fixed for the metal

while it can be tuned by changing the dopant concentration for the semiconductor leading to electrical performance variation. qχ refers to the semiconductor electron affinity, it depicts the energy required to extract one electron from the conduction band to the vacuum energy level. Then, taking as example a configuration obtained using a metal and a n-type semiconductor, Fig. 3.1.(a), assuming the materials not connected, the average energy of an electron in the semiconductor is higher than the metal $q\Phi_M > q\Phi_S$; while vice-versa occurs taking into account a p-type semiconductor $q\Phi_M < q\Phi_S$ Fig. 3.1.(b).

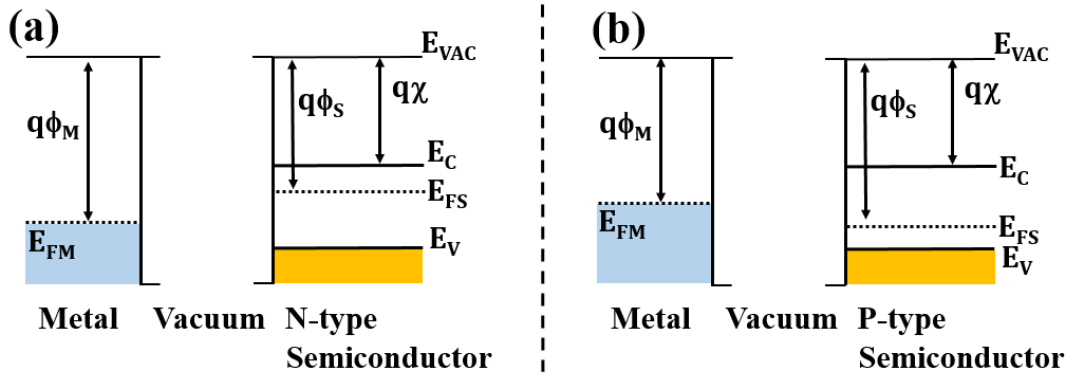


Figure 3.1: *Schematic of the energy band diagram for metal semiconductor when materials are not in contact. (a) Metal and n-type Semiconductor not in contact ($q\Phi_M > q\Phi_S$). (b) Metal and p-type Semiconductor not in contact ($q\Phi_M < q\Phi_S$). adapted from [183]*

It is noteworthy that the EF in both materials are not aligned; therefore when the two elements come in contact a charge redistribution is needed to restore the equilibrium between the two entities. Thanks to substantial higher *density of states* (DOS) in the metal, the WF in this part is basically unaffected by the contacting process; while in the semiconductor it changes according to the difference between the two WF.

Therefore to establish the equilibrium, considering an n-type semiconductor with $q\Phi_M > q\Phi_S$, the electrons in the conduction band of the semiconductor will migrate into the metal until the EF are aligned. The carriers movement causes the formation of fixed ionized impurities that leads to the creation of a depletion region and consequently to the development of a built-in electric field.

The electrical field variation achieved causes the electronic bands to bend upward in the semiconductor counteracting the electron diffusion until thermal equilibrium is restored [24, 183], as shows in Figure 3.2.(a).

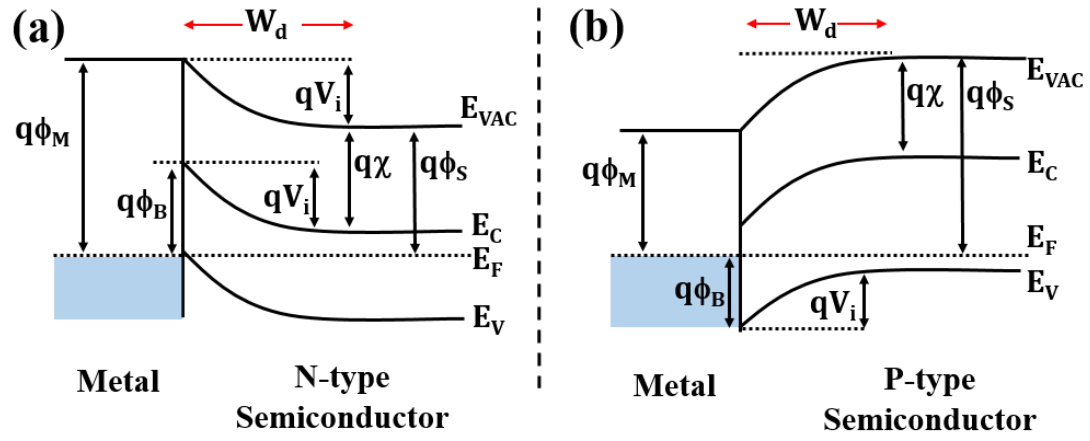


Figure 3.2:*Schematic of rectifying contact for metal semiconductor. (a)Band diagram for Metal and n-type Semiconductor in contact ($q\Phi_M > q\Phi_S$). (b) Band diagram for Metal and p-type Semiconductor in contact ($q\Phi_M < q\Phi_S$). adapted from [183].*

In this scenario, the electrons from the semiconductor side is going to see the potential barrier created at the interface to prevent the further movements of the carrier given by:

$$qV_i = q\phi_m - q\phi_s \quad (3.1)$$

While the electrons from the metal side due to the built-in potential barrier created, known as *electron Schottky Barrier Height (eSBH)*, will see the barrier equal to:

$$q\phi_B = q\phi_m - q\chi \quad (3.2)$$

The description for a p-type semiconductor is analogous, the carrier flow is due by the holes from the valence band and the migration leads to downward bending of the electronic bands in the semiconductor as shown in Figure 3.2.(b). Moreover in this case, the *hole Schottky Barrier Height (hSBH)* is given by $q\Phi_B = E_G - q(\Phi_M - \chi)$.

After the contact formation, the potential barrier seen from the semiconductor might by modified according to the voltage applied. Therefore if a positive voltage bias is applied to the MS contact the net current flow from the semiconductor to the metal is increased due the potential barrier reduction that promotes the migration of the electrons; while the opposite occurs if a negative voltage is applied to the MS contact. In that case the barrier will increase hampering the passage of the electrons. In both situations the metal barrier remains unchanged leading to a non-linear Current-Voltage behaviour. Similar analysis is utilized for p-type semiconductor

with holes as majority carrier [184]; anyway both using n or p-type semiconductor the MS contact shows a diode/rectyfing behavior. Conversely, as shown in Figure 3.3.(a) if n-type semiconductor is degenerately doped or if $q\Phi_M < q\Phi_S$ (for a p-type semiconductor $q\Phi_M > q\Phi_S$), an Ohmic contact is achieved respectively due to the shrinkage of the depletion region, that promotes tunneling effect, or due to the low barrier formation that promotes the movement of free carriers between the MS contacts.

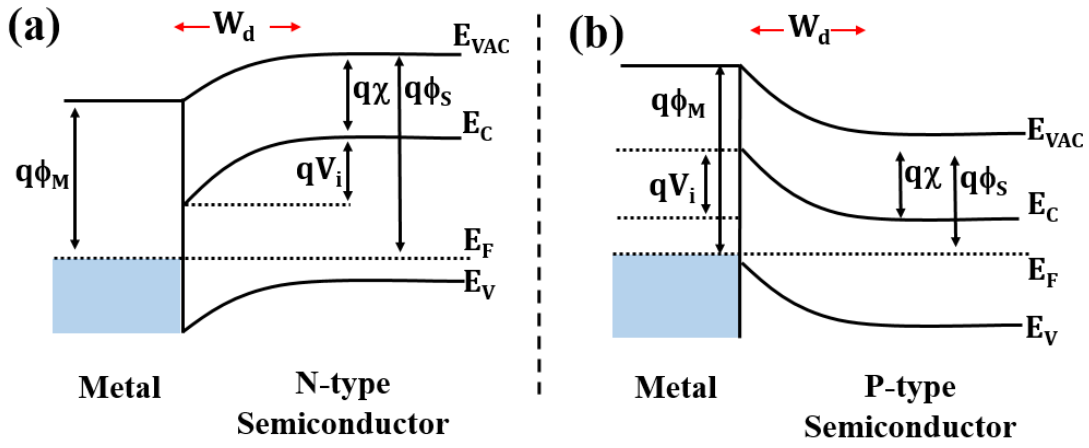


Figure 3.3: *Schematic of Ohmic contact for metal semiconductor. (a)Band diagram for Metal and n-type Semiconductor in contact ($q\Phi_M > q\Phi_S$). (b) Band diagram for Metal and p-type Semiconductor in contact ($q\Phi_M < q\Phi_S$) adapted from [183].*

One of the major efforts in handling new semiconductor materials for nanoelectronic devices is the achievement of stable contacts at semiconductor interfaces, with low contact resistance and linear I-V behaviour. The study of the process steps required to obtain a MS contact and the characterization using different metals are critical for the electrical performance and reliability of semiconductor devices because contacts with rectifying behaviour renders the device useless for the external circuitry.

3.3 State-of-the-art for $Ge_{1-x}Sn_x$ contacts

Through the years extensive studies on Ge and its alloys have been made in order to explore the possibility to integrate $Ge_{1-x}Sn_x$ in CMOS platforms [185]. Research moved from the physical modelling analysis and characterization [174, 186] to process optimization [121, 187-189] up to the initial planar FET demonstration. The first outcomes were a starting point which have now progressed onto the development of electrical and optoelectronics devices such as quantum-well

devices [127, 190], FinFETs [125], photodetectors [124], and lasers [137] that have shown the potential uses of the material.

Nevertheless as FET channel dimensions shrink, the source/drain contact resistance becomes relatively more significant in the overall parasitic resistance in the transistor. In fact in some cases contact resistance is the bottleneck for certain technologies. Therefore in analogy with Si, where the *metal-Silicon (Silicide)* alloys are used to create metal contacts with low contact resistance [191], the *metal-Germanium (Germanides)* and *metal-$Ge_{1-x}Sn_x$ (Stanogermanides)*, seem to be natural candidates for metal contacts in these devices. Although Ge solutions proposed have a strong appeal, investigations of alloy contacts to $Ge_{1-x}Sn_x$ are still immature; consequently an intensive study on contact formation is essential to ensure good $Ge_{1-x}Sn_x$ device performance.

Judging from the recent literature on $Ge_{1-x}Sn_x$, much work has been focused on NiGeSn contacts [192-196], and TiGeSn [197-199]; or alternatively on a possible mix among different metals to increase the thermal stability of the alloy [200-202]. Li [192] et al. and Zhang et al. [200] reported an electrical and material investigation of NiGeSn under several thermal annealing conditions; in these works the contact resistivity was found to decrease with increasing annealing temperature, while the defect density increased. Yi Tong et al. [193] studied NiGeSn contact formation, where low resistivity $Ni(Ge_{(1-x)}Sn_{(x)})$ was formed using an annealing temperature of 350 °C for 30 seconds. Nishimura et al. [194] showed the formation of NiGeSn layers using a solid phase reaction and investigated the crystalline properties of the layers; the formation of β-Sn was observed after annealing above 450 °C due to the Sn precipitation and the roughness also degraded as the annealing temperature increased, linked to a poorer thermal stability for samples with high Sn content. Wirths et al. [195] carried out a comprehensive work on the NiGeSn using samples with different Sn percentage. They extracted both morphological and electrical parameters, among which was the sheet resistance as a function of the annealing temperature. Liu et al. [201] and Wang et al. [202] also reported NiGeSn sheet resistance variation. The lowest sheet resistance value was respectively $10\ \Omega/sq$ for Wirths et al. (using an annealing temperature of 325 °C) and $5\ \Omega/sq$ for Liu et al. and $6\ \Omega/sq$ Wang et al.

However, a focused study is still lacking, and is needed, on the contact formation to $Ge_{1-x}Sn_x$ using different metals. Therefore, following in this chapter a systematic and comparative study is presented, employing three of the most common metals used to create contacts [203], such as Ni, Ti, and Pt on $Ge_{0.92}Sn_{0.08}$.

3.4 Contacts made by Rapid Thermal Annealing

For extremely scaled FETs devices contact resistance in the *Source/Drain* (S/D) regions is one of the key factors that limit the transistor drive current. For many years Silicides and Germanides have been the most widely used technique to contact S/D regions of FET devices due to the massive impact in the final performance [204]. The well-established reaction between some specific MS contacts such as NiSi, TiSi, NiGe TiGe or PtGe, leads to a more reliable contact that improves the conduction providing higher performance with lower parasitic resistance. Therefore in the following section a comparative and systematic study is displayed on contact formation for $Ge_{1-x}Sn_x$ thin films using Ni, Ti or Pt.

3.4.1 Experimental procedure

Usually samples examined are doped in order to improve the contact performance exploiting the tunneling effect, nevertheless the $Ge_{0.92}Sn_{0.08}$ samples used here were un-doped because achieving high-doping is a critical difficulty for the material under investigation. To activate the dopant without degrading the substrate is required a really precise temperature control; moreover the thermal activation process might lead imperfections such as presence of defects, Sn precipitation or Sn surface segregation. Therefore the following work has been carried out on un-doped substrates to avoid complication coming from the doping process. The analysis aim is to point out the best metal candidate, in terms of low resistance, low formation temperature, and high thermal stability, for future stanogermanide contact formed in a typical thermal budget used for $Ge_{1-x}Sn_x$ processing.

A schematic representation of the process flow and variables considered is shown in Fig. 3.4. The starting material comprises of a nominally un-doped epi-layer of $Ge_{0.92}Sn_{0.08}$ (28 nm thick) on a nominally un-doped virtual substrate layer of Ge. The Ge layer undergoes 800 °C annealing before growth of $Ge_{0.92}Sn_{0.08}$ to reduce the epi-layer defect density. The un-doped $Ge_{0.92}Sn_{0.08}$ is grown at 320 °C using Ge_2H_6 and $SnCl_4$ in H_2 ambient by *CVD* [124, 137, 192, 193]. GeSn surfaces

were cleaned using a standard recipe; the sample was dipped for 30 s in acetone, 30 s in *isopropyl alcohol* (IPA), and subsequently rinsed under *Deionized* (DI) Water for another 30 s.

Thereafter a 20 nm layer of either Ni, Ti or Pt, was deposited on the samples. The metal deposition was carried out using the FC2000 electron beam evaporator at a pressure of 6.6×10^{-5} Pa. Ni and Pt were evaporated with a rate of 0.2 nm/s while the Ti with a rate of 0.1 nm/s. Then the samples underwent at 30 s RTA in *nitrogen (N_2)* ambient at different temperatures; ranging from 300 - 500 °C with a difference of 50 °C. The ramp rate used for each RTA was 100 °C/min and the cool down time was 15 min.

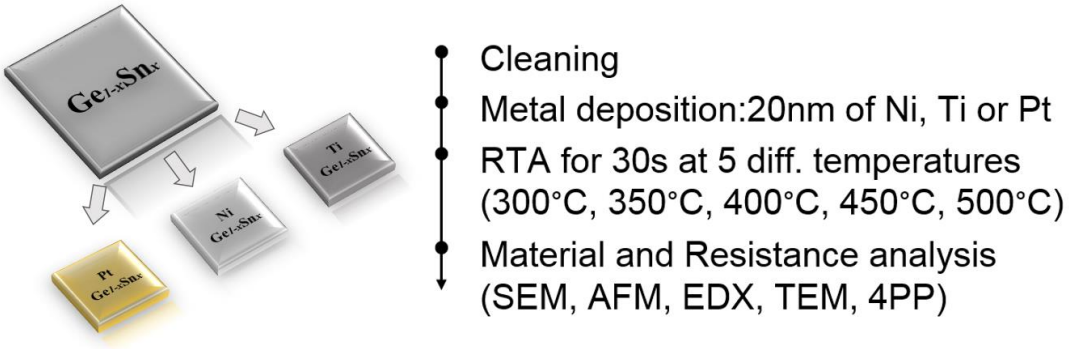


Figure 3.4: *Schematic representation of the stanogermanide process flow and variables considered in this work.*

To have a comprehensive study we characterized all the samples as a function of the different RTA temperatures and of the metals used. As regards the material features, the study was performed using *Scanning Electron Microscopy (SEM)*, *Atomic Force Microscopy (AFM)*, cross sectional *Transmission Electron Microscopy (TEM)* and *Electron Dispersive X-ray (EDX)*; while for the electrical investigation, *4 Point Probe (4PP)* analysis was done to extract the sheet resistance of the different stanogermanide materials formed.

SEM surface investigation was performed using a Zeiss Supra55VP machine at 15kV acceleration voltage, while the AFM study was carried out with Veeco Multi-mode V AFM in tapping/non-contact mode at room temperature and in air, considering a 5 μm × 5 μm area. Cross-sectioned samples were prepared by focused ion beam etching, using a FEI's Dual Beam Helios Nanolab system using a *Gallium (Ga)* ion beam. Layers of protective material, consisting of electron beam deposited C, Pt, and ion beam deposited C, were used. Subsequently *Cross-sectional*

Transmission Electron Microscopy (XTEM) was realized using a JEOL 2100 HRTEM operated at 200 kV in bright field mode using a Gatan Double Tilt holder. Scanning TEM imaging as well as point and line-scan EDX analysis of the cross-sections were performed using FEI's Dual Beam Helios Nanolab system equipped with Oxford Instruments X-MAX-50 EDX detector at 30 kV acceleration voltage. The EDX data collection and quantification was accomplished using software. For the electrical test a 4PP measurement was made using the LUCAS LABS-S-302 4 Manual four point resistivity probing station.

3.4.2 Results and discussion

In the following sections the systematic analysis employed to characterize the material and the electrical contact behaviour will be introduced, with the purpose of identifying the most promising stanogermanide contact candidate, in terms of low sheet resistance, low surface roughness and low formation temperature.

3.4.2.1 Electrical characterisation

The contact is one of the simplest and the most common components in an *integrated circuit* (IC). However, understanding of contact resistance effects are not that straightforward. Basically the *contact resistance (R_C)* and the *contact resistivity (ρ_C)*, are the two fundamental parameters that quantify how a contact interface resists to the electric current flow. Equation (3.3) shows the standard equation used to estimate the contact resistance, where ρ_C is the contact resistance, L is the length while t and W represents thickness and width respectively.

Equation (3.4) is the definition of sheet resistance *(R_{sh})*, basically it measures a resistance between opposite sides of a square and it is a common electrical property used to characterize thin films of conducting and semiconducting material; while equation (3.5) defines the contact resistance.

$$R_c = \rho_c \frac{L}{t * W} \quad (3.3) \qquad R_S = \frac{\rho_c}{t} \quad (3.4) \qquad R_c = R_S \frac{L}{W} \quad (3.5)$$

Previous research reported in the literature was focused on contact resistance but there are very little data on $Ge_{1-x}Sn_x$ sheet resistance. Therefore, in this section the routine performed to extract the data was based on 4PP methodology and the electrical characterization will be discussed below in detail.

It is noteworthy that the resistance results obtained depend on the complete or partial reaction of the metal with the underlying material; indeed it will be seen that Ni and Pt react readily with the $Ge_{1-x}Sn_x$ thin film, while Ti remains unreactive, leading to the poor resistance values seen here.

4PP is one of the most common methodology used to characterize the material resistance. R_{sh} is a specific property for any thin film because it depicts the ability of the carriers to travel along the material rather then pass through it.

The procedure used to extract the electrical data involves the usage of 4 probes in a line, with equal spacing between them as shown in Figure 3.5(a). It operates by applying a current on the outer two probes and measuring the resultant voltage drop between the two inner probes.

Using the 4PP configuration the contact and wire resistances contributions will be eliminated from the measurement. Basically the current enters and leaves the sample via the outer probes because, due to the high impedence of the voltmeter, the current will not flow through the inner probes. Then the measurements will be not affected by any other resistive contribution less than the one provided by the thin film.

$$R_S = C * \frac{\Delta_V}{I} \tag{3.6}$$

The sheet resistance can be calculated using equation (3.6) where C represents the corrective factor and it depends from the sample geometry, while Δ_V and I the voltage drop and the current respectively.

In this work $Ge_{0.92}Sn_{0.08}$ undoped samples with rectangular geometry ($1cm * 1cm$) and thickness of $28 * 10^{-9}m$ has been used; therefore according to literature [205] the corrective factor used was 4.53236.

The measurement have been performed in the middle of each sample as shown in Fig.3.5.(b) applying a current from -5mA to 5mA and recording the potential drop achieved. Subsequently, for each sample measured, the sheet resistance values have been extracted. Fig. 3.6 shows R_{sh} values measured by the 4PP [205].

The plot displays the data obtained for the three different metals as a function of the formation temperature. Ni-Stanogermanide layers shows lower R_{sh} up to a formation temperature of 400 °C, which correlates with that seen for Ge [203, 206]. At higher formation temperatures PtGeSn outperforms the NiGeSn in terms of R_{sh}.

With regard Ti, the values are approximately one order of magnitude higher compared to the other two materials.

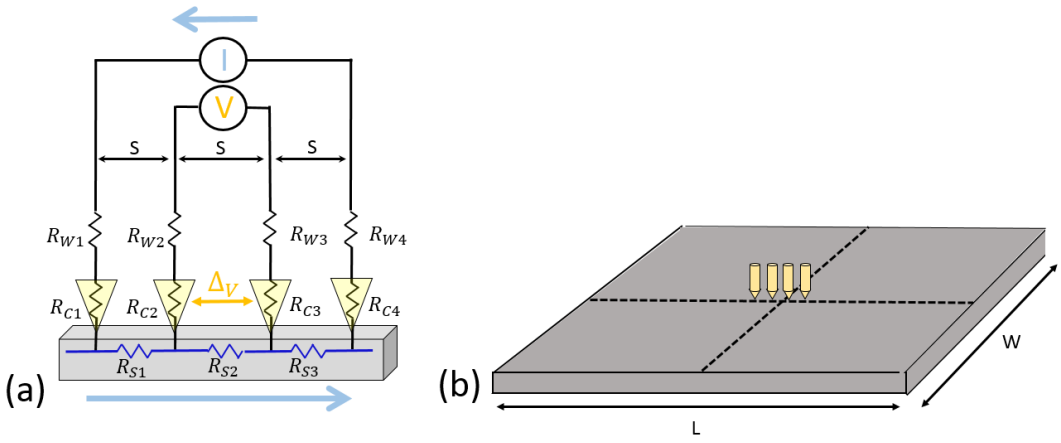


Figure 3.5: *(a) Four point probe sketch with all the possible resistive contributes, wires (R_{W1} to R_{W4}), contacts (R_{C1} to R_{C4}) and series (R_{S1} to R_{S4}), (b) configuration used to extract the sheet resistance in this work*

Despite the high *Oxygen* (O) solubility and diffusion in Ti no obvious oxide layers were found in the Ti cross-section investigation. Therefore has been hypothesized that Ti behaviour comes from the lack of reaction of the metal with the underlying $Ge_{0.92}Sn_{0.08}$ substrate; further confirmed from the SEM analysis where a remarkable degradation of the material will be shown.

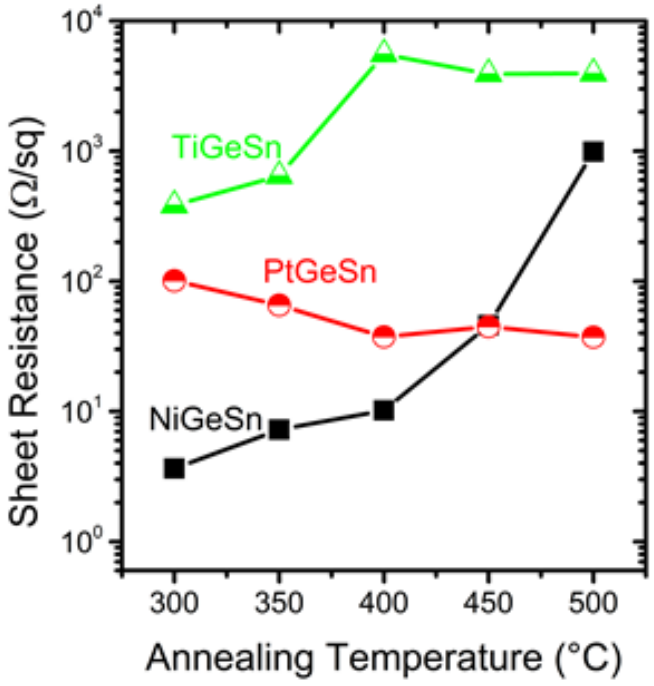


Figure 3.6: *Sheet resistance for Ni, Ti and Pt stanogermanides as a function of the formation temperature.*

3.4.2.2 Morphological and Composition Analysis

The analysis that follows in this section explores the changing structural trends of the stanogermanides with increased formation temperature. The most interesting condition in Fig. 3.6, i.e. the lowest measured sheet resistance. All the samples under investigation have been analysed by SEM to characterize the surface quality as a function of the different metals and formation temperatures used.

Fig. 3.7 shows representative SEM images for the two RTA temperature extremes (300 °C and 500 °C). At 300 °C, all of the Ni, Ti, and Pt samples showed continuous layer formation (Fig. 3.7.(a), 3.7.(c) and 3.7.(e)). In contrast at 500 °C Ni and Ti samples showed the formation of discontinuous layers, while the Pt sample preserved its uniformity, see Fig.3.7.(b), 3.7.(d) and 3.7.(f).

Further SEM analysis revealed that the Ni-stanogermanide reactive growth resulted in continuous layers up to 400 °C, whereby for Ti samples, surface agglomeration started at 450 °C, according to the temperature reported in literature where the metals starts to react with underlying Ge substrate [203].

In comparison, the Pt samples showed continuous structures over the entire temperature range studied. The development of unwanted discontinued layers suggests the formation of island-type inclusions or surface aggregates; further cross-sectional analyses confirmed that Ni-stanogermanide layers degraded by forming island-type inclusions, while Ti-samples showed surface aggregation at these high temperatures.

In addition, AFM investigations were undertaken on all of the samples; considering a scan area of 5 μm × 5 μm. For each sample, the data was extracted by analysing the central portion of the sample, avoiding edge effects. Fig. 3.8 highlights the surface roughness of the samples as a function of temperature and metal composition (inset table details the roughness values obtained). From the data achieved GeSn bare surface has been assumed to not substantially influence the final results which instead are strongly dependent from the metal reaction with the underneath GeSn layer.

For all of the samples inspected, the surface roughness increased with increasing annealing temperature absolutely in accordance with previous works found in literature [207] where the same trend has been already observed. At 500 °C the NiGeSn and TiGeSn surfaces start to agglomerate, resulting in a *root mean*

square (RMS) roughness around 7 nm. The lowest surface roughness in average was obtained for PtGeSn. The data obtained are in good accordance with previous reports found in literature [194, 208] which have shown an increasing roughness with rising annealing temperature for Ni.

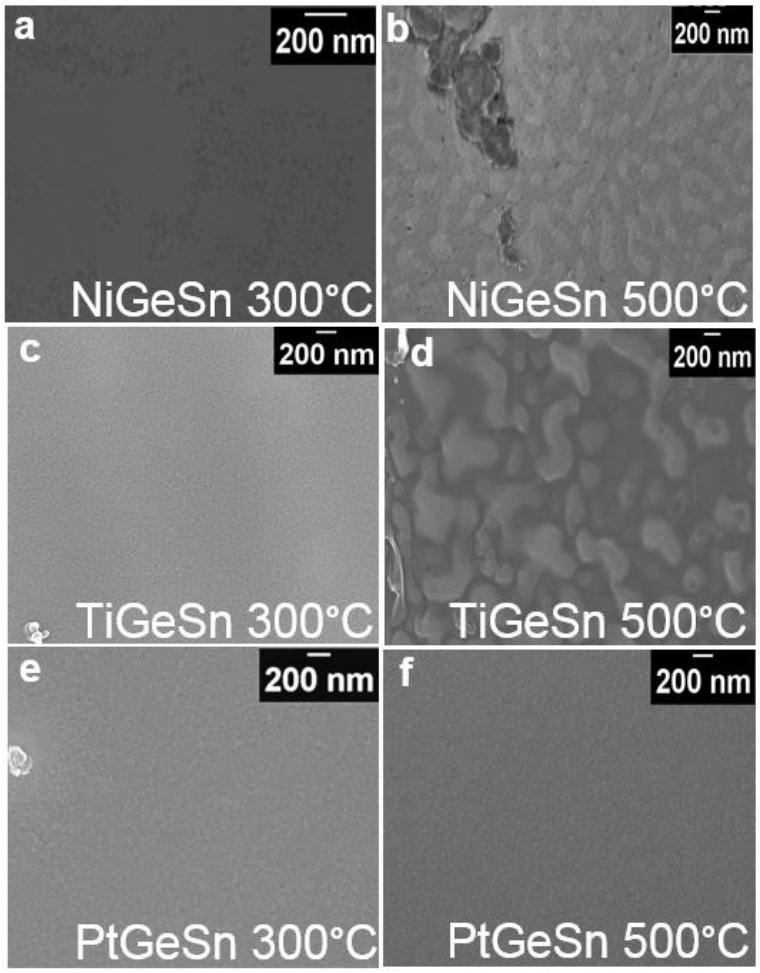
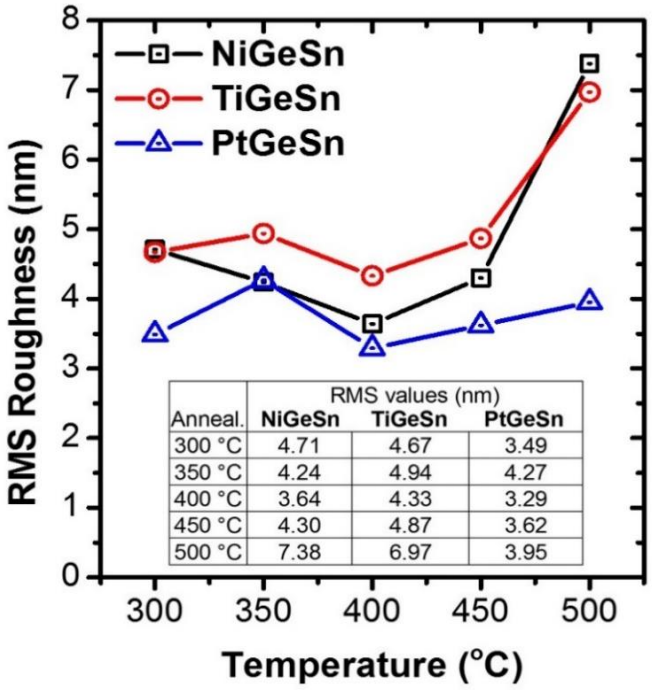


Figure 3.7: *Representative SEM images showing the continuity, or lack of, for the stanogermanides formed in this work; the left-hand column is related to the annealing at 300 °C : a) NiGeSn; c) TiGeSn; e) PtGeSn while the right-hand column refers to the annealing at 500 °C: b) NiGeSn; d) TiGeSn; f) PtGeSn.*

The thickness and the overall morphology of the metal-GeSn layers after formation at 300 °C and 500 °C were then investigated by cross-sectional TEM analysis (Fig. 3.9). As shown in Fig. 3.9.(a), 3.9.(c) and 3.9.(e) analysis confirmed that reactively grown structures, creating surface layer alloys, were formed only with Ni and Pt in this temperature range, while the Ti did not appear to react at 300 °C with the underlying GeSn, displaying a superficial layer of 20 nm.

Comparable results have been found as well for the 500 °C RTA process as highlighted in Fig. 3.9.(b), 3.9.(d) and 3.9.(f), in which the Ni and Pt form stanogermanide layers while Ti does not react with the underlying GeSn alloy.



Anneal.	RMS values (nm) NiGeSn	TiGeSn	PtGeSn
300 °C	4.71	4.67	3.49
350 °C	4.24	4.94	4.27
400 °C	3.64	4.33	3.29
450 °C	4.30	4.87	3.62
500 °C	7.38	6.97	3.95

Figure 3.8: *AFM analysis as a function of the different metal and formation temperature. As inset there is a table with all the RMS values of NiGeSn, TiGeSn and PtGeSn formed from 300 °C up to 500 °C.*

In an overall sense, the solid-state growth process proceeded towards the GeSn layer (nominal thickness of 28 nm) and for the 30 sec. anneal resulted in structures with different thickness depending on the temperature. The corresponding depth, thickness variation, grain size and stoichiometry (obtained by quantification of point EDX spectra) are summarized in Table 1.

Basically, all Ni and Pt structures were composed of crystal grains with specific size and orientation, justified by observing the variation of the diffraction contrast in the TEM images. In accordance with SEM analysis (Fig. 3.7), it was also seen that the continuity of the NiGeSn layers had degraded at 500 °C, resulting in the formation of well-defined island-type inclusions within the GeSn layer, as shown in Fig. 3.9.(b). In comparison, the PtGeSn structures appeared continuous at both temperatures.

Generally, the NiGeSn annealed at 300 °C exhibited the smoothest structure with the largest lateral size of the crystal grains as well as the best quality of the interface with the underlying $Ge_{0.92}Sn_{0.08}$.

Using EDX analysis on the Ni and Pt samples, we further confirmed that the reactive growth indeed resulted in formation of metal stanogermanides with varying stoichiometry (Table 1).

Two major characteristics of the growth process with regards to the composition were observed: i) all samples showed a reduction in the Sn content from the initial non-annealed alloy (nominally the GeSn contained 8 at.% Sn), and ii) formation of Me_x - $(GeSn)_y$ structures with a higher (GeSn) component.

The only sample that showed composition that is close to $Me_{x=1}(GeSn)_{y=1}$ is that of the NiGeSn sample formed at 300 °C. Interestingly, the TiGeSn samples (no stanogermanides formed) showed almost no reduction in the Sn content at 300 °C and only a modest reduction at 500 °C in the GeSn layer.

Sample	**Morphology**	**Thickness (nm)**	**Lateral grain size (nm)**	**Composition (line scan EDX) (averaged at.%)**
Ni(GeSn) 300 °C	continuous layer	23.5 ±0.6	165 ±9.4	Ge:53; Sn: 4; Ni: 43
Ni(GeSn) 500 °C	inclusions	50.6 ±8.9	132.5 ±34.1	Ge:65; Sn: 1.2; Ni: 33.8
Pt(GeSn) 300 °C	continuous layer	21.3 ±2.6	<10	Ge:59; Sn: 6; Pt: 33
Pt(GeSn) 500 °C	continuous layer	31.3 ±7.4	49.4 ±16.2	Ge:67; Sn:3.8; Pt: 29.2
Ti(GeSn) 300 °C	no reaction	-	-	Ge:92; Sn: 8;
Ti(GeSn) 500 °C	no reaction	-	-	Ge:94; Sn: 6;

Table 3.1: *Summary of the obtained structure for the three metals, Ni, Pt and Ti, annealed at different temperature, from 300 °C up to 500 °C. In the table will be highlighted form right to left respectively the morphology, the thickness, the lateral grain size and the composition of layer formed after the different RTA process.*

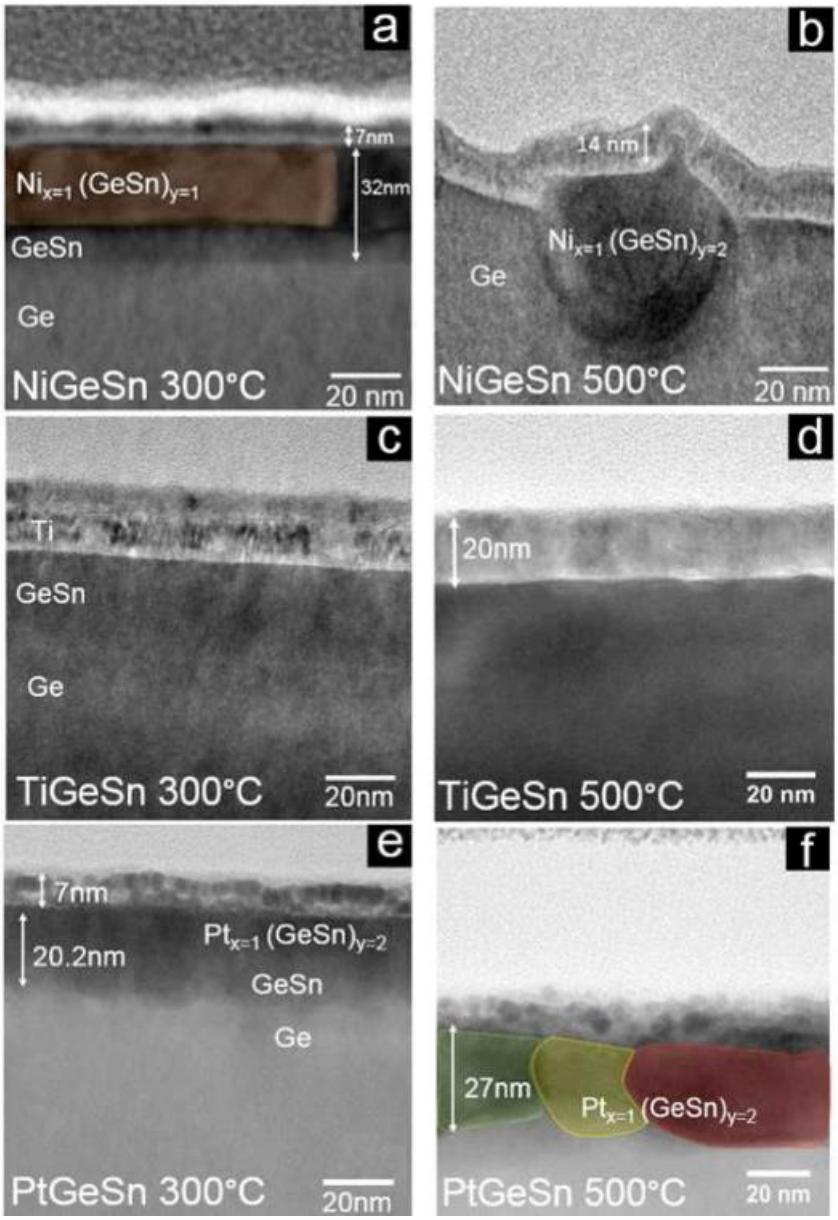


Figure 3.9 : *Representative cross section TEM images at the same magnification with related mixing depth of a) NiGeSn at 300 °C, b) NiGeSn at 500 °C, c) TiGeSn at 300 °C, d) TiGeSn at 500 °C, e) PtGeSn at 300 °C, f) PtGeSn at 500 °C. Colour coded areas depict different grains in the layer.*

To provide further details with regards to the composition of the Ni and Pt structures, EDX line scans were used to obtain compositional profiles for all samples.

Figure 3.10 points out the EDX line scan results for all the other samples analysed, NiGeSn (Fig. 3.10.(a)) and PtGeSn (Fig. 3.10.(a)) annealed at 500°C and TiGeSn annealed at 300°C (Fig. 3.10.(c)) and 500°C (Fig. 3.10.(d)). In all the circumstances the metal will be always highlighted with blue curve, Ge with red while Sn in green. Basically it is possible to note that Ti curve, in both annealing

extremes analysed (300 °C and 500 °C) Ti will never reacts with the underlying GeSn substrate. While for Ni and Pt the blue curves fit under Ge and Sn profiles clearly indicating the reaction among them. Therefore in this analysis, despite the annealing window selected was enough to show/start the formation of stanogermanide layer, only Ni and Pt shows reaction with the underlying GeSn substrate.

Figure 3.11 provides an example of the analysis performed for two samples, Ni and Pt annealed at 300 °C. From the Fig. 3.11 it can be seen that the Sn content (both averaged values across the stanogermanide layer and point measurements within the layer) decreased to about 4.0 and 6.0 at.% for the Ni and Pt samples, correspondingly. The values decreased further down to 1.2 and 3.8 at.% when the samples were annealed at 500 °C. The Sn content for the non-annealed sample (Fig. 3.11, blank spec); measured under similar EDX conditions showed a Sn content of about 8.0 at.%; perfectly in accordance with the nominal composition for the $Ge_{0.92}Sn_{0.08}$ alloy.

Looking at the Sn EDX profile in the underlying Ge substrate and indeed at the point measurement (Fig.3.11, spec 3) at a distance of about 100 nm away from the stanogermanide layer, the Sn signal is within the background noise, which is at the limit-of-the detection of the measurement (about 0.1 at.%). It is worth to mention that the compositional profiles for all Ni_x-$(GeSn)_y$ and Pt_x-$(GeSn)_y$ structures were relatively uniform both across (perpendicular) and along (parallel) the layer surface. Across different grains no major variation in the composition was observed, which can indicate formation of different stanogermanide phases within the layers

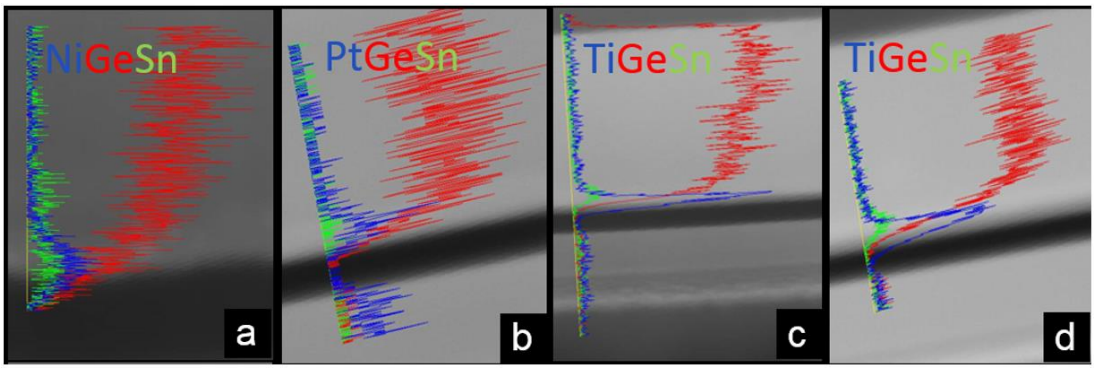


Figure 3.10: *EDX linescan for NiGeSn (a) and PtGeSn (b) sample annealed at 500 °C. In addition both TiGeSn samples respectively annealed at 300 °C (c) and 500 °C (d). The blue, red and green curves will always show respectively metal, Ge and Sn.*

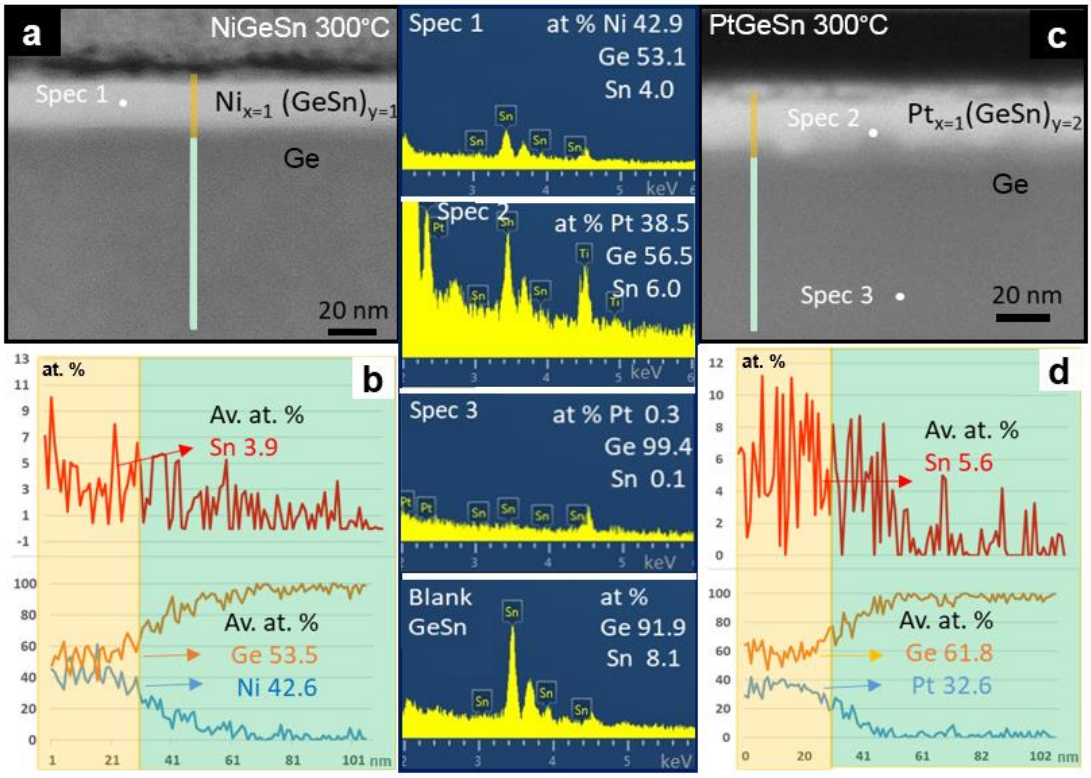


Figure 3.11: *STEM imaging and corresponding EDX line scans for the regions marked with brown and blue measured for the Ni(GeSn) sample (a and b), and Pt(GeSn) sample (c and d), both annealed at 300 °C. Middle column shows EDX point spectra from the marked regions together with the blank GeSn spectrum. Corresponding quant data averaged across the region marked in brown and from the point spectra are also shown.*

3.4.2.3 Detailed Lattice analysis

To further confirm the corresponding stanogermanide phases formed a lattice resolution TEM imaging has been performed on several different grains within Ni and Pt stanogermanide layers. Investigation was focused on Ni and Pt samples due to the lack of reaction of Ti. Fig. 3.12.(a) shows a lattice resolution TEM image of one of the crystal grains for the NiGeSn sample formed at 300 °C and corresponding *Fast Fourier Transformation (FFT)* of a selected area from the image. For this grain, the crystal interface with the underlying GeSn appeared abrupt with (111) sets of planes of the $Ni_{x=1}(GeSn)_{y=1}$ phase, at 3.7 degrees misalignment with the (111) set of planes of the GeSn. In comparison, the lattice resolution images for the PtGeSn sample formed at 300 °C showed a variation of crystal orientations of very small (sub-10 nm) crystallites.

This is indicated by the FFT pattern shown on Fig. 3.12.(b) whereby all reflections are arranged in diffraction rings. The most common reflections were with

d-spacing of about 3.2 and 2.7 Å that are indicative for existence of (200) and (210) set of planes of the orthorhombic $Pt_{x=1}(GeSn)_{y=2}$ phase. Additional analysis of other crystal grains from the two samples also suggested the appearance of the $Ni_{x=1}(GeSn)_{y=1}$ and $Pt_{x=1}(GeSn)_{y=2}$ phases. In the case of the PtGeSn sample formed at 500 °C, cross-sectional TEM showed the formation of well-developed grains; the lattice resolution image with the corresponding FFT for one such grain is shown on Fig. 3.12.(d). In the case of a NiGeSn sample annealed at 500 °C, a more distinct change in the morphology compared with a NiGeSn sample formed at 300 °C, *e.g.* formation of island-type inclusions, was observed.

The lattice resolution TEM imaging shows in Fig. 3.12.(c) suggested the appearance of $Ni_{x=1}(GeSn)_{y=2}$ phase, evidence by a d-spacing of about 2.7 Å, that corresponds to (400) set of planes of the $Ni_{x=1}(GeSn)_{y=2}$ phase. It is important to note that nickel stanogermanides with higher Ge content are not part of the binary phase diagram. However, we and others have shown that a meta-stable $NiGe_2$ phase exists and it can be produced by using annealing conditions away from equilibrium, as for example laser annealing. Herein has been observed the formation of unusual $Ni_{x=1}(GeSn)_{y=2}$ stanogermanide with relatively low Sn content.

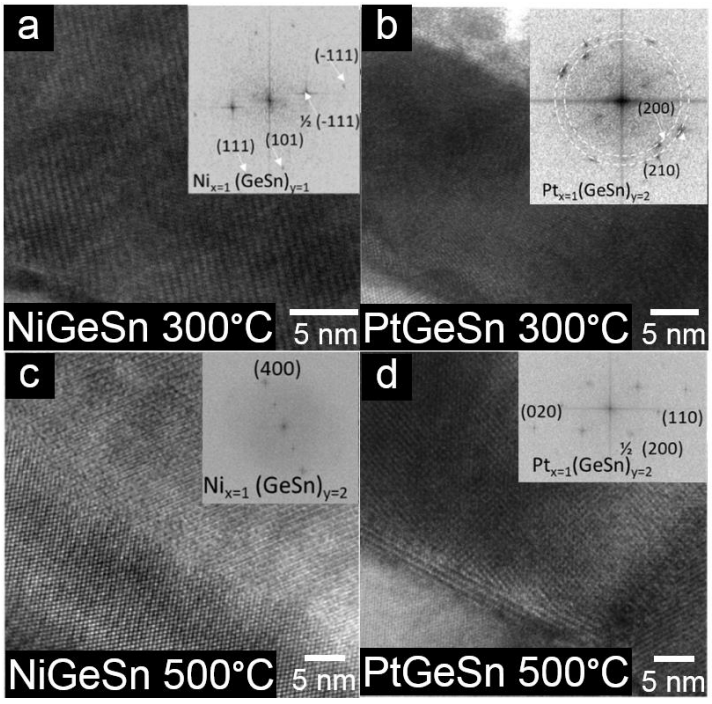


Figure 3.12: *Lattice resolution TEM images of NiGeSn sample formed at 300 °C (a) and 500°C (c), depicting individual crystal grain and of PtGeSn sample formed at 300 °C (b) and 500 °C (d) featuring small crystallites with random orientations. Insets are corresponding FFTs.*

3.5 Contacts made by Laser Thermal Annealing

Nowadays, the emergence of three dimensional devices and architectures in the nanoscale range lead to the rearrangement of both doping and annealing schemes. Although all the previous contact formation reports in literature have been achieved using an RTA technique, recently the *laser thermal annealing* (LTA) methodology showed an enhanced thermal budget control leading to an even increasing interest for the formation of nanometer devices. Essentially LTA is able to precisely control the annealing process localizing the laser spot on a precise area without damage the surrounding regions [209].

In the recent past, specifically for Ge, LTA has been used in multiple works showing impressive results [210-213] even if for $Ge_{1-x}Sn_x$ so far LTA has been used only to study the epi-layer growth [97, 207]. Therefore as the $Ge_{1-x}Sn_x$ contact formation is still relatively unexplored, this work aims to investigate the contact formation using LTA.

3.5.1 Experimental procedure

Fig. 3.13 show the basic sample composition, process flow and variables considered in the LTA experiment. The starting material comprises of a nominally un-doped epi-layer of $Ge_{0.91}Sn_{0.09}$ (1.2 µm thick) on a nominally un-doped virtual substrate layer of Ge (700 nm thick). Samples have been grown by an MBE process by IQE partner and schematic illustration of the basic structure illustration is reported in Figure 3.13.(a).

The experimental procedure previously reported in Section 3.4.1 has been repeated on the new batch of substrates, therefore $Ge_{0.91}Sn_{0.09}$ surfaces were firstly cleaned using a standard recipe already reported in Section 3.4.1 and after a layer of 10 nm of either Ni, Ti or Pt was deposited on the samples using the FC2000 electron beam evaporator using the same pressure and deposition rate stated previously for the precedent experiment.

Subsequently the samples underwent to laser annealing process using a Compex PRO201F. An area of 5×5 mm^2 was subjected to 22 ns laser annealed using a Krypton Fluoride (KrF) source with a wavelength of 248 nm. The density power range used for the annealing ranges from 100 to 500 mJ/cm^2 in order to have a wide analysis window.

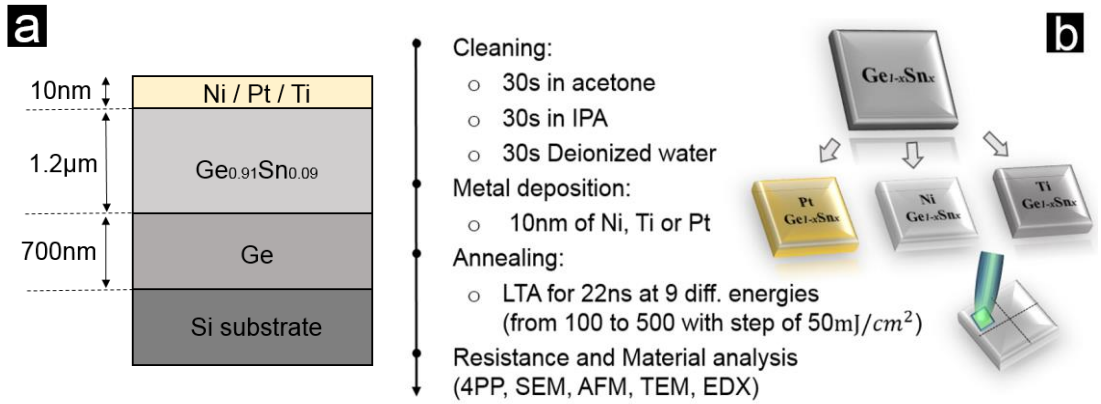


Figure 3.13:*(a)Illustrative structure composition (b)Schematic representation of the stanogermanide process flow and variables considered in this work.*

To have a comprehensive and comparative study, all the samples have been electrically and morphologically characterized as a function of different laser energy densities range (100–500 mJ/cm^2) and metals (Ni, Pt and Ti) used. Concerning the material characterization several analysis optical as optical microscope, SEM, AFM, XTEM and EDX have been performed on the samples to inspect the surface and the alloy features; while as a regards of the electrical characterization 4PP measurement was carried out using a manual four point resistivity probing station as before.

3.5.2 Results and discussion

Following an accurate study on contacts formed by LTA is reported; the samples have undergone to electrical and morphological characterization with the aim to outline the most promising stanogermanide candidate. In addition all the data obtained have been compared with RTA counterpart to show strengths and weaknesses of the two different annealing approaches.

3.5.2.1 Electrical characterization

Figure 3.14.a displays the sheet resistance measured for $Ge_{0.91}Sn_{0.09}$ as a function of the different metals used (Ni, Pt or Ti). In literature reports, although using RTA as the formation anneal, Ni showed the best performance for Ge[203] and $Ge_{1-x}Sn_x$[214], while in this work within the LTA power range investigated PtGeSn shows both the lowest and the highest sheet resistance values.

According to the sheet resistance data achieved an interesting decreasing trend as a function of the laser density increase has been observed. The downward tendency might be explained considering the stanogermanide layer thickness

growth. Indeed, as the energy density of the laser increases the growth of the melted section cause a material sheet resistance reduction.

Within the energy density range investigated (100-500 mJ/cm^2) the smallest and the largest sheet resistance achieved are respectively 11.45 Ω/sq and 86.55 Ω/sq. Ni and Pt, highlighted respectively with black and red curves in Figure 3.14.(a) show roughly a similar trend; even if Pt has a more pronounced deflection up to 350 mJ/cm^2 compared to Ni. Conversely for Ti, displayed in green, greater resistance values have been obtained compared with Ni and Pt counterparts maybe due to the possible O incorporation during the alloy formation as Ti as a strong tendency to oxidise when exposed to the ambient.

Compared with previous data obtained by RTA [214] the outcomes achieved by LTA shows less variability. Figure 3.14.b illustrates the sheet resistance comparison with our precedent work; in the graph highlighted in black there are the sheet resistance values extracted using RTA, while in red there are the data related to LTA. Values confined in the blue box in Figure 3.14.b, show the small variability when compared with RTA.

The LTA energy density defines the melt depth therefore we hypothesize that the tiny fluctuation reached with LTA is strictly related to the LTA ability to melt respectively completely and partially the metal and the underlying $Ge_{0.91}Sn_{0.09}$ semiconductor surface.

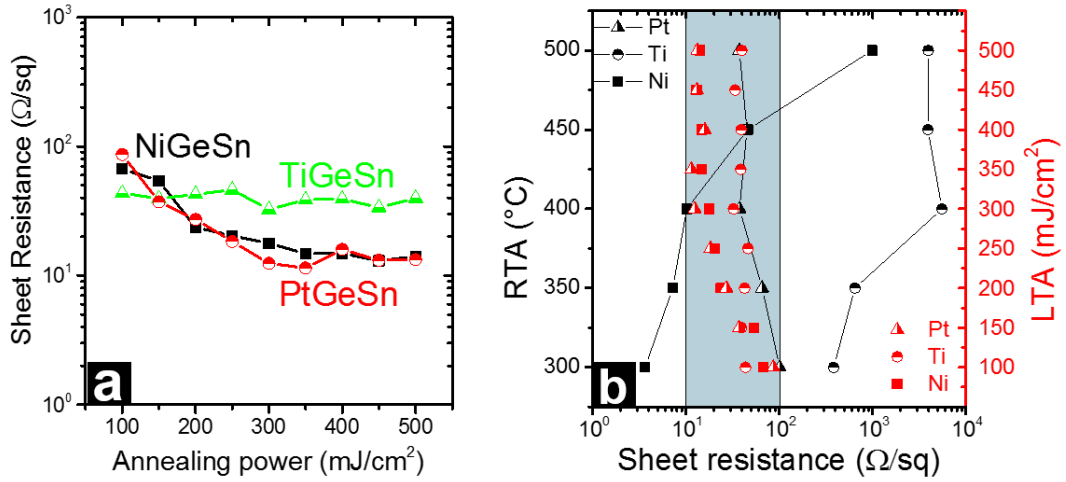


Figure 3.14: *(a) Sheet resistance for Ni, Ti and Pt stanogermanides as a function of the energy density using laser thermal annealing. (b)Direct sheet resistance comparison between the RTA and LTA technique as a function of three different metals, Ni, Ti and Pt, Conventional RTA data are highlighted with black and while LTA with red.*

Data achieved in this work have a similar order of magnitude to the results found so far in literature using RTA [195, 200, 214]; therefore LTA annealing is a promising solution to improve the contact resistance value. Nevertheless further studies are necessary to further characterize the solid epitaxial regrowth process as a function of the different energy and metals used.

3.5.2.2 Morphological analysis

To characterize the surface quality all the samples have been firstly undergone at optical microscope and SEM investigation. The optical microscope analysis shows clearly a surface transformation via a colour change between the section hit by the laser beam and the zone without the LTA treatment.

Conversely Fig. 3.15 shows SEM images as a function of LTA laser density range (100-500 mJ/cm^2). An interesting trend for all the metals has been outlined; namely as the laser density increases the surface starts to become smoother. Figs. 3.15.(a), 3.15.(d) and 3.15.(g) describe respectively NiGeSn, PtGeSn and TiGeSn annealed at 100 mJ/cm^2; Ni and Ti shows high amount of particle/residue on the surface, while Pt shows the tendency to cluster forming small and isolated islands. For Ni and Pt the amount of particle on the surface clearly decreases as the power increases (Fig.3.15.(b), Fig.3.15.(e), Fig.3.15.(c) and Fig.3.15.(f)). In addition at 500 mJ/cm^2 Ni shows smooth surface while the Pt case shows a discontinuous structure. Conversely for Ti, the isolated islands starts to agglomerate without forming a continuous layer (Fig 3.15.(h) and Fig.3.15.(i)) that jeopardize the final result.

Therefore according to the results obtained, LTA samples at high energy density show greater tendency to have surface texture or to agglomerate compared with RTA counterpart. Overall Pt and Ti seem to be more sensitive elements for stanogermanide film agglomeration compared with Ni.

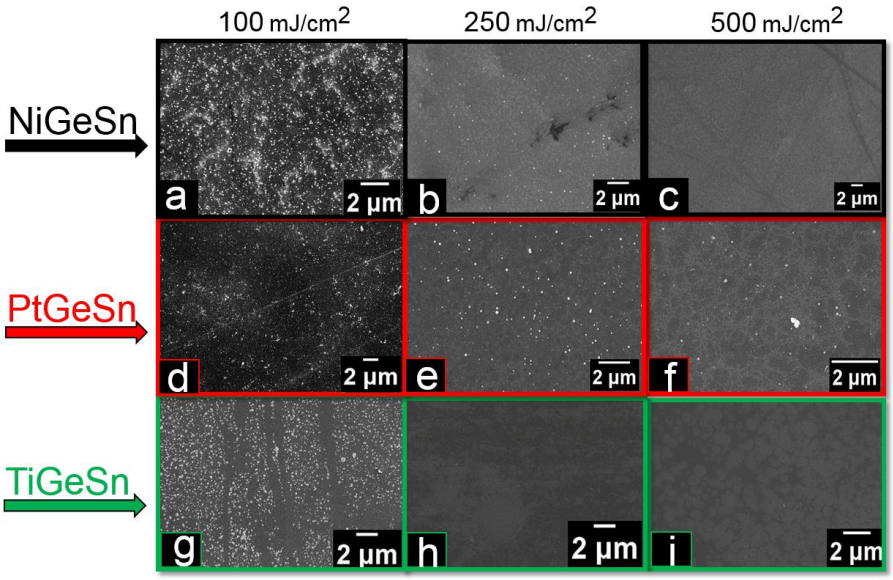


Figure 3.15: *Representative SEM images as a function of the different material and laser density formation. Black red and green curves represent respectively NiGeSn, PtGeSn and TiGeSn. First column on the left point out the value obtained for 100mJ/cm^2, central column at 250mJ/cm^2 and right column the ones obtained at 500mJ/cm^2.*

Afterward, all the samples have been investigated by AFM technique considering a scan area of 5×5 µm. Fig. 3.16 shows the results achieved for the different metals as a function of the laser density used; data has been extracted analysing the central portion of the laser annealed section, avoiding edge effects. The highest *Root Mean Square* (RMS) data of 44nm has been reported for NiGeSn and PtGeSn at 100 mJ/cm^2; while the lowest data of 3.6 5nm has been reported for Pt at 450 mJ/cm^2. Overall according to the SEM analysis done, as the energy density increases, a remarkable smooth surface layer has been achieved. Moreover each metal outlines different operational window essentially as the power involved in the process increases, the RMS values tend to stabilize leading to a plateau after 250 mJ/cm^2.

Table 3.2 summarize the RMS values as a function of the different annealing temperatures, laser energy densities and metal compositions. In addition to compare directly the two different annealing methodologies Table 3.2 reports also the RMS data achieved in previous work using RTA [214]. Examining the AFM data it is noteworthy that LTA has a remarkable higher fluctuation compared with RTA; furthermore two opposing trends have been reported. RTA analysis shows that the roughness increases as the annealing temperature rises up, conversely LTA approach shows that the roughness decreases as the laser power increases.

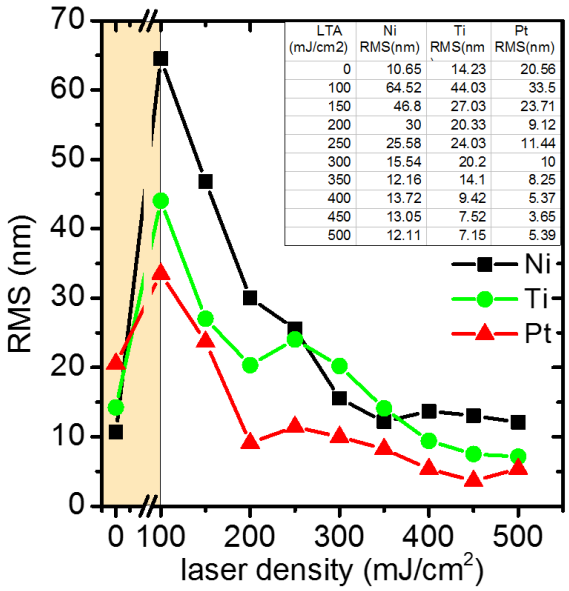


Figure 3.16: *AFM data as a function of the different metal and laser density used. Scatter data point with black, red and green respectively represent Ni, Ti and Pt RMS value while as inset there is the table with all the RMS data obtained*

NiGeSn		**PtGeSn**		**TiGeSn**	
RTA(nm)	LTA(nm)	RTA(nm)	LTA(nm)	RTA(nm)	LTA(nm)
4.71 *(300°C)*	**44.52** *(100mJ/cm²)*	**4.67** *(300°C)*	**44.03** *(100mJ/cm²)*	**3.49** *(300°C)*	**33.5** *(100mJ/cm²)*
4.24 *(350°C)*	**36.80** *(150mJ/cm²)*	**4.94** *(350°C)*	**27.03** *(150mJ/cm²)*	**4.27** *(350°C)*	**23.71** *(150mJ/cm²)*
3.64 *(400°C)*	**30.00** *(200mJ/cm²)*	**4.33** *(400°C)*	**9.12** *(200mJ/cm²)*	**3.29** *(400°C)*	**20.33** *(200mJ/cm²)*
4.30 *(450°C)*	**25.58** *(250mJ/cm²)*	**4.87** *(450°C)*	**11.44** *(250mJ/cm²)*	**3.62** *(450°C)*	**24.03** *(250mJ/cm²)*
7.38 *(500°C)*	**15.54** *(300mJ/cm²)*	**6.97** *(500°C)*	**10.00** *(300mJ/cm²)*	**3.95** *(500°C)*	**20.20** *(300mJ/cm²)*
------	**12.16** *(350mJ/cm²)*	------	**8.25** *(350mJ/cm²)*	------	**14.10** *(350mJ/cm²)*
------	**13.72** *(400mJ/cm²)*	------	**5.37** *(400mJ/cm²)*	------	**9.43** *(400mJ/cm²)*
------	**13.05** *(450mJ/cm²)*	------	**3.65** *(450mJ/cm²)*	------	**7.52** *(450mJ/cm²)*
------	**12.1** *(500mJ/cm²)*	------	**5.39** *(500mJ/cm²)*	------	**7.15** *(500mJ/cm²)*

Table 3.2: *AFM data for two different annealing approaches as a function of the different metals. Listed are the RMS values of NiGeSn, TiGeSn and PtGeSn formed from 300 °C up to 500 °C for RTA while highlighted in black, red and green the values for LTA formed from 100 mJ/cm² up to 500 mJ/cm².*

Subsequently selected samples were examined by XTEM analysis pointing out an interesting trend as a function of the laser energy densities. The stanogermanide layer thickness tend to grow as the laser energy densities raise up. Nevertheless the trend is not homogeneous among the different material because each metal tend to react (absorb or reflect) in a different way within the energy range take into account.

Ni and Pt stanogermanide layers are inclined to degrade above 250 mJ/cm^2 while Ti shows Sn segregation above 200 mJ/cm^2. Therefore according to the data shown each metal respectively form layer with different thickness; NiGeSn (70nm – 420nm); PtGeSn (50nm to 280nm) TiGeSn (150nm -700nm). If from one perspective the thickness improvement leads to smaller sheet resistance from the other side, as undesirable effect, the samples show really drastic Sn segregation and defect formation within the layer formed.

Figure 3.17 shows the stanogermanide formation process for NiGeSn samples as a function of laser energy density. A lot of works was devoted to improve the knowledge on the liquid to solid phase transformation and the impurity behaviour in the most common group IV semiconductor [215]. Nevertheless for $Ge_{1-x}Sn_x$ this aspect has not been completely analysed yet due to the physical and chemical constraints that severely limit the experiments[131, 216].

Since the liquid-solid regrowth mechanism govern the recrystallisation process, the laser density energy control is important to avoid the formation of defects, Sn segregation and misfit dislocation within the stanogermanide layer. Basically as for RTA, also for LTA, the thermal budget control is essential to avoid the Sn cluster formation[217], the Sn surface segregation[207]. Therefore the energy density range and the reflectivity have to be carefully inspected to successfully fabricate superior electronic or photonics devices.

In addition from XTEM analysis was found that, independent of the metal used, when the LTA exceeded a threshold energy density, the stanogermanide layer tended to form two different layers, one with a vertical pillar structure and one smooth layer near the underlying $Ge_{0.91}Sn_{0.09}$. The structure obtained was in contrast with the results obtained by RTA techniques where a relatively homogeneous polycrystalline layer was observed. In literature it has been suggested that Ge undergoes amorphization and nanocrystallization under extreme thermal shock,

nevertheless as the laser energy increases it can generate high stress in the melted layer, developing cracks, planar defects and grains.[218].

In the samples analysed here, the misfit dislocations were generated between the Ge and GeSn layer due to the difference in the thermal expansion coefficients for the two materials. Furthermore, increasing the thermal budget, Sn tended to form clusters and to segregate toward the layer surface due to the low melting point of Sn.[219]

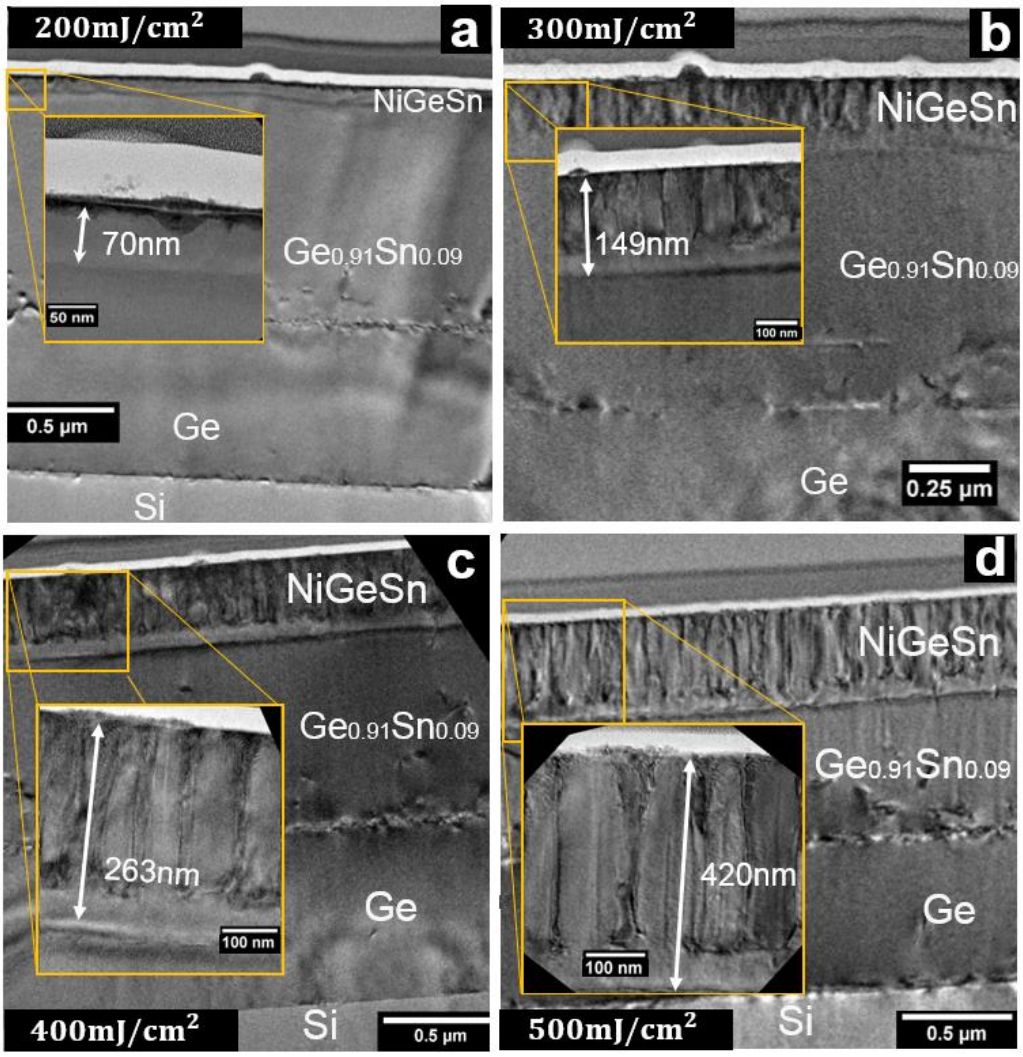


Figure 3.17: *TEM inspection of NiGeSn samples undergone to different LTA energy density. In all the images a zoom on the melting section has been reported as inset to outline the formation of different thickness stanogermanide layer as a function of the energy used. (a)200mJ/cm^2, (b)300mJ/cm^2, (c)400mJ/cm^2 , (d)500mJ/cm^2*

Finally, to analyse the layer composition and the Sn dispersion, EDX analysis has been performed on the NiGeSn sample annealed at 500 mJ/cm^2, shown in Fig. 3.18. The EDX investigation along the cross section revealed that a Sn layer

was localized in vertical columns or pillars in the upper part of the $Ge_{0.91}Sn_{0.09}$ layer leading to the decrease of Sn content in the middle of each cell (areas between the vertical columns of Sn). The Ni map confirm the formation of stanogermanide layer on top of the wafer.

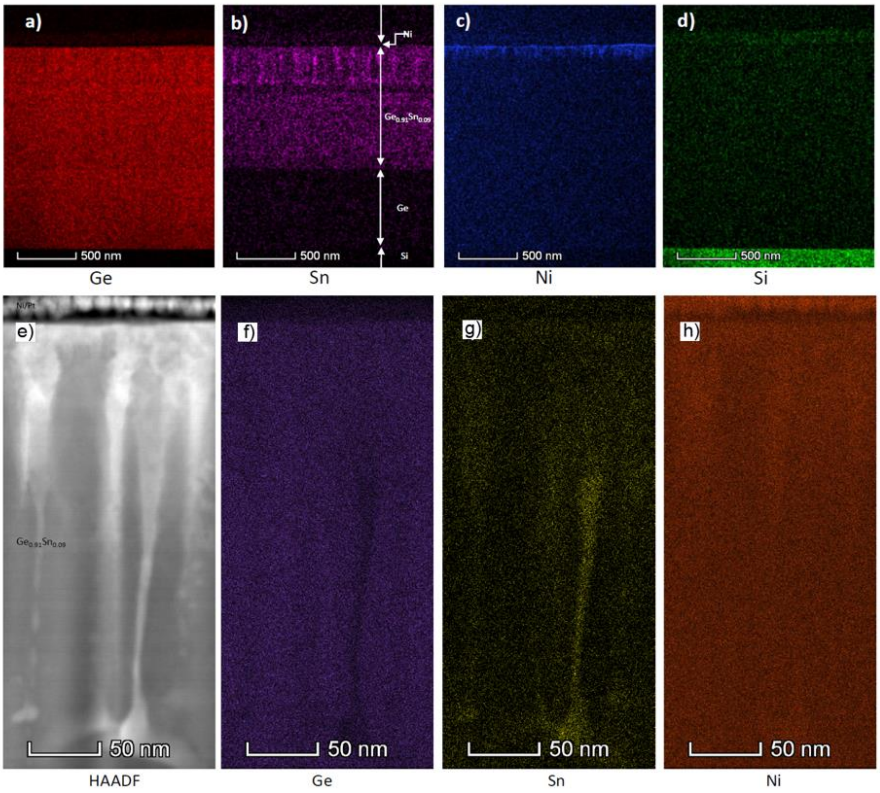


Figure 3.18*: EDX inspection for NiGeSn samples annealed at 500mJ/cm2; the maps (a to d) represent the material dispersion along the lamellae; while the maps (e to h) show respectively the HAADF of Ge, Sn and Ni.*

The high angle annular dark filed (HAADF) image in Fig. 3.18 layer shows the column formation as reported in Fig. 3.17. EDX maps (Figs. 3.18b-d) reveal the depletion of Ge in the column due to Sn accumulation, while Ni distribution is rather uniform, with a very slight increase on the top (e.g., in the Ni/Pt layer) and also in the $Ge_{0.91}Sn_{0.09}$ layer, near the Sn column. Although conclusion of the Ni omnipresence cannot be drawn definitely because the Ni EDX peak is close to the Cu peak in EDX analysis; and the latter can be seen everywhere due to the TEM sample being on a Cu grid.

White et al.[220] reported an early work of supersaturation effects in As and Sb doped Si. Subsequently Narayan et al.[221] described a model for cell formation in Sb-Si and In-Si alloys. Experimentally they observed vertical columns of Sb in sample cross-sections similar to those here. In essence as the supersaturated GeSn

alloy (Sn at 9 %) is melted locally by the LTA, a liquid-solid interface is formed and, as the sample cools, then sweeps to the surface using the underlying crystal as a template. Under certain conditions the material system becomes unstable, due to the distribution coefficients of Sn and Ni in Ge, the melt depth, and the velocity of recrystallisation, where a Sn supersaturation threshold is achieved, however the excess Sn is expelled from the growing layer, in this case laterally, thus forming the vertical Sn features.

3.6 Conclusion

In this chapter a comprehensive stanogermanide contact investigation has been performed on two different $Ge_{1-x}Sn_x$ alloy composition near the predicted direct B_g onset (8%). The two experiments have been made with the aim to outline the most promising metal material and annealing technique for future contact formation. The quality of the stanogermanide contacts was inspected as a function of different energy densities and temperature and systematically compared with the counterpart.

As a regards the electrical characterization, LTA presents a smaller resistivity fluctuation compared to the RTA; even if the lower sheet resistance has been obtained with the most common RTA technology. As a function of the morphological characterization both RTA and LTA tend to deteriorate the sample morphology as respectively the laser energy or the temperature increase. XTEM and EDX investigation for LTA samples allow to characterize and define the correct operational windows for three different metals (Ni, Pt, and Ti) according to the onset of Sn segregation and layer defects. Although LTA seems to be promising solution for the formation of future device contacts further calibration process has to be performed on the alloy due to its ability to withstand limited thermal budget.

Additional investigation are required to improve the knowledge on the solid regrowth epitaxy process, the defects formation and the Sn segregation, because they might severely influence the contact performance. Therefore it is imperative explore new solutions to further optimize the performance in accordance with the alloy feature.

4|Doping on $Ge_{1-x}Sn_x$ devices

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4 | Doping on $Ge_{1-x}Sn_x$ devices

4.1 Introduction

An essential aspect for future photonic and nano-electronic devices is the material doping control with the formation of shallow junctions without defects. Since, for lasing and FET applications, typical n- and p-type junctions are essential, a thorough doping investigation and characterization is needed to move towards smaller device dimensions. Nevertheless the physical material limitations of $Ge_{1-x}Sn_x$, such as the low thermal stability and the tendency for Sn to segregate at high temperatures, represent a barrier to overcome for $Ge_{1-x}Sn_x$.

Then in this chapter, firstly a state-of-the-art overview on doping techniques of Ge and $Ge_{1-x}Sn_x$ is presented. Subsequently a simulation investigation through the ion implantation modelling software (*Stopping and Range of Ions in Matter (SRIM))* is shown, which is then followed by an experimental doping study with two different approaches on $Ge_{0.91}Sn_{0.09}$ substrates. Experiments have been developed during an internship at *Applied Materials (AMAT)* in Gloucester MA, USA.

4.2 Theory/Background

With respect to semiconductors, doping corresponds to the intentional introduction of impurities into an intrinsic material for the purpose of modulating its electrical and optical behaviour. For Group IV semiconductors such as *Silicon (Si)* and *Germanium (Ge)* the most common dopants used to alter the electrical behaviour are (1) acceptors from Group III or (2) donors from Group V.

To conceptually understand the doping process, a typical 2D Si crystal representation is drawn in Fig. 4.1.a. Si belongs to group IV of the periodic table, then each Si atom has respectively 4 valence electrons. So, if two or more atoms aggregate they tend to share valence electrons with neighbours forming covalent bonds, respectively represented in the image with two black dots between atoms, to respect the octet rule. Then, without any kind of external excitement, configuration (a) does not support the formation of free electrons able to conduct the current. Though considering thermal energy, the covalent bond might break itself creating a conduction electron able to move within the crystal and a void behind in the crystal lattice called hole which in turn can create an alternative current flow.

Conversely, as shown in Fig. 4.1.(b) when a group IV semiconductor (Si in the

example shown) is doped with group V elements, such as *Arsenic (As)*, the electronic configuration changes because the inserted atom, used to dope, has 5 valence electrons. Therefore four of them, respectively highlighted in red, are used to form covalent bonds with neighbours; while the fifth electron is able to move if subjected to external force, as an electric field. Then, the impurities belonging to the group V are called donors because they donate electrons and the final result is defined as n-type semiconductor.

Alternatively as shown in Fig. 4.1.(c), when a group III impurity, such as *Boron (B)*, is introduced into Si, the impurity is able to accept an electron from the close atoms to form covalent bond because it presents a hole in the electronic configuration. Nevertheless the electron movement create holes behind and allow the formation of current, therefore such dopants are typically known as acceptors and the final result is called p-type semiconductor.

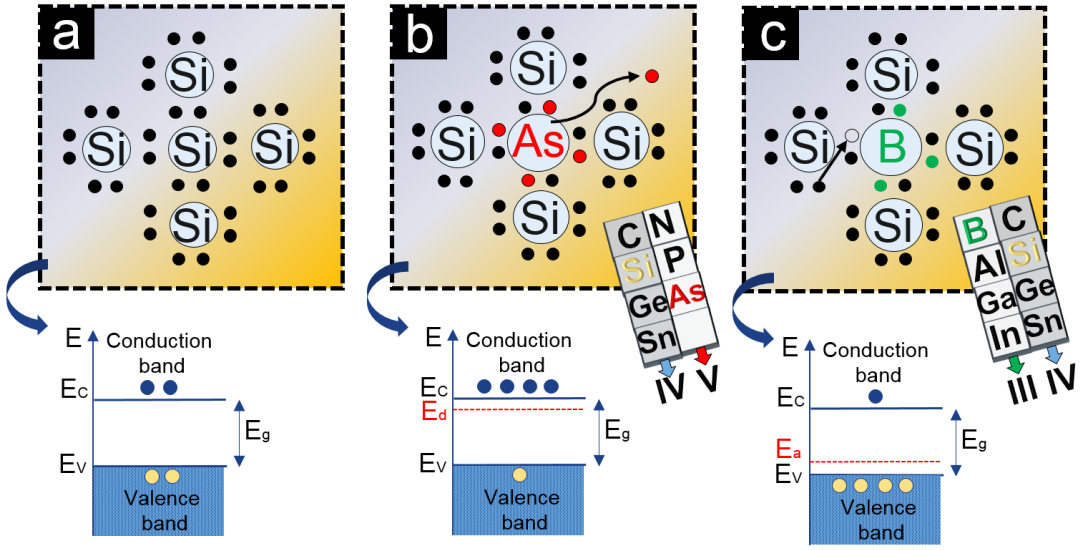


Figure 4.1: *Schematic representation for a group IV semiconductor with relative band structure configuration. (a) shows Si un-doped material, (b) n-type Si doped with As while (c) p-type Si doped with B.*

Furthermore, without going into too much detail, because these aspects have been already widely discussed in literature [24], to have a more comprehensive investigation the energy bands concepts such as the *VB, CB, energy gap (Eg)* should be considered. Basically the introduction of doping into the crystal allows the formation of energy states in the CB and VB respectively for donor and acceptor impurities, as shown in Figure 4.1 below each 2D representation. The band alteration in turn alters the carrier concentration affecting the electrical properties of

the semiconductor. A full comprehension of the dopant behaviour is fundamental to successfully manage the doping process even if the representation shown here is an ideal case, while in reality there are a lot of variables to be taken into account.

4.3 Doping and annealing methodologies

The introduction of impurities into a semiconductor material essentially can be performed by diffusion and it consists in a transportation of atoms from areas with higher concentration to areas of lower concentration. Movement is controlled by the interaction between the impurity and the crystal lattice point-defects such as vacancy, self-interstitial or impurity-interstitial pair [222]. The process is governed by several factors such as the gradient concentration, temperature and semiconductor crystallographic orientation, even if the mechanism is based on two key steps (1) the pre-deposition, where a large quantity of the dopant is deposited on the surface and the (2) drive-in, where the dopant is driven to the required depth according to the Ficks law [24, 223].

Among all the techniques reported in semiconductor world, ion implantation is the most conventional methodology used to dope the materials [224]. In the ion implant process, dopant ions are accelerated onto the wafer, but in contrast to the in-diffusion process the particles do not penetrate into the crystal due to their own movements, by diffusion, but due to their imparted velocity. Then the process causes a high amount of damage to the lattice, so to recover it and to activate the dopants, annealing steps are fundamental [24]. In the past several ion implantation variations were created with the intention to improve the process, including cryogenic or hot implants [225] or the co-implants process that provides benefits due to the interactions of *Carbon (C)*, *Fluorine (F)* and *Nitrogen (N)* with interstitials and vacancies point-defects [226]. Plasma doping in another innovative methodology highly used in Silicon technologies that enables conformal doping profiles on 3D structures, fundamental for FinFET devices [227, 228]; furthermore the *molecular monolayer doping (MLD)* process has been proposed as a novel doping methodology usable for aggressively scaled semiconductor due to its atomic accuracy [229, 230].

After the dopant impurity incorporation process, a heat treatment called annealing is performed to activate the dopants and remove the damage from the crystal lattice. Numerous annealing methodologies have been explored and

investigated for group IV semiconductors. Although each annealing technique has its distinctiveness, the substantial difference lies in the different thermal budget profiles and time dependences; for instance *solid phase epitaxial regrowth (SPER)* executes an annealing treatment in the range of minutes with temperatures around 600 °C [231], low temperature *microwave anneal (MWA)* in the range of seconds-minutes achieving temperatures of 500 °C [232], *RTA* for few seconds with temperature ranging from 300 °C to 1200 °C [233], *flash lamp anneal (FLA)* operates for few millisecond with temperature up to 1200 °C [233] while *LTA* carry out annealing treatment for nano-micro second providing temperatures higher than 2000°C in a localized area [210].

Table 4.1 summarises the most common doping and annealing techniques used for group IV semiconductors. Nevertheless further inspection and experiments are required on any novel semiconductor material because it is imperative to achieve and understand ultra-shallow junction formation required in emerging devices.

Process	Technique
Doping	Ion implantation
	Cryogenic implantation
	Hot implant
	Co-Implants
	Deposition
	Plasma doping
	Molecular layer doping

→

Process	Technique
Annealing	SPER
	Microwave anneal
	Rapid thermal anneal
	Spike Annealing
	Flash lamp anneal
	Laser thermal anneal

Table 4.1 *Most common doping and annealing techniques used on group IV semiconductors. Highlighted in red are the main processes explored in the experimental section of this Chapter.*

4.4 State-of-the-art for $Ge_{1-x}Sn_x$

The progressive evolution of FET technology over the last decades required a highly accurate doping control to achieve ultra-shallow doping regions. So, breakthrough solutions exploiting new materials such as Ge and its alloy [63, 185] or innovative doping methodologies [230] with specialized thermal processes [234, 235] have been proposed. Although Si doping processes mostly rely on ion implantation there remains a lack of specific knowledge in relation to on Ge and its

alloys. Most of the works reported to date on Ge and GeSn encompasses thin body devices, such as multi-gate FETs and FinFETs, fabricated with relatively long channel. Though recently few reports show the ability to fabricate p-MOS Ge devices and FinFET respectively with a gate length of 30 nm [236] and 40 nm [237, 238]. Furthermore, Ikeda et al fabricated and benchmarked p-type Ge NWs FET with width of 20 nm, opening new glimpses in Ge ultra-scaled technology.

In most of the aforementioned applications, dopant impurities were introduced into Ge substrates using the ion implantation process, and an extensive literature review on Ge have been proposed in Ref. [226]. Overall to date, to the best of our knowledge the shallowest profile for Ge n-type dopants has been achieved in [239, 240] while for p-type dopants has been produced by [241]. Another interesting point so far is represented by the limited Ge defect-engineering literature reported to date. Experimental work of hot/cold implants applied to Ge are difficult to find while the theory of co-implant for Ge has been described in great detail in the following work [242] and some experimental results have been reported in [243-245].

As regards the annealing, the most common techniques used so far are the *furnace annealing (FA)* and RTA; although recently reports show the ability to use LTA on Ge highlighting the improvement reached melting the material [210, 213, 239, 246, 247]. However considering the importance of the topic, further work is still needed in this area to generate innovative solutions.

Therefore according to the improvement obtained in the last years on theoretical understanding of Ge, preliminary investigations on $Ge_{1-x}Sn_x$ alloys have been proposed due to its characteristics; though considering the material limitations such as the low solid solubility and the limitation on thermal budget, the doping options for $Ge_{1-x}Sn_x$ are challenging. Essentially $Ge_{1-x}Sn_x$ is a metastable material that has a limited thermal budget due to Sn diffusion, β-Sn precipitation and Sn segregation [216, 248]; furthermore the limited thermal budget does not allow also the recrystallization process needed to repair the implantation damage.

Despite the increasing number of articles on $Ge_{1-x}Sn_x$ devices, the doping process for this innovative material is still under investigation because the annealing procedure, necessary to activate the dopant and recover the crystal damage, has to be handled with care.

Nevertheless, taking into account the thermal budget limitations, only few experiments report the fabrication of long gate channel devices [108, 129, 249]. In addition Tran et al. reported novel results on ion implantation at cryogenic temperatures followed by millisecond FLA [121].

Conversely "in situ" doping experiments have been proposed as a suitable way to achieve n and p- type doping with high activation level and high crystalline quality [87, 96] even if it is challenging to obtain typical MOSFET structures using such techniques. Therefore the doping debate for $Ge_{1-x}Sn_x$ alloy is still open, and further experiments and optimization are required before identifying the ideal doping process, in order to reduce the structural and surface defects that severely limit the electrical performance of sub-100 nm devices.

4.5 SRIM simulations

In this Section, modelling of the ion implantation process is investigated. SRIM modelling software has been used to study ion implantation physics in order to have both a better understanding and a prediction of the results developed in AMAT. SRIM is a famous modelling software developed by F. Ziegler and J.P. Biersack [250, 251] which allows the study of ion interactions with matter and the damage produced based on the noteworthy program *transport of ions in matter (TRIM)*. Nevertheless before presenting the simulation results, an overview on some basic concepts frequently used in the software are introduced in order to have a clear picture of the situation.

4.5.1 Definitions

For many years ion implantation was source of extensive and comprehensive study [252] therefore below is a general summary on the main parameters that influence the process. Ion implantation turn out to be strongly influenced by the following process variables:

- Range and Projected Range
- Dopants
- Dose and ion energy
- Tilt angle
- Damage

Range and Projected Range

As shown in Fig. 4.2, the implantation process assumes that the accelerated ions penetrate in a solid target following a specific trajectory which is determined by the interactions with the target atoms nuclei. The total distance travelled by an implanted impurity in the target is called Range and it is reached when the ion has completely lost its kinetic energy. The average depth of the dopant distribution along the implanted direction is called *Projected Range* (Rp) that usually correspond to the depth at which the dopant profile has the maximum value.

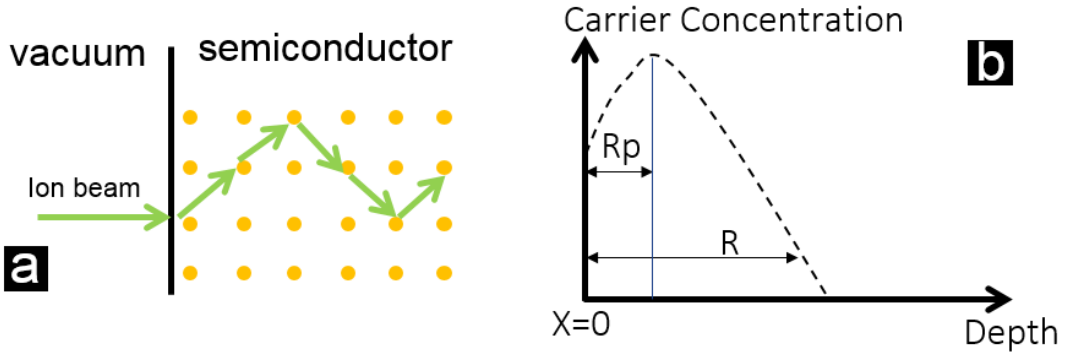


Fig. 4.2: *(a) Implanted ions collision with target atoms (b) Typical schematic illustration of ion range and projected range obtained after the ion implantation process.*

Dopants

Impurities usually belonging to Group III and Group V used for ion implantation applications. The most common n-type source are As, P, and sometimes Sb; while B is the predominant p-type dopant. The distribution of these dopants depends substantially from the diffusivity of the material within the semiconductor; indeed, if different ions are implanted with the same energy, heavy ions are going to stop at a shallower depth compared with the light dopants creating a different doping profile.

Dose and ion energy

The implanted ions inside the target usually are identified as dose and commonly it is expressed in ions/cm^2; while ion energy represents the strength supplied to the ion to travel along the target and it controls the penetration depth profile. In MOS device fabrication energy ranges from 100 eV to 3 MeV and the energy used depends from application even if the small energy range process, below 1 keV, is becoming more attractive for the formation of ultra-shallow junctions.

Tilted ion beam

The direction of the beam with the respect to the target is identified as tilt angle and it is the angle formed between the ion beam direction and the normal to the surface of the substrate. According to this parameter it is possible control the depth profile and minimize the channelling effects defined as the space through which the ion can travel without significant scattering. Channelling effects are not desired as they widen the doping distribution profile by the formation of tail, that hinders the formation of shallow profiles.

Damage

During the implant process the impinging ions are able to move along the solid target losing energy steadily due to the electronic and nuclear collisions. Then when an implanted ion is penetrating the target the stationary atoms are able to recoil and to absorb the energy deflecting the incoming ion trajectory. The interaction mechanism is governed by the energy and usually the implant damage is caused by the nuclear collision which can displace the target atom from the lattice site creating Frenkel defects [252]. In addition the energy required to knock off a target atom far from its site is called *Energy displacement (Ed)*, so if the implanted ion energy exceeds the Ed value it is possible create defects in the lattice. Basically after the collision between the ion and the target three possible scenarios are possible: (1) during the impact an empty space is created in the lattice, it is called vacancy defect, see Fig. 4.3.(a); instead when the incident ions or the target atoms stops in the solid the defect is called interstitial, see Fig. 4.3.(b); finally if the energy provided is lower than Ed the lattice atom does not have enough energy to leave the site then it recoils releasing energy as phonons and it resides in the lattice, see Fig. 4.3.(c).

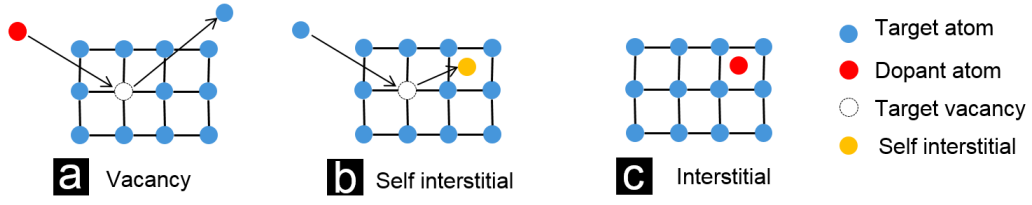


Fig. 4.3: *Defects in the lattice after the ion implant process: (a) impinging ions knock out target atoms from the lattice site creating a vacancy (b) Recoiling atoms with enough energy to knock other atoms out residing in the lattice creating a self-interstitial defects (c) the incoming ions stop in the lattice creating interstitial defects.*

4.5.2 Simulations

Considering material limitations and the necessity to obtain shallow doping profiles, simulations were necessary to evaluate different experimental parameters such as the energy range, the projected range obtained, the amount of damage caused, and the thickness of the surface capping layer. From previous investigations on $Ge_{1-x}Sn_{x,}$ remarkable improvement were noticed when using a capping layer that protects the surface from a direct ion beam [97, 99].

The first simulation aim was to identify the feasible energy range for the experiment; consequently implantation energies ranged between 10 keV and 100 keV. The simulation considers As implantation (dose = 1×10^{14} atoms/cm^2) into SiO_2/GeSn material, that respectively represents a capping layer (30 nm thick) and the target material (200 nm thick).

Furthermore, since the capping layer had to be developed through *plasma enhanced chemical vapour deposition* (PECVD), a certain fluctuation into the process had to be take into account, thus the simulations were repeated considering the cap thickness variability. Nevertheless for this study the energy range has been limited to 40–60 keV according the tool available in AMAT for the implantation. The simulations have been set-up using different capping layer thicknesses ranging from 10-30 nm with a step of 5 nm. Considering the same implant energy, the simulations show a decreasing trend for the Rp in the GeSn layer as the cap layer thickness increases; namely for 40 keV, the expected Rp passes from 25.1 nm for 5 nm of SiO_2 to 19.4 nm for 30 nm of SiO_2, while considering 60 keV the Rp moves from 31 nm for 5 nm of SiO_2 to 25.2 nm for 30 nm of SiO_2. Furthermore looking at the ion distribution profile as the implanted energy decreases, a shift towards the cap layer occurs, reducing the width of the Gaussian shape profile.

Finally, to have as more realistic prediction as possible, considering both the tool set-up and the capping layer variability, the simulations have been repeated taking into account a cap layer thickness of 25 nm within the energy range outlined previously (40-60 keV). As shown in Fig.4.4 increasing the implantation energy the doping profile is deeper into the target material, as the Rp passes from 29 nm with a peak concentration of 6×10^{19} atoms/cm^3 for 40 keV to 38 nm with a concentration peak of 3.5×10^{19} atoms/cm^3 for 60 keV.

The graphs below have been obtained considering three different implantation energies respectively written in the inset of each specific plot. Depth vs Y axis describes the ion track within the target as a function of the implanted energy, the white dots represent the damage created by the implanted ion while the red dots are the recoil cascade. Ion range graphs plot the ion distribution within the structure created and left Y axis allow to obtain the final peak concentration. Finally the collision events graphs show the total number of vacancies created by the implantation process as a function of the depth and energy.

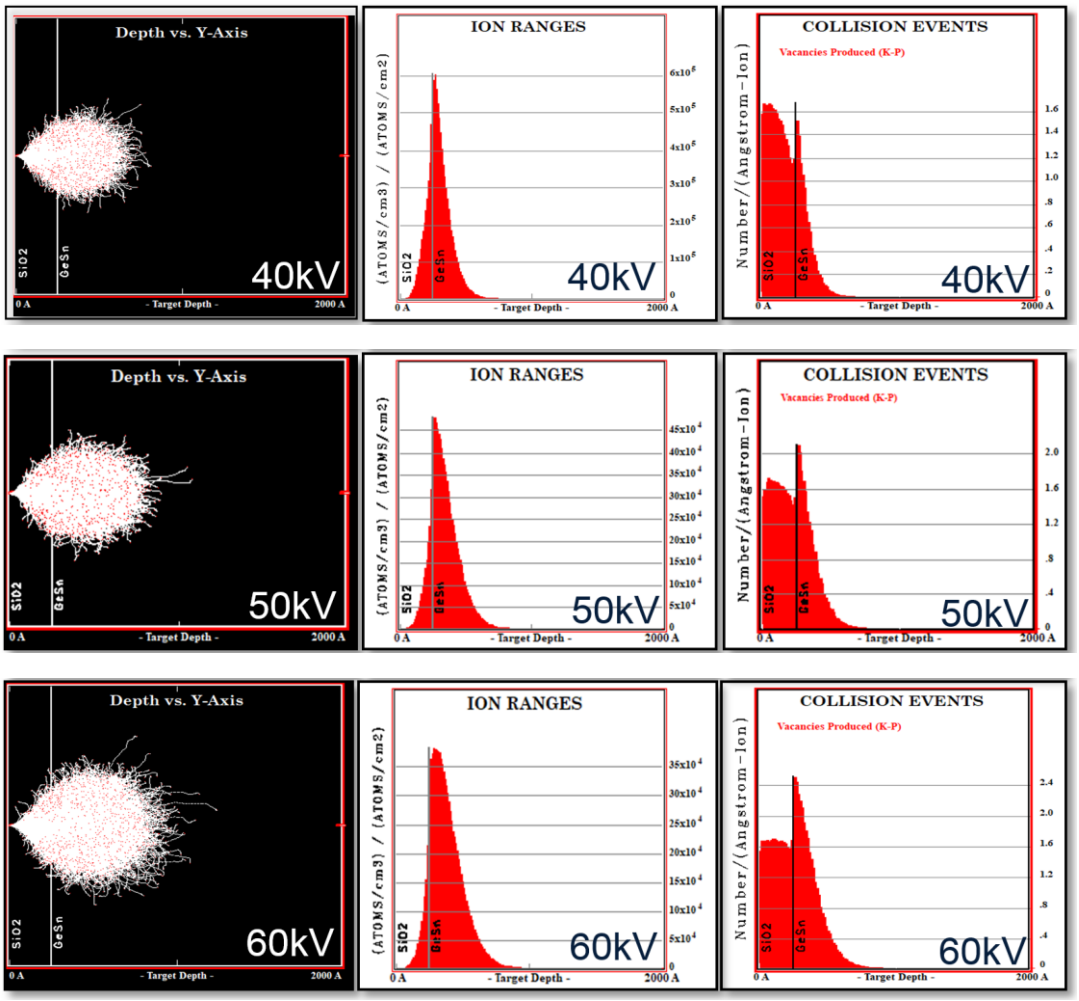


Fig. 4.4: *Simulations results using 40 keV, 50 keV and 60 keV are represented respectively on the first, second and third row. The graphs have been obtained considering three different implantation energy respectively written as the inset*

4.6 Doping investigation

During the internship period three different experiments have been performed on $Ge_{0.91}Sn_{0.09}$ substrates, that were epitaxially grown by *MBE* by project partner IQE. The first analysis was focused on the morphological study of $Ge_{0.91}Sn_{0.09}$ after the ion implantation process; while the other two investigations have been targeted

more on the doping aspects in order to outline the potentiality and the weaknesses of each doping technique.

4.6.1 Morphology study

The following analysis represents an initial step for further inspections for $Ge_{1-x}Sn_x$ doping options. The morphological study aim is to explore the porosity effect for $Ge_{0.91}Sn_{0.09}$ as a function of different capping layer and current rate dose for As implantation at *room temperature (RT)*.

In literature has been already demonstrated that the implantation of some heavy ions in Ge can lead to the formation of nanoporous structures on the semiconductor surface; furthermore control of the porosity by varying implantation parameters has been demonstrated in Ref. [253]. Conversely, other manuscripts show the possibility to reduce the porosity effect through the use of *liquid nitrogen temperatures (LN_2T)* during the ion implantation step.[254, 255]

Although nanoporous materials are potentially useful for the construction of several sensors thanks to the unusual structural characteristics [256], they can be extremely interesting for the photovoltaic sector where the presence of nanoporous structure allows a greater surface area that can be advantageous. The nanoporous structure formation derives from the damage caused by ion implantation and this phenomena is observed in Ge and its alloys, and the possible explanation of such an effect might come from the ability of the vacancy defects to cluster within the semiconductor lattice during the ion bombardment [257].

Before implanting As into $Ge_{0.91}Sn_{0.09}$ samples, 6 substrates were partially covered by two different capping layer in order to have half surface coated and half not. The deposition of both capping layer was carried out through PECVD and 3 samples has been coated with 25nm of SiO_2 while other 3 with 25 nm of *Silicon Nitride* (SiN).

Subsequently, as shown in Fig. 4.5.(a), all of the above samples were partially protected with a piece of Si wafer to implant the $Ge_{0.91}Sn_{0.09}$ only on two different sections, one with capping layer on top and the other one without cap. The configuration obtained allow to detect the porosity degradation as a function of the capping layer and current rate dose used. Ion implantation conditions for the experiment are reported below:

a) Ion dose = As 5×10^{16} atoms/cm^2
b) Room Temperature
c) Three different current rate dose = 1mA - 6mA – 12mA
d) Ion energy = 50 keV

Optical microscope analysis showed different results as expected due to the different surface configuration; the uncovered section (bare $Ge_{0.91}Sn_{0.09}$) became black due to the porosity and segregation effects; while the section with the capping layer showed different reaction as a function of the material used to coated the surface, see Fig. 4.5.(b). In addition from the SEM analysis the SiN capping layer tended to decrease the porosity effect even if the Sn segregation is massive with both the capping layers.

Compared with previous study made by Tran et al. [99] where the implantation has been made at LN_2T using a SiO_2 cap layer to suppress the porous effect; in this study two different results have been achieved; although both sections with and without capping layer reveal porous structure with different yield the area without cap layer show massive porous structure and void defects compared with the one with cap.

In addition the SiN cap layer exhibited better performance compared with the SiO_2 counterpart as well as the sample implanted at lower current dose rate showed a lower amount of void defects and Sn surface segregation compared with the other implanted at higher current dose.

Definitely in this work the implant temperature and the current rate dose substantially affect the final results due to the mobility of point of defects. Then for $Ge_{0.91}Sn_{0.09}$ alloy the low temperature regime combined with the capping layer that act as an obstacle, allowing inhibition of the pore formation; instead we show that implanting at RT the porosity effect is hard to suppress.

The study showed that the porous effect and void defects are hard to suppress using the RT implantation and for next experiment the use of LN_2T is highly recommended. Further investigation on different cap layer thickness, temperature, and ion fluence might provide attractive insight for the understanding of the suppression process, the role of the capping layer and the influence of Sn.

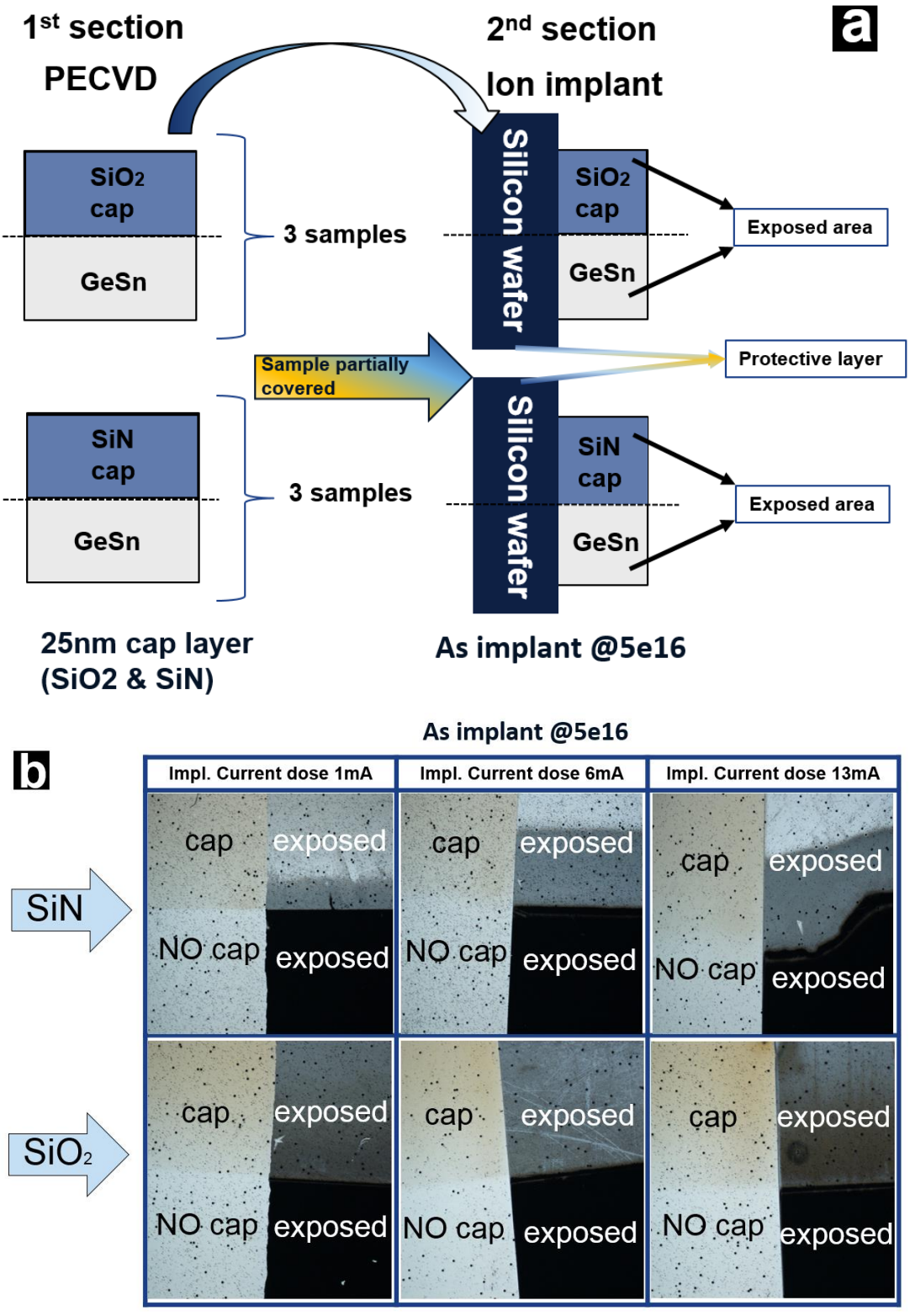


Fig. 4.5. (a) *Representative explanation of process done in the experiment.* ***(b)*** *Optical images of the structures obtained after the ion implantation as a function of the different current dose and capping layer developed.*

4.6.2 Ion beam approach

In this section a systematic analysis of $Ge_{0.91}Sn_{0.09}$ samples doped with As is described. The processes were performed by using the classic ion beam

methodology combined with spike annealing carried out in AMAT facilities. Despite the annealing recipe being developed by a support team to replicate the same thermal budget used in [121] the tool available did not allow anneal of the sample only from the rear side. Then in this experiment, the samples underwent a process of 11 seconds, where 4 seconds have been used to ramp up the spike from 550 – 700 °C while the other 7 seconds have been used to cool down the system.

Table 4.2 summarize the experimental parameters such as the capping layer, the dose rate, and the implant temperatures (RT=25 °C; HT=250 °C) used during the experiment. After the implantation both SiN and SiO_2 capping layer were removed through a wet etching process. The SiO_2 layer was etched by dipping the sample in *buffered oxide etching BOE* (5: 1) for 3 minutes while for SiN capping layer the samples have been immersed for 2 min in the solution and all the samples developed have been undergone to the same annealing procedure.

Wafer	*Pre-process*	*Energy*	*Dose (ions/cm²)*	*T(°C)*	*Tilt(°)*	*Twist(°)*
GeSn_1	SiO_2 cap layer	50 KeV	1e14	25	7	22
GeSn_2	SiO_2 cap layer	50 KeV	5e14	25	7	22
GeSn_3	SiO_2 cap layer	50 KeV	1e15	25	7	22
GeSn_4	SiO_2 cap layer	50 KeV	5e15	25	7	22
GeSn_5	SiN cap layer	50 KeV	1e14	25	7	22
GeSn_6	SiN cap layer	50 KeV	5e14	25	7	22
GeSn_7	SiN cap layer	50 KeV	1e15	25	7	22
GeSn_8	SiN cap layer	50 KeV	5e15	25	7	22
GeSn_9	SiO_2 cap layer	50 KeV	1e14	250	7	22
GeSn_10	SiO_2 cap layer	50 KeV	5e14	250	7	22
GeSn_11	SiO_2 cap layer	50 KeV	1e15	250	7	22
GeSn_12	SiO_2 cap layer	50 KeV	5e15	250	7	22
GeSn_13	SiN cap layer	50 KeV	1e14	250	7	22
GeSn_14	SiN cap layer	50 KeV	5e14	250	7	22
GeSn_15	SiN cap layer	50 KeV	1e15	250	7	22
GeSn_16	SiN cap layer	50 KeV	5e15	250	7	22

Table 4.2: *Parameter modification taken into account during the ion implantation. All the samples after the ion implantation have been undergone to the same annealing recipe.*

To inspect the doping profile a *secondary ion mass spectroscopy (SIMS)* study has been made highlighting two essential results (1) the high implant dose obtained within $Ge_{1-x}Sn_x$ (2) the high Sn surface segregation. Samples developed at RT and HT with the higher dose energy have been analysed. All the graphs presented in Fig. 4.6 are divided in two sections the first row display the results of the experiment obtained implanting the sample at RT while the second row the results coming from the HT implantation. In addition in all the graphs blue curve reports the As concentration while the red one represents the Sn distribution.

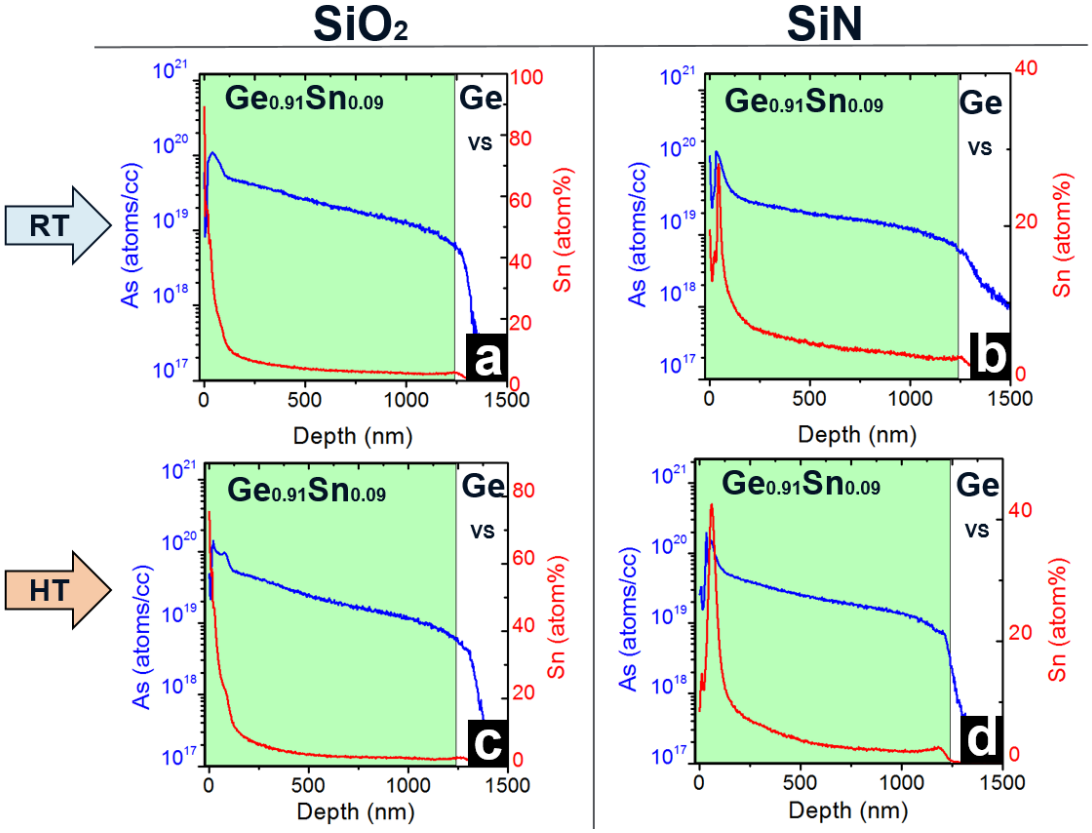


Fig. 4.6: *SIMS profile for sample developed at RT and HT; in the first row are the profiles for GeSn_4 (a) and GeSn_8 (b) while in second row there are the profile for GeSn_12 (c) and GeSn_16 (d). In the graph As and Sn distribution will be always represented respectively with blue and red curves and they will refer to right and left Y axis.*

SIMS data for the samples implanted at RT (GeSn_4 and GeSn_8) shows similar As concentrations even if the part with the SiO_2 capping layer pointed out two different aspects; (1) broader shoulder and (2) higher Sn surface segregation, see Figs. 4.6.(a) and 4.6.(b) compared with the counterpart. From HT investigation, see Figs. 4.6.(c) and 4.6.(d) the peak result to be deeper but the trends are almost similar

between the two samples under test (GeSn_12 and GeSn_16); in addition a double peaks has been recognized in test wafer implanted with SiN capping layer.

Another interesting point is the As diffusion within the material. From Fig. 4.6. drastic doping diffusion reduction was observed as soon as the material switches from $Ge_{1-x}Sn_x$ to Ge. This indicates that As diffusion is enhanced on the $Ge_{1-x}Sn_x$ relative to the Ge, the implication is that the doping can be confined within the predefined $Ge_{1-x}Sn_x$ region with careful selection of implant and anneal parameters. This is a positive aspect in controlling the movement of dopants and for the formation of ultrashallow junctions.

Since the Sn atoms show massive surface segregation a partial movement of atoms has been hypothesized which might favours the development of vacancy in the lattice and therefore the spread of As atoms. Overall in this study a clear doping mechanism has been obtained in all the samples since As concentration is almost 1×10^{20} atoms/cm^3 with energy ranging from 40 keV to 60 keV. The capping layers used shows only a small influence on the process maybe due to the thickness or from the dose used. Furthermore the RT implantation procedure exhibits shallower doping profiles compared with HT ones, highlighting the T influence on the process.

Nevertheless further analysis should be addressed to understand the different capping layer impact because the double peak obtained for SiN capping layer might be an artefact but in the same time it could come from a possible reaction between the capping layer and the underneath $Ge_{0.91}Sn_{0.09}$ substrate. Therefore, a much wider range of capping materials, ion fluence and temperature should be investigated to understand the possible repercussion on the doping procedure; then further experiments and calculations have to be addressed to fully explore this intriguing process. Subsequently the samples have been undergone to an optical microscope, SEM and AFM analysis in order to outline possible morphological differences before and after the cap etching. Concerning the optical microscope analysis, see Fig. 4.7.(a), regardless of the capping layer used, increasing the ion dose the samples tended to show an accentuated bluish colour; conversely changing the temperature no substantial alterations have been distinguished. SEM investigation instead shows significant increment in surface roughness and Sn segregation after the capping layer removal. Indeed, from Fig. 4.7.(b), as both the dose and temperature increase, $Ge_{0.91}Sn_{0.09}$ samples manifest remarkable defects caused by the Sn segregation.

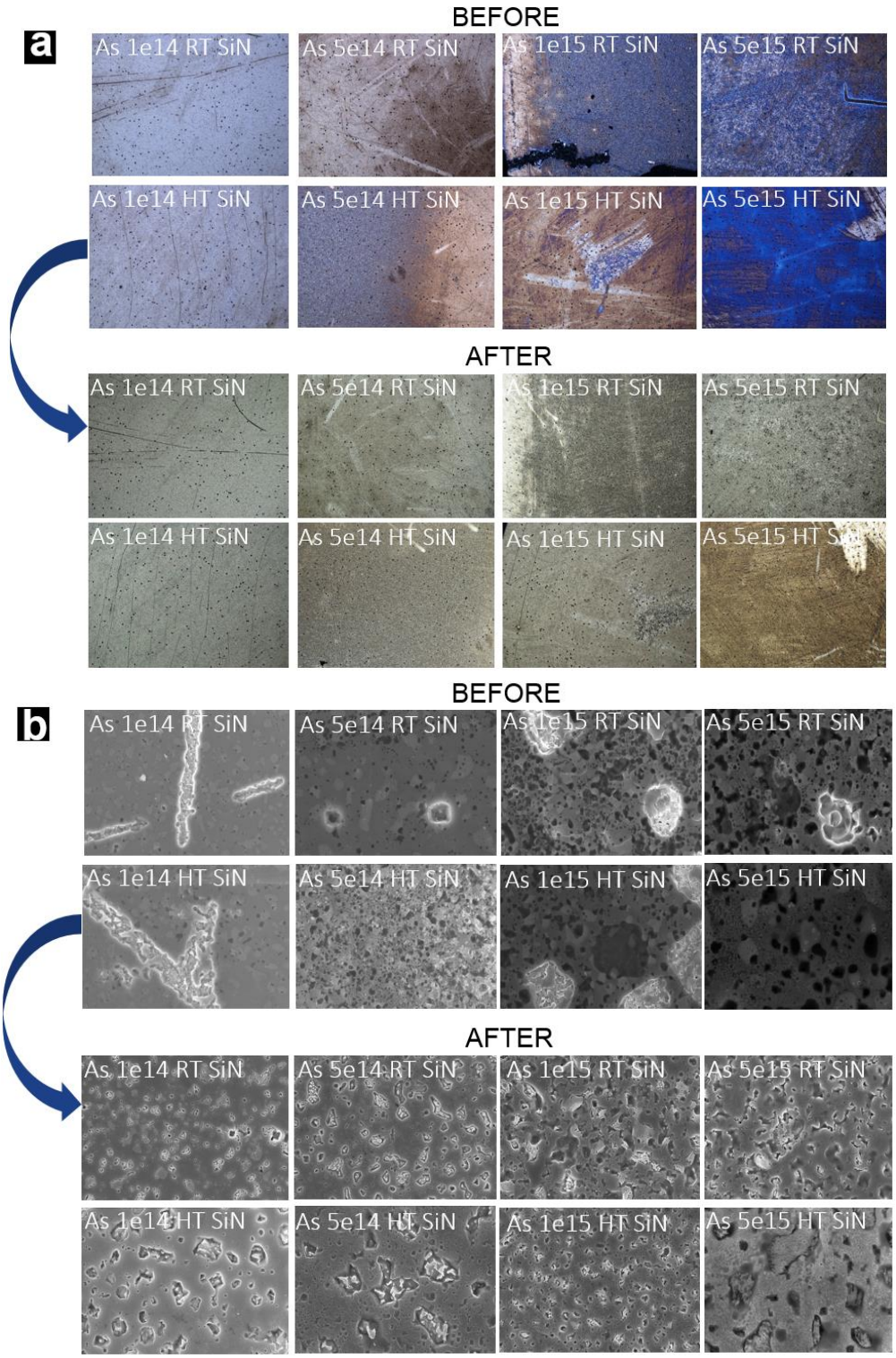


Fig. 4.7. *Surface analysis images before and after the capping removal for $Ge_{0.91}Sn_{0.09}$ samples using respectively optical microscope (a) and SEM (b). Each image has an inset describing the implant condition such as the dopant (As), the dose, implant temperature (RT and HT) and capping layer.*

Basically Sn segregation is driven by the ion implant breaking the surface bonds, the main consequence of the segregation is the morphology variation with the formation of craters on the surface [258, 259]. This blistering effect is a very common phenomenon in ion implant and it occurs when the impurities are hardly soluble in the material such as Sn into Ge, they tend to segregate into cavities, thus deforming the surface. Moreover from previous works it has been stated that blistering effects are highly influenced also by particular conditions such as the presence of hydrogen, the usage of high dose or energy and the annealing variability [260, 261]. Understanding the surface degradation effects for $Ge_{1-x}Sn_x$ alloy is difficult because it might be caused from several aspects such as the dopant diffusion defects, from thermodynamically effects or from the inclusion of low soluble impurities such as *Helium (He)* or *Hydrogen (H)*.

Regarding the AFM results the samples were analysed taking into account an area of 5×5 μm^2. Figure 4.8 summarizes the results achieved outlining an increasing trend as a function of the ion fluence and temperature used; in addition a couple of intriguing behaviours for the two different capping layer used were delineated. (1) Samples with SiO_2 capping layer show a *Root mean square (RMS)* cross-over before and after the cap removal; (2) samples with SiN demonstrate higher RMS values compared with counterpart.

Fig. 4.8.(a) and Fig. 4.8.(b) show the data for the sample with SiO_2 capping layer; from the images it is evident that the RMS data after the etch overtake the data before the etch in two different ranges; respectively 5×10^{14} - 1×10^{15} atoms/cm^2 and 8×10^{14} - 1×10^{15} atoms/cm^2 for implant at RT and HT. Then, although the surface still presents void defects and massive Sn segregation, the data pointed out an interesting aspect. As long as the ion fluence is lower than 5×10^{14} atoms/cm^2 it is possible to reduce the $Ge_{0.91}Sn_{0.09}$ surface roughness using a SiO_2 capping layer. Nevertheless further analysis are required to optimize the process before definitely conclude. Instead for samples with SiN capping layer the RMS transition step never occurs; furthermore as the implant T increases a RMS gap reduction is evident, see Fig.4.8.(c) and Fig. 4.8.(d). RMS data are, on average, 4.5 times to 1.25 times higher, and in addition the values obtained are far bigger compared with the counterpart especially for the data obtained after the cap removal.

However in both cases even if the samples had a capping layer acting as a mask the surface will still result to be rough and the effect tends to amplify as the temperature increases maybe due to the increased carrier defect mobility.

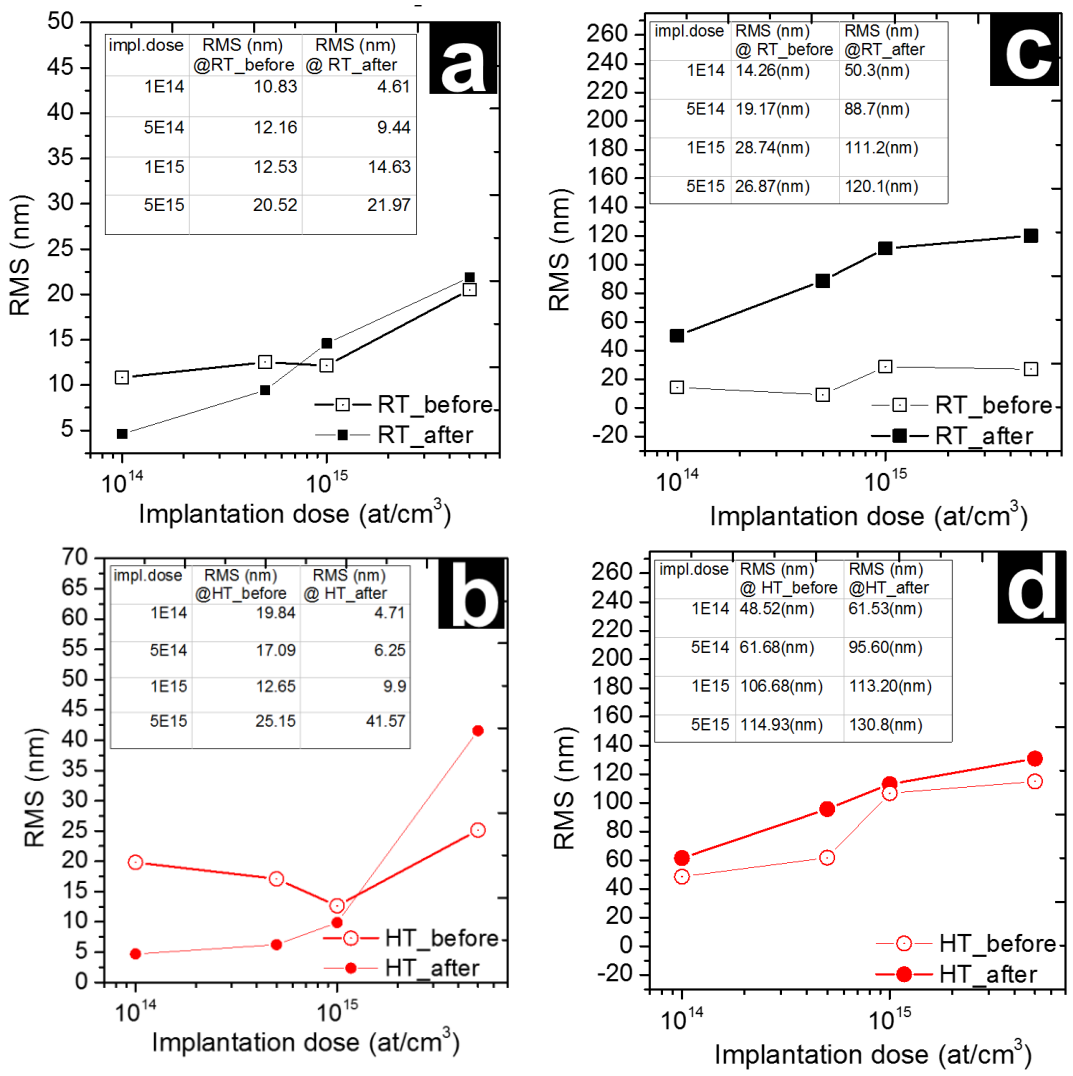


Fig. 4.8. *AFM data before and after the capping removal as a function of the ion fluence; each graph has a table as inset with the value obtained during the measurements. Image* ***(a)*** *and* ***(b)*** *respectively represent SiO_2 samples implanted at RT and HT while graphs* ***(c)*** *and* ***(d)*** *show SiN samples respectively implanted at RT and HT.*

With regard to the XTEM analysis several cracks and void defects have been observed in the $Ge_{0.91}Sn_{0.09}$ layer. The defects presumably derive from the agglomeration of vacancies within the layer or from the Sn surface segregation and they tend to form conical shape and cracks along the implanted zone, see Figs. 4.9.(a) and 4.9.(b). Defect formation, with and without a cap layer, as a function of the dose and temperature is consistent with previous results found in literature [99].

Basically, increasing the temperature and the dose the atoms in the lattice reallocate themselves according to the energy site available and the less soluble material tend to segregate to the surface creating defects near the surface and along the substrate. Furthermore using SiO_2 capping layer often an inter mixing layer close to the surface has been noticed, see Figs. 4.9.(c) and 4.9.(d). The band formation effect has been seen also from Janssens et al. that report Si and O contamination in the subsurface regions [262].

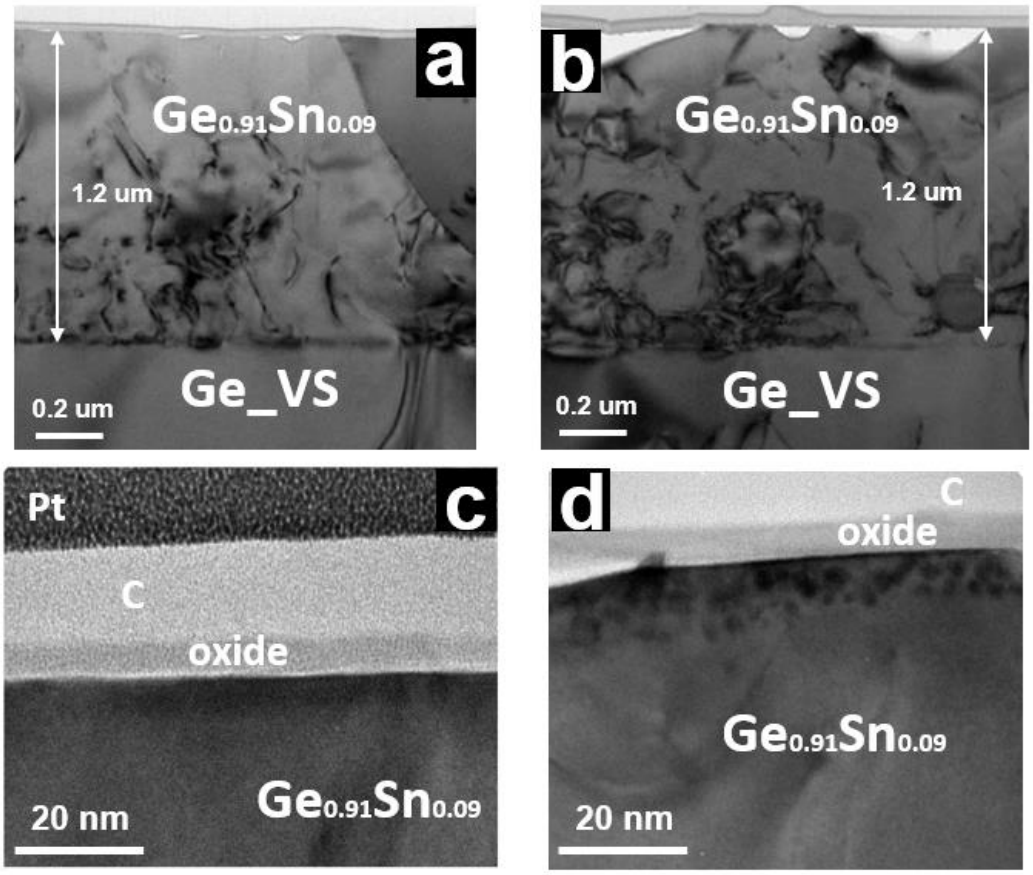


Fig. 4.9: *XTEM images of GeSn_4 (a) and GeSn_8 (b); while images (c) and (d) represent respectively high zoom XTEM image of GeSn_1 and GeSn_9.*

Finally, the porous structure for samples with a capping layer seems to be relatively uniform and well-ordered, compared with the cases without the cap layer for almost all the fluence.

4.6.3 Layer deposition

The last experiment carried out consisted in doping $Ge_{0.91}Sn_{0.09}$ substrate through the deposition of an As and SiN (25 nm) capping layer. Compared with the more known ion implantation methodology the layer deposition technique turns out

to be less destructive since the dopant is not physically implanted but it will diffuse within the substrate during a thermal anneal. Below in Table 4.3 all the different case studies analysed have been listed. The layers have been deposited by PECVD.

Deposition time and the dc bias power were varied respectively to have different deposition rates and to introduce directionality to the process. After the processing, the samples were subjected firstly to the same annealing procedure developed for the ion implantation samples and subsequently the SiN capping layers were removed from all of them. All the characterisation previously carried out on the ion implanted samples have been repeated here in order to compare the two different doping techniques and to extract trends.

Dopant	Temperature (°C)	Capping layer	Time (s)	Bias	
As	25	SiN	5	With	Without
As	25	SiN	30	With	Without

Table 4.3: *Layer deposition experiment conditions.*

XTEM analysis revealed the formation of a superficial void defects in the substrate even if a substantial reduction of cracks (threading dislocations) within the layer is observed. The tendency to create voids in the material might arise directly from the physical and chemical $Ge_{0.91}Sn_{0.09}$ features. In addition, as pointed out in Figs. 4.10.(a) and 4.10.(b), as the bias increases the defects start to become wider giving a possible correlation between the dc bias used and the defects size. As occurred previously during the ion implantation, the data collected show the defects agglomeration towards the surface. The lack of connection among the craters indicates that the process occurs creating random nucleation site without long range interactions.

Figures 4.10.(c) and 4.10.(d) show the SIMS investigation; from the data is noteworthy that As concentration in $Ge_{0.91}Sn_{0.09}$ substrate is higher compared with the ion implantation experiment while the Sn segregation is lower. Although the thermal budget limitation severely restricts the application due to the formation of void and Sn segregation; from the results obtained, it is possible assume that the layer deposition methodology is the most reliable technique to dope $Ge_{1-x}Sn_x$ material.

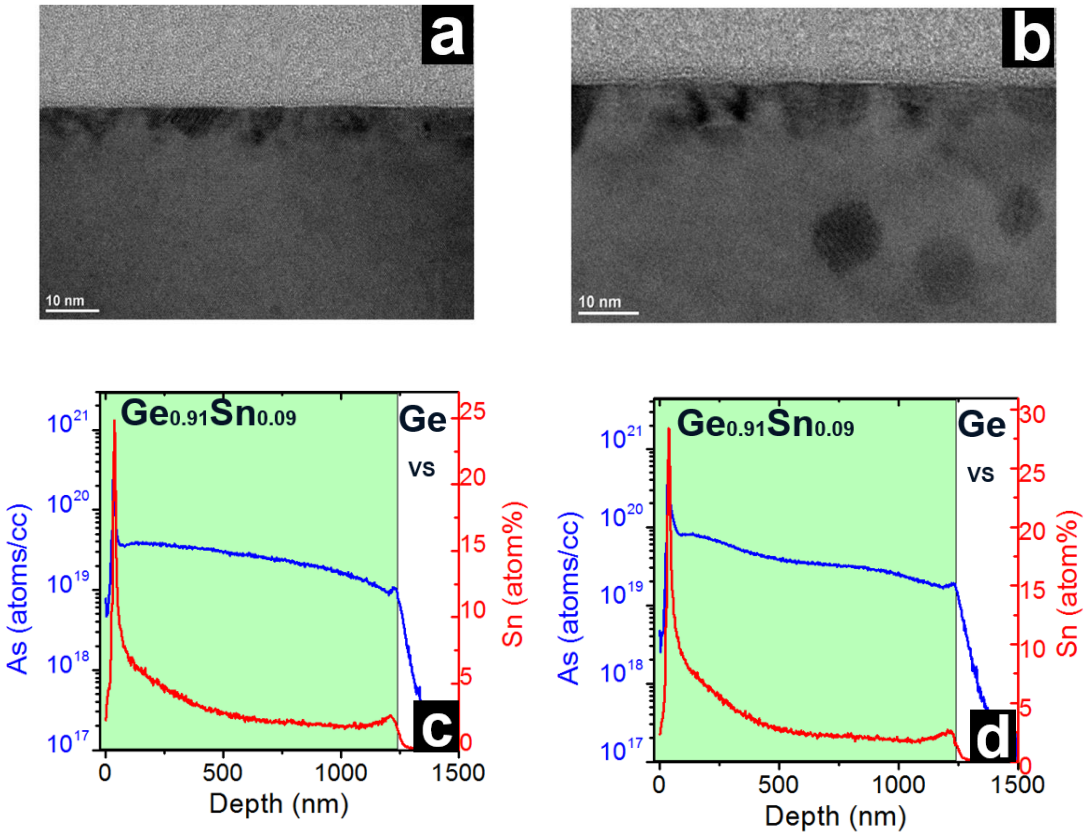


Fig. 4.10: *XTEM images of $Ge_{0.91}Sn_{0.09}$ sample with As deposition respectively for 5 sec. (a) and 30 sec. (b). SIMS profile investigation obtained activating bias condition respectively for 5 sec.(c) and 30 sec. (d).*

Subsequently an optical microscope and SEM investigation have been carried out on the samples to compare the wafer surface before and after the SiN capping layer etching. From optical microscope images a substantial difference is not evident, other than the colour changes passing from light blue to gold. Conversely from SEM prospective (see Fig. 4.11) there is a remarkable difference on the surface; when the SiN capping layer is removed, a high amount of surface defects and blisters are presented on the superficial section.

The defects size increases as the deposition time increases; moreover the blister and craters rate increase as the dc bias is increased, outlining a possible trend. Essentially as the dc power increases, ions tend to be attracted to the material surface more enhancing the formation of surface defects thought capping layer. Also in this study case, from the data observed, the main deterioration cause lies in the thermal budget, because in all doping circumstances the surface results to be highly impacted from Sn segregation void defects. Data obtained previously in SEM

investigation are further confirmed by AFM analysis and the values have been reported in Table 4.4.

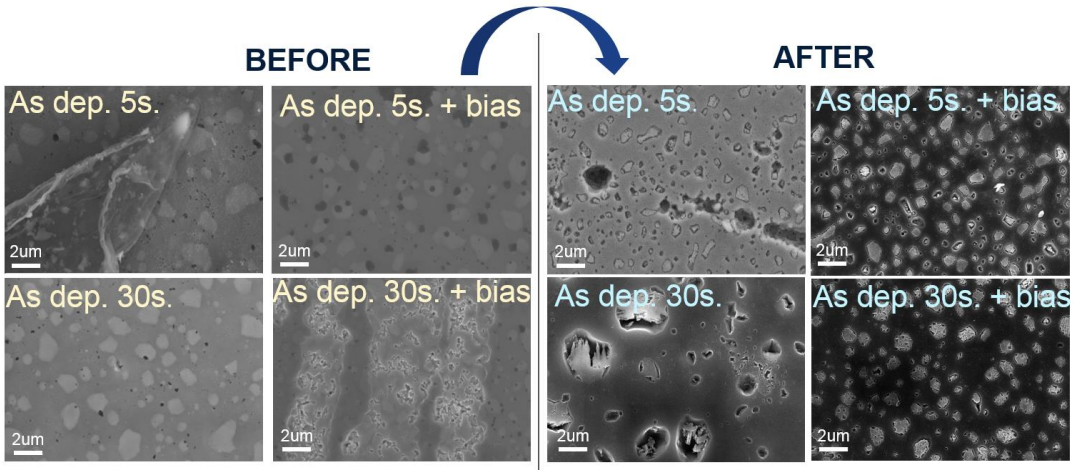


Fig. 4.11: *SEM images of samples before (a) and after the cap removal (b) considering the different the study case described respectively as inset in the figure.*

Deposition condition	RMS before cap removal (nm)	RMS after cap removal (nm)
$Ge_{0.91}Sn_{0.09}$_5s	33.74	65.4
$Ge_{0.91}Sn_{0.09}$_5s+bias	15.90	42.2
$Ge_{0.91}Sn_{0.09}$_30s	13.34	71.4
$Ge_{0.91}Sn_{0.09}$_30s+bias	22.67	60.3

Table 4.4. *AFM data with the RMS results obtained before and after the cap removal.*

Overall, the samples have higher RMS data after the cap removal. In addition the inclusion of dc bias did not return a significant benefit in terms of adhesion. An interesting aspect to take into account is the choice of the correct range for the dc bias in order to reduce the impinging ions energy because it might cause severe damage such as material stress, refractive index changes, electrical resistivity affecting the surface topography [263]. Indeed, if the critical value is exceeded, the stress result to be so high that the film will no longer be able to adhere and it peels off. Then as long as the deposition time increases an RMS improvement was detected maybe because the layer was inclined to form a more homogeneous structure but further investigation using different bias conditions are needed to clearly state the optimum process window.

4.7 Conclusion

In conclusion a comparative work among different doping methodologies has been made on $Ge_{0.91}Sn_{0.09}$ to outline the most reliable techniques as a regards doping options. Results carried out highlight both the ability to highly dope the material using the most common ion implantation process and also the layer deposition methodology, that both show the bottlenecks such as the material sensitivity to thermal budget and Sn segregation.

From the results obtained, Sn segregation and thermal budget severely affect the substrate surface up to the point to compromise the possible usage in nanoelectronics application. Nevertheless due to the high number of variables taken into account and the lack in literature about $Ge_{1-x}Sn_x$ doping, it is hard to compare the results and extract clear trend, but according to the information achieved in this study the most reliable process both in terms of morphology damage that in term of dopant activation appears to be the diffusion through highly doped surface formed layer. Further study will be necessary to obtain shallow implantation usable in new device architectures and to go beyond the physical limits of the alloy understanding and defining the Sn role in the process.

5|$Ge_{1-x}Sn_x$ Nanowires: device fabrication and characterization

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This chapter is adapted from the following publication:

Galluccio E., Doherty J., Biswas S., Holmes J., Duffy R., *Field-Effect Transistor Figures of merit for VLS grown $Ge_{1-x}Sn_x$* (x=0.03-0.09) *Nanowire devices,* ACS Applied Electronic Materials doi.org/10.1021/acsaelm.0c00036. 2020.

5 | $Ge_{1-x}Sn_x$ Nanowires device: fabrication and characterization

5.1 Introduction

In the last 50 years semiconductor companies focused relentlessly on Moore's law to reduce the size of the transistor. For much of that time, scaling meant following the Dennard scaling rules [4]. Although for a long time, considering extremely small transistor features, in nm scale Dennard's law has become ineffective. From the 90 nm process node onwards, in order to continue the device shrinkage ideology, new concepts such as material strain [51, 52] or usage of high-k [10, 53], up to the development of new device architectures [54-57] (FinFET, GAA, JNT, TFET) have been introduced. As a consequence of continued scaling toward atomistic dimensions, new semiconductor materials have been proposed with the purpose of creating Si compatible, scalable, and tunable channel materials to improve the device performance. In this context, group IV semiconductors such as Ge or its alloys, like $Ge_{1-x}Sn_x$, have gained a lot of interest [63] and further investigation is warranted.

In this Chapter despite the enormous difficulties involved in new semiconductor material growth and device fabrication, an overview on $Ge_{1-x}Sn_x$ device state-of-the-art will be shown. In the second part the potential and disadvantages of NWs FET fabrication will be described, and subsequently the electrical characterization of $Ge_{1-x}Sn_x$ low power NW devices, obtained from a bottom up growth approach, will be introduced and discussed in detail.

5.2 State-of-the-art for $Ge_{1-x}Sn_x$ device

Within the last year $Ge_{1-x}Sn_x$ alloys have attracted scientific interest due to unique potential, such as the ability of varying its B_g as a function of the Sn content [69, 162, 264, 265] and the possibility to achieve higher electron and hole mobility compared with Ge [67]. The ability to tune the B_g represents an opportunity for this new semiconductor material because it might be used both in low power and optoelectronic applications. A direct B_g semiconductor is a valuable solution for more efficient band-to-band-tunneling devices, such as *Tunnel-Field-Effect-Transistor (*TFET*)* [188, 266], lasing applications [76, 267] and for the development of *mid-infrared* (IR) photonics devices [268].

Although the remarkable properties of $Ge_{1-x}Sn_x$ alloys and the straight forward integration with the well-established Si platforms, all the steps needed to fabricate $Ge_{1-x}Sn_x$ circuitry need to be adapted and specifically developed. During recent years a series of limitations have been addressed to obtain alloys with acceptable electrical performance. The low solid solubility of Sn into Ge (<1 at. %) with the tendency for Sn to segregate at high temperature [131, 269] and the large lattice mismatch between Ge and Sn (≈15%) were significant restrictions to overcome, in order to obtain direct semiconductor substrates [71]. Therefore, promising solutions such as the use of Ge virtual substrate layers or the transition toward 1-D nano-structures [270] have been proposed to overcome the aforementioned restrictions.

Though the transition from planar structures to a 3D architecture occurred very quickly, several studies aimed for lithography process optimization, including etching [271, 272], gate stack development [272, 273], or the doping [121] in order to address all the possible limitations to achieve astonishing device results.

Mobility and I_{ON}/I_{OFF} ratio benchmarking as a function of the Sn content for the state-of-the-art reported so far in literature are represented in Table 5.1 and in Figure 5.1. Though, mostly results have been achieved using a planar device configuration, it is interesting to note the continuous performance improvement reached during the years.

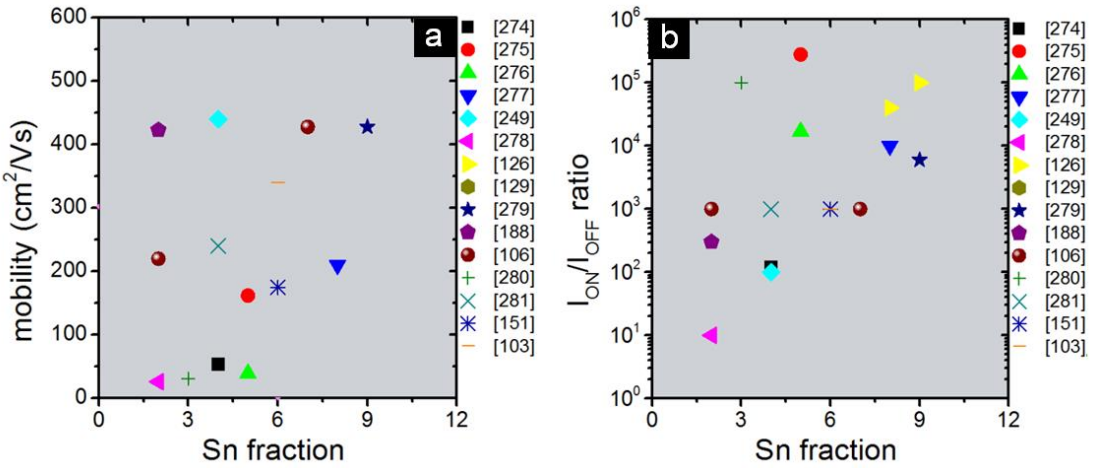


Figure 5.1: *Device benchmark plots for two of the most important electrical parameters (a) mobility and (b) I_{ON}/I_{OFF} ratio as a function of the Sn fraction involved in the alloy.*

Work	Device	Year	Sn%	I_{ON}/I_{OFF} ratio	Mobility (cm^2/Vs)
[274]	Junctionless (top-gate)	2019	4	1.2×10^2	μ=54
[275]	Junctionless (top-gate)	2019	5	2.8×10^5	μ=162
[276]	Junctionless (bottom-gate)	2018	5	Ar = 1.7×10^4 N_2 = 2.2×10^2 N_2O = 9.5×10^2	μ_{Ar} = 39.3 μ_{N2} = 8.1 μ_{N2O} = 0.6
[277]	FinFET	2018	8	≈1×10^4	μ=210
[249]	N-MOSFET (top gate)	2018	4.5	≈1×10^2	μ=440
[278]	P-MOSFET (top-gate)	2017	2	≈1×10^1	μ=26
[126]	P-MOSFET (top-gate)	2017	IM=8 JNT=9	IM=4×10^4 GAAFET=1×10^5	Not extracted Not extracted
[129]	p-i-n structure (top-gate)	2016	6	Not extracted	Not extracted
[279]	P quantum well	2016	9	6×10^3	μ=428
[188]	N-MOSFET (tunnel diode)	2016	7 to 14	Not defined	Plot as a function of Sn% (0-14)
[106]	Planar (top gate)	2015	2	3×10^2	μ=423
[106]	Planar (top gate)	2015	2 7	≈1×10^3	$\mu_{2\%}$ = 220 $\mu_{7\%}$ = 428
[280]	Tri gate	2014	3	1×10^5	μ=31
[281]	P-MOSFET (top gate)	2013	4	≈1×10^3	$\mu_{(100)}$ = 240 $\mu_{(111)}$ = 31
[151]	MOSFET (top gate)	2013	(P)→6 (N)→6	P-type ≈1×10^3 N-type ≈1×10^3	P-type μ≈175 N-type μ≈185
[103]	MOSFET (top-gate)	2011	6	≈1×10^3	μ=340

Table 5.1*: State-of-the-art GeSn device metrics present in literature. From right to left, device architecture, year, Sn %, I_{ON}/I_{OFF} ratio and mobility.*

5.3 Moving from planar to 1D nanostructure devices

Planar MOSFET configurations consist of a lowly doped semiconductor substrate with two opposite doped regions called respectively “Source" and “Drain” (S/D) which are used as a charge reservoir. Basically the planar design behaves as “inversion mode” device because the surface region underneath the oxide and between S/D regions forms a channel, as long as the gate potential is able to deplete the majority carrier and attract the minority carrier to the surface. Therefore by controlling the gate potential it is possible to form the surface charge inversion layer, while regulating the S/D bias it is possible manage the current flow within the channel.

Taking as example Figure 5.2, where an N-type MOSFET configuration is shown, the *Metal-Oxide-Semiconductor* (MOS) structure is clearly visible. The substrate in this case is p-type semiconductor while the S/D regions are highly doped n-type regions. A thin insulating layer, with a thickness of t_{ox}, is deposited on top of the semiconductor material defining the channel region. Channel length (L) and width (W) are measured considering respectively the parallel and the perpendicular current direction flow. Finally, above the dielectric layer and on top of the S/D regions, the metal gate and the S/D contacts are placed to control the device performance.

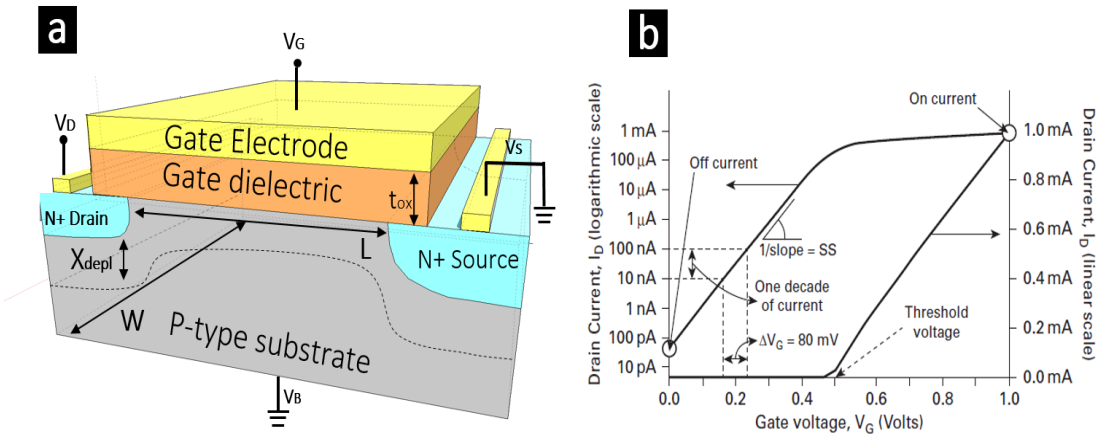


Figure 5.2: *(a) Typical bulk n-type MOSFET schematic view, (b) drain current as a function of the gate voltage in a MOSFET with low drain voltage, the two curves represent the identical data plotted either using linear scale (right hand y-axis) that logarithmic scale (left-hand y-axis) taken from* [3].

The inversion-mode MOSFET device typically behaves as a switch and these concepts will be explained further below.

Assuming source and p-type substrate grounded *(V_S=V_B=0V)*, drain region biased with a positive voltage (V_D>0) and the gate voltage equal to zero *(V_G=0)*, the conduction channel is not formed. In this configuration the drain p-n junction is reverse biased hindering the current flow, while the source p-n junction provides zero current due to the bias condition. As a result there is no current flow between the S/D then in this situation the transistor is in OFF mode.

Conversely if a positive bias is applied to the gate, the holes underneath the dielectric substrate are pushed away forming a depletion region with size equal to X_{depl} that is inversely proportional to the substrate doping concentration. When the gate voltage exceeds the threshold voltage, the gate potential starts to attract negative carriers from S/D to form electron rich layer called “inversion channel”. In this configuration the transistor works as a closed switch therefore it is in ON mode.

Whenever the transistor is ON, according to the gate and drain voltage applied, it is possible define two different working areas. Basically if the drain voltage is low (typically hundreds of mV) and the gate bias is high enough to exceed the threshold voltage; the drain current increases linearly with the gate voltage. This regime is called "linear" or "non-saturation" and the classical textbook equation is 5.1 [3].

$$I_D lin = \mu C_{OX} \frac{W}{L} [(V_G - V_{th})V_D - \frac{1}{2} V_D] \tag{5.1}$$

Where μ represents the mobility, C_{OX} the gate capacitance, W and L channel width and length while V_G, V_{th} and V_D are the gate voltage, the threshold voltage, and the drain voltage respectively.

While for larger values of drain voltage (when V_D>V_{GS}-V_{th}) the channel is pinched off therefore the drain current saturates according to equation 5.2 [3].

$$I_D sat = \mu C_{OX} \frac{W}{L} [(V_G - V_{th})^2] \tag{5.2}$$

After establishing the operating principles of a MOSFET, it is also relevant to introduce some of the most important electrical figures of merit to benchmark different device structures and architectures. Figure 5.2.b illustrates the drain current evolution in a MOSFET as a function of the gate voltage using a low drain bias. The OFF current is the first value (I_{OFF}) outlined; it is a parameter used to define the device off state and in the example here, it is set to 50 pA. While the ON current

(I_{ON}) is defined using a fixed gate voltage overdrive to the off state (1 V in this example). Moreover, the threshold voltage *(V_{th})* is defined as the point where the transistor starts to turn itself ON while the subthreshold slope *(SS)* is the drain current increment rate before the threshold voltage is reached. Usually the SS is defined by equation 5.3 [3] and it is calculated by one decade change of the drain current.

$$SS = n\frac{K_B T}{q}\ln(10) \tag{5.3}$$

n represents the body factor that describe the electrostatic coupling between the gate and the channel, K_B is the Boltzmann's constant, *T* is the temperature and *q* is the electron charge. SS describes how fast the transition is from the OFF to ON state for a specific device. In the ideal case, at room temperature, the best SS value obtainable is 59.6 mV/dec. Moreover, for planar device configurations it has been shown that it is impossible to beat this limit due to thermodynamics, unless using impact ionization [282] or tunneling effects [283], where the current is not limited by K_BT/q but only by the geometry, that can be engineered to reach lower values [284].

The planar MOSFET and its figures of merit represent key achievements for logic device electronics, nevertheless the unrestrained race towards the ever smaller feature sizes has caused certain constraints to arise. For example, short channel effects in the planar structures have been an insurmountable obstacle. Basically, either S/D p-n junctions create depletion regions that penetrate in the channel from both sides, reducing the gate control and the effective channel length. As a result, the potential and the electron concentration in the channel are not controlled solely by the gate electrode but they are influenced both by the distance of the S/D regions and by the voltage applied to the drain. Some of the most important and visible effects are the threshold voltage variation, the SS degradation and the growth in leakage current.

Therefore, in devices with less than 20 nm channel length, to maximize the electrostatic gate control and mitigate the short channel effects, new geometries have been proposed to fully control the channel. Multigate devices have been introduced to enhance the MOSFET performance, and among several candidates the *gate all around* (GAA) structure, obtained using *nanowires* (NWs), seems to be the most promising due to the high electrostatic control induced by its wrap-around gate, and

the possibility to fabricate device without any p-n junctions when fabricated in a JNT transistor design [285].

From an essential point of view the transport of carriers in NW structures might be formulated based on the non-equilibrium Green function (NEGF) and Poisson equation [285, 286]. If the NW channel length is below the mean free path of the carrier, the ballistic transport regime and quantum confinement effects have to be taken into account [285]. While when the NW channel dimensions are greater than the carrier free path the conventional model of field effect transistor is widely used to estimate the electrical performance [287],[288],[289]. Therefore the FET model used in the following sections of this Chapter to extract the electrical figures of merit and characteristics from the NWs complies with the diffusive transport regime approximation and only differs from the planar MOSFET device for the gate capacitance calculation [286].

5.4 Bottom up process

Semiconductor NWs growth and device assemblage can be achieved essentially following two main approaches: (a) the top down process, in which the nanostructures are formed by combining patterning and etching sequences; or by (b) the bottom up process, based on the epitaxial growth/integration of the NWs from a seeding substrate without using etching techniques.

In literature to date a variety of techniques have been reported for the NWs bottom up growth. Typical semiconductor materials, such as Si and Ge, have been studied in order to achieve NWs with stable crystal structure. The most common technique was found to be the *vapour-liquid-solid (*VLS*)* and the *chemical vapour deposition (CVD).*

Specifically for the $Ge_{1-x}Sn_x$ alloy, due to the low equilibrium solid solubility of Sn in Ge and possible low thermal stability, has necessitated a study into alternative novel growth methodologies. NWs have been grown in this Chapter via a *liquid-injection-chemical-vapour-deposition (LICVD)* technique as described in recent literature works [100, 102].

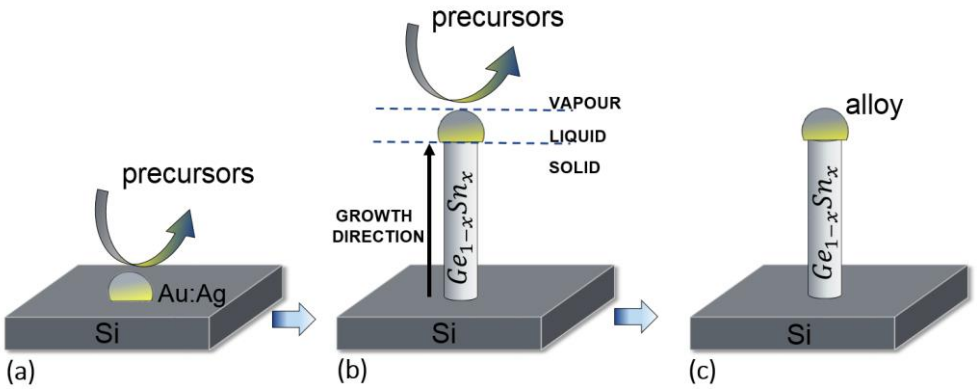


Figure 5.3: *Growth mechanism of $Ge_{1-x}Sn_x$ NWs catalysed by Au:Ag alloy droplet; (a) Deposition of seeds on the silicon substrate. (b) Precursors gas reacts with the seeds dissolving GeSn used to grow the NWs. (c) Au:Ag droplet is removed.*

Despite the first report on GeSn NWs dating back to 2003 by M.S. Seifner *et al* [290], in a few years surprising results have been achieved [100, 291]. Figure 5.3 briefly summarizes the process employed to develop the NWs provided for the electrical characterisation here. They have been synthesised adopting a continuous-flow reaction for nanowire growth on Si (001) substrates. Basically the substrate have been coated with AuAg (90:10 and 80:20) nanoparticle seeds and thereafter a solution of Ge and Sn precursors in anhydrous toluene were injected into the metal reaction cell using a syringe pump at a constant rate of 0.025 ml min^{-1} with a parallel flow of H_2/Ar at a rate of 0.5 sccm. The growth temperature was set at 440 °C. LICVD technique produces non-directional NWs growth, then they were transferred onto a Si substrate and subsequently washed with toluene and dried under N_2 flow before further characterisation.

5.4.1 Experimental procedure and process optimization

After NW growth, the final device structures have been developed using *electron beam lithography (*EBL*)*. The choice to use EBL methodology compared to the more common UV lithography is due to several considerations; first the NWs size, second the extreme precision of the process, and third but not the least, the high degree of freedom of the EBL process. Figure 5.4 shows the flow chart with the steps used to connect the NWs with metal pads, and thereby realise the final device structure. It is noteworthy that along these steps some sections was tested several times before reaching good reliability and high yield. In other words there was some "trial and error" in this procedure. Below, all the changes have been reported and explained in detail further below.

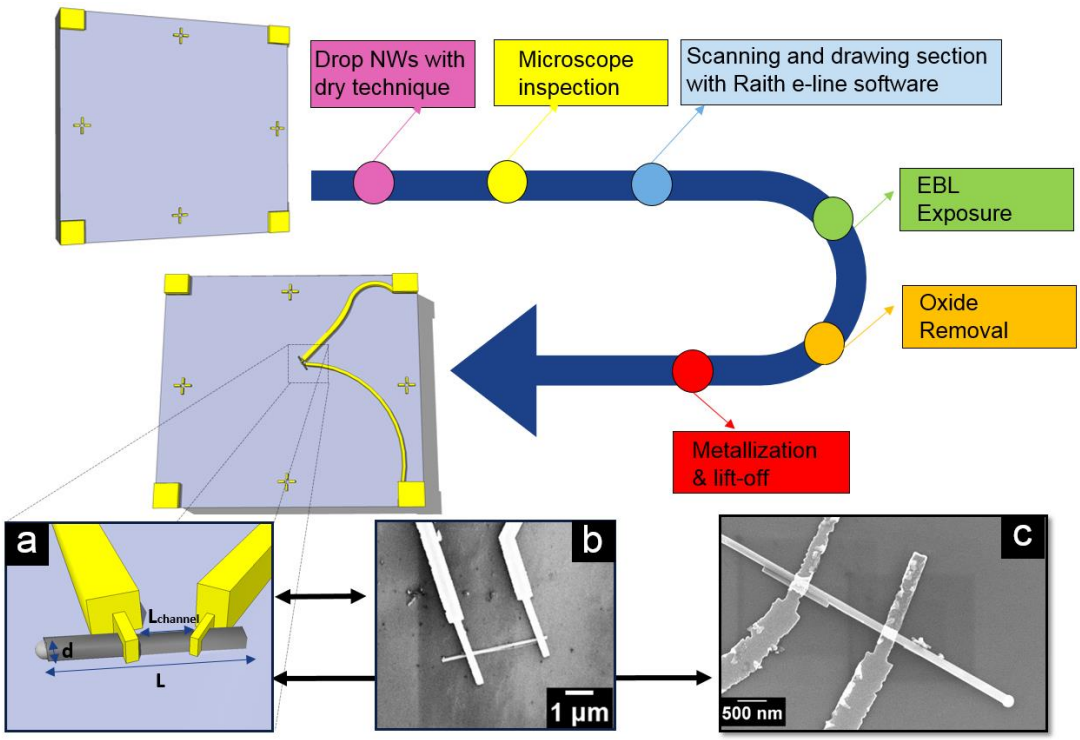


Figure 5.4: *Process flow and illustrative images of the contacting scheme for bottom-up grown nanowire devices. In the flow chart all the steps used in this work are listed with illustrative images of substrate without the contacting scheme in the beginning of the process and with the contact pattern in the end of the process. (a) A close up schematic of the device structure (b) and (c) are representative SEM images of* $Ge_{1-x}Sn_x$ *nanowire device obtained.*

Initially, NWs with different mean Sn contents ($Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$, and $Ge_{0.91}Sn_{0.09}$) were transferred onto a highly p-doped Si substrate with a thermally grown silicon dioxide (*SiO_2*) layer on top (250 nm thick). The Si/SiO_2 wafer was pre-patterned with a predefined macroscopic Ti-Au metal bonding pad pattern and cross markers necessary for the EBL alignment part. Prior to dropping the NWs, the Si/SiO_2 pre-patterned wafer was cleaned, dipping it for 30 sec in acetone, 30 sec in *isopropyl alcohol (*IPA*)*, and subsequently rinsed with *Deionised (*DI*)* water for another 30 sec to completely remove all the contamination from the top of the surface. After the cleaning, the NWs transfer procedure was tested using two different methodologies: dry and wet. Essentially the dry procedure exploits the electrostatic force, indeed the NWs have been transferred mechanically trying to be as directional as possible; while with the wet technique, NWs have been transferred dispersing a wet solution on the substrate.

Figure 5.5 shows the two techniques with the respective steps needed to transfer the NWs. It is clearly visible that the dry technique allows us to obtain a spread and

directional deposition compared to the wet solution, where the NWs tend to agglomerate themselves in the form of clustered structure. Moreover using the dry technique was also possible reduce the IPA contamination on the surface obtaining homogeneous resist deposition as shown in the optical microscope image in Fig. 5.5.

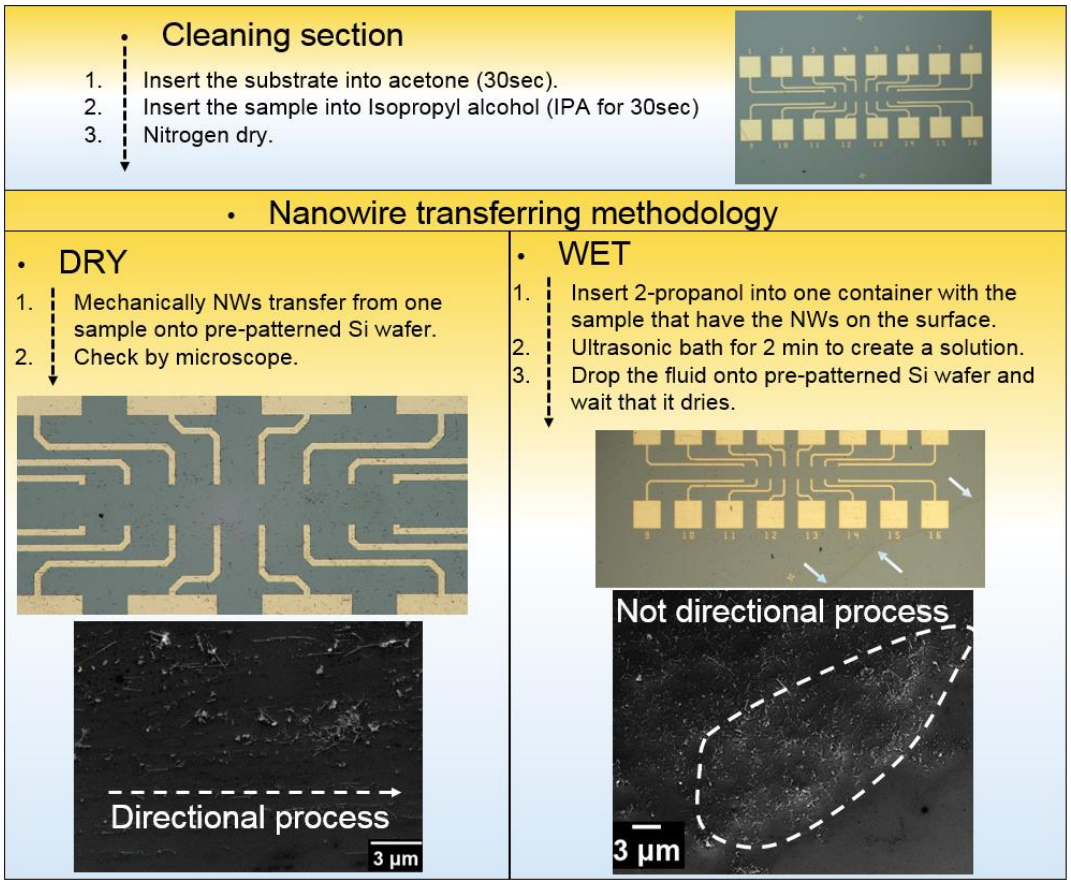


Figure 5.5: *Process flow for dry and wet NWs transferring technique, along with representative optical and scanning electron microscopy images selected from the work done.*

Subsequent to the NWs transfer, the substrate has been subjected to microscope inspection. Basically each sample was initially scanned by SEM, to obtain the correct position of the NWs and subsequently the contact paths have been drawn using Raith e-line software. Following, 150 nm of *poly methyl methacrylate (*PMMA*)* photoresist was spun on the sample, PMMA is widely used as high resolution positive resist for direct e-beam writing. Afterwards the sample was exposed at 10 keV to create the patterned structures. Following the exposure they were developed for 75 sec in a specific solution (AR 600-56) and subsequently rinsed in IPA for other 30 sec.

Directly after the S/D contact region exposure and development, the samples underwent a native oxide removal in the exposed surfaces. They were dipped for 10

sec in a BOE solution (6 parts 40 % NH4F and 1 part 49 % HF), 30 sec in DI water and subsequently dried with a nitrogen gun. The oxide removal part was critical due to the tendency of the native oxide layer to regrow as soon the sample was in contact with air. Therefore to avoid the exposure with air as soon as the etch section was finished the sample was immediately transported into a metallization chamber using a sample preserver filled with nitrogen.

The metallisation was carried out in a FC2000 electron beam evaporator at a pressure of 6.6×10^{-5} Pa. A thermal treatment for stanogermanidation formation was not applied in this work to date. The metal thickness deposited has been chosen according to the standard lift off procedure that requires a metal depth maximum of half of the total resist thickness. Therefore firstly 25 nm of *nickel* (Ni) has been deposited to improve the adhesion with the underlying material and subsequently 35 nm of *gold* (Au) has been spilled on top to improve the electrical contact performance. The source and drain contacts lie on top of SiO_2 in regions away from the NWs and do not contact the Si substrate. At the end the devices were inspected by SEM again as shown in Figure 5.6 in order to detect possible misalignment and errors.

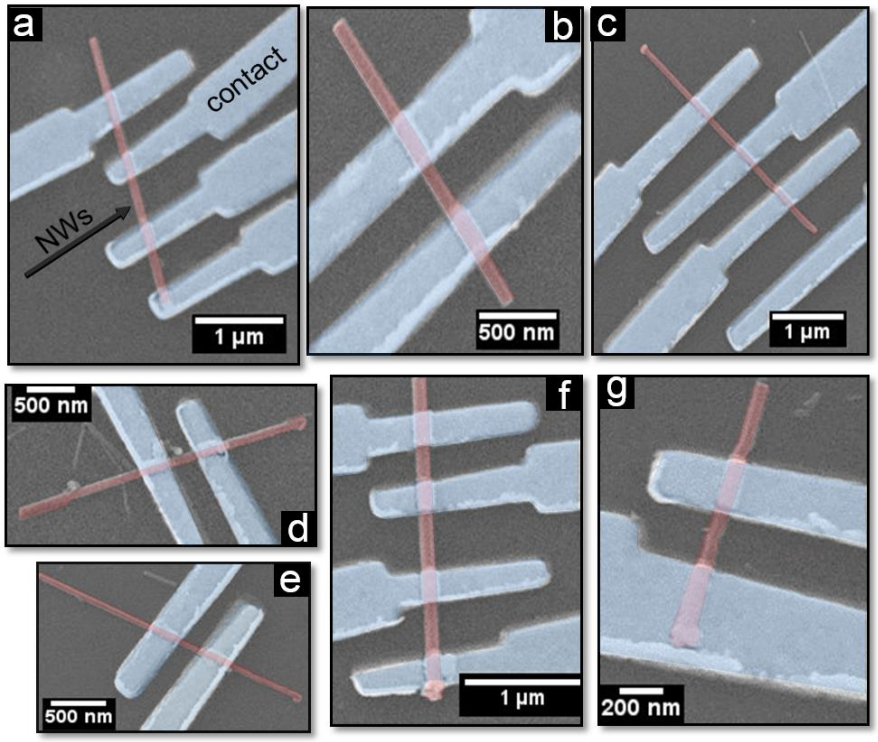


Figure 5.6: *Representative SEM images using different magnification for the three different undoped NW obtained after the processing steps. Blue and red highlight the contacts and the NWs respectively. Images (a),(b),(c) correspond to* $Ge_{0.97}Sn_{0.03}$*; (d),(e) to* $Ge_{0.94}Sn_{0.06}$ *and (f),(g) to* $Ge_{0.91}Sn_{0.09}$ *.*

5.4.2 Results and discussion un-doped NWs

Thereafter, some of the most important electrical parameters of $Ge_{(1-x)}Sn_{(x)}$ doped and un-doped NWs devices have been extracted and compared with planar structure devices present in literature. The benchmark is going to show the potential and possible future applications of $Ge_{1-x}Sn_x$ NWs device made by bottom-up approach.

5.4.2.1 Electrical characterisation

In this section the electrical performance of undoped $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$, and $Ge_{0.91}Sn_{0.09}$ NWs are reported. Overall more than 50 devices have been prepared for each Sn content and the most reliable results have been selected to extract the electrical trend , excluding devices where the contact tracks were open circuited.

The choice of undoped NWs is due to several bottlenecks related to doping, such as the extreme precise control of the thermal budget during the doping process and the high device size variability. Therefore, NWs structure without intentional dopant impurities have been tested to report the material performance as a function of the Sn content.

Before the electrical test, each device structure was analysed by SEM to check and detect the morphological quality of the contacts and the device features, e.g. channel length and NW diameter.

Firstly for each structure, the current conduction using the top-side contacts (see Fig. 5.4.(a)) was analysed. As expected since the material is non-intentionally doped, I-V characteristic shows quasi linear behaviour through the origin, as shown by the representative data in Fig. 5.7. Red, green, and blue curves depict $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$, and $Ge_{0.91}Sn_{0.09}$ respectively, they show a really high variability even considering NWs with the same Sn percentage.

The great variance generally is caused by the Schottky barrier height formed between the metal electrodes and the semiconductor material, even if the devices were fabricated with the same identical approach and conditions. Notwithstanding the quasi linear features of most NWs, indicating a non-ideal contact, the great I-V variability might come also from other variables as the partial presence of some oxide layer at the contacts or due to the relatively low dopant concentrations within the NWs. Therefore further investigation of the NWs Schottky barrier and on doping

optimisation should be addressed in future work to possibly reduce the barrier height enhancing the tunneling current transport mechanism.

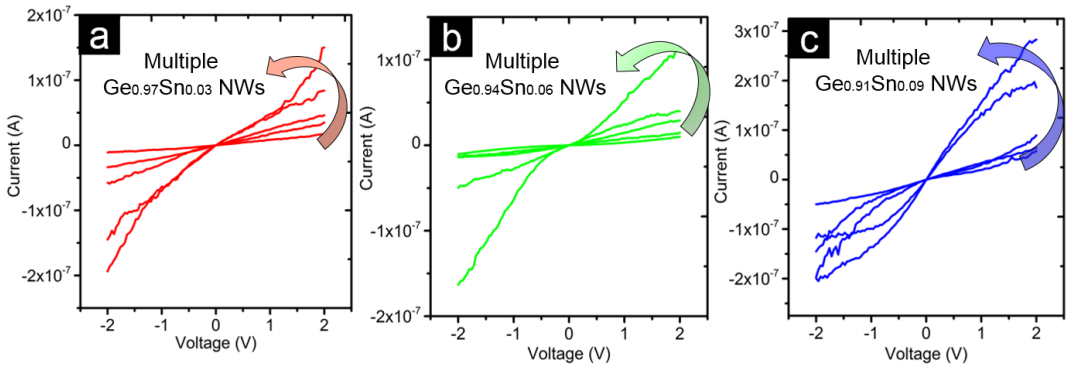


Figure 5.7: *Representative I_{ds}-V_{ds} inspection for (a) $Ge_{0.97}Sn_{0.03}$, (b) $Ge_{0.94}Sn_{0.06}$ (c) $Ge_{0.91}Sn_{0.09}$ obtained setting (V_s=0V; V_d=swept from -2V to 2V; V_{bg} = 0 V). The different lines within the images respectively represent the output of different individual NWs with same Sn content.*

After the preliminary inspection of the contact behaviour, FET transfer characteristic *(I_d-V_{bg})* measurements were performed sweeping the backgate voltage between -10 V to 10 V and setting the S/D bias voltage as -0.2 V or -1 V. The aforementioned measurement range has been carefully selected in order to avoid NW fractures due to the high current density and consequently the partial degradation of the devices.

Figure 5.8 shows representative NWs I_{ds}-V_{bg} as a function of the Sn content in the alloy. It is clearly possible to see the current modulation for all the Sn % used even without intentional doping. Although NWs are non-intentionally doped, as it is possible to see from Fig. 5.8, they show typical p-type semiconductor features. These characteristics are similar to the observed in pure Ge nanowires, that tend to accumulate holes due to the formation of a negative trapped charge layer at the semiconductor surface [292]. Furthermore, defects in bulk Ge tend to produce p-type charge, for example Romano et al. showed that damage from Ge ion implants into Ge created p-type carriers [293]. Even though these NWs were not ion implanted, intrinsic point defects within the GeSn crystal structures here are likely to be p-type in nature.

Due to the lack of p-n junctions these NW devices act as a *junctionless* (JNT) transistor, basically as resistors with a MOS gate able to control the current flow. In equilibrium state (V_g=0), setting a proper WF value, the current is not able to flow inside the NWs due to the presence of the depletion region into the channel.

Conversely as V_g exceeds the threshold voltage the NWs enters in a partially depletion state allowing the current to flow within the NW.

As already demonstrated in previous literature works, JNT physics is quite different compared with "inversion mode" devices and this feature allows superior gate control without abrupt junction formation [165, 285]. Nevertheless the potential drawbacks for the architecture are the increased requirement to control the NW size and doping in order to completely deplete the channel. The extreme JNT size variability might lead to high threshold voltage variance as well as the highly doped channel might lead to a mobility degradation due to the high surface scattering.

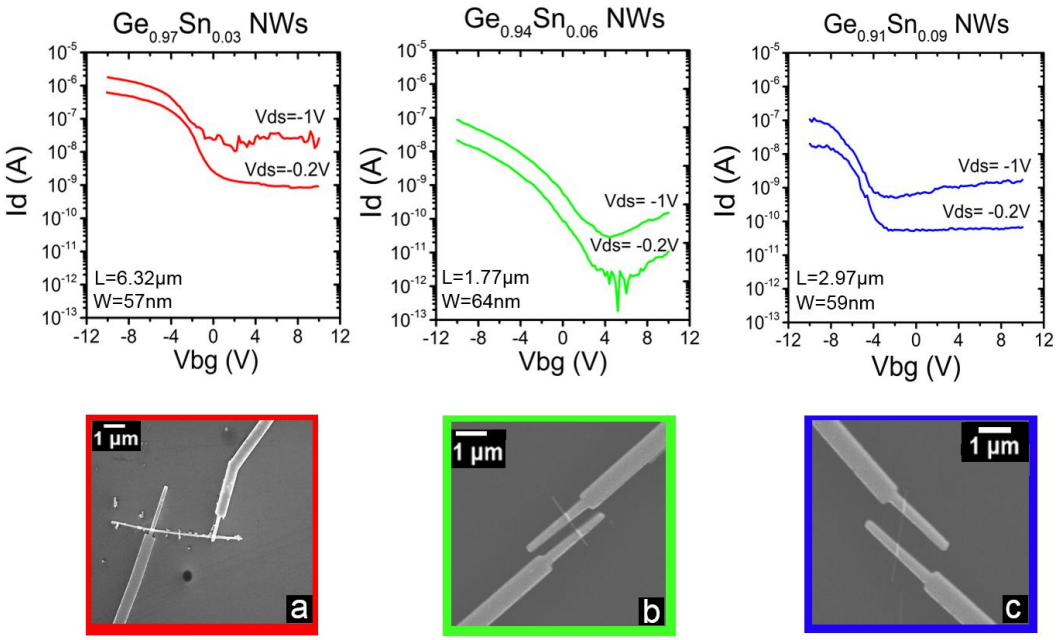


Figure 5.8: *(Top row) Representative room temperature I_d-V_{bg} characteristics for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ NWs with two different V_d values (-0.2V and -1) and specific NW dimensions inserted as inset (L and W respectively illustrate overall NW length and width). (Bottom row) Representative SEM images of typical NW devices with 3, 6, and 9% of Sn in (a), (b), and (c) respectively.*

Next, threshold voltage *(V_{th})* values were extracted using the transconductance derivative methodology at low drain voltage ($\partial^2 I_D/\partial V_g{}^2$) [294]. Basically the second derivative procedure can determine the V_{th} as the point at which the current is maximum. Fig. 5.9 shows the V_{th} variation as a function of Sn concentration in the nanowire and each point in the graph represents a unique device. The values have been categorised as a function of Sn content and from these the averaged V_{th} were calculated in order to compare the NWs with different Sn %.

V_{th} variance highlighted in the box plot in Fig. 5.9 might derive from several factors such as the NWs size variability, the surface states and effective gate oxide thickness. Therefore assuming the doping concentration roughly similar the only plausible variations might come from the different surface states, oxide thickness and device size. Nevertheless since the size variability among the NWs with equal Sn content is limited we hypothesized that the V_{th} variation come from the negative surface charge layer given by the oxides or form the underlying SiO_2 layer. Actually it is well-known that Ge surface layer has a significant concentration of electron traps approximatively located at 0.15 eV below the middle of the band gap [292]. Then if the NW Fermi level is higher than the traps level automatically an electron will fill the trap level promoting hole accumulation. Nevertheless the presence of surface states, apart from explaining the p-type characteristic, might also alter the "effective" gate potential due to a possible charge redistribution. Basically when the gate potential is applied to the NWs the overlying GeSn oxide layers, being a source of traps, might introduce a redistribution of charge and consequently a shift of the "effective" applied potential [295, 296]. The charging or discharging effect could result in a different local flat band potential and consequently to a V_{th} shift as a function of the gate voltage applied (see inset of Fig. 5.9).

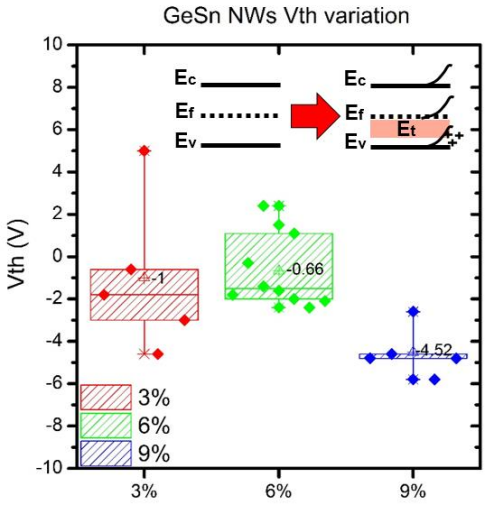


Figure 5.9: *Box plot for the V_{th} extracted as a function of the Sn % in the GeSn NWs. In black text there is the averaged number per data set, while all the values measured are presented as scattered points for the three different Sn content analysed. As inset there is an illustrative effect of the surface traps on the band diagram.*

In addition, the I_{ON}/I_{OFF} ratio, SS, and g_m, typical figures of merit to compare the electrical performance of device architectures, have also been extracted from the experimental characteristics considering 30 % of the V_{gs} swing, below V_{th}, is assigned to the off state while the remaining 70 % is assigned to the on state [297]. This methodology allows us to compare the device performance as a function of the different Sn content. Since all the devices fabricated show very wide variations, mean data have been estimated using a plot box. Trends and data are highlighted in Fig. 5.10.

The highest individual device I_{ON}/I_{OFF} ratio of 10^5 has been reported in a $Ge_{0.97}Sn_{0.03}$ NW device, however based on the average values it is clearly visible that I_{ON}/I_{OFF} ratio decreases with increasing Sn %. A possible reason for the decreasing trend is due to the relative I_{OFF} current gain coming from the bandgap reduction as the Sn content increases in the alloy.

Concerning SS, $(\partial(\log_{10} I_{DS})/\partial V_{GS})^{-1}$, the values for each dataset have been extracted at the midpoint of the subthreshold characteristic. As expected using a back-biasing device architecture, the values reported are quite large compared with a typical top-gate biasing FET. The mean value of SS varies from 2164 mV/dec, obtained for the $Ge_{0.97}Sn_{0.03}$ NWs, to 1525 mV/dec for $Ge_{0.91}Sn_{0.09}$ NWs. The minimum of SS value reported for individual NWs are 1081 mV/dec for $Ge_{0.97}Sn_{0.03}$, 426 mV/dec for $Ge_{0.94}Sn_{0.06}$ and 829 mV/dec for $Ge_{0.91}Sn_{0.09}$ respectively. Despite the magnitude of the SS variation for each set of NWs, it was possible to observe a decreasing trend in SS with increasing Sn content. Top-gating and a gate-all-around device architecture would be necessary to reduce these SS values in future work.

Conversely, mean transconductance ($g_m = \delta_{Id}/\delta_{Vbg}$) shows a decreasing trend as the Sn % increases in the alloy. The mean value varies in the range 0.02-0.09 µS with the maximum value of 0.28 µS detected for $Ge_{0.97}Sn_{0.03}$ NW devices. All the parameters extracted have been summarized in Table 5.2.

We speculate that both the SS improvement and the g_m deterioration as a function of Sn content are strictly correlated to the material bandgap reduction that in one case encourage the tunneling effects affecting the SS, but in the same time leads to the formation of higher leakage current that tend to degrade the g_m values.

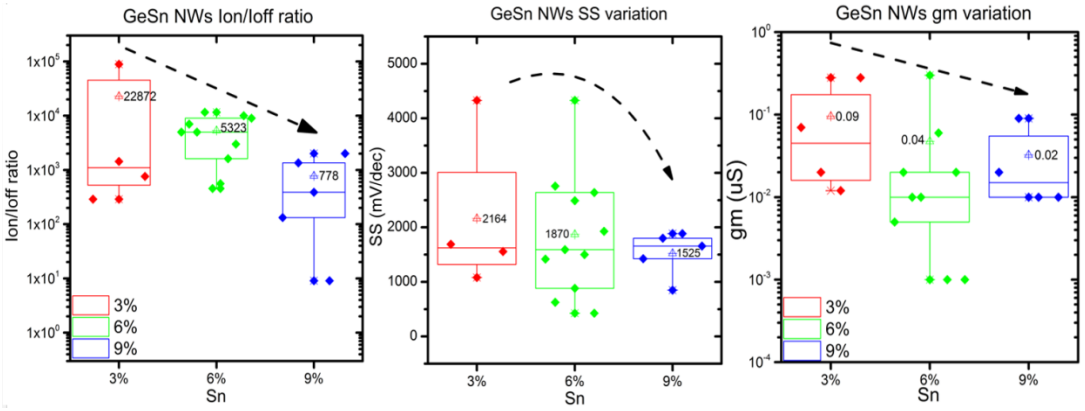


Figure 5.10: *Bar plot of I_{ON}/I_{OFF}, SS, and g_m extracted from GeSn NW FET devices, as a function of the Sn %. Red, green and blue data will refers respectively to 3% , 6% and 9% Sn content. On each bar the dispersion with the highest and the lowest point has been reported, while the average value has been written in black and highlighted with different symbol.*

$Ge_{1-x}Sn_x$ NWs	**Electrical parameters**			
	I_{ON}/I_{OFF} ratio	*SS* (mV/dec)	g_m (µS)	V_{th} (V)
$Ge_{0.97}Sn_{0.03}$	2.28×10^4	2164	0.095	-1
$Ge_{0.94}Sn_{0.06}$	5.32×10^3	1870	0.047	-0.66
$Ge_{0.91}Sn_{0.09}$	7.80×10^2	1525	0.032	-4.52

Table 5.2: *Summary of the averaged values for the GeSn NW FET devices in this work as a function of the Sn % in the alloy.*

Trends shown in Fig. 5.10, reported in Table 5.2, might be understood taking into account the gate electrostatic effects. Generally in a p-type device for $V_g>0$ holes are depleted from the channel leading to a conductivity reduction; while the opposite behaviour will happen for $V_g<0$. In the case studied, since the devices shows p-type behaviour, by reducing V_g we observe a remarkable current increment due to the band bending in the channel.

The off current increment and the theoretical reduction of the B_g with increasing Sn % explain the good electrical performance for the $Ge_{1-x}Sn_x$ NWs with a Sn content up to 6 %. Beyond 6 % it appears that $Ge_{1-x}Sn_x$ alloys become difficult to manage for electronic applications particularly in a back-gate device architecture, due to the lower electrostatic control compared to a top-gate or gate-all-around architectures.

Furthermore for the JNT device structure the width of the channel is extremely critical to define the electrical performance. Therefore in Fig. 5.11 there are scatter plots regarding the I_{ON}/I_{OFF}, SS and g_m as a function of NW width for the three different Sn compositions.

For the current ratio and the g_m it is difficult to find a clear trend due to the diameter sizes that are relatively large for the JNT design; in addition the NWs are un-doped, meaning that they are likely to be fully depleted when off, and partially depleted when on. While for the SS, even slightly, it is possible to see that the value get worse as the width decreases.

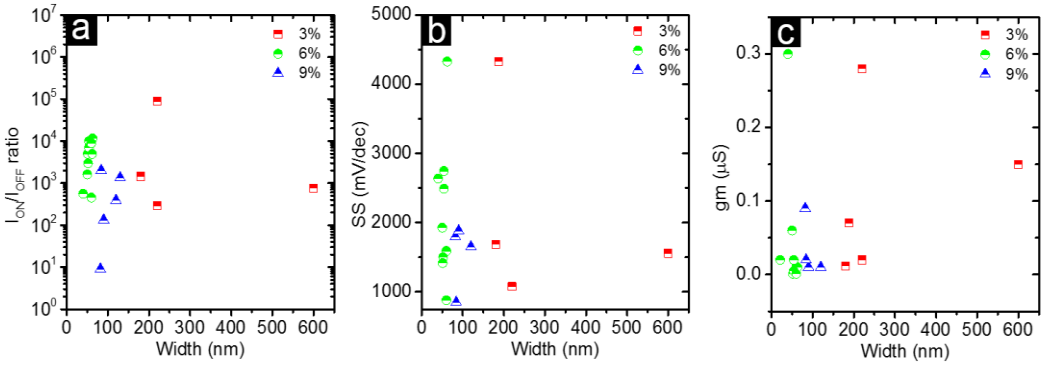


Figure 5.11: *Scatter plot of (a) I_{ON}/I_{OFF}, (b) SS and (c) g_m as a function of NW width for the three different Sn compositions. In all three plots red, green and blue markers will respectively refers to Sn content of 3, 6, and 9 %.*

Subsequently the carrier mobility, another key electrical parameter, was extracted from the transfer characteristics considering the devices in the linear region and using equation 5.4.

$$\mu = g_m L/(WCV_{sd}) \tag{5.4}$$

Since the device acts as Junctionless transistor (JNT) with small doping concentration the depletion region of the device strongly influences the control over the channel lengths; the NWs are completely depleted in off-state and completely accumulated in on-state. Thus we assume the device width is the entire width of the NW. Therefore to take into account the previous feature the device geometric factors have been inserted in the mobility formula. L and W are respectively NW length and width, V_{sd} is the bias between source and drain; C is the capacitance for a backgated nanowire device [298] obtained using equation 5.5

$$C = 2\pi\varepsilon\varepsilon_0 L(\cosh^{-1}(\frac{d+2h}{d}))^{-1} \tag{5.5}$$

With ε as the dielectric constant of the SiO_2 layer of h thickness, and d is NWs diameter. Usually carrier mobility refers to both electron and hole mobility and in general it characterises how quickly an electron/hole can move through a metal or semiconductor, when pulled by an electric field.

For semiconductor materials mobility is a crucial factor because it defines the transistor output. The FET performance might vary depending on the mobility achieved for the particular configuration and material used and almost always, higher mobility means better device performance. Semiconductor mobility hinges on several physical and environmental factors such as the doping level, defect concentration and temperature. In literature several studies on JNT mobility have been made [299, 300] highlighting the advantage of this device design. In the JNT configuration the most critical contribution for the mobility degradation comes from Coulomb scattering, while phonons and surface scattering contribute play a minor role [165, 300].

Taking into consideration the different size of the NWs, the carrier mobility was extracted for all the devices using the maximum g_m value according to equation 5.4. The average carrier mobility was evaluated for the three different GeSn compositions and the values obtained were 2.67 cm^2/Vs for $Ge_{0.97}Sn_{0.03}$, 8.51 cm^2/Vs for $Ge_{0.94}Sn_{0.06}$ and 11.87 cm^2/Vs for $Ge_{0.91}Sn_{0.09}$ respectively.

Nevertheless the values obtained using previous methodology tend to underestimate V_{th} and carrier mobility due to the non-negligible contribution of the contact resistance. Therefore to take into account the contact resistivity contribution, the Y-function method was used [301] to extract both V_{th} and carrier mobility. Usually the most common two-terminal methods are the Y-function and *transfer-length methods* (TLM). However due to the difficulty to develop specific pattern on $Ge_{1-x}Sn_x$ NWs, the contact resistance contribution has been estimated using the Y-function method. In comparison, the split C-V measurement is a more detailed technique used to extract the FET electrical parameters, considering the device size, however this method becomes problematic due to non-negligible overlap capacitance values at scaled dimensions. In a recent work, the Y-function methodology and the split C-V measurement have been compared, and have been shown to produce similar results.

The Y-function technique relies on the transfer characteristic scan (I_d–V_g) of an individual device in linear regime. If the transconductance g_m starts to decrease from a certain V_g (usually for large values of V_g and small channel lengths L), then the contact effect starts to dominate the mobility attenuation, therefore a contact

resistance and a contact-free transistor mobility can be extracted from the Y-function using equation 5.6.

$$Y = \frac{I_{ds}}{gm^{\frac{1}{2}}} = (\frac{W}{L}\mu_0 C_{0x} V_{ds})(V_{gs} - V_{th}) \quad (5.6)$$

From the equation (5.6) is possible extract respectively the carrier mobility and the V_{th} from the slope and the intercept of the curve, as shown in Fig. 5.12(a). In addition, using the Y-function methodology contact resistance *(R_C)* of the backgate MOSFET device using the mobility degradation parameter has been estimated for each sample using equation 5.7.

$$\theta = \left[\left(\frac{I_{ds}}{g_m(V_{gs} - V_{th})}\right) - 1\right]/(V_{gs} - V_{th}) \quad (5.7)$$

After the extraction, the parameter values have been inserted in the following equation $\theta = \theta_0 + R_c C_{ox} \mu_0 \frac{W}{L}$. θ_0 represents the mobility degradation factor related to the channel scattering, considering that at large values of V_{gs} ($V_{gs} - V_{th} = 10V$) it is negligible [302]; therefore the major contribution comes from the second term.

In Fig. 5.12.(b) there are the values of R_C extracted. Figure 5.12.(c) shows the V_{th} variation after the removal of the R_C contribution. It is possible to see that the V_{th} decreases drastically compared with previous data in Fig. 5.9 for $Ge_{0.97}Sn_{0.03}$ and $Ge_{0.91}Sn_{0.09}$ respectively changing from -1 to -7.25V and from -4.25 to -9.25 V; while for $Ge_{0.94}Sn_{0.06}$ V_{th} shows a different trend moving from -0.66 to -0.25V. This highlights the importance of extracting and removing the R_C contribution when estimating electrical parameters from this type of nanowire devices.

Figure 5.12.(d) shows the mobility extracted considering the Y-function in equation 5.7; it is noteworthy that mobility data reported earlier do not take into account the contribution of the contact resistance (2.67 cm^2/Vs for $Ge_{0.97}Sn_{0.03}$, 8.51 cm^2/Vs for $Ge_{0.94}Sn_{0.06}$ and 11.87 cm^2/Vs for $Ge_{0.91}Sn_{0.09}$). With the contribution of R_C accounted for, the μ values become 4.25 cm^2/Vs for $Ge_{0.97}Sn_{0.03}$, 14.54 cm^2/Vs for $Ge_{0.94}Sn_{0.06}$ and 14.88 cm^2/Vs for $Ge_{0.91}Sn_{0.09}$ respectively. Therefore from Fig. 5.12.(d) it is evident that for all the NWs the carrier mobility increases by 60, 70, and 25 % for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ NWs respectively on average, again highlighting the importance of removing the R_C contribution.

Data extracted are in accordance with previous work found in literature [151] where the carrier mobility increases as a function of the Sn % due to the proportional increment of the channel compressive strain and or electronic structure variations such as the lower effective mass which boosts the hole mobility; whilst the major mobility limitations are the phonons and alloy scattering. Note, as expected in a 3D structure like a nanowire, with surfaces on all sides, and consequently enhanced surface carrier scattering, the mobility values are lower than those extracted in thick-films which have minimal surface scattering effects.[103, 106, 108, 275-277]

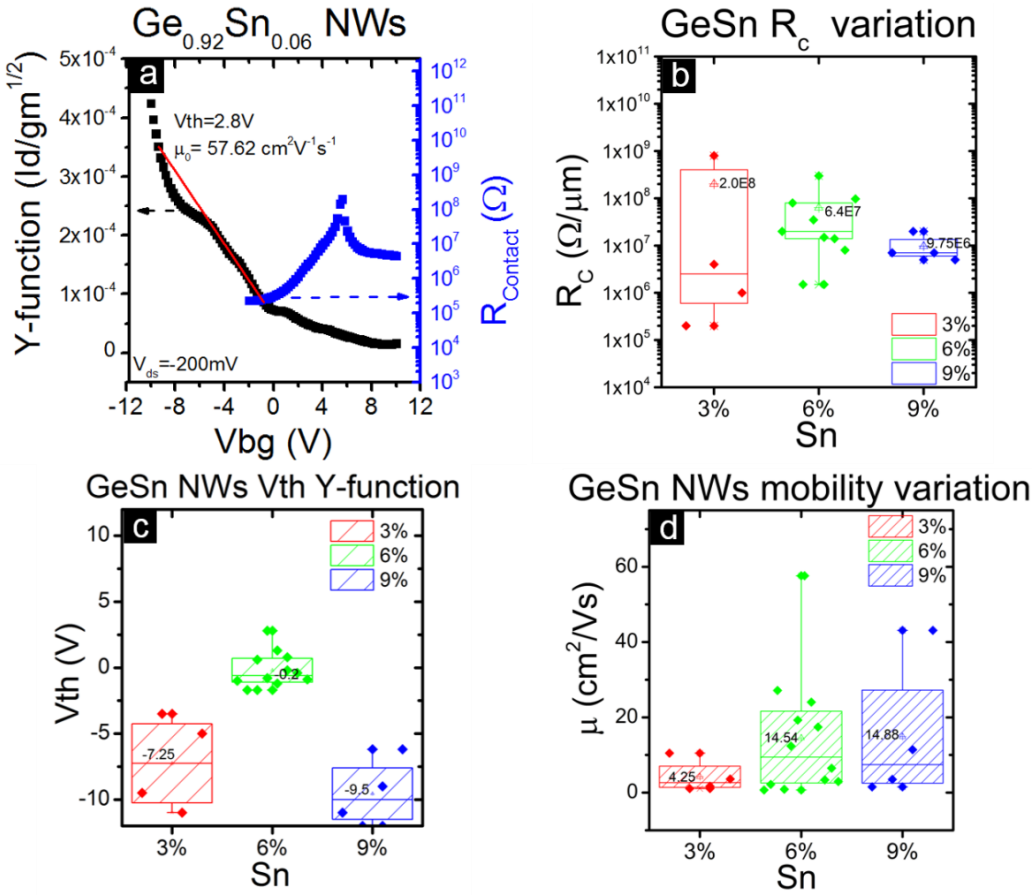


Figure 5.12: *(a) Y function and contact resistance extraction for a representative 6 % Sn NW device. (b)* R_C *extracted as a function of the Sn %, (c) and (d) show respectively* V_{th} *and mobility trends after the Y function application. In red there are data related to 3 %, in green data related to 6 % and in blue data related to 9 % .*

5.4.2.2 Figures of merit comparison for different GeSn devices

Although several devices have been developed so far, the research on GeSn NWs is still immature; therefore in this section the electrical performance as a function of the different Sn content is discussed and compared in order to have a comprehensive and systematic analysis. In Table 5.3 and Figure 5.13 are the most common electrical parameters obtained to date on experimental devices with different architectures and GeSn channel compositions considering process temperatures below 1000 °C [274-276, 278, 280, 303, 304].

It is noteworthy that all the documents reported, except for this work, refer to top or bottom gated planar FET devices. Nevertheless, it is possible to see that the values obtained in the present report are comparable with ones achieved in literature. Figure 5.13a shows the mobility data obtained as a function of $Ge_{1-x}Sn_x$ channel composition; most data-points are located between 0 to 50 $cm^2/V.s$ with exception of [275] and [304] that show a mobility of 162 and 423 $cm^2/V.s$ respectively. Moreover, considering the extreme sensitivity of the material with respect to process temperature Fig. 5.13b reports I_{ON}/I_{OFF} ratio as a function of the maximum process temperature used, where it is possible to observe decreasing I_{ON}/I_{OFF} at temperatures approaching 1000 °C.

In Fig. 5.13c the I_{ON}/I_{OFF} ratio versus mobility graph shows NWs benchmarked versus the planar structures, their results highlight the potential of the architecture for future works. Finally in Fig. 5.13d we observe how the VLS grown NWs compare with planar device architectures in terms of I_{ON}/I_{OFF} ratio versus Sn %. Considering Sn %, processing temperature, device figures of merit, the bottom-up NWs have potential in applications where a high on to off current ratio is important, and in particular where thermal budget and processing temperature are needed to be kept to a minimum.

Therefore in conclusion comparing GeSn device figures of merit, the VLS bottom-up grown have a clear advantage over other fabrication routes, in that the maximum process temperature is 440 °C which is relatively low, and thus compatible with back-end-of-line integration schemes in nanoelectronic chip production.

Year	2019, this work			2019 [274]	2019 [275]	2018 [276]	2017 [278]	2016 [303]	2015 [304]	2014 [280]
Sn%	9	6	3	4	5	5	2	0	2	3
Temp (°C)	<440	<440	<440	<300	500	500	>938	500	>938	N/A
Dev Strc.	NWs bot.gate	NWs bot.gate	NWs bot.gate	Planar top gate	Planar top gate	Planar bot. gate	Planar top gate	Planar top gate	Planar top gate	Tri gate
Peak μ	μ=4.3 cm^2/Vs	μ=14.5 cm^2/Vs	μ=14.9 cm^2/Vs	μ=54 cm^2/Vs	μ=162 cm^2/Vs	μ=39.3 cm^2/Vs	μ=26 cm^2/Vs	μ=19 cm^2/Vs	μ=423 cm^2/Vs	μ=31 cm^2/Vs
I_{on}/I_{off} ratio	2×10^4	5.3×10^3	7.8×10^2	1.2×10^2	2.8×10^5	1.7×10^4	$\approx 10^1$	2×10^3	3×10^2	$\approx 10^5$

Table 5.3: *Electrical parameters comparison for the most important figures of merit extracted from different $Ge_{1-x}Sn_x$ device structures. Data related to this work has been highlighted with red, green and blue as a function of the different Sn %, namely 3, 6, and 9 %.*

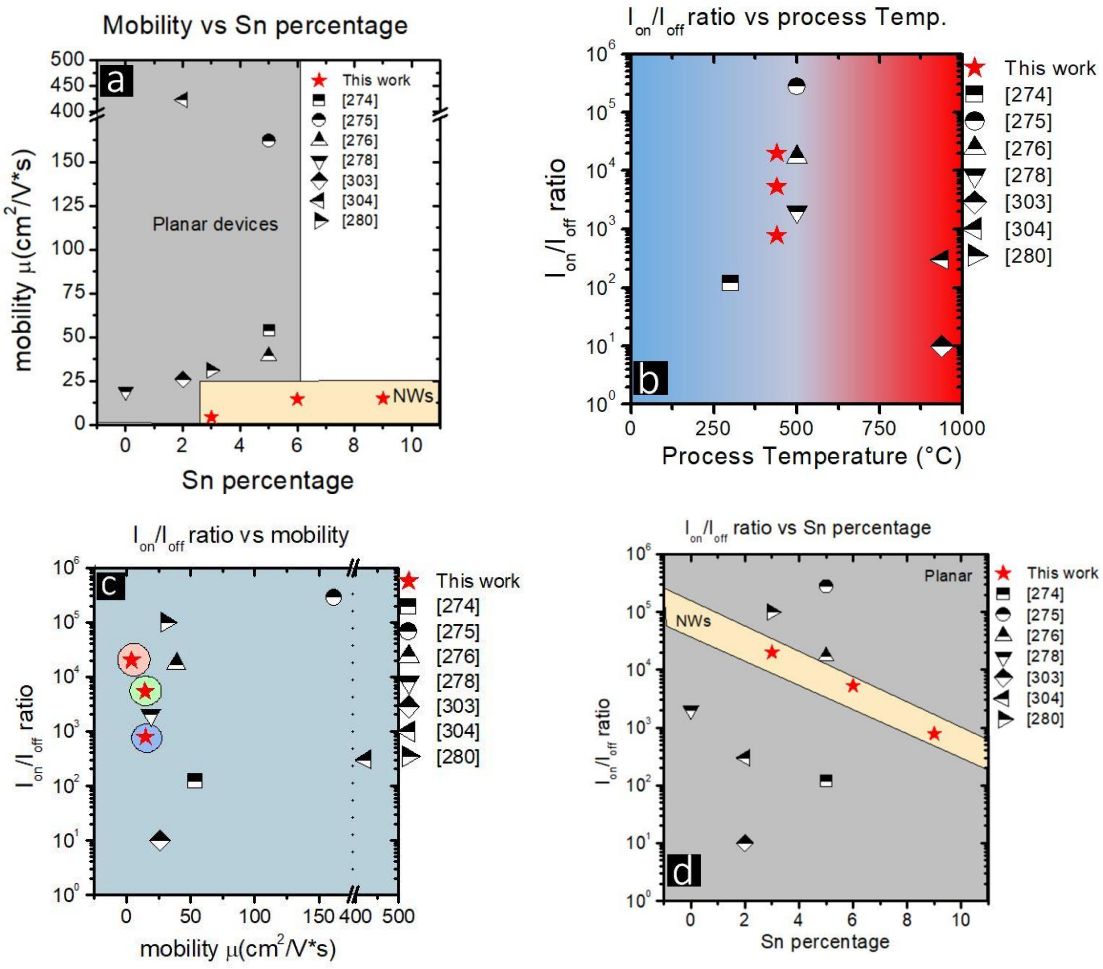


Figure 5.13: *Electrical parameter comparison with previous works found in literature (a) mobility as a function of different Sn %,(b) I_{ON}/I_{OFF} ratio as a function of the process temperature, (c) I_{ON}/I_{OFF} ratio versus mobility for NWs and planar structures, (d) I_{ON}/I_{OFF} ratio as a function of Sn %.*

5.4.3 Results and discussion in-situ doped NWs

The study previously made on non-intentionally GeSn NWs was repeated on intentionally in-situ doped NWs and outlined further below. Basically after the promising performance exhibited by un-doped $Ge_{1-x}Sn_x$ NWs, in situ doped $Ge_{1-x}Sn_x$ NWs were synthesised, processed, and tested in order to compare the device results achieved.

5.4.3.1 Experimental procedure

NWs used in this section have been developed with solution based CVD technique with the important difference that they were to be intentionally doped; then Ge and Sn precursors remain unchanged (Ge precursor was diphenylgermande while Sn precursor was Allyltributtylstannane) but in addition in the solution also P precursor was inserted (trioctylphosphine). The reaction has been carried out at 440 °C for 2h and Argon and Hydrogen gas was strictly controlled during the process. The final NWs resulted doped with phosphorus and electrical test was used to determine the dopant incorporation. In theory dopant atoms could be spread out non-homogeneously along the NW, part of them will be on the surface and part will be incorporated in the alloy producing an electrical response in terms of lower resistance than in the previous set of NWs.

The contact procedure is the same as before as was explained in Section 5.3; the only difference with the previous procedure is the NW size and Sn composition (in this experiment $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.90}Sn_{0.10}$ NWs have been used). Further below in Fig. 5.14 the procedure used to fabricate the device is summarised in a bullet list, while on the left there are the SEM images of the NWs obtained at the end of the process using different magnification.

Figure 5.14.(a) represents the SEM picture for $Ge_{0.94}Sn_{0.06}$ while Fig. 5.14.(b) and Fig. 5.14.(c) show the SEM images for $Ge_{0.90}Sn_{0.10}$. It is noteworthy that the process yield obtained for the doped GeSn NWs is greater compared with the un-doped ones due to the small NWs diameter size variability, then the metallization layer during the lift off process was able to contact more NWs.

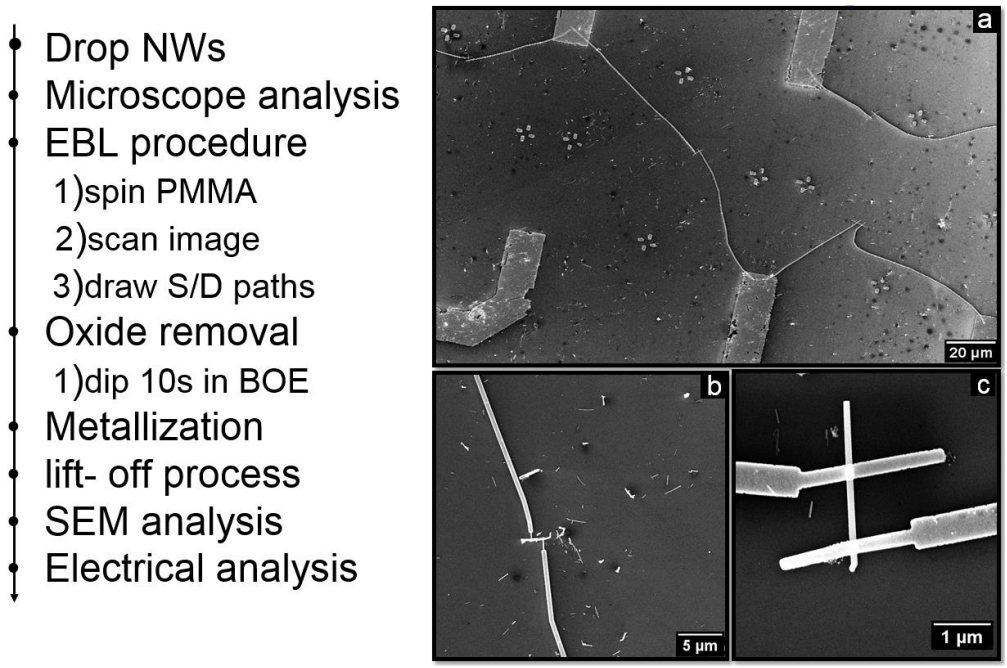


Figure 5.14*: on the right there is list of the bottom up process flow used to develop JNT with in-situ doped Ge(1-x)Snx NWs. Image (a), (b) and (c) are representative images at different zoom*

5.4.3.2 Electrical characterisation

A similar electrical test procedure has been used to classify the electrical performance of the doped JNT NWs as before. Firstly NWs have undergone SEM analysis to examine the contact connections and possible errors; afterwards only the samples that had contact tracks effectively linked with the NWs have been subjected to the I-V analysis to check the conductive path created between the S/D contacts and the NW.

Results obtained show slightly higher current amount compared with the un-doped structures even if the output was not always almost linear. The almost linear feature suggests the presence of high Schottky barrier as already reported also in un-doped structure.

Therefore the conduction enhancement has not been demonstrated and it is difficult to draw concrete conclusions about the possible doping presence. In Fig. 5.15 there are two of the most representative results obtained for the I-V current analysis. From Fig. 5.15 it is clearly visible that that the current is able to flow within the NWs even if there is high output variability among the wires.

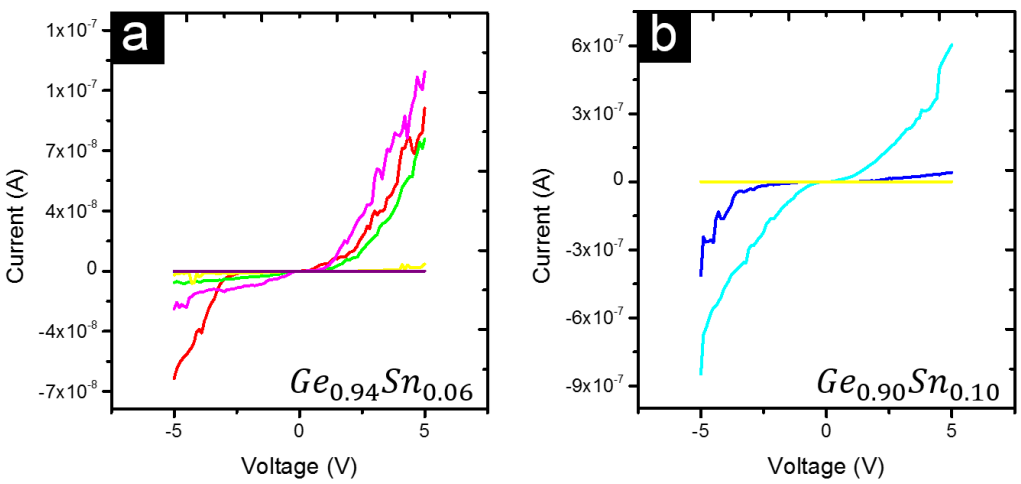


***Figure 5.15**: I-V curve obtained for JNT with doped $Ge_{(1-x)}Sn_x$ NWs. Image (a) is the characteristic of $Ge_{0.94}Sn_{0.06}$ while image (b) is the characteristic of $Ge_{0.90}Sn_{0.10}$*

After the I-V inspection only the NWs that pass the test has been undergone the backgate analysis in order to extract the transfer characteristic (I_d-V_{bg}) and extract the electrical figures of merit. Since the bias range used for the un-doped JNT NWs did not return encouraging results higher V_d and V_{bg} values have been used to stimulate the device. V_d has been changed from 50 mV up to 5V considering a V_{bg} sweep from -40V up to +40V.

Nevertheless, despite the higher horizontal and vertical electrical field, the I_d current obtained was not as expected. Basically the JNT was not able to modulate the current showing mostly a flat transfer characteristic with the presence of some hump as shown in Fig 5.16(b). The lack of ability to modulate the current might depend from several factors and they are summarized in Fig 5.16.

The first possible reason could be the presence of an oxide layer that led to the presence of higher Schottky barrier height or to the traps states formation that are hard to overcome. The second possible reason maybe be the high dopant concentration that might reduce the depletion region up to the point to compromise the device functionality without turning it completely off or finally by the presence of dopant atoms that acts as scattering centre reducing drastically the mobility within the device.

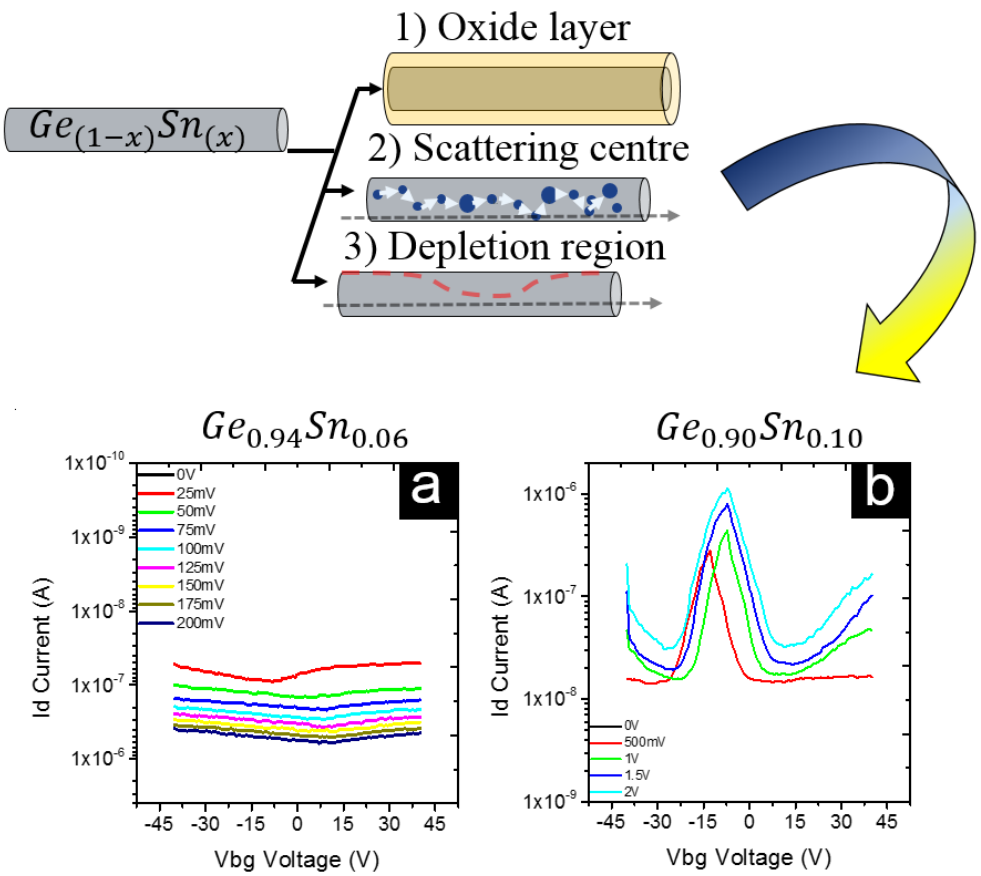


Figure 5.16: *Possible reason for the missing current modulation of the doped NWs. (a) I-V characteristics for $Ge_{0.94}Sn_{0.06}$ in-situ doped NWs, (b) representative transfer characteristics of $Ge_{0.90}Sn_{0.10}$ in-situ doped NWs.*

5.5 Conclusion

A comprehensive investigation has been made on the electrical performance of $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$, and $Ge_{0.91}Sn_{0.09}$ VLS-grown doped and undoped NWs which were fabricated using a relatively low-temperature process; with a maximum temperature of only 440 °C. From the transfer characteristics of the undoped NWs, obtained by sweeping the backgate at low V_{ds} voltage, several electrical parameters such as the I_{ON}/I_{OFF} ratio, SS, gm and mobility were extracted. Comparing the different Sn % it appears that the better electrical performance is obtained using $Ge_{0.97}Sn_{0.03}$ due to the intrinsic characteristic of the material.

The data extracted in this study represents one of the first in-depth electrical investigations of $Ge_{1-x}Sn_x$ nanowires which could potentially be used to calibrate on-going modelling studies, *e.g.* quantisation phenomena as a function of channel length reduction.

Finally, in comparing $Ge_{1-x}Sn_x$ device figures of merit, the VLS bottom-up grown have a clear advantage over other fabrication routes, in that the maximum process temperature is only 440 °C, which is relatively low, and thus compatible with back-end-of-line integration schemes in nanoelectronic chip production.

Despite the attractive results, further analysis such as the extraction of material resistivity as a function of the Sn content, using Transfer Length Method or 4-point-probe approaches, have to be addressed to assist the improvement of the device performance. The investigation of a surface passivation layer might lead to better surface control. The formation of a top gated device architecture, or the possibility to use doped nanowires with stanogermanide contacts, would lead to improved electrostatic control and a reduction of contact resistance respectively.

As a regards of in-situ doped NWs the electrical parameter extraction was not possible to perform due the missing current modulation. The difficulty to control the process steps and the challenging to direct toward extreme small scale dimension are hard to address. Therefore in future a deeper study on the doping process is required to allow doped GeSn NWs to overcome the perfomance highlighted in the undoped counterpart.

6|Top-Down Patterned Gate-All-Around devices

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6 |Top-Down Patterned Gate-All-Around devices

6.1 Introduction

As the relationship between Si and SiO_2 was broken in the 2000s, Si device performance deteriorated due to uncontrollable gate leakage current, the semiconductor industry choose to explore new materials and new device architectures for future CMOS scaling. The use of a multi-gate structures represent a substantial technology boost for the electronics industry due to the inherent enhanced electrostatic channel control.

Considering the extensive device miniaturization at which the electrical devices have undergone, the introduction of three dimensional (3D) structures (double, triple and gate all around devices) was necessary to achieve the low power consumption target [3]. Essentially, as the device dimension shrinks the development of new device architectures is a necessity to further enhance the electrical performance, because the multi-gate structures enable the mitigation of short channel effects, compared to planar structures [305].

The intensive study of new semiconductor materials, started with the approach to the 90 nm node. Ge and its alloys, in particularly $Ge_{1-x}Sn_x$, attracted the interest of the scientific community for the ability to potentially integrate both low power circuitries with optoelectronic devices by tuning the material B_g [67, 69, 162, 264, 265]. However despite $Ge_{1-x}Sn_x$ exhibiting greater theoretical potential compared to Si, the material research and the realisation of new device architectures is still at an immature point.

In the few last years with the improvement of growth techniques [71], electronic and optoelectronic high performance structures have been developed. However, notwithstanding the compatibility with Si processing platforms, as the device size shrinks several procedures and processes still need to be re-adapted and optimized. Approaching the nanometer era the necessity for extensive study of the $Ge_{1-x}Sn_x$ processing has become essential for the development of future advanced device architectures. $Ge_{1-x}Sn_x$ alloys might represent a serious candidate to replace Si in future technological nodes; therefore in this work a fabrication process of $Ge_{1-x}Sn_x$ GAA devices has been outlined using EBL and optimized selective and non-selective etching recipes.

6.2 State-of-the-art: nanometric multigate $Ge_{1-x}Sn_x$ devices

Within the recent past, $Ge_{1-x}Sn_x$ alloys has attract the scientific interest leading to extensive theoretical analysis [64, 70, 265]. To prove the astonishing $Ge_{1-x}Sn_x$ properties, several outstanding optoelectronic [76, 267, 268] and electrical devices [110] have been developed. Although the alloy easily integrate in well-established Si manufacturing process, the processing aspects need to be adapted to overcome the intrinsic material weakness, such as the low thermal stability and Sn segregation.

The first planar structures have been developed less than 10 years ago, G. Han et al. [103]; in 2011 showed the realization of p-MOSFET with a gate length of 3.5 µm. Following S. Gupta et al. in 2012 [110, 151] fabricated the first n-MOSFET with gate length in the µm range scale. Within the last years, due to the extensive investigation on the process modules such as etching [118, 119] and doping [121]; the research community has tried to jump over the µm wall by developing nm device structures, projecting the material into a new challenging era. This steady process exploration lead to different multi-gate nm device architecture development.

As a regards of FinFET structures, Y. Chuang et al. [306] reported the formation of FinFET architecture with gate length = 100 nm, with lowest reported contact resistivity and high electrical performance (SS=198 mV/dec; $I_{on}/I_{off}=10^3$); while D. Lei et al. [125] reported the highest hole mobility for the GeSn p-FinFET (208 cm^2/Vs) with 20 nm fin structure.

Conversely as a regards of GAA device architectures, a limited number of works have been recently explored; Y. -S. Huang et al. [126] developed both a single channel and the first vertically stacked $Ge_{1-x}Sn_x$ p-GAAFET.

Decananometer single (L_{ch}=90 nm) and stacked (L_{ch}=80 nm) structures show respectively extremely good SS results (single channel=103 mV/dec and 2 stacked channels=96 mV/dec); even if the stacked structure exhibited superior drive current due to the higher number of parallel conduction paths. Furthermore Y. -S. Huang et al. [307] reported the formation of triangular vertically stacked p-GAAFETs with high drive current (19.3 µA) and low SS (84 mV/dec) at low overdrive voltage of -0.5V.

Therefore considering the extremely interesting results and the rapid alloy evolution, it is imperative to think about the possibility to further investigate multi-gate structures in the decananometer range with this novel semiconductor material.

6.3 Top down Device processes

Over the last few years the feature size in *ultra-large-scale integration (ULSI)* has been continuously decreased, leading to the fabrication of nanostructures using a sky tower approach. Top down device processes are the most state-of-the-art techniques used to obtain both electronic and optoelectronic devices. Top down methodologies, conversely to bottom up approaches, rely on two essential steps: (i) the lithography, used to transfer the pattern from a mask to the substrate, and (ii) the etching, used to remove the material in excess and release the channel area from the underlying substrate. Figure 6.1 show the basic difference between the top and bottom up approaches.

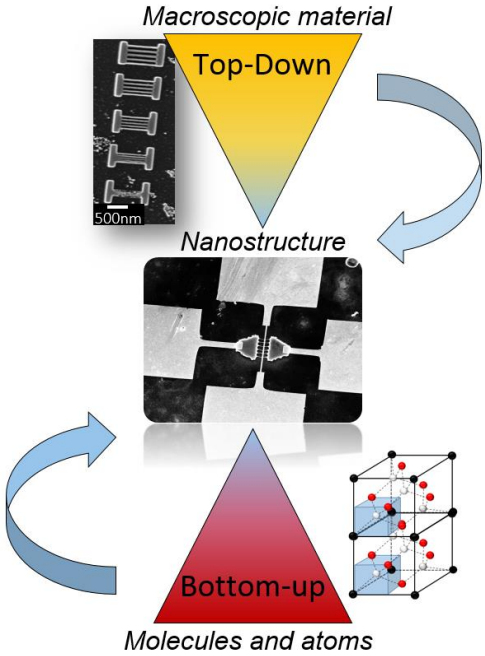


Figure 6.1: *Schematic representation of top down and bottom up approaches for the realization of nanostructure devices.*

As the technology evolves, the necessity to study and implement new lithography methodologies and refined etching recipes becomes essential to succeed in the market demand. Nowadays, various lithography techniques are used to create small features such as nano-imprinting, the self-assembled monolayers, EBL; however among all the methodologies arose in recent years, the most suitable technique used to obtain top down patterned nanometer structures is the EBL.

In addition, as the lithography processes improve, the etching procedures also need to be tailored to achieve nm features with straight vertical sidewalls. Then in this Chapter an overview of the lithography and the etching steps used to achieve $Ge_{1-x}Sn_x$ GAA structures has been outlined.

6.3.1 Experimental procedure

Figure 6.2 illustrates the starting wafer schematic used to realize the GAA structure. The two substrates were developed thorough an MBE technique and they come from collaborators in the National University of Taiwan. According to schematic representation illustrated in Figure 6.2 the two structures have different Sn content and in addition the thickness of the front end substrates (Ge VS-$Ge_{1-x}Sn_x$-SiO_2) slightly varies between them.

The un-doped substrate, reported in Figure 6.2.(a), presents 290 nm of un-doped Ge VS and on top of it there is 28 nm of $Ge_{0.92}Sn_{0.08}$.

Conversely Figure 6.2.(b) shows the doped structure where the Ge virtual substrate layer is 140 nm thick and on top of it there is a highly doped $Ge_{0.90}Sn_{0.10}$ layer.

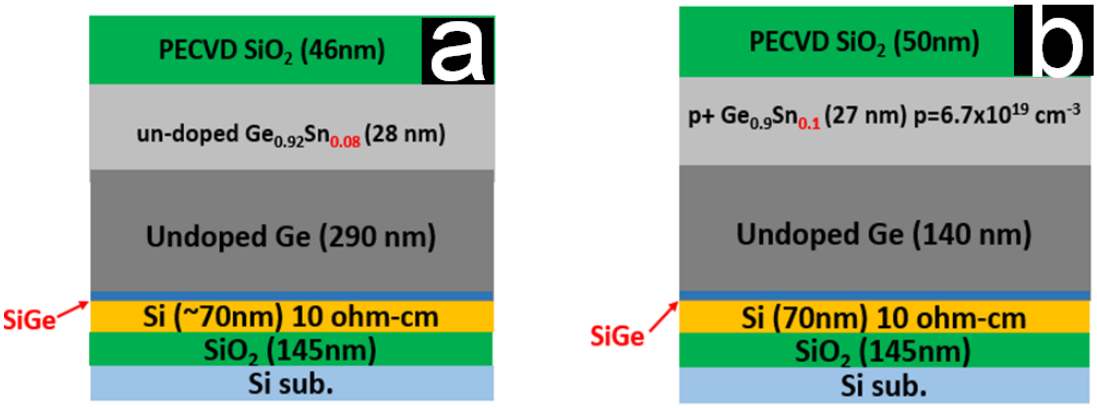


Figure 6.2: *Representative schematic of starting un-doped (a) and doped (b) substrate. Each layer was highlighted with different colour and it was labelled with the chemical composition and film thickness.*

In the present section all the lithography processes and different etching procedures are introduced to outline the most reliable process flow used to obtain GAA $Ge_{1-x}Sn_x$ patterns. Figure 6.3 shows the procedure and the schematic representation of the most representative top down processing steps used to develop both doped and un-doped GAA device.

Firstly, both doped and un-doped $Ge_{1-x}Sn_x$ substrates, have undergone a surface cleaning and native oxide removal. To remove all the possible contamination and native GeSnO, a mixture of HF:HCl (1% aq.;1% aq.) has been made; in addition all the samples processed have not undergone a water rinse but they were sealed in a nitrogen atmosphere [308].

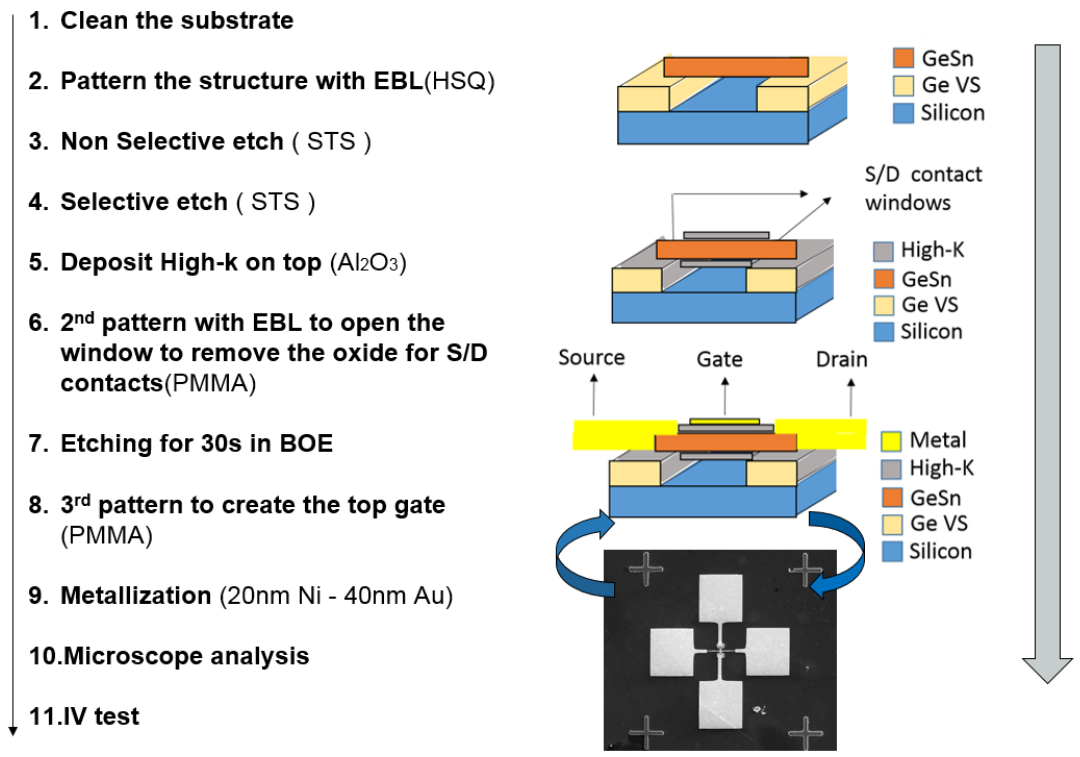


Figure 6.3: *Process flow of the top down procedure used to obtain GAA structures with schematic representation of the most representative steps.*

After the cleaning procedure, *hydrogen silsesquioxane* (HSQ) resist was spun on the samples in order to transfer the desired pattern with first exposure using Raith Pioneer machine. Since HSQ is a negative resist, the unexposed material will deteriorate during the development phase leaving the exposed section as the pattern on the surface. After the development, the samples were subjected respectively to non-selective and selective etching using respectively Cl and F based chemistry to release the channel areas from the underlying substrate.

Subsequently 8 nm of *aluminium oxide* (Al_2O_3) has been deposited on the released structure through *Atomic Layer Deposition* (ALD) and later on a second pattern has been transferred using positive tone resist (PMMA). Basically the second exposure was used to open contacts windows respectively on Source and Drain regions. Once the two contact windows have been opened, the samples were subjected to BOE etching, and afterwards a third patterning procedure was used to define the Gate, Source, and Drain paths and to create the big pads used for the electrical characterization.

Finally the metallization (deposition of 20 nm Nickel and 40 nm Gold) and lift off patterning processes have been made to contact Gate, Source and Drain.

Fig. 6.4 reports respectively the microscope image of the pattern after the two etching steps (Fig.6.4.(a)) and the completed GAA device structure after all the processing procedure (Fig.6.4.(b)). Finally, the devices have been electrically tested to extract the device performance as a function of the different gate lengths.

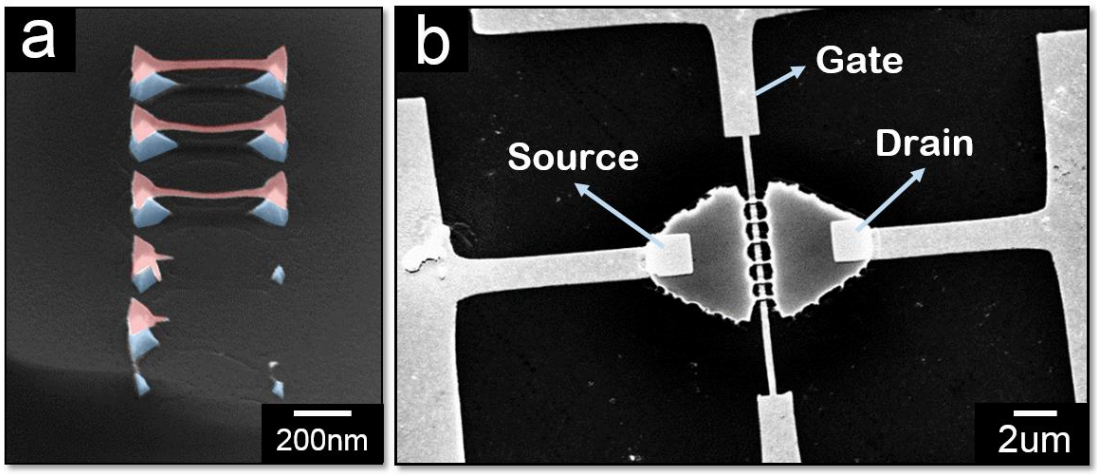


Figure 6.4: *SEM image of the GAA structure; (a) floating NWs obtained after the selective and non-selective etch steps (b) complete GAA structure after all the process steps.*

The procedure outlined was a result of the several attempts, both the lithography and the etching refinements have been extensively inspected in order to tailor the top down process. All the parameters and recipes were tuned according to the tools available in Tyndall cleanroom and in the further paragraphs the recipes are more broadly explained.

6.3.1.1 Lithography procedure

The most suitable technique to develop nanostructures at Tyndall is represented by EBL lithography. Despite the new lithography technologies that use charged particles to pattern the substrate, EBL it still is a resist-based process due to the lightweight nature of the electron. Therefore specially formulated resist undergoes a chemical reaction when exposed to an electron beam, and the final patterning result is determined by the optimization of several parameters such as the choice of the resist, the beam energy used, the development process and the exposure dose.

Although very small features (2-5 nm) have been obtained with *Poly methyl 2-methylpropenate* (PMMA) [309, 310] multiple factors such as the instability of the pattern and the low etch resistance, narrow the resist usefulness in nanometer applications.

Basing on difficulties encountered with ZEP and PMMA resists, HSQ has been used as a possible e-beam resist to develop nanometer dimension patterns [311, 312].

In literature, it has been demonstrated that high resolution patterns can be obtained mainly using ultrathin resist layers with high acceleration voltages; nevertheless other important preventive measures, such as baking the resist at lower temperatures after spinning or the usage of the weak developer at lower temperature, might improve the final yield due to the interaction of the electrons with the resist [313].

For the realization of GAA structures, three different EBL steps were necessary, they were listed below in Table 6.1. The parameters listed in the table have been obtained after the EBL dose test calibration process, and the pattern achieved showed reliable and fine structures of 25 nm line-widths. Since high resolution is required, several EBL dose tests have been made both with HSQ, used in the first exposure as hard mask, then with PMMA, used to develop respectively the S/D contact windows, and to pattern the gate. In addition the masks for each step have been made through the Raith e-beam line software.

Figure 6.4 shows all the details related to the design. Basically single-NWs and multi-NWs structures were designed, organizing the device layout in three different rows. Each row has devices with 4 different NWs lengths, respectively 1, 2, 5 and 10 µm, and in addition each row has NWs with distinctive widths, namely 100, 50 and 25 nm. Furthermore the multi-NWs design also has different gates as a function of the selected row in order to analyse the final resolution achievable (see Fig. 6.5.(a)).

Moreover, to further clarify the process flow, the three distinct mask layers are shown in in Figs. 6.5.(b), 6.5.(c) and 6.5.(d). Essentially, in the first pass the NW structure have been designed with two lateral support regions as a bridge. In the second step, a rectangular shape was designed respectively on each lateral support with the aim to open a S/D contact window, and finally the gate, the source, and the drain regions have been drawn with the specific big contact pads used to electrically test the structure.

The three different exposure steps allow us to obtain the final GAA structure.

	Resist	Spin	Post bake	dose	Energy	aperture
1st exposure	HSQ	2000rpm for 30s	180sec. at 120°C	Area=900μC/cm^2 Line=780μC/cm^2	10KeV	30μm
2nd exposure	PMMA	5000rpm for 60s	15min. at 120°C	Area=275μC/cm^2 Line=275μC/cm^2	20KeV	10μm
3rd exposure	PMMA	--	--	Area=250μC/cm^2 Line=250μC/cm^2	20KeV	10μm

Table 6.1 *Schematic table with all the parameters set for each exposure step*

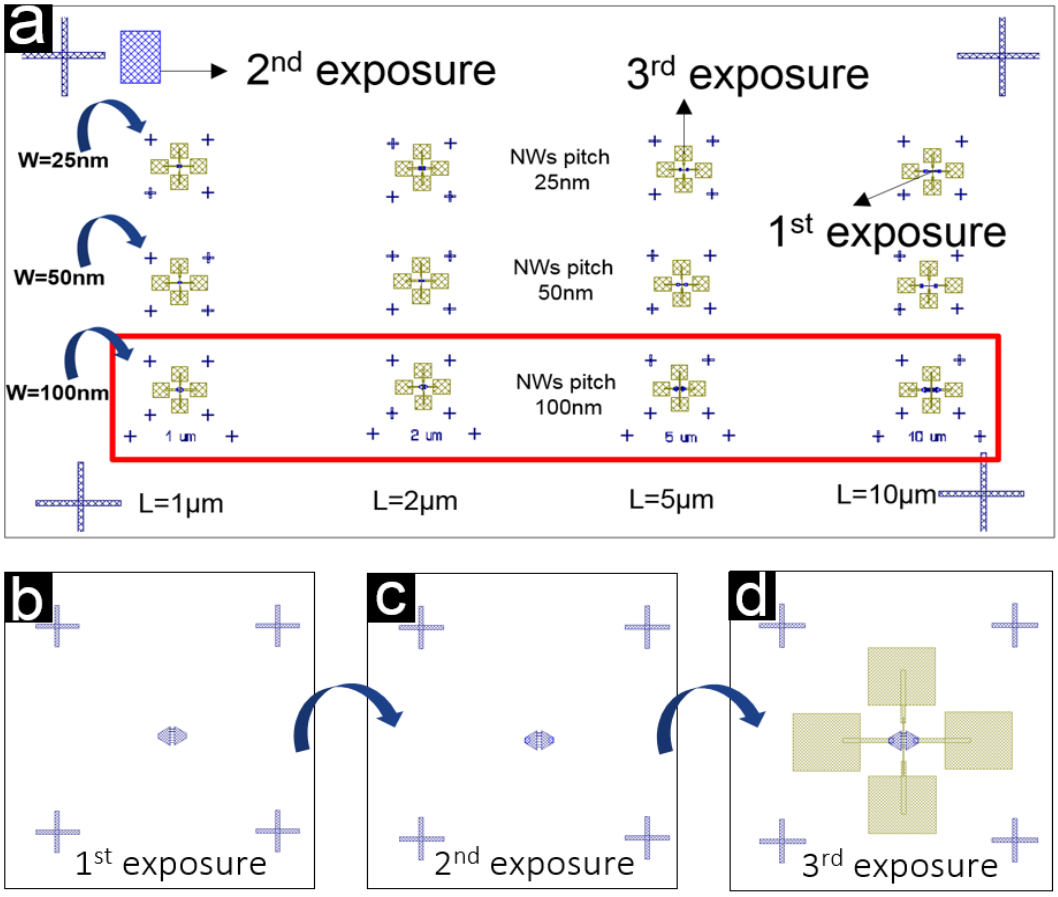


Fig 6.5: *(a) Schematic images of final GAA design; 4 different lengths respectively reported in the bottom part of the image have been defined for the structures; three rows with distinctive NW pitch (reported in the center of the image) and NWs width (reported in the left part as W) have been drafted (b) representative schematic of 1st exposure (c) 2nd exposure (d) 3rd exposure used to obtain the GAA structure.*

6.3.1.2 Etching procedures

In this section, non-selective (for pattern definition) and selective etch (for undercut and substrate release) recipes have been analysed and calibrated according to previous works reported in literature [272, 308].

To realize new disruptive device architectures such as suspended NWs it is necessary etch the pattern and afterwards remove selectively the Ge virtual substrate below the $Ge_{1-x}Sn_x$ thin layer. Gupta et al. [272] were an early demonstrator of this etch approach; they developed a F-based chemistry recipe for *Reactive Ion Etching* (RIE) with extremely high selectivity; subsequently a few other works investigated the etch process, comparing the dry and the wet etch yield [118, 314, 315].

In this Chapter a RIE with *inductive coupled plasma* (ICP) was utilised to vertically etch the active area pattern. Previous works reported the low selectivity of Cl-based chemistry compared with F-based chemistry, due to reactant sensitivity and reaction. As a regard of the vertical non-selective process, due to the higher yield obtained, Cl-based chemistry has been used in the first etch step.

The assessment of the existing recipe has been performed on the STS ICP etcher in Tyndall and a summary of the non-selective etch recipe is reported in Table 6.2. In the non-selective etch recipe, both the pressure and the bias powers were modified to calibrate the process. Essentially, to increase the chemical etch part the RF:ICP power were both reduced respecting the power ratio listed in previous work; furthermore the pressure was increased in order to reduce the ions and electron mean free path.

Etchant	**Parameters**			**Etch rate**	**Results**
ClH_4:Ar	Gas,	pressure,	RF:ICP	120 nm/min	Ge etch with low anisotropic process, pattern transferred
	8 sccm; 20 sccm;	3.75 mTorr;	RF = 20 W; ICP = 200 W		

Table 6.2: *Summary of condition and results of non-selective vertical etching process based on the recipe developed in [308].*

Moreover, below in Fig. 6.6 there are representative microscope images of the inspection post-etch. The optical microscope images show the correct transfer methodology of the lithography process (see Fig. 6.6.(a)) while the SEM inspection shows that the vertical etch was obtained.

On average the recipe developed produced a vertical etch of 120-130 nm, several structures have been inspected to determine the value. The data obtained was

acceptable since the initial sample maps show a structure with 28 nm of doped or undoped $Ge_{1-x}Sn_x$ on 700 nm of Ge VS layer. Therefore a vertical etch of at least 28 nm was required in order to overcome GeSn layer (see Fig. 6.6.(b)).

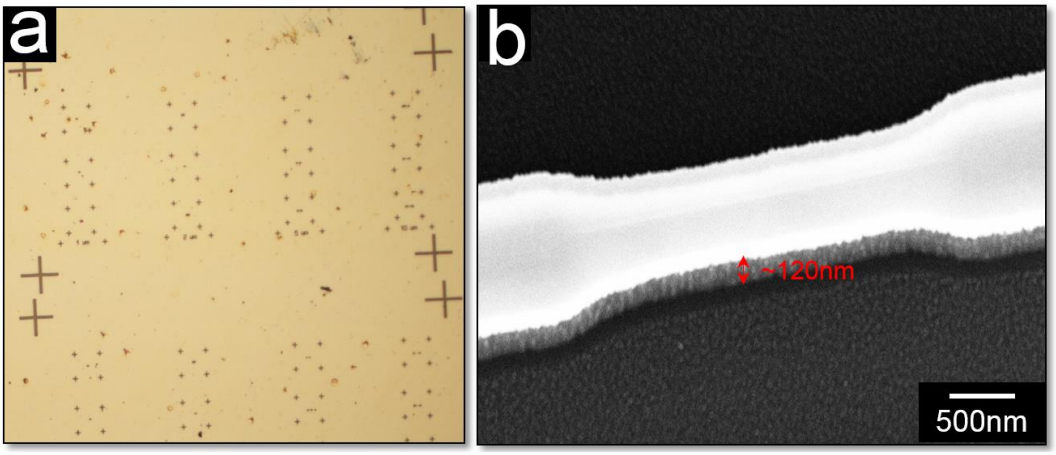


Fig 6.6: *(a) Optical images of etched pattern after the non-selective process; (b) SEM image of 2µm feature with the height of 120 nm.*

Conversely for the selective etch the F-based chemistry exhibits superb features compared with the Cl counterpart. Basically during the plasma process, the CF_4 precursor tends to produce highly reactive F radicals that will bond with $Ge_{1-x}Sn_x$ surface forming a solid SnF layer that hampers further surface reaction while the Ge reaction products are inclined to desorb.

To achieve high selectivity the chemical component in the etch has to be dominant compared with the physical aspect. Therefore ion energy and mean free path in the plasma should be low to avoid any sputtering. Then the selective etch recipe, carried out with CF_4, has been tuned as a function of the power and time to find the most reliable option to obtain $Ge_{1-x}Sn_x$ GAA structure. From the inspection, the best aspect ratio, in terms of high selectivity and low surface degradation, has been obtained using the recipe reported in Table 6.3. and the results obtained have been reported in Fig. 6.7.

Etchant	Parameters			Etch rate	Results
CF_4	Gas,	pressure,	RF:ICP	80 nm/min	Selective etch of Ge over $Ge_{1-x}Sn_x$
	40 sccm;	100 mTorr;	RF = 0 W; ICP = 100 W		

Table 6.3: *Overview on parameters and results of selective etching process based on the recipe developed in [308].*

Structures with 1 µm and 2 µm length show clearly straight NWs (see Fig.6.7.(a)-(b)) compared with 5 µm and 10 µm length that show wavy patterns maybe due to stress deformation linked to the NWs dimension. (see fig.6.7.(c)-(d).

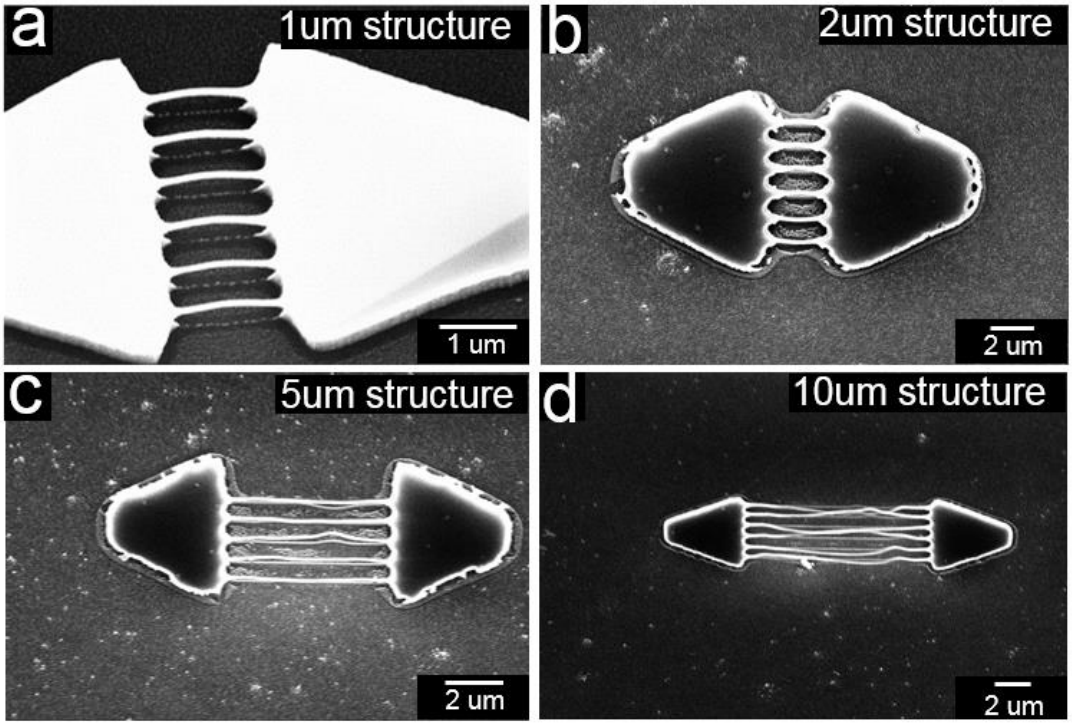


Fig 6.7: *SEM image of all the pattern drawn (a)1µm (b) 2µm (c)5µm and (d)10µm.*

Finally the S/D contact windows etch has been also inspected. Since the second step needs a PMMA resist spinning session where the material is deposited on the etched structure, the possibility that the PMMA deposited (160 nm) was removed after the wet etch in BOE solution for 20 sec was not remote. Therefore the resist layer was inspected by a profilometer and the PMMA showed a thickness decrease of only 20 nm after the wet etch. Moreover, since from SEM investigation the resist layer seemed not to be dramatically affected, it was decided not spin further resist, and thus avoid any extra mechanically stress. Indeed the third exposure has been done without spinning any other resist material.

Encouragingly, the final etch has a very anisotropic result with partially smoothed sidewalls. An under etched single- NW and multi-NW structure have been analysed with the purpose to inspect the etch recipe before the high-k deposition. Figure 6.8 shows a TEM inspection of some etching tests and SEM of the final GAA structure obtained. Superb under etch has been achieved on all structures (Fig. 6.8.(a), 6.8.(b) and 6.8.(c)) showing the ability to develop substrate-released NWs.

In addition the final GAA structure outline quality of the process (Fig.6.8.(d)) that allow to obtain GAA device architectures with $Ge_{1-x}Sn_{x.}$

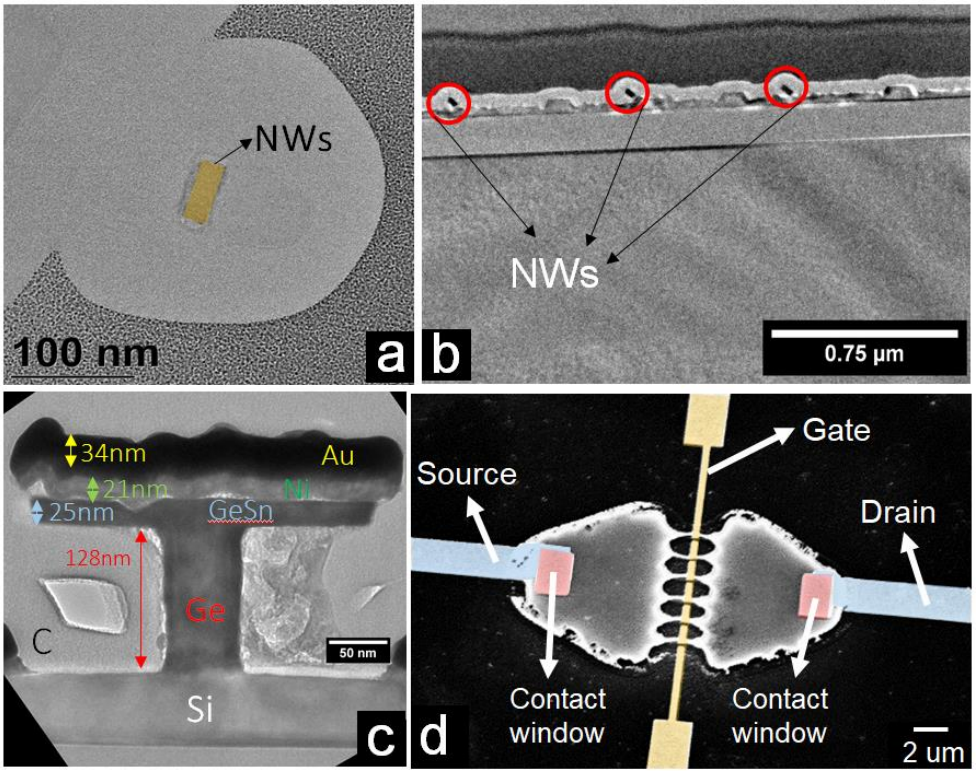


Fig 6.8: *Representative XTEM images before the high-k deposition of (a) single NW structure and (b) multi-NW pattern (c) images of non-selective etch and finally (d) representative SEM of the full device structure with all the pattern highlighted.*

6.3.2 Preliminary electrical results and discussion

After the device processing part all the samples have been tested in order to electrically characterize the GAA structure. Although the process yield was superb, almost 80%, compared with bottom-up device that shows a final yield of 30%, the electrical characterization produced good learning into the process flow, but it is acknowledged this process requires a second round of optimisation.

Figure 6.9 shows the electrical results for a doped and an un-doped GAA structure. Basically each device, both $Ge_{1-x}Sn_x$ doped and un-doped, have firstly undergone the I_d-V_d inspection (see Fig. 6.9.(a) and 6.9.(c)), to see the current flow in the NWs. The setup used had both Gate and Source contacts grounded while the Drain contact was swept from -4V to 4V. The results show that the current was able to pass within the pattern created and there was a lack of hysteresis. Charge trapping in the oxide can cause unwanted hysteresis, and might be related to surface contaminations. In any case further investigation would be needed to address the

small hysteresis variation. Subsequently the I_d-V_g test has been performed sweeping both Gate voltage while the Drain was fixed, and the Source was set to ground.

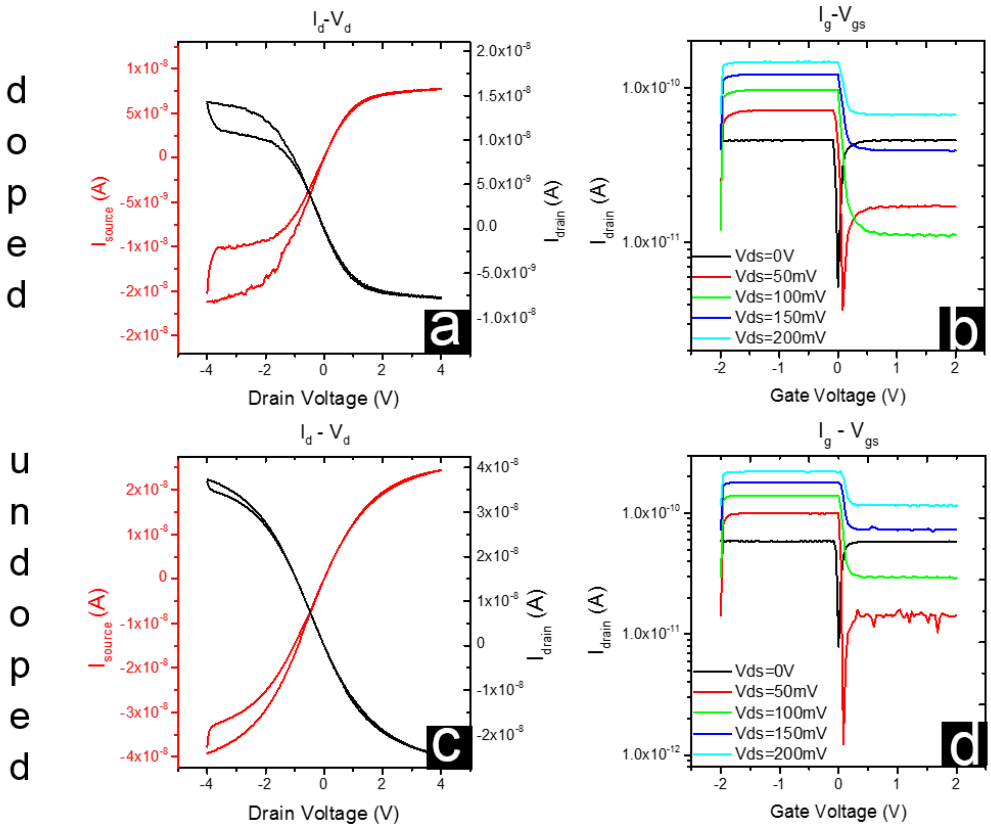


Fig 6.9: *Electrical characteristics respectively for doped (a)Id-Vd and (b)Id-Vgs and undoped (c)Id-Vd and (d)Id-Vgs $Ge_{0.91}Sn_{0.09}$ GAA structure.*

Figure 6.9.(b) and 6.9.(d) shows a lack of modulation in the I_d-V_g characteristics. Then, notwithstanding the good device processing, these specific GAA structures cannot be used as switch. From the electrical investigation a high gate leakage current was detected in fact all the measurements have been done setting the gate compliance at 100 pA in order to avoid the leakage effects.

The lack of modulation by the gate may come from an unwanted parasitic channel under the $Ge_{1-x}Sn_x$ layer, within the Ge virtual substrate. Also it was seen in the XTEM that the metal gate was not conformal around the etched structure. Both of these effects would reduce the ability to electrostatically confine and control the source-drain current. Although the doped material should exhibit lower resistance compared with the un-doped Ge material, the B_g difference is really small; therefore the thermal energy might allow the current to overflow the GeSn layer compromising the current gate control of GAA structure.

Therefore further analysis need to be addressed to trace the possible failure reason, however the top down process analysis and recipe developed in this work show the possibility to form either GAA structure, but mostly it might be easily adapted to develop other sub nm device architecture such as FinFET or microdisk.

6.4 Conclusion

In this study a top down process investigation for the realization of $Ge_{1-x}Sn_x$ GAA structures has been made. Two of the most important process aspects such as the lithography and the etching have been comprehensively investigated. EBL recipes, selective and non-selective etch have been developed for the realization of original device architecture. The process flow shows the ability to form GAA structure with exremely high resolution; nevertheless the electrical characterisation shows that the procedure needs further optimisation; particularly in terms of a longer Ge VS etch, to completely release the $Ge_{1-x}Sn_{x,}$ and an alternative process to improve the metal deposition (ALD).

Therefore further study has to be addressed to enhance the device characteristics, different process aspects such as the high-k deposition, the substrate design and the metallization procedure need to be further investigated to avoid the undesirable effects such as the tunneling path from the GeSn and the underlying Ge VS or the formation of a discontinuous metal layer unable to completely wrap around the $Ge_{1-x}Sn_x$ NWs.

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7 | Conclusion and final outlooks

7.1 Summary

Considering the unique and the astonishing features of $Ge_{1-x}Sn_x$ the alloy can be sincerely designed as future semiconductor material for both electrical and optoelectronic platforms. However several key bottlenecks as contact resistance, doping control and leakage current suppression need to be addressed before that the material overcome the most classical semiconductor. Then steadily improvements in modelling, processing and device fabrication are required.

In this work as a regards the modeling, initial study on the material properties allowed us to extract the physical alloy features as a function of different Sn content. The properties extracted through first principle analysis, were inserted into TCAD library with the aim to extract the electrical features of the material with continuum based analysis. The library created, took into account several models, and according to experimental results a calibration process was performed.

Concerning the processing, although the alloy presents great compatibility with Si procedure, the necessity to tailor the processes in accordance with the Sn content represented a key point for the material evolution. Then targeted studies were essential to boost the interest in the material.

In this thesis a comprehensive investigation on the contact formation as a function of three different metals (Ni, Pt and Ti) has been made. Considering the limited thermal budget stanogermanide layers were realized and analyzed using two different annealing procedures; the most common RTA and the innovative LTA methodology in order to extract the the most promising metal material and annealing techniques for future contact formation.

Furthermore an ex-situ doping investigation have been made to highlight the most attractive solution to obtain the right compromise between the layer doping control and the morphological degradation. Two of the most common doping techniques, ion implantation and diffusion through high dopant layer have been thoroughly investigated. The doping procedure highlighted the possibility to obtain high As implant even if only using cap layer the material showed reduced surface degradation. Therefore further study using alternative methodologies such as MLD are required to address the possibility to create shallow doped regions.

In the final part of the thesis, combining the availability of substrates with high Sn content and the ability to develop nanometer structure, innovative device configurations have been developed using both bottom-up and top-down structures. As regards the bottom-up procedure, JNT devices were realized using NWs developed by a VLS procedure. Three different Sn content ranging from 0.03 to 0.09 were inspected with the aim to extract and benchmark the electrical features of the NWs. The work show the ability to use the NWs as a switch enabling new prospective for the realization of sensor or memory applications.

Conversely for the top-down approach GAA structure have been realized and electrically tested. The structure was not able to exhibit great electrical results due to the higher leakage path between the GeSn layer and the underlying Ge material then further study are necessary to improve the device geometry or the substrate layer considering counter doped materials.

In conclusion different aspects of GeSn were detailed analyzed showing the material benefits, significant advancements on several process aspects combined with the tailored recipes will allow the integration in both electrical and optoelectronic circuitries in future.

7.2 Future works

In light of the B_g control as a function of Sn content, $Ge_{1-x}Sn_x$ alloys attract even more interest of the scientific community for the possible integration of low power electronic devices and optoelectronic circuitries.

Based on the studies reported in this thesis $Ge_{1-x}Sn_x$ future directions can be mainly articulated in three main topics: the modelling section, the processing optimization, and the realization of new device architectures.

- As a regards of the modeling section, the previous chemical and physical literature studies allowed to create material models able to predict both the electrical and the optical device performance as a function of the Sn content. Nevertheless the lack of experimental results did not permit an accurate calibration process yet. Therefore, since the model has been developed from the scratch in future it will be necessary continue to refine the library developed considering both the inclusion of more detailed models either the calibration with new experimental devices.

- Concerning the processing aspects, the necessity to develop new devices architecture such as JNT, TFET or GAA need a very accurate material control. Therefore innovative solutions to improve the material thermal stability (using alternative annealing procedure) or the possibility to optimize the contact resistance (alloying several metals) are essential to improve the future device performance. Furthermore, taking into account the future device size and the not trivial geometry, the precise control on both the doping and the etch processes represent a must for the alloy development.
- Finally the third aspect can be seen as the head of the chain, essentially all the processing refinement obtained in the last years were targeted to the realization of innovative device architectures. Therefore, considering the possibility to develop nanometer structures with precise Sn content, combined with the ability to interchange both the top-down and the bottom-up methodologies, aim for the realization of alternative device configurations able to support electrical low power devices and optoelectronics circuitries.

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