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# An Improved Linearity Ring Oscillator Based Current to Digital Converter

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***Abstract*—Many biosensors produce single-ended current outputs. Lab-on-chip applications demand parallel readout channels requiring low area current-to-digital converters. High HD2 has limited the Current Controlled Ring Oscillator's adoption as a low area, single-ended converter. This work improves CCRO open loop linearity by 10 dB. A wide-bandwidth current buffer is also designed. A low area (0.0025 mm$^2$), low power (357 $\mu$W), single-ended, 1 MHz bandwidth converter suitable for array readout is presented with measured performance.**

***Index Terms*—Data Converters, ADC, Current, Ring Oscillator, Phase to Digital, Current to Digital, VCO Based ADC, Direct Digitization, Flipped Voltage Follower, Linearization Techniques**

## I. Introduction

THE COVID-19 pandemic has created a surge in demand for new biosensors to detect viruses and other micro-organisms. Many yield an output current proportional to their stimulus e.g. electrochemical sensors, photodiodes, nanopore sensors, ISFETs etc. Lab-on-chip applications also require multiple sensors and multiple readout channels in parallel [1]. We propose a low area, low power, single-ended current-to-digital converter (CDC) which can be used in an array to readout multiple biosensors in parallel. Presently, the use of Transimpedance Amplifiers and subsequent voltage-mode ADCs limits the area and power efficiency of existing readout circuits. In this work, a Current Controlled Ring Oscillator (CCRO) is implemented as a low area CDC solution. HD2 is the performance limitation in CCROs. While pseudo-differential architectures are a common workaround, most biosensors yield a single-ended current so can't exploit differential HD2 cancellation. An improved single-ended open loop CCRO with 10 dB improved linearity, compared to a traditional CCRO, provides the highest open-loop linearity seen to date in a CCRO. The proposed architecture is shown in Fig. 1. It consists of a Flipped Voltage Follower (FVF) current buffer and an open loop CCRO-based ADC.

## II. The Proposed Circuit

### A. Flipped Voltage Follower

The FVF [2], shown in Fig. 1, is a current buffer achieving superior bandwidth compared to a traditional Common Gate (CG) stage. It achieves this with the same power consumption, noise and current dynamic range as the CG by using negative feedback. The FVF's operation is examined by considering a small voltage increase $\partial v_{in}$ at the IN pin. The drain of $M_2$ is HiZ; no current can flow downwards, but the source of $M_1$ has an impedance $1/g_m^{M1}$, so current $\partial i_{M_1}$ flows through $M_1$ to the $V_{G2}$ node. This node is high impedance (dominated by $r_o^{M_1}$ and $r_o^{M_3}$), so $\partial i_{M_1}$ causes voltage increase at $V_{G2}$, $\partial v_{G2}$. This actuates the gate of $M_2$ and thus additional current $\partial i_{M_2}$ flows through $M_2$. This $\partial i_{M_2}/\partial v_{in}$ is akin to the input impedance of a CG multiplied by $g_m r_o$. $Z_{IN}$ of the FVF is thus:

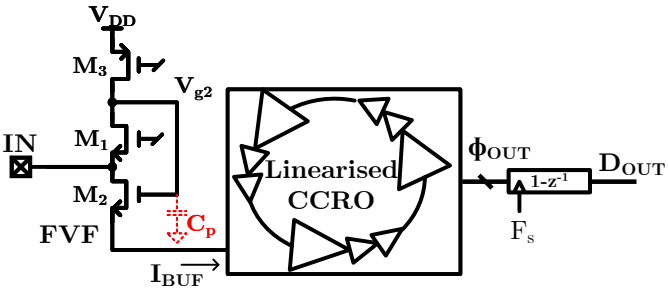



Fig. 1. Proposed readout with FVF current buffer and CCRO CDC.

$$Z_{IN} \simeq \frac{1}{g_m^{M_1}\left(1+\frac{1}{2}g_m^{M_2}Z_{g2}\right)} \simeq \frac{2}{g_m^2 r_0} = \frac{2Z_{IN}^{CG}}{A_0} \quad (1)$$

assuming $Z_{IN}^{CCRO} = 1/g_m^{M2}$. Since $Z_{g2} \simeq r_o^{M_1}$ is the impedance at the $V_{G2}$ node, $Z_{IN}$ is decreased by $A_0$, the intrinsic gain of a device, compared to a CG. Thus the FVF has a wider 3 dB point than the CG by the same margin:

$$f_{3dB}^{FVF} \simeq A_0^{M_1}\frac{I_{BIAS}\left(g_m/I_D\right)_{M_2}}{4\pi C_{IN}} \quad (2)$$

assuming the pole due to the parasitic capacitance, $C_p$, at $V_{G2}$ is much greater than that due to $C_{IN}$.

Comparing the FVF and CG in simulation, given the same bias current (3 $\mu$A) and load ($C_{in} = 1$ pF), the bandwidth of the FVF ($f_{3dB} = 101$ MHz) is 8.4× that of the traditional CG ($f_{3dB} = 12$ MHz). Usually [2], the output current is taken by mirroring M2 but in this work, the CCRO is under the FVF; reusing the FVF $I_{BIAS}$ to bias the CCRO, saving power.

### B. Improved Linearity CCRO

Previous single ended, open loop, uncorrected, MHz bandwidth CCROs have been limited by linearity to $< 6$ b ENOB [3]. This work extends linearity to $> 8.6$ b without feedback or calibration. Fig. 2a shows a traditional, inverter-based 3-element CCRO, its waveforms shown in Fig 2b. Ideally, the cell charges from GND to the $V_{TH}$ of the next inverter, ending the charging phase and beginning another. The equation for such an oscillator would be:

$$f_{CCRO}(t) = I_{IN}(t)/\left(3C_L V_{TH}\right) \quad (3)$$

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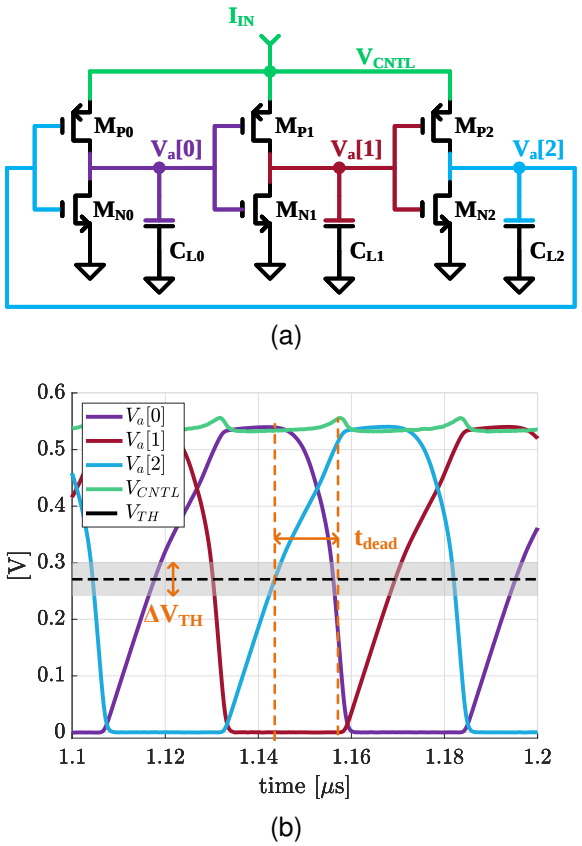



Fig. 2. Inverter-based 3-element CCRO (a) schematic and (b) waveforms.

however the circuit possesses significant non-linearities. These non-linearities are derived from two main sources, namely that $V_{CNTL}$ is not constant but varies with $I_{IN}(t)$ and that the finite time required to discharge each cell in the ring adds an additional delay into the ring named the dead time, $t_{dead}$.

Fig 3a shows that as the input current, $I_{IN}$ charges the delay cell load capacitor, $C_L$, the $V_{CNTL}$ node voltage is set by $V_{GS}$ of the PMOS device, in this case $M_{P0}$. $V_{CNTL}$ is the supply node for all the inverters in the CCRO, and so as $V_{CNTL}$ changes due to $I_{IN}$, the threshold, $V_{TH}$, of the other delay cell inverters in the ring also changes. This causes the $V_{TH}$ term in Eqn. 3 to have a log-like relationship with $I_{IN}$ and results in a very non-linear transfer charateristic. Once a delay cell has completed charging, a cell discharge must occur in order for the phase to propagate around the ring (as seen in Fig. 2b). This takes a finite time, known as the dead time, $t_{dead}$, and since the oscillator phase is not advanced during $t_{dead}$, the transfer characteristic is modified:

$$f_{CCRO}(t) = \frac{1}{(3C_L V_{TH}/I_{IN}(t)) + 3t_{dead}} \tag{4}$$

The cell discharge mechanism is shown in Fig. 3b. When $V_a[0]$ reaches $V_{TH}$ of the inverter formed by $\{M_{P1}, M_{N1}\}$ (and continues toward $V_{CNTL}$), $C_{L1}$, initially charged to $V_{CNTL}$ begins to discharge through $M_{N1}$. The time taken for this node, $V_a[1]$ to fall below $V_{TH}$ and thus for the phase to propagate is $t_{dead}$, shown in Fig. 2b. $t_{dead}$ depends on $I_{DSAT}^{M_{N1}}$, which, since $V_{GS}^{M_{N1}} \simeq V_{CNTL}$, has an approximately linear inverse relationship with $I_{IN}$. The CCRO linearity is greatly improved by keeping $V_{TH}$ constant across $I_{IN}$ and reducing

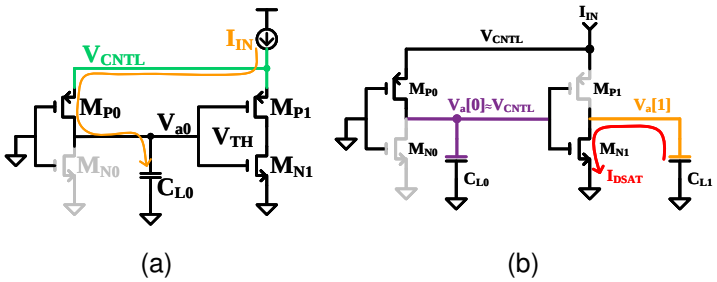
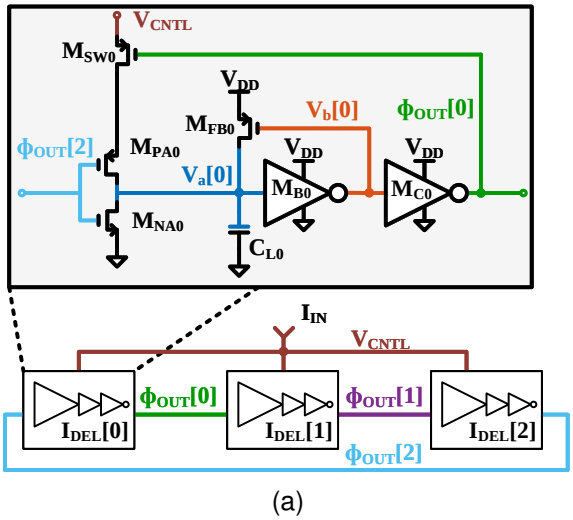



Fig. 3. Schematics illustrating (a) the effect of $I_{IN}$ on $V_{CNTL}$ and $V_{TH}$ and (b) the finite cell discharge time $t_{dead}$.



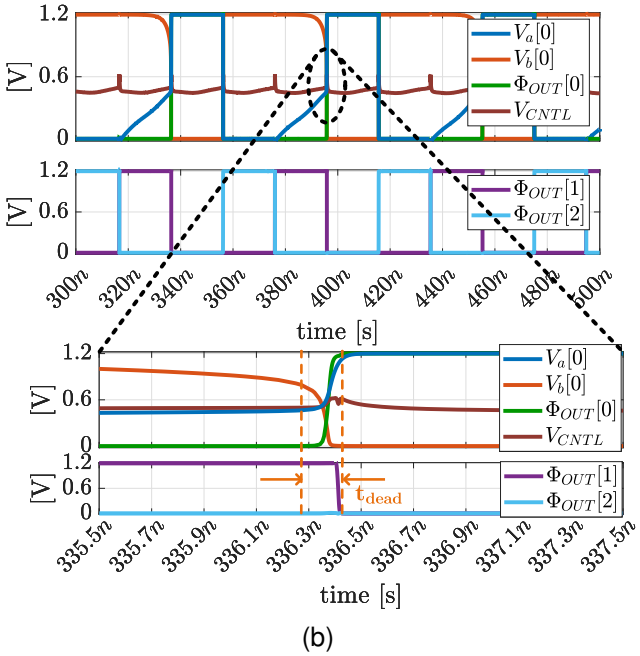




Fig. 4. (a) Schematic and (b) associated waveforms of the improved CCRO.

$t_{dead}$ as much as possible. Recent work [4] placed squaring inverters at the output of each delay cell, making inverter $V_{TH}$ constant and reducing $t_{dead}$ by driving the NMOS with a rail-rail signal. Silicon results were not provided, however, and several shortcomings were noted upon simulation, namely residual nonlinearities due to parasitic charging of multiple cells in parallel and metastability at low input currents.

An improved CCRO implementation is shown in Fig. 4a, comprising of 3 delay cells which reduces $t_{dead}$ and the dependence of $V_{TH}$ on $I_{IN}$ . $M_{B0}$ is a supply-connected inverter, so its $V_{TH}$ is constant and thus the $V_{TH}$ required for the phase to propagate to the next cell is always constant and independent of $I_{IN}$. The second squaring inverter, $M_{C0}$ provides the necessary inversion and ensures that the output of the cell is rail-to-rail (See $\Phi_{OUT}[2]$ in Fig. 4b). Thus, the first inverter NMOS of the subsequent cell (e.g. $M_{NA0}$ shown in Fig. 4a) has $V_{GS} = V_{DD}$ and the highest possible $I_{DSAT}$, greatly reducing the discharge time, $t_{dead}$. $t_{dead}$ now consists of the reduced discharge time, and also the propagation delay of the $M_B$ and $M_C$ inverters. The total delay is $< 200$ ps in the implemented circuit (see zoomed-in waveform of Fig. 4b) as compared with the 10 ns seen at the same bias point in the traditional CCRO (Fig. 2b).

At very low input currents, the cell's $V_a$ node charges slowly, causing the $M_B$ inverter to transition slowly; resulting in large short-circuit current consumption and large $t_{dead}$. A positive feedback device, $M_{FB}$, was placed around the $M_B$ inverter such that when $V_a$ approaches $V_{TH}^{M_B}$, $M_{FB}$ begins to turn on and latches $V_a$ to $V_{DD}$, causing $M_B$ to transition quickly at all input current levels. This is seen in the zoomed-in section of Fig. 4b; as $V_a[0]$ slowly approaches $V_{TH}$, it is suddenly latched to $V_{DD}$ as soon as $V_{TH}$ is reached. In a 3-element CCRO, two cells' PMOS $M_{PA}$ are on at any given time (as seen by two $\Phi_{OUT}$ signals being LOW at any given time in Fig. 4b). This is true of the traditional CCRO also and provides two paths for $I_{IN}$; the primary charging cell path and another secondary path into a cell which has already completed charging. Some unknown portion of $I_{IN}$ will leak into the secondary path and not contribute to the main cell charging, another source of non-linearity. A device, $M_{SW}$ is added to ensure that only one primary cell charging path is available in the CCRO so all of $I_{IN}$ contributes to the charging of the delay cell. The gate of $M_{SW}$ is low until the cell has received its charge, then $\Phi_{OUT}$ transitions high, turning off $M_{SW}$ and preventing any further charging until the next cycle.

The $t_{dead}$ is now the only significant contributor to CCRO non-linearity. The level of harmonic distortion is a function of the cell charge time to $t_{dead}$ ratio, so $HD2 \propto I_{IN}t_{dead}/3C_LV_{TH}$. This presents a tradeoff with the input-referred quantisation noise of the CCRO, which is proportional to $1/K_{CCRO}$, where $K_{CCRO} = 1/(3C_LV_{TH})$. $V_{TH}$ was fixed by the headroom requirements of the FVF atop the CCRO, so $C_L$ was adjusted so that the input-referred quantisation noise of the converter falls just below the input-referred thermal noise but is still large enough to provide sufficient linearity. A value of $\sim 120$ fF was chosen for $C_L$, implemented as a combination of MOM capacitor and the MOS capacitance of the $M_B$ inverter. Simulation results show that the input-referred phase noise of the improved oscillator is the same as the traditional oscillator.

## III. Measurement Results

The FVF and CCRO are coupled to form the CDC, implemented in a 65 nm CMOS process, at a supply voltage of 1.2 V. The transfer characteristics of both the traditional (simulated) CCRO and the improved (measured) CCRO are shown in Fig. 5. At the 3 $\mu$A bias point, the centre frequency is $f_0 \simeq 16$ MHz and the CCRO gain is $K_{CCRO} \simeq 5$ MHz/$\mu$A. The improved CCRO closely approximates the linear characteristic of an ideal CCRO. The traditional CCRO shows 16 % gain deviation at 3 $\mu$A $\pm$ 2 $\mu$A compared to 9 % for the improved oscillator. This improved static linearity results in lower harmonic distortion, which is illustrated in Fig. 6. The improved CCRO presents consistently lower HD2, being 9.75 dB lower at the peak SNDR point.

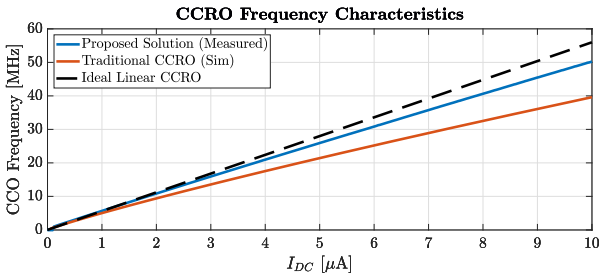



Fig. 5. CCRO transfer characteristic comparison between traditional and measured CCRO

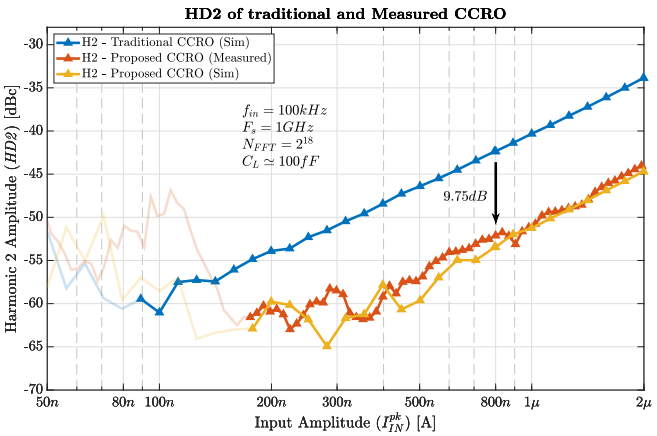



Fig. 6. Plot of HD2 vs. $I_{IN}$ comparing the traditional and measured results from the improved CCRO.

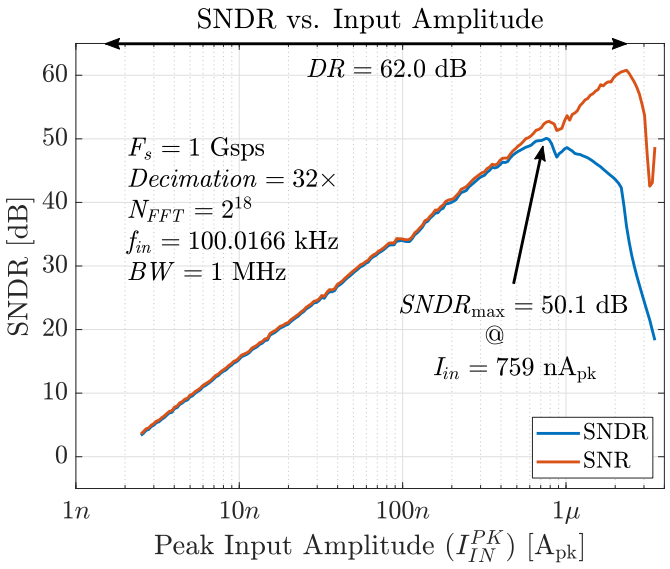



Fig. 7. Measured dynamic range plot of the CDC.

The CDC is sampled at 1 GS/s using a 1st order difference

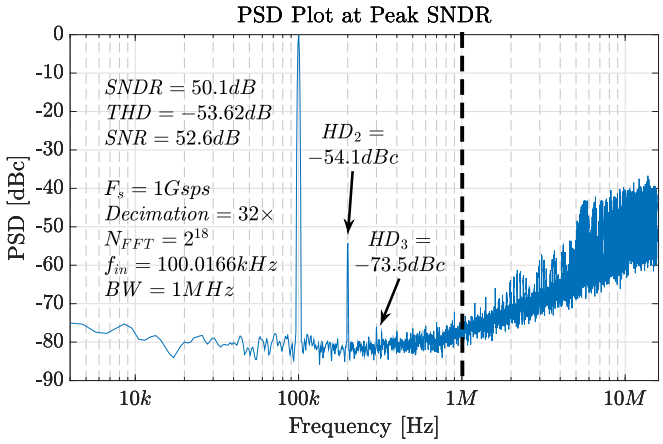



Fig. 8. FFT plot at peak SNDR.

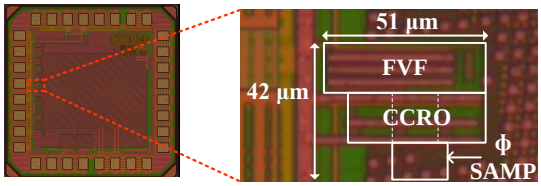



Fig. 9. Die micrograph showing zoomed-in view of the CDC.

DFF+XOR arrangement and then decimated by 32 to bring the data off-chip. The dynamic range of the CDC is shown in Fig. 7. The plot shows a noisefloor at $\sim$ 1.85 nArms limited by FVF thermal noise and CCRO quantisation noise. Beyond the peak SNDR point, the SNDR is instead limited by distortion - specifically the CCRO HD2. Once the input amplitude approaches the 3 $\mu$A FVF bias current, the oscillator and FVF become increasingly non-linear. Taking the input range as $\sim$ 1.85 $\text{nA}_{\text{pk}} \rightarrow$ 2.35 $\mu\text{A}_{\text{pk}}$, the dynamic range is 62.0 dB. The notches seen in the SNDR plot at 100 nApk and 1 $\mu$Apk are due to the CCRO pulse-frequency modulated tone (PFM) harmonics aliasing in-band due to the decimation filter. An FFT is shown for the peak SNDR case in Fig. 8. The flicker noise corner is seen at $\sim$ 30 kHz and the 1$^{\text{st}}$ order noise shaping corner at $\sim$ 700 kHz. It is clear that the harmonic distortion is limited by HD2 of the CCRO, with HD3 being close to the noisefloor. Aliased PFM tones can be seen just out of band, and these tones aliasing in-band at certain amplitudes limits performance also.

Fig. 9 shows the CDC's area to be 0.0025 $\text{mm}^2$, with the FVF current source consuming the majority of the area (for low flicker noise). The CDC consumes a total power of 357.6 $\mu$W with the CCRO consuming 81 %, the FVF consuming 14 % and the 1$^{\text{st}}$ difference phase sampler consuming 5 %. Table I shows a comparison with the state of the art. [5] is pseudo-differential and uses an analog control loop to stabilise $V_{CNTL}$, limiting scalability and power efficiency. [6] uses an input resistor network to compensate for CCRO nonlinearity, but requires a voltage input and is not robust to PVT variation. It was sampled off-chip at 10 Gs/s; the power consumption of which is not included in the analysis, inflating the reported SNDR and FoM. [7] appears to use a large delay cell capacitance to linearise the transfer function at the cost of higher quantisation noise, which is counteracted by a narrower bandwidth and second order noise shaping. [8] uses non-linear feedback to compensate for the CCRO non-linearity, but suffers from high power consumption and area.

TABLE I
COMPARISON WITH THE STATE OF THE ART.

| Specification | This Work | [5] | [6] | [7] | [8] |
|---|---|---|---|---|---|
| Architecture | OL CCRO | OL CCRO | OL CCRO | OL CCRO | OL CCRO |
| Non-Linearity Correction | Improved Squaring | $V_{CNTL}$ Regulation | Input Resistor Network & Cancellation | Large Load Capacitance | Non-Linear Feedback & Calibration |
| Single-Ended/ Pseudo-Differential | SE | PD | SE | SE | SE |
| Technology [nm] | 65 | 180 | 65 | 130 | 130 |
| Supply Voltage [V] | 1.2 | 1.8 | 1.0 | 1.8 | - |
| Max Input | 6 $\mu\text{A}_{\text{pp}}$ | $\sim$ 37 $\mu\text{A}^{\text{pp}}_{\text{diff}}$ | 1 $\text{V}^{\text{pp}}$ | 640 $\text{mV}^{\text{pp}}$ | 400 $\text{mV}^{\text{pp}}$ |
| DR [dB] | 62.0 | - | $\sim$ 70 | 93.5 | 66 |
| HD2 [dBc] | 54.1 | 83.8 *** | 51 | $\sim$ 76 | $\sim$ 61 |
| HD3 [dBc] | 74 | 84 *** | 74 | $\sim$ 88 | $\sim$ 75 |
| SNDR [dB] | 50.1 | 68.2 *** | 56 | 69.6 | 60.2 |
| BW [MHz] | 1 | 1 | 2 | 0.02 | 2 |
| Power [$\mu$W] | 357.6 | 2,900 | 650 * | 280 | 25,000 ** |
| Area [$\text{mm}^2$] | 0.0021 | 0.03 | 0.0015 * | 0.02 | 0.048 |
| Schreier FoM (SNDR) [dB] | 143.9 | 153.6 *** | 150.9 * | 148.1 | 139.23 ** |
| Walden FoM [fJ/conv − step] | 684 | 1910 *** | 315 * | 2835 | 3000 ** |

* Offchip Input Buffer & Sampling at $10GS/s$, Power & Area not Included
** Pad Driver Power Included
*** Pseudo-Differential Result not conducive to Single-Ended sensor readout

## IV. CONCLUSION

Table I shows a lack of single-ended, open-loop, current-mode CDCs. All existing solutions are either pseudo-differential or voltage mode, limiting their power and area efficiency and their suitability for use with single-ended sensors. The improved squaring delay cell with positive feedback and cell selection results in the lowest area, lowest power open-loop, single-ended, MHz-bandwidth CCRO-based CDC.

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