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Structural analysis, elemental profiling, and electrical characterization of HfO_2 thin films deposited on $In_{0.53}Ga_{0.47}As$ surfaces by atomic layer deposition

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Structural analysis, elemental profiling, and electrical characterization of HfO_2 thin films deposited on $In_{0.53}Ga_{0.47}As$ surfaces by atomic layer deposition

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In this work results are presented on the structural analysis, chemical composition, and interface state densities of HfO_2 thin films deposited by atomic layer deposition (ALD) from $Hf[N(CH_3)_2]_4$ and H_2O on $In_{0.53}Ga_{0.47}As/InP$ substrates. The structural and chemical properties are investigated using high resolution cross-sectional transmission electron microscopy and electron energy loss spectroscopy. HfO_2 films (3–15 nm) deposited on $In_{0.53}Ga_{0.47}As$ are studied following a range of surface treatments including *in situ* treatment of the $In_{0.53}Ga_{0.47}As$ surface by H_2S exposure at 50–350 °C immediately following the metal organic vapor phase epitaxy growth of the $In_{0.53}Ga_{0.47}As$ layer, *ex situ* treatment with $(NH_4)_2S$, and deposition on the native oxides of $In_{0.53}Ga_{0.47}As$ with no surface treatment. The structural analysis indicates that the $In_{0.53}Ga_{0.47}As$ surface preparation prior to HfO_2 film deposition influences the thickness of the HfO_2 film and the interlayer oxide. The complete interfacial self-cleaning of the $In_{0.53}Gas_{0.47}As$ native oxides is not observed using an ALD process based on the $Hf[N(CH_3)_2]_4$ precursor and H_2O. Elemental profiling of the $HfO_2/In_{0.53}Ga_{0.47}As$ interface region by electron energy loss spectroscopy reveals an interface oxide layer of 1–2 nm in thickness, which consists primarily of Ga oxides. Using a conductance method approximation, peak interface state densities in the range from 6×10^{12} to 2×10^{13} cm^{-2} eV^{-1} are estimated depending on the surface preparation. © *2009 American Institute of Physics*. [doi:10.1063/1.3243234]

I. INTRODUCTION

To continue complementary metal oxide semiconductor (MOS) development beyond the 22 nm node, replacement channel materials in combination with high dielectric constant (k) gate layers are currently under investigation. High-mobility III-V materials such as $In_xGa_{1-x}As$ are realistic candidates for the channel replacement in n-type field effect transistors (MOSFETs),[1–4] and the growth of high In content metal semiconductor FETs on a silicon substrate has recently been demonstrated.[5] However, the implementation of these new channel materials faces many challenges, one of which is the lack of stable high quality gate insulators, which yield sufficiently low density of electrically active defects at the interface between the III–V channel and the high-k gate layer. Although significant effort has been dedicated to investigate HfO_2 thin films formed by atomic layer deposition on $In_xGa_{1-x}As$ (Refs. 6–8) and resultant $In_xGa_{1-x}As$ MOSFET structures,[9] an improvement in the $In_xGa_{1-x}As$ MOSFET performance is expected from an increased understanding of the structural and chemical properties of the interface region between the $In_xGa_{1-x}As$ substrate and the high-k gate layer and analysis of the resulting electrical performance of the devices.

In a recent publication,[10] an *in situ* treatment of n-type $In_{0.53}Ga_{0.47}As$ using H_2S at the end of metal organic vapor phase epitaxy (MOVPE) growth was demonstrated to result in comparable electrical properties to those of *ex situ* aqueous sulfur treatments using $(NH_4)_2S$ for $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures. The objective of this paper is to investigate the effect of the $In_{0.53}Ga_{0.47}As$ surface preparation on the structural properties of the ALD deposited HfO_2 thin films and to investigate the composition of the oxide interface layer (IL) between the HfO_2 and the $In_{0.53}Ga_{0.47}As$ using high angle angular dark field scanning microscopy and electron energy loss spectroscopy (EELS). The defect concentrations at the $HfO_2/In_{0.53}Gas_{0.47}As$ interface are also estimated using an approximation of the conductance method.

II. EXPERIMENTAL DETAILS

The n-type lattice matched 2 μm $In_{0.53}Ga_{0.47}As$ layers were grown on 350 μm InP(100) substrates by MOVPE at 670 °C. At the end of the MOVPE growth, the $In_{0.53}Ga_{0.47}As$ surface was subjected to H_2S exposure [flow rate of 0.1 SCCM (SCCM denotes standard cubic centimeter per minute at STP) in H_2] for 90 minutes at temperatures of 50, 200, or 350 °C. The use of H_2S is particularly suited to *in situ* passivation of $In_{0.53}Ga_{0.47}As$ as it is used as the n-type dopant source in the MOVPE process. As a comparison, an *ex situ* aqueous sulfur treatment of the MOVPE $In_{0.53}Ga_{0.47}As$ sur-

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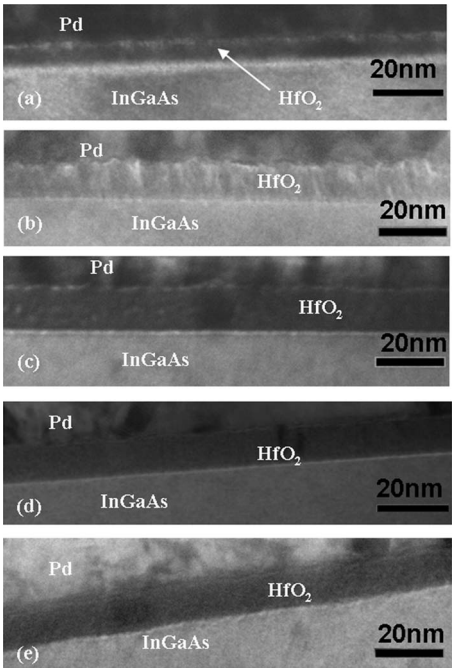


FIG. 1. High resolution cross-sectional TEM of the Pd/9 nm $HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures with various $In_{0.53}Ga_{0.47}As$ starting surface conditions: (a) no treatment, (b) H_2S at 350 °C, (c) H_2S at 200 °C, (d) H_2S at 50 °C, and (e) $(NH_4)_2S$.

face was also carried out using 20% $(NH_4)_2S$ in de-ionized (DI) water at ~60 °C for 20 min. The HfO_2 film was deposited by ALD using $Hf[N(CH_3)_2]_4$ and H_2O at 250 °C on $In_{0.53}Ga_{0.47}As/InP$ samples with typical size of 20 $\times 30$ mm^2. The $Hf[N(CH_3)_2]_4$ is the first pulse in the ALD sequence. In the interim between surface passivation and the ALD process, the samples were exposed to air for ~2 min. Metal gate formation (100 nm Pd) was achieved by electron beam evaporation and a lift-off process. The samples analyzed in this work did not receive either post oxide deposition annealing or post gate metallization annealing. No back contacts were formed. More details on the sample processing can be found in Ref. 10. Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam thinning procedures[11] in an FEI 200 Workstation and examined at 200 kV in a JEOL2000FX. Capacitance and conductance measurements were performed on-wafer at 25 °C in a humidity-controlled ambient using a Cascade Microtech probe station and an Agilent B1500A semiconductor device analyzer.

III. RESULTS AND DISCUSSION

Figure 1 shows the high resolution cross-sectional TEM micrographs of the $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures for the various treatment approaches examined: (a) no treatment (i.e. native oxide), (b) H_2S at 350 °C, (c) H_2S at 200 °C, (d) H_2S at 50 °C, and (e) $(NH_4)_2S$. The TEM micrographs for the untreated sample (a) and the H_2S at 50 °C treatment (d), already published by O'Connor *et al.*,[10] are included for completeness. There are a number of comparisons to be made from the TEM micrographs relating to the thickness of the HfO_2 film, the interface oxide layer present between the HfO_2 film and the $In_{0.53}Ga_{0.47}As$ substrate, and the surface roughness of the $HfO_2/In_{0.53}Ga_{0.47}As$ interface.

TABLE I. HfO_2 and $HfO_2/In_{0.53}Ga_{0.47}As$ IL thickness measurements of samples with varying $In_{0.53}Ga_{0.47}As$ surface treatments, as obtained from high resolution cross-sectional TEM. The substrate surface conditions appear to influence the subsequent dielectric growth.

Condition	HfO_2 nominal (nm)	HfO_2 measured by HR-TEM (nm)	IL measured by HR-TEM (nm)
Untreated	9	5.2	1.90
H_2S, 50 °C, 90 min	9	9.4	0.83
H_2S, 200 °C, 90 min	9	13.5	0.90
H_2S, 350 °C, 90 min	9	10.8	0.90
$(NH_4)_2S$	9	11.0	1.30

All samples have an IL oxide present between the HfO_2 film and the $In_{0.53}Ga_{0.47}As$ substrate, which is expected since the ALD process involves the exposure of the $In_{0.53}Ga_{0.47}As$ substrate surface to H_2O at 250 °C. However, there are differences in the IL thicknesses across the samples. These thicknesses, as measured by conventional TEM, are listed in Table I. The sample exposed to *in situ* H_2S treatment at 50 °C has the thinnest IL. The sample treated with the *ex situ* aqueous $(NH_4)_2S$ solution has the thickest IL (1.3 nm) of all the $In_{0.53}Ga_{0.47}As$ samples which experience a surface treatment prior to HfO_2 ALD growth. The untreated $In_{0.53}Ga_{0.47}As$ sample has an IL oxide thickness of 1.9 nm and is comparable to the native oxide thickness of 2 nm found on $In_{0.53}Ga_{0.47}As$ by Kobayashi *et al.*[12] A number of recent publications have demonstrated that ALD deposition of Al_2O_3 [using $Al(CH_3)_3$] and HfO_2 {using $Hf[N(CH_3)\times(C_2H_5)]_4$} on GaAs and $In_xGa_{1-x}As$ substrates can reduce the thickness of interfacial Ga and As oxides during the ALD growth process.[6,7,12,13] This is referred to as an interfacial "self-cleaning process" and is most likely precursor dependent. The thickness of the IL oxide for the untreated sample (1.9 nm) indicates that limited or no interfacial self-cleaning process is occurring using the $Hf[N(CH_3)_2]_4$ and H_2O water process. This result is in agreement with the work of Shahrjerdi *et al.*[14] where no self-cleaning was observed using the same precursor [tetrakis(dimethyl-amino) hafnium] on GaAs.

The thicknesses of the ALD deposited HfO_2 films as measured by TEM are also given in Table I. The untreated sample has a dielectric thickness of 5.2 nm, while all of the treated samples [*in situ* H_2S and $(NH_4)_2S$] have film thicknesses closer to the nominal value of 9 nm. This suggests that the pre-ALD surface treatment has an impact on the nucleation of the HfO_2 growth and therefore the thickness of the subsequent HfO_2 film. A similar observation has been reported on GaAs.[15] The sample with the deposited thickness closest to the nominal 9 nm was the sample subjected to the *in situ* H_2S treatment at 50 °C. The TEM micrographs in Fig. 1 also present a variation in contrast within the HfO_2 layer, indicating density variations through the HfO_2 film as well as variability in the roughness of the HfO_2/Pd interface. These effects are most pronounced in the 350 °C *in situ* H_2S treated sample and the sample with no surface preparation

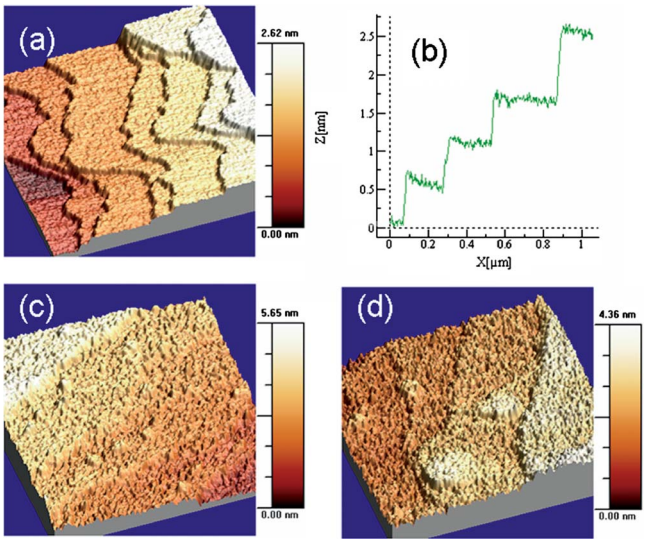


FIG. 2. (Color online) AFM images and atomic step height of $In_{0.53}Ga_{0.47}As$ surfaces [(a) and (b)] before, (c) after $(NH_4)_2S$ solution and (d) after $(NH_4)_2S$ solution and annealing. The sample was in the $(NH_4)_2S$ for 20 min at 60 °C. The $(NH_4)_2S$ is 20% in DI water. The annealing was under vacuum at 200 °C for 5 min.

and are least pronounced for the sample treated with *in situ* H_2S at 50 °C.

From the TEM micrographs, it is evident that the $In_{0.53}Ga_{0.47}As$ surface subjected to the aqueous $(NH_4)_2S$ solution [Fig. 1(e)] has an increased semiconductor surface roughness when compared to the samples treated *in situ*. This roughening of the $In_{0.53}Ga_{0.47}As$ has also been reported in a recent publication[16] and is consistent with an etching of the $In_{0.53}Ga_{0.47}As$ by the $(NH_4)_2S$ solution. This has the potential to increase surface scattering in MOSFET structures, reducing electron mobility in the inversion layer. This roughening effect was examined further using atomic force microscopy to examine the $In_{0.53}Ga_{0.47}As$ surface morphology and root mean square (RMS) surface roughness before and after 20 min in 20% $(NH_4)_2S$ at ~60 °C followed by a de-ionized water rinse and N_2 dry. Samples were also analyzed following the $(NH_4)_2S$ treatment and a vacuum anneal at 200 °C for approximately 5 min. The AFM results for a 1×1 μm^2 scan area are shown in Fig. 2, with the tabulated RMS surface roughness values, as measured from individual terraces, in Table II, obtained using a Veeco Dimension 3100. Table II also lists the average height of the surface roughness (taking the lowest point as the zero level and measuring the height of the other features with respect to it) and the maximum feature height observed. The $In_{0.53}Ga_{0.47}As$ surface prior to the $(NH_4)_2S$ exhibits atomic steps (~0.6 nm) and atomically smooth terraces (200–400 nm wide), with an RMS roughness of 0.1 nm. The 0.6 nm single atomic steps are consistent with the 0.5869 nm lattice constant of $In_{0.53}Ga_{0.47}As$.[17] This type of surface morphology has been reported for AlGaAs/GaAs/AlGaAs quantum well structures grown by MOVPE.[18] Following the $(NH_4)_2S$ treatment the terraces are still evident, but a clear roughening of the $In_{0.53}Ga_{0.47}As$ surface has resulted, with a doubling of the RMS roughness to 0.2 nm.

TABLE II. RMS roughness data measured from individual terraces for the $In_{0.53}Ga_{0.47}As$ surface as measured by AFM, with no treatment (native oxide), following $(NH_4)_2S$ solution and following $(NH_4)_2S$ solution and annealing under vacuum (200 °C for 5 min). The $(NH_4)_2S$ treatment significantly roughens the $In_{0.53}Ga_{0.47}As$ surface.

Condition	Ave. height (nm)	Max. height (nm)	RMS roughness (nm)
InGaAs (native oxide)	0.3	0.5	0.1
$(NH_4)_2S$ treatment	0.8	1.7	0.2
$(NH_4)_2S$ and anneal	0.9	1.6	0.2

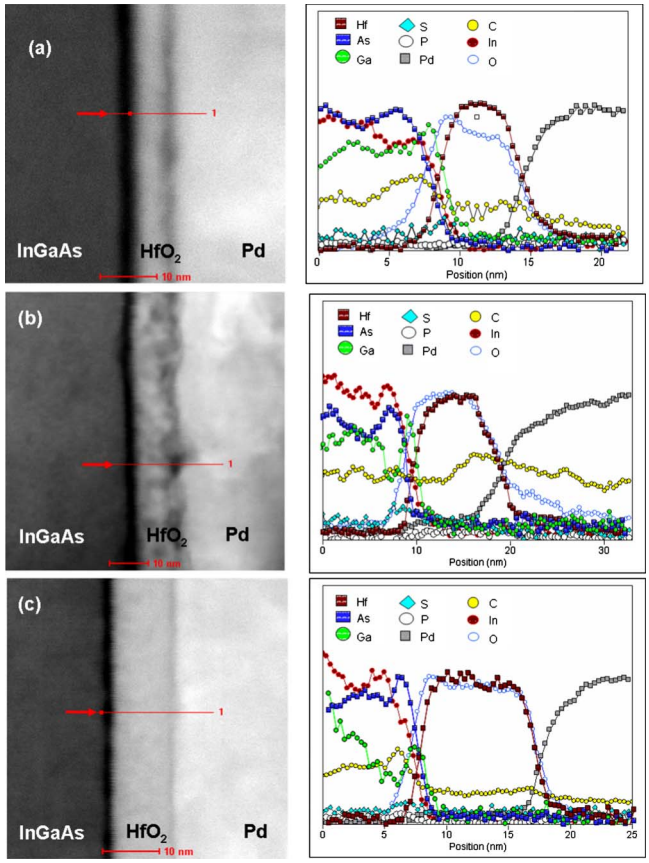


FIG. 3. (Color online) HAADF-STEM/EELS of $Pd/HfO_2/In_{0.53}Ga_{0.47}As$ structures: (a) untreated, (b) H_2S at 350 °C, and (c) H_2S at 50 °C. EELS analysis reveals an interface oxide layer of 1–2 nm in thickness, which consists primarily of Ga oxide.

High angle annular dark field scanning TEM (HAADF-STEM) and EELS results for the untreated sample and the samples subjected to the *in situ* H_2S at 350 and 50 °C are shown in Figs. 3(a)–3(c), respectively. In the HAADF-STEM micrographs, the IL oxide can be seen as a darker layer (lower average atomic number) between the $In_{0.53}Ga_{0.47}As$ and the HfO_2. The variations in density of the HfO_2 layer across the samples as observed by conventional TEM are also seen in the corresponding HAADF-STEM micrographs. The EELS data for each sample are representative of a single line scan. However, the results are repeatable, and the scans shown in Fig. 3 are representative of each sample as a whole. It should be noted that profile heights do not represent stoichiometric concentrations but instead only show relative change in each element's signal along the profiled line.

The HAADF-STEM micrographs of the untreated sample [Fig. 3(a)] and the sample treated with H_2S at

TABLE III. $HfO_2/In_{0.53}Ga_{0.47}As$ IL thicknesses measured by high resolution cross-sectional TEM and by HAADF-STEM. HfO_2 thickness measured by HAADF-STEM concurs with conventional TEM thickness measurements; however IL thickness measurements differ in magnitude between the two techniques.

Condition	HfO_2 Nominal (nm)	IL measured HR-TEM (nm)	IL measured HAADF-STEM (nm)	HfO_2 measured HR-TEM (nm)	HfO_2 measured HAADF-STEM (nm)
Untreated	9	1.90	2.2	5.2	6.0
H_2S, 50 °C, 90 min	9	0.83	1.7	9.4	9.4
H_2S, 350 °C, 90 min	9	0.90	2.1	10.8	10.5
H_2S, 200 °C, 90 min	9	0.90	···	13.5	···
$(NH_4)_2S$	9	1.30	2.0	11.0	10.7

350 °C [Fig. 3(b)] show an interlayer between the HfO_2 and the Pd. This could either be organic residue from the metal lift-off process or voids due to the roughness of the HfO_2 surface. This effect could also be enhanced as a result of Pd delamination during cross-sectional analysis. From the corresponding EELS line scan, there is no significant increase in the carbon signal at this interface, suggesting that it is more likely to be voids. The voids are not evident for the sample treated *in situ* with H_2S at 50 °C [Fig. 3(c)], and this sample also exhibits the lowest leakage current density.[10]

From the EELS line scans in Figs. 3(a)–3(c), the region corresponding to the III–V/high-*k* interfacial oxide layer for all samples shows the oxygen signal increasing before the Hf signal and overlapping with the substrate elements' signals. This indicates the presence of an interface oxide in all cases. The composition of each interlayer appears similar, with some In and As oxides, but mostly comprising of a Ga oxide, seen by the peak of the Ga signal at each interface. The oxidation state of the Ga has not been determined. It has been reported for GaAs that oxygen will bond preferentially to Ga atoms that are below As dimers, with subsequent oxidation of nearby Ga dimers, and the formation of As clusters.[19] In each of the EELS profiles, we can see a slight increase in the As and In signals in the $In_{0.53}Ga_{0.47}As$ substrate near the $HfO_2/In_{0.53}Ga_{0.47}As$ interface, with an increase in the Ga signal overlapping the oxygen at the interface. This is consistent with the proposed model for GaAs oxidation.

The Ga signal increases with the rising oxygen signal at the top of the substrate (the In and As signals do not) and then decreases as the Hf signal increases. At each interface there appears to be a peak of the As signal, which may not be real, as the Ga signal becomes less prominent, allowing easier detection of the As signal. With regard to the presence of sulfur, the EELS agrees with the x-ray photoelectron spectroscopy results previously published,[10] with no sulfur at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface for the untreated sample, as expected, and an increase in the sulfur concentration at the interface for the sample exposed to H_2S at 350 °C. However, for the sample treated *in situ* at 50 °C, the EELS cannot conclusively determine whether sulfur is present at the interface or not. A clear carbon signal was observed throughout the EELS line scan for all samples. This carbon is most likely from surface contamination during sample preparation, shipping, and handling.

In all cases, the HfO_2 thicknesses measured by HAADF-STEM concur with the conventional TEM thickness measurements, shown in Table III. However, the IL oxide thicknesses from conventional TEM and HAADF-STEM images are not in full agreement. Even though the trends in the thickness of the IL agree with both methods, the HAADF-STEM images yield consistently thicker IL oxides (Table III). One possible explanation for this discrepancy is that the HAADF-STEM image is based on atomic number contrast and the IL is the thickness of the region with average low atomic number. The conventional TEM, by comparison, provides structural information, and the IL oxide is the thickness of the amorphous region between the InGaAs substrate and the HfO_2 layer. Consequently, the two measurements are not directly comparable. Further research is required to fully understand this discrepancy.

To investigate the effect of HfO_2 film thickness on the IL properties, HfO_2 films with nominal thicknesses from 3 to 15 nm were examined by cross-sectional TEM. All samples were subject to H_2S exposure at 50 °C prior to the HfO_2 ALD growth. The resulting TEM micrographs are shown in Fig. 4 for nominal thicknesses of 3, 9, and 15 nm in (a), (b), and (c), respectively. Thickness measurements obtained using conventional TEM are shown in Table IV. The variation

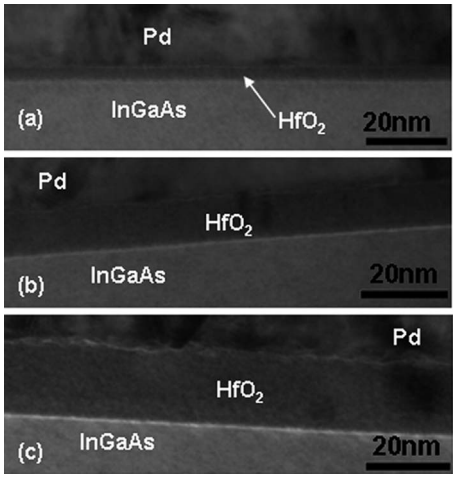


FIG. 4. High resolution cross-sectional TEM of samples treated *in situ* H_2S at 50 °C with varying nominal HfO_2 thicknesses of (a) 3, (b) 9, and (c) 15 nm. The interfacial layer thickness and the $In_{0.53}Ga_{0.47}As$ surface roughness do not change significantly with varying HfO_2 thicknesses.

TABLE IV. HfO_2 and $HfO_2/In_{0.53}Ga_{0.47}As$ IL thickness measurements of samples with varying dielectric nominal thicknesses obtained from conventional high resolution cross-sectional TEM. All samples had the same surface treatment: H_2S at 50 °C for 90 min. The thickness of the IL is constant within experimental limitations at ~0.8 nm for the 3, 9, and 15 nm HfO_2 films, indicating that the IL oxide of ~0.8 nm is formed prior to or at the initial stages of the HfO_2 film growth.

Condition	Nominal (nm)	HfO_2 measured TEM (nm)	IL measured TEM (nm)
H_2S, 50 °C, 90 min	3	3.0	0.80
H_2S, 50 °C, 90 min	9	9.4	0.83
H_2S, 50 °C, 90 min	15	16.8	0.85

in the deposited HfO_2 film thicknesses across the three samples as measured by TEM is within ~10% of the nominal ALD target thickness. The thickness of the IL is constant within experimental limitations for the 3, 9, and 15 nm HfO_2 films, indicating that this IL is formed at the initial stages of the HfO_2 film growth or air exposure prior to ALD, and is not being altered during the ALD process. Note the presence of crystalline regions in the 9 and 15 nm HfO_2, which are present even though the maximum temperature experienced by the HfO_2 during the ALD growth process is 250 °C.

Figure 5 shows the capacitance-voltage (*CV*) characteristics of the 9 nm sample treated *in situ* with H_2S at 50 °C from 1 kHz to 1 MHz. The *CV* characteristic for positive gate bias (1–2 V) is representative of accumulation of electrons at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface based on the insensitivity of the accumulation capacitance to frequency (1 kHz–1 MHz) and temperature (−50 to 75 °C).[20] The region from 0 to −1.5 V, however, is not representative of inversion at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. The measured capacitance passes through a peak value and subsequently decreases with increasing negative bias (see the open symbol 10 kHz *CV* sweep in Fig. 5). This is characteristic of an interface defect response where the interface state distribution exhibits a peak at a specific energy in the band gap at the dielectric/semiconductor interface.[21–23] For the case of inversion at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface with an associated minority carrier response, the capacitance should acquire a constant value in inversion, where the magnitude of the capacitance increases with decreasing ac signal frequency. The inset of Fig. 5 shows the 1 MHz curve for each of the three thicknesses of HfO_2, illustrating a positive V_{fb} shift with increasing dielectric thickness.

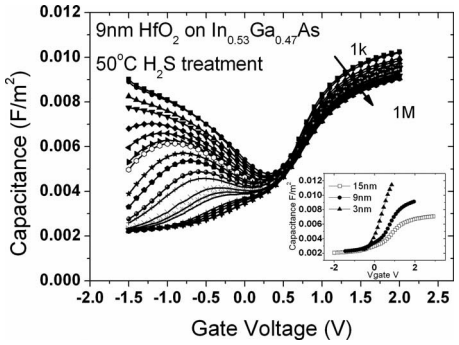


FIG. 5. *CV* curves from 1 kHz to 1 MHz of the sample with 9.4 nm of HfO_2 treated *in situ* with H_2S at 50 °C. The curves correspond to the extracted equivalent parallel conductance measurements shown in Fig. 6. Inset: to illustrate the flatband voltage shift as a function of dielectric thickness, the 1 MHz *CV* curves are shown for the devices with 3.0, 9.4, and 16.8 nm of HfO_2 (all have similar substrate surface treatment).

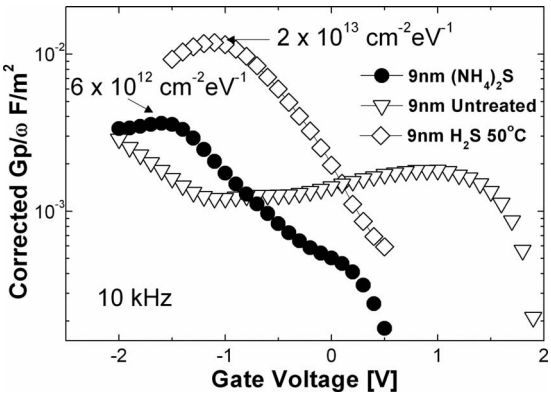


FIG. 6. G_p/ω vs *V* curves at 10 kHz for the samples treated *in situ* with H_2S at 50 °C (9.4 nm HfO_2), the $(NH_4)_2S$ treated sample (10.8 nm HfO_2), and the sample with an untreated $In_{0.53}Ga_{0.47}As$ surface (5.4 nm of HfO_2). The approximate equivalent parallel conductance has been corrected for series resistance effects and also for the lossy dielectric effects. The peak value in the conductance is not observed within the measured voltage range for the sample with the untreated InGaAs surface and the samples treated with H_2S at 200 °C and 350 °C.

The corresponding conductance (*G*) of the $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ MOS structure was measured simultaneously with the capacitance as a function of voltage at the selected ac frequencies. The equivalent parallel conductance (G_p/ω) was extracted from the measured data and then corrected for series resistance[24] and for a "lossy dielectric" as demonstrated by Kwa *et al.*[25] The resulting corrected equivalent parallel conductance is shown in Fig. 6 at 10 kHz for the samples with a nominal HfO_2 thickness of 9 nm. The capacitor with a 50 °C *in situ* H_2S treated $In_{0.53}Ga_{0.47}As$ surface exhibits a peak equivalent parallel conductance loss located between −1 and −1.5 V, corresponding to an approximate interface state densities of $\sim 2\times 10^{13}$ cm^{-2} eV^{-1} taking $D_{it}=(2.5|G_p/\omega|_{peak}/q)$. The HfO_2 film on the $In_{0.53}Ga_{0.47}As$ surface treated with $(NH_4)_2S$ exhibits a similar G_p/ω versus bias dependence profile to the *in situ* H_2S at 50 °C treated sample. However, the equivalent parallel conductance loss is lower on the aqueously treated sample by a factor of ~0.32, yielding an approximate peak interface state density of $\sim 6\times 10^{12}$ cm^{-2} eV^{-1}. It should be noted here that due to the ability of the defects to communicate with both the conduction and the valence bands (the $In_{0.53}Ga_{0.47}As$ energy gap is ~0.75 eV), the D_{it} values may be an overestimation of the actual D_{it} level, as discussed by Martens *et al.*[26] The profile for the untreated sample, shown in Fig. 6, and the samples treated with H_2S at 200 and 350 °C (not shown) do not exhibit a peak equivalent parallel conductance loss within the bias range studied. However, these samples display a higher equivalent parallel conductance loss over the bias range 0–1 V, when compared to the *in situ* H_2S and the $(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ surfaces, and this is reflected in a higher *CV* stretch-out for these samples in this bias range.[10] Table V compares the resulting interface state den-

TABLE V. Interface state density values at peak G_p/ω at 10 kHz (where possible) and at flatband voltage. The $(NH_4)_2S$ and the H_2S at 50 °C treatments are effective at reducing the interface state density in the upper gap (from E_i to E_c). The corresponding energy positions in the $In_{0.53}Ga_{0.47}As$ energy gap for the peak D_{it} and at flatband are estimated from *CV* measurements at 77 K and 1 MHz, where D_{it} effects are minimized (Ref. 28).

Condition	Peak $D_{it}(cm^{-2}\,eV^{-1}) \sim E_v + 0.4$ eV	D_{it} at $V_{fb}(cm^{-2}\,eV^{-1}) \sim E_v + 0.7$ eV
Untreated	Peak D_{it} outside bias range	$\sim 2.8\times10^{12}$
9 nm H_2S at 350 °C	Peak D_{it} outside bias range	$\sim 2.6\times10^{12}$
9 nm H_2S at 200 °C	Peak D_{it} outside bias range	$\sim 2.3\times10^{12}$
9 nm H_2S at 50 °C	$\sim 2\times10^{13}$	$\sim 1.1\times10^{12}$
9 nm $(NH_4)_2S$	$\sim 6\times10^{12}$	$\sim 3.75\times10^{11}$

sities for the 10 kHz peak value of the conductance and also at the flatband voltage.

From these values it is evident that the *in situ* H_2S and the $(NH_4)_2S$ surface preparations both reduce interface state densities in the upper region (from E_i to E_c) of the $In_{0.53}Ga_{0.47}As$ energy gap at the $In_{0.53}Ga_{0.47}As/HfO_2$ interface. If we assume that sulfur is the main passivating element for the *in situ* H_2S and $(NH_4)_2S$ processes, then the *in situ* H_2S process is considerably more effective when considering the differing amount of sulfur available between the $(NH_4)_2S$ *ex situ* treatment and the *in situ* 50 °C H_2S treatment, which is 20% $(NH_4)_2S$ in DI water versus a flow rate of 0.1 SCCM of H_2S in H_2.

Considering the results in Table III, it is evident that the interface state densities are not related to the thickness of the IL oxide, as the IL oxide is thicker for the $(NH_4)_2S$ samples (1.3 nm) when compared to the *in situ* H_2S samples (0.83–0.9 nm), while the $Pd/HfO_2/InGaAs/InP$ MOS structure with the $(NH_4)_2S$ surface preparation exhibits a reduced interface state density. In addition, the frequency dependence of the *CV* response as shown in Fig. 5 has also been observed for different $In_{0.53}Ga_{0.47}As$ surface preparations and different high-*k* oxide layers.[8,27] These results indicate that the interface defects detected by the *CV* and *GV* analysis originate from the $In_{0.53}Ga_{0.47}As$ surface.

This work has presented the results of a study examining the structural properties, chemical composition, and interface defect concentrations in $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ MOS structures for varying $In_{0.53}Ga_{0.47}As$ surface treatments prior to HfO_2 deposition. All samples exhibit an IL oxide, suggesting that the "self-cleaning" phenomenon is either limited or not present for ALD $Hf[N(CH_3)_2]_4+H_2O$ on $In_{0.53}Ga_{0.47}As$. The composition of the IL is primarily a gallium oxide as determined by EELS. Varying the substrate surface starting conditions affects the IL oxide thickness, with a reduced IL thickness for either *in situ* H_2S or $(NH_4)_2S$ when compared to deposition on the InGaAs native oxides. The $(NH_4)_2S$ process results in a marked increase in $In_{0.53}Ga_{0.47}As$ surface roughness, which may have implications for electron mobility degradation in InGaAs MOSFETs. The $(NH_4)_2S$ and H_2S at 50 °C treatments are the most effective at reducing the peak interface state density in the upper gap with approximate peak interface state densities at $\sim E_v+0.7$ eV of 1×10^{12} $cm^{-2}\,eV^{-1}$ and 3.7×10^{11} $cm^{-2}\,eV^{-1}$ for the *in situ* H_2S sample treated at 50 °C and the $(NH_4)_2S$ treated samples respectively. The HfO_2 n-/InGaAs/InP structures also exhibit a peak in the interface defect density at ~0.4 eV above the valence band edge with peak concentrations of 2×10^{13} $cm^{-2}\,eV^{-1}$ for the *in situ* H_2S sample treated at 50 °C and 6×10^{12} $cm^{-2}\,eV^{-1}$ for the $(NH_4)_2S$ treated sample. The experimental results are consistent with the interface defects originating from the $In_{0.53}Ga_{0.47}As$ surface.

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