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Can Metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ / InP MOSCAP Properties Translate to Metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ / InP MOSFET Characteristics?

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In this paper we present the electrical characteristics of Metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ / InP MOS capacitor (MOSCAP) structures formed using a relatively straightforward capacitor process flow and for MOSCAPs which experience the full process flow of an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ n channel MOSFET. From analysis of the capacitance-voltage response over a range of ac signal frequencies fixed oxide charge densities and interface state concentrations are determined for the MOSCAP structures and the impact of forming gas annealing on oxide and interface state densities is presented. The MOSCAP results are compared to the properties of fully processed metal/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ / InP n channel MOSFETs, and the results indicate that the findings from the MOSCAPS do translate to the measured InGaAs MOSFET characteristics.

Introduction

Currently, a large research effort is dedicated to replacing silicon with alternative high mobility channel materials such as compound semiconductors for future nanoelectronic metal oxide semiconductor field effect transistors (MOSFETs) (1). A significant part of this work relies on an analysis of the high- k / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stack using basic MOS capacitor (MOSCAP) structures as opposed to full MOSFETs, due to their ease of fabrication. For instance, these simple test structures are useful for the screening of suitable dielectrics, the optimization of the III-V surface passivation, and the investigation of interface states and oxide fixed charges in the high- k /III-V gate stack. However, this raises the following question: would the findings obtained from III-V MOSCAP studies necessarily translate to the performance of a fully fabricated III-V MOSFET? In this study we examine the oxide and interface charge densities of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors fabricated with a simple capacitor flow and for capacitors formed adjacent to fully fabricated InGaAs surface channel MOSFETs. The quantification of the oxide charge and interface state densities from the MOSCAP studies are compared to the device characteristics of relatively long channel $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ n-MOSFETs to assess the validity of applying the findings of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitor studies to the performance of fully fabricated $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs.

MOSCAPs Results

Before presenting the metal/high- k /In_{0.53}Ga_{0.47}As/InP MOSFET characteristics, this section will summarize the main findings resulting from studies carried on metal/high- k /In_{0.53}Ga_{0.47}As/InP MOSCAP structures, with the main focus on p -type MOSCAPs since the MOSFET comparison will be made to conventional surface inversion mode n -channel MOSFETs fabricated in p doped In_{0.53}Ga_{0.47}As.

Bulk Charge in the Oxide

We recently established that Al₂O₃ formed by ALD (at 270 °C using TMA and H₂O in this case) presented a large bulk positive oxide charge (2). The capacitors consisted of Pt(75nm)/Al₂O₃/In_{0.53}Ga_{0.47}As/InP stacks with Al₂O₃ nominal thicknesses ranging from 2 nm to 15 nm. These structures did not receive any surface passivation before oxide deposition; therefore, the impact of a native oxide on the results should not be neglected. A negative flat band voltage (V_{FB}) shift with increasing oxide thickness confirmed the presence of bulk positive oxide charge ($0.8\text{--}2 \times 10^{19} \text{ cm}^{-3}$) distributed across the Al₂O₃ thickness. The origin of this positive charge was attributed to Al dangling bonds (3). The availability of both n - and p -type (doping = $4 \times 10^{17} \text{ cm}^{-3}$) In_{0.53}Ga_{0.47}As/InP structures enabled us to compare the V_{FB} between n - and p -type MOSCAPs. The V_{FB} difference yields an integrated density of interface states (D_{it}) $\sim 1.3 \times 10^{13} \text{ cm}^{-2}$ covering the band gap range between $E_c\text{--}E_f = 0.04 \text{ eV}$ and $E_f\text{--}E_v = 0.04 \text{ eV}$. It must be emphasized that the D_{it} contribution resulted in a constant positive charge added to the p -type samples, meaning that the interface states are positively charged when empty, i.e. the interface defects are predominantly donor type. The total charge as a function of Al₂O₃ thickness characteristic extrapolated to 0 nm of Al₂O₃ enabled us to distinguish a sheet of negative fixed charge ($-9 \times 10^{12} \text{ cm}^{-2}$) located near the interface, which could originate from the native oxide or the Al₂O₃/native oxide interface.

Interface States and Surface Passivation

The capacitance voltage (CV) characteristics of metal/high- k /In_{0.53}Ga_{0.47}As/InP MOSCAP structures often exhibit large frequency dispersion in the depletion/weak inversion region (4, 5). This dispersion is attributed to frequency-dependent interface defect state capacitance contributions to the overall measured MOSCAP CV characteristics. When no surface passivation is applied prior to ALD of Al₂O₃ or when HfO₂ is directly formed on In_{0.53}Ga_{0.47}As/InP, a large density of interface states ($> 10^{13} \text{ cm}^{-2}$) is observed (5).

In order to minimize the D_{it} at the Al₂O₃/In_{0.53}Ga_{0.47}As interface, we have optimized the (NH₄)₂S passivation method (6). The optimal (NH₄)₂S In_{0.53}Ga_{0.47}As surface treatment prior to oxide deposition involves a 20 min dip in 10% concentrated (NH₄)₂S aqueous solution at room temperature. By employing a combination of CV and parallel conductance techniques on the best samples, we have detected a defect level located at approximately $E_v + 0.4 \text{ eV}$ in n - and p -type Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As/InP structures (doping = $4 \times 10^{17} \text{ cm}^{-3}$) (6). The two methods yielded similar integrated D_{it} values of $\sim 2.5 \times 10^{12} \text{ cm}^{-2}$ and D_{it} energy profiles in the In_{0.53}Ga_{0.47}As bandgap. The origin of this interface defect is likely intrinsic to the In_{0.53}Ga_{0.47}As surface; as similar defect states have been observed in different high- k /InGaAs systems (7, 8).

It must be highlighted that the minimization of the air exposure duration prior to loading in the ALD reactor is crucial to the success of this passivation method (6). The study showed that 30 min air exposure after the surface treatment is enough to degrade the interface properties. In a more recent work, we demonstrated substantial benefits when fast (less than 3 min) sample transfer to the ALD chamber was implemented (9). The measured D_{it} value was $6-9 \times 10^{11} \text{ cm}^{-2}$.

In addition to the well characterized midgap state at $\sim E_v + 0.4 \text{ eV}$, $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOS structures generally exhibit two extra features: a large interface state defect density located close to the valence band edge (10), and the presence of interface states which extend into the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band (11, 13). This usually manifests itself in high frequency CV dispersion in accumulation for n- or p- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAPs. It is not yet clear whether these interface states are interface defects or “border traps”, i.e. charge trapping sites in the oxide. N type $\text{In}_x\text{Ga}_{1-x}\text{As}$ samples with low In content ($x = 0, 0.15$ and 0.30) show huge frequency dispersion in accumulation with a total collapse of the capacitance at very low temperature indicating the probable occurrence of Fermi level pinning (11). As the In percentage is decreased, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ band gap widens mainly by an upward shift of the conduction band minimum. The frequency dispersion in accumulation observed in n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ could then be explained by interface states that extend into the conduction band of high In content $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x \geq 0.53$). An example of the frequency dispersion present in accumulation for a p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAP is shown in figure 1.

Post Metal Gate Forming Gas Annealing

Low temperature, post-metal gate ($< 350^\circ\text{C}$) forming gas annealing (FGA) in an open furnace at atmospheric pressure of N_2/H_2 (95%/5%) has demonstrated significant benefits regarding the properties of metal/high- $k/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOS structures (2, 11). $\text{Pt}/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ structures subjected to a 350°C FGA for 30 min showed a reduction of bulk positive charge from $0.8-2 \times 10^{19} \text{ cm}^{-3}$ down to $5 \times 10^{18} \text{ cm}^{-3}$ together with a decrease in D_{it} from $1.3 \times 10^{13} \text{ cm}^{-2}$ down to $4 \times 10^{12} \text{ cm}^{-2}$ (2). As discussed earlier, this study also distinguished negative fixed charge at the interface, which was also reduced after the FGA (from $-9 \times 10^{12} \text{ cm}^{-2}$ down to $-7 \times 10^{11} \text{ cm}^{-2}$). The reduction in bulk positive charge was attributed to the hydrogen passivation of Al dangling bonds in Al_2O_3 . In a different study, a 250°C FGA for 30 min was carried out on $\text{Pd}/\text{HfO}_2/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ structures and resulted in D_{it} reduction (11). In the same study, another cumulative FGA at 325°C induced further D_{it} decrease as indicated by the reduction of the interface state associated conductance peak (11).

Metal Gates

The choice of metal for the gate of the MOS test structure is motivated by several considerations. The most important factor is the inertness of the metal in contact with the oxide. In the past, we have used Platinum and Palladium gate electrodes for their non-reactivity. Pd was selected in this work for its catalytic properties, as during post-metallisation FGA the Pd cracks the molecular hydrogen, H_2 , which helps H-diffusion towards the oxide/III-V interface and makes the hydrogen more reactive for passivation purposes.

CV characteristics of Pd/Al₂O₃/p-In_{0.53}Ga_{0.47}As/InP MOSCAPs

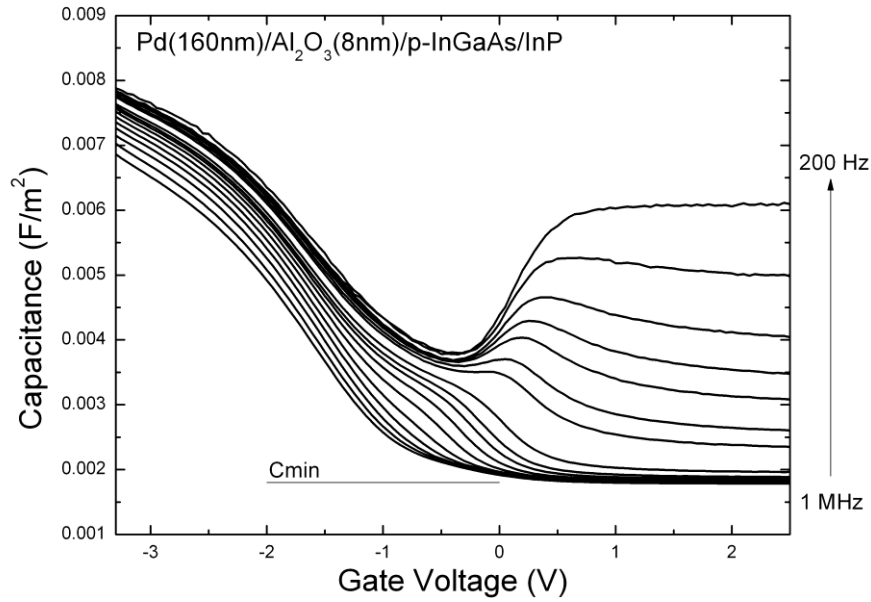


Figure 1. Multi-frequency CV characteristics of a Pd(160 nm)/Al₂O₃(8 nm)/p-In_{0.53}Ga_{0.47}As/InP MOSCAP. The structure received an optimal (NH₄)₂S surface treatment prior to the Al₂O₃ formation. This simple MOSCAP process flow did not include the dopant activation annealing.

We will focus the MOSCAP electrical analysis of p-type In_{0.53}Ga_{0.47}As/InP structures since the MOSCAP results will be compared to the In_{0.53}Ga_{0.47}As/InP n-MOSFET results. Figure 1 presents the multi-frequency CV characteristics of a Pd(160 nm)/Al₂O₃(8 nm)/p-In_{0.53}Ga_{0.47}As/InP MOSCAP. In order to fabricate this structure, the samples received a degrease (1 min each in acetone, methanol, IPA), then we applied the optimized (NH₄)₂S surface treatment described previously (10% concentrated solution and 20 min dip at room temperature). The samples were transferred with minimum air exposure (under 3 min) to the ALD chamber for 8 nm Al₂O₃ deposition at 300 °C using Al(CH₃)₃ (TMA) and H₂O pulses. The Pd gate electrodes were then defined using e-beam evaporation and a lift-off lithography process. The structures did not receive any pre or post metal thermal treatment. The CV characteristics of figure 1 show marked frequency dispersion in all parts of the CV. In the region (V_g) < -2 V, the dispersion is probably caused by hole trapping by “border traps” located in the oxide. The D_{it} contribution is fully or in-part responsible for the CV frequency dispersion in the depletion region, it emerges as a shoulder/peak in capacitance at around -0.5 V < V_g < 0.5 V. The D_{it} response then merges with the minority carrier response in inversion (V_g > 0.5 V). The minority carrier capacitance response is rarely observed in Si MOSCAPs even at very low measurement frequencies. This can be explained by the combination of low In_{0.53}Ga_{0.47}As band gap (0.75 eV) and the probable presence of midgap defects in the bulk of the InGaAs layer resulting in faster generation of minority inversion charge and, therefore, a measurable capacitance response associated with minority carriers compared to silicon. Recently, the temperature dependance of the minority carrier response in In_{0.53}Ga_{0.47}As was analysed and enabled the distinction between the generation-recombination regime at low temperature and the diffusion of minority carriers from the neutral region at high

temperature (9). The minimum high frequency capacitance in inversion for a $4 \times 10^{17} \text{ cm}^{-3}$ doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAP with 10 nm Al_2O_3 ($k = 8.6$) is $C_{\min} = 0.0018 \text{ F/m}^2$. The minimum experimental capacitance at 1 MHz does reach the theoretical $C_{\min}$ consistent with surface inversion.

Figure 2 shows the multi-frequency CV characteristics of $\text{Pd}(200 \text{ nm})/\text{Al}_2\text{O}_3(10 \text{ nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAPs processed on the same substrates and in parallel with the MOSFET devices which will be discussed in the next section. The MOSCAP fabrication conditions are nearly identical to the structures analyzed in figure 1. The ALD deposition temperature is 250°C (as opposed to 300°C previously) and the Al_2O_3 thickness is 10 nm (as opposed to 8 nm previously).

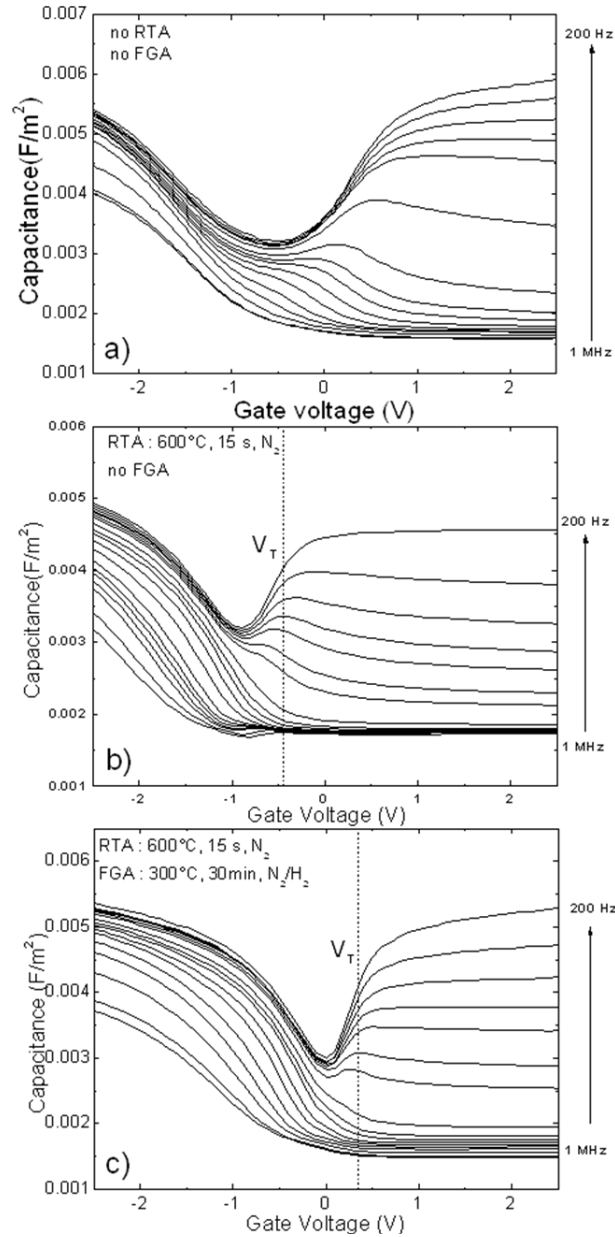


Figure 2. Multi-frequency CV characteristics $\text{Pd}(200 \text{ nm})/\text{Al}_2\text{O}_3(10 \text{ nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAP structures processed in parallel with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs: a) before the dopant implant activation RTA, b) after RTA and c) after FGA. The Al_2O_3 ALD temperature is 250°C (as opposed to 300°C for figure 1 MOSCAPs).

The fabrication of these MOSCAPs involved an extra oxide etching step to enable metal contacts directly on the p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$. Comparing the results of figure 1 and figure 2a demonstrate that the electrical properties of the two structures are very similar except for a slightly more stretched out CV characteristic in figure 2a. This could be due to the extra processing steps or a slightly longer air exposure after passivation.

Figure 2b presents the MOSCAP multi-frequency CV after a 600 °C for 15 s rapid thermal anneal (RTA) in N_2 intended to activate the implanted dopants in the source/drain region of the MOSFET located on the same sample/substrate. The most remarkable difference between the CVs of figure 2a (MOSCAP pre-RTA) and 2b (MOSCAP post-RTA) is the steeper capacitance increase in accumulation or inversion and the larger frequency dispersion in accumulation after the RTA. It is difficult to compare the evolution of oxide charge after the RTA due to the difficulty in extracting accurately the threshold voltage (V_T) in figure 2a. However, despite the CV stretch-out of the pre RTA characteristic, the RTA seems to induce a negative shift of the CV. Figure 2c shows the MOSCAP CV characteristics after the RTA (600 °C, 15 s, N_2) and then an FGA at 300 °C for 30 minutes in 95% N_2 / 5% H_2 . It is important to note that the V_T values reported in figures 2b and 2c were extracted from the MOSFET characteristics presented in the next section. There is an obvious V_T shift post FGA. The theoretical V_T in these structures is expected at about 0.7 V, this indicates that the FGA reduces the positive charges in the oxide. In addition, the capacitance increase in inversion is noticeably steeper at low frequencies after FGA, which could be due to a lower D_{it} near the conduction band, consistent with previous reports (11).

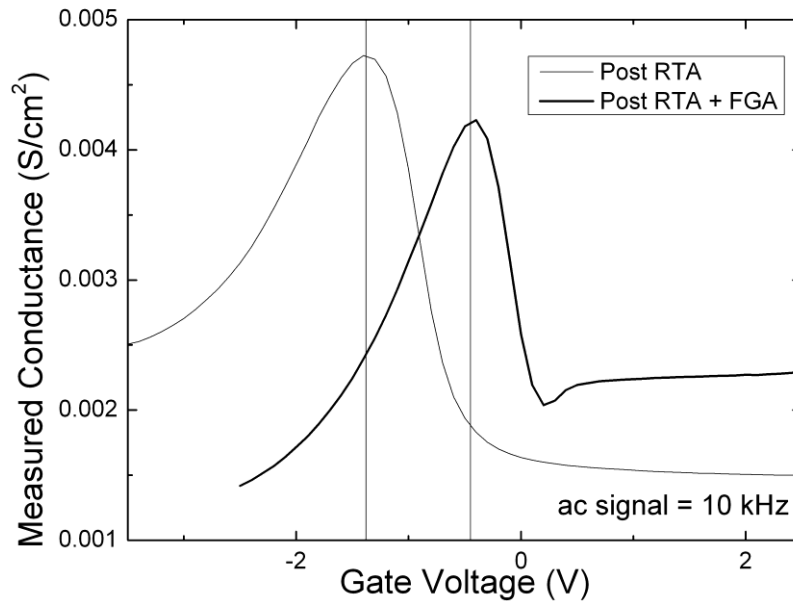


Figure 3. Measured (uncorrected) conductance versus gate voltage comparing the post-RTA to the post-RTA, post-FGA $\text{Pd}(200 \text{ nm})/\text{Al}_2\text{O}_3(10 \text{ nm})/\text{p-In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ MOSCAP structures. The measured conductance peaks at the selected ac signal: 10 kHz, which enables qualitative D_{it} comparison pre and post FGA.

Figure 3 compares the measured conductance at 10 kHz on a capacitor before and after FGA. In order to accurately extract the D_{it} , the Conductance Method must be applied (14). However, figure 3 shows that the midgap interface state profile exhibits a conductance peak at 10 kHz and enables us to compare qualitatively the evolution of D_{it} after FGA. It is interesting to note that on these structures, which received the optimal $(NH_4)_2S$ surface passivation and a dopant activation RTA, the FGA has very little effect on the midgap D_{it} . The FGA may not be effective at reducing D_{it} for structures with low starting D_{it} levels. It is interesting to note the conductance peak voltage shift after FGA of ~ 0.9 V, which is very close to the V_T difference extracted from the MOSFET characteristics (0.8 V) and discussed in the next section.

MOSFET Results

The MOSFET devices investigated in this study were fabricated on a Zn-doped ($4 \times 10^{17} \text{ cm}^{-3}$) p-type $In_{0.53}Ga_{0.47}As$ epitaxial layer grown by MOVPE on p-type InP. The MOSFET devices were fabricated based on a gate oxide-first process. The surface treatment and oxide growth are identical to the case of the MOSCAPs (figure 2) described previously. The source and drain (S/D) regions were formed by Si implantation (dose of $1 \times 10^{14} / \text{cm}^2$ at 80 keV and $1 \times 10^{14} / \text{cm}^2$ at 30 keV). The implant activation was achieved by RTA at 600 °C for 15 s in a N_2 atmosphere. The S/D contacts were defined by lithography and selective wet etching of the Al_2O_3 in dilute HF and electron beam evaporation of Au(14 nm)/Ge(14 nm)/Au(14 nm)/Ni(11 nm)/Au(200 nm) (15). The Pd gate (200 nm) was defined by electron beam evaporation and lift-off.

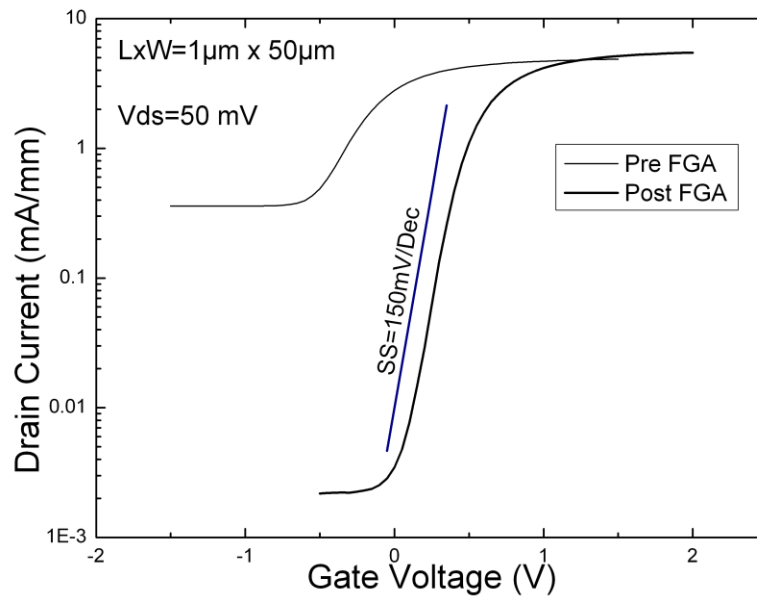


Figure 4. Transfer characteristics before a) and after FGA b) measured at $V_{ds} = 50$ mV on a 1- μm -gate-length and 50- μm -gate-width $In_{0.53}Ga_{0.47}As$ MOSFETs.

Figure 4 shows the transfer characteristics of 1- μm -gate-length and 50- μm -gate-width MOSFET at $V_{ds} = 50$ mV before and after FGA. A clear positive V_T shift is observed after the FGA from -0.45 V before FGA to 0.35 V after FGA. This result is consistent with the presence of bulk positive charge in the Al_2O_3 and its reduction by FGA treatment

as observed on MOSCAP devices (figures 2b and 2c) and as reported in a previous study based on MOSCAP structures (2). The off-state current reduction is another remarkable consequence of the FGA. Since the MOSFETs used in this study do not include a ring-gate and are not fully isolated, the sufficiently high positive oxide charge (equivalent sheet charge at the interface $> 2 \times 10^{12} \text{ cm}^{-2}$) induces $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface inversion in areas not controlled by the gate. After FGA, the positive charge is reduced to a density where it cannot generate inversion in the periphery of the device.

The effective mobility (μ_{eff}) extracted from identical MOSFETs but with longer channel lengths (20 μm -50 μm) has been previously reported (16). μ_{eff} increased from 650 $\text{cm}^2/\text{V.s}$ to 750 $\text{cm}^2/\text{V.s}$ due to the reduced coulomb scattering by the lower density of positive charge in the oxide. The lower D_{it} near the conduction band as observed in the CV response in figure 2c) after FGA could also explain the improved μ_{eff} . The subthreshold swing extracted from the transfer characteristic post FGA is 150 mV/dec, which yields a midgap $D_{\text{it}} \sim 5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. This D_{it} value was confirmed using the Conductance Method (14, 16).

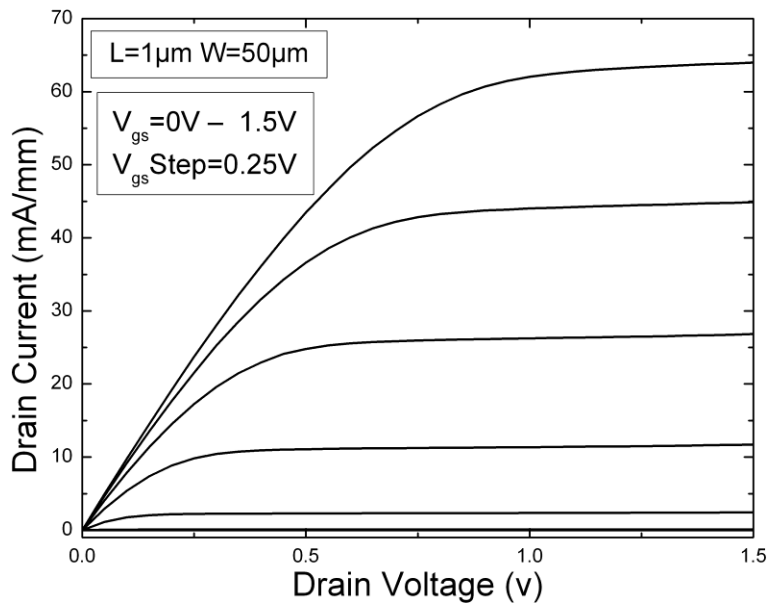


Figure 5. Output characteristics measured on a 1- μm -gate-length and 50- μm -gate-width $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET after FGA. $V_{\text{gs}} = 0 \text{ V}, 0.25 \text{ V}, 0.5 \text{ V}, 0.75 \text{ V}, 1 \text{ V}$ and 1.5 V .

The output characteristics of the 1 $\mu\text{m} \times 50 \mu\text{m}$ MOSFET (figure 5) show excellent transistor operation after FGA. The linear and saturation regions are clearly distinguished. Note the relatively high W/L value transistor data presented in figure 5 is affected by S/D resistance. The longer channel InGaAs MOSFET device characteristics reported in (15) are less affected by S/D resistance effects.

Conclusion

Based on analysis of the C-V response of $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAP structures, the Al_2O_3 contains positive oxide charge distributed throughout the oxide layer prior to

forming gas annealing. The forming gas anneal reduces the density of oxide charge. A quantitative agreement was found between the density of oxide charge reduction resulting from the FGA process based on CV analysis of MOSCAP structures and the threshold voltage shift of fully fabricated n channel $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs. The MOSCAP structures enabled us to monitor the effect of RTA on the electrical properties of these stacks, which is not possible on the MOSFET devices, which require the RTA for the source and drain dopant activation. The RTA treatment seems to deteriorate the oxide electrical properties as seen from the larger frequency dispersion in accumulation. However, improvements in the CV response are observed after RTA in the region approaching surface inversion. Additional positive charge in the oxide is generated by the RTA process, which can be removed or passivated with a subsequent FGA anneal. In conclusion, this study supports the approach of simplified MOSCAP analysis for the development of gate stack processes for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs.

Acknowledgments

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