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Thermal and Electrical Study of Glass Interposers in Co-Packaged Electronic-Photonic Systems

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***Abstract*—This paper investigates the use of glass interposers as a scalable and cost-effective solution for co-packaged electronic-photonic systems, with a focus on optimizing thermal management and electrical transmission. The thermal management study is carried out through design, assembly and characterization of a thermal test vehicle. The thermal test vehicle is used to study the heat dissipation in glass interposers by varying the Through Glass Via (TGV) pitch (100 µm to 400 µm). The outcomes indicate a maximum surface temperature rise of 2.9 °C, which is also confirmed by finite element method simulations. Moreover, the simulations also suggest that changes in TGV pitch below 100 µm do not significantly impact the temperature variation. The electrical transmission through the glass interposer package is investigated using three different design scenarios (Transmission Lines on Glass, Glass Interposer and Electrical Test Vehicle). The RF performance of each design is studied up to 40 GHz to analyze the losses incurred by different components in the package. In conclusion, this work presents an optimized electrical design for the test vehicle. By employing strategically designed geometries for TGVs, microvias, and ball grid array (BGA) pads, we achieved a significant reduction in insertion loss of approximately 11 dB at 40 GHz. This design approach can be compatible with 2.5D and 3D integration schemes, enabling high-density and high-performance electronic-photonic packages.**

Keywords- Co-packaging, Thermal Management, Electrical Design, Glass Interposer, Through Glass Vias, Reference Thermal Chip.

I. Introduction

Due to the escalating performance demands of data centers and HPC (High-Performance Computing) systems, traditional pluggable optical transceivers face challenges in keeping up with the rapidly increasing bandwidth density and energy efficiency requirements [1]. Co-packaged optics (CPO) emerges as a solution by integrating photonic devices in close proximity with high-performance electronics on the same package substrate through advanced integration schemes. CPO significantly reduces SerDes (Serializer/Deserializer) distances, thereby substantially reducing power consumption [2].

Various integration schemes for transceivers exist, including monolithic, 2D, 2.5D, or 3D integration approaches [3], involving either permanently attached transceivers (e.g., solder reflow assembly) or those inserted into electrical sockets. These methods offer diverse strategies for effectively combining electronic and photonic components to meet the evolving demands of data center architectures [1, 4].

In scenarios involving hundreds of channels or more, the utilization of interposers for 2D or 3D integration facilitates the combination of driving electronic integrated circuits (EICs) with photonic ICs (PICs), thereby enhancing power efficiency. The integration of EICs and PICs through such interposers helps alleviate electrical interconnect loss by minimizing the required reach and the number of electrical transition points [5].

This co-packaging approach involves bringing optical and electrical chips into close proximity using 2.5D interposers, enabling the realization of ultra-high bandwidth channels with reduced power consumption compared to conventional packages assembled on boards [6, 7]. To accommodate the demand for higher bandwidth per channel (112G) and the implementation of advanced modulation schemes like Pulse Amplitude Modulation 4-level (PAM4), the EIC-PIC interconnects need to be upgraded to flip-chip bumps. These bumps provide low parasitic effects and shorter interconnects, ensuring signal integrity at higher frequencies, such as 28 GHz and beyond [8]. As the line rate for high-speed systems escalates from 50G to 100G and then to 200G, the losses experienced in a standard system rise from less than 10dB to more than 20dB [9]. The LGA socket in [10] shows <0.5dB IL and <-10dB RL with 95 Ohm reference impedance up to Nyquist frequency of 28GHz for 112G PAM4 signaling. An approximate 8.6 dB loss is achieved at the Nyquist frequency for 112Gbps signaling, meeting the XSR channel loss target [10] in the switch interposer electrical model. The authors recommend advanced substrate technologies to mitigate electrical losses. Glass core substrates present a solution [11].

Glass offers several key benefits for CPO applications. Glass has excellent electrical and optical properties, enabling high-frequency signal transmission with minimal loss [12]. TGVs also provide a thermal management mechanism, further aided by the incorporation of the heat sink in the assembly [13]. In addition to this, glass interposers can integrate optical waveguides, through vias, and electrical redistribution layers, facilitating fine-line routing and efficient assembly [14]. A comparison between glass interposers and organic substrates is discussed in [15-17]. In this paper, the term 'glass interposer' refers to a glass core interposer.

However, thermal crosstalk between EICs and PICs in such co-packaged systems can impact the optical functionality of thermally sensitive components on the PIC (such as micro-ring resonators, amplifiers etc.) [18-20]. The thermal isolation feature of glass interposers for co-packaging EICs and PICs can be leveraged for targeted thermal management [19-22].

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Through Glass Vias (TGVs) in these glass interposers aid in dissipating heat generated by electronic chips locally, while the low thermal conductivity of glass prevents thermal crosstalk between electronic and photonic chips. TGVs and redistribution layers (RDLs) within the glass interposer facilitate electrical connections between assembled integrated circuits and the PCB [23], as illustrated in Figure 1.

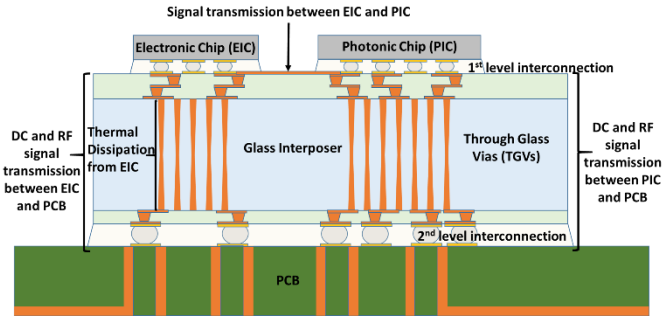


Fig. 1. A 2.5D glass interposer package consisting of co-packaged electronic (EIC) and photonic (PIC) chips bonded on the glass interposer (first-level interconnections); which is subsequently bonded on the PCB (second-level interconnections).

The literature discusses the enhancement in thermal performance of glass interposers with the implementation of TGVs [22, 24]. Cho et al., also highlight that increasing the effective thermal conductivity of the TGVs and interconnects beyond 100 W/m.K leads to an insignificant change in the out-of-plane thermal resistance of a glass interposer assembly [22]. However, the value of this effective thermal conductivity, beyond which the heat dissipation through the TGVs stagnates, is dependent on the interposer's volume for heat conduction, as discussed in this paper. This study seeks to address the gap between the constrained heat dissipation capabilities of Through Glass Vias (TGVs) and the necessity for integrating vapor chambers into Printed Circuit Boards (PCBs) (as denoted by reference [24]). This paper involves the design, assembly and characterization of the glass interposer for thermal characterization. The assembled glass interposer is referred to as a "thermal test vehicle", which undergoes thermal characterization.

The TGVs also play a critical role in reducing channel losses compared to Through Silicon Vias (TSVs) [25]. In this research, the focus lies on investigating the insertion loss and return loss associated with co-packaging EICs and PICs on a glass interposer. The investigation involves three design scenarios:

1. Transmission Lines on Glass: The electrical transmission between EIC and PIC on the glass interposer is characterized using co-planar waveguide (CPW) transmission lines on the glass substrate.
2. Glass Interposer: The study examines signal transmission through CPW transmission lines, TGVs, microvias, and Ball Grid Array (BGA) pads on the glass interposer.
3. Electrical Test Vehicle: The effect of packaging on signal transmission through the glass interposer is analyzed by characterizing a glass interposer packaged on the PCB, referred to as an "electrical test vehicle".

The design of glass interposer (both thermal and electrical) is discussed in section II. The assembly process and characterization of the thermal test vehicle is discussed in section III. Section III also analyzes the impact of variation in TGV pitch on heat dissipation performance of the glass interposer. Similarly, the assembly process and characterization of the electrical test vehicle is discussed in section IV. Section IV (B, C and D) also includes the characterization and analysis of the three design scenarios mentioned above.

II. Design of Glass Interposer for Thermal and Electrical Characterization

The test vehicles for thermal and electrical characterization of the glass interposer are constructed with a 460 µm thick Borofloat® Schott 33 glass core featuring hourglass-shaped copper-filled TGVs [18]. This core is stacked between polyimide layers both above and below, as depicted in Figure 2, with a single polyimide layer on the bottom and two polyimide layers on top of the core. The metal wiring on top of the glass surface and polyimide layer (1st polyimide layer) on the upper side is denoted as RDL1 and RDL2 (redistribution layers 1 and 2), while that on the lower side is termed as Backside RDL (BRDL). To mitigate stress in the polyimide layers, the pads are designed with rounded corners, and the microvias are arranged in a staggered configuration (Figure 2(a)). The larger pads (exceeding 300×300 µm²) incorporate holes to prevent cracks resulting from outgassing during fabrication and soldering. The Under Bump Metallization (UBM) pads on the glass interposer corresponding to the pads on the chip intended for soldering comprise a material stack including gold, copper and nickel, aimed at enhancing solder adhesion during chip bonding onto the glass interposer. The fabrication process of the glass interposers is detailed in our previous work [18].

A. Design of Glass Interposer for Thermal Characterization

The thermal characterization of the glass interposer requires a heat source, such as a reference thermal chip that has tungsten heater loopbacks acting as hotspots [26]. The glass interposer for thermal characterization comprises UBM pads and a sizable gold pad atop the second polyimide layer, as seen in Figure 2(a). These components serve two different purposes: facilitating the soldering of reference thermal chip pads to corresponding UBM pads and aiding in the thermal spreading of heat generated by the reference thermal chip, respectively. The microvias establish the connection between the UBM pad/gold pad and RDL2 on the 1st polyimide layer. RDL2, in turn, is connected to RDL1 situated atop the glass core via microvias. TGVs within the glass interposer core establish the connectivity between RDL1 and the BRDL on the lower surface of the glass

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core, as detailed in Figure 2(a). The diameter of the TGVs is 50 µm.

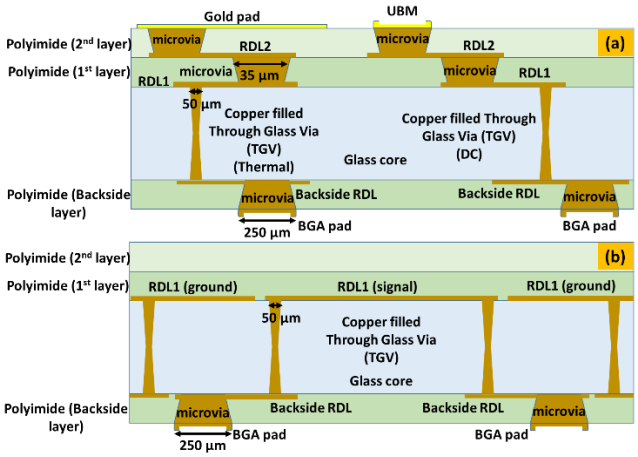


Fig. 2. Details of the glass interposer stackup for (a) thermal characterization with different components such as BGA pads, thermal and DC connection TGVs, microvias, RDL wiring and UBM; (b) electrical characterization with different components such as RDL wiring, signal and ground TGVs, microvias and BGA pads.

Subsequently, on the lower surface of the glass core, microvias within the backside polyimide layer connect the BRDL to the Ball Grid Array (BGA) pads. These circular BGA pads on top of the backside polyimide layer feature a diameter of 250 µm and a pitch of 500 µm (refer to Table I in supplementary information S1). Thus, the DC connections follow a path, commencing from the UBM pads (bonded to the chip pads through solder) on the 2nd polyimide layer. These connections then fan out on both sides of the large gold pad, as seen in Figure 3(a).

The thermal connection starts with a large gold bond pad atop the 2nd polyimide layer, designated for thermal spreading, connecting to a network comprising several RDL2 pads and a large RDL1 pad through a matrix of microvias. The RDL1 pad is then linked to the same sized (4.5×5 mm^2) backside RDL pad through thermal TGVs featuring different pitches (100 µm, 200 µm, 300 µm, and 400 µm). Subsequently, the backside RDL pad connects to the BGA pads through microvias, establishing the thermal link to the PCB (Figure 2(a)). The supplementary information (Table I in S1) provides details about the sizes of the different components in the glass interposer used for thermal characterization.

B. Design of Glass Interposer for Electrical Characterization

The stackup of the glass interposer for electrical characterization mirrors that of the thermal characterization stackup, excluding the utilization of UBM, RDL2, and microvias connecting RDL2 to RDL1 (Figure 2(b)). The Ground-Signal-Ground (GSG) conductor-backed coplanar waveguide (CBCPW) transmission lines on the top and bottom of the glass core (RDL1 and backside RDL) are interconnected through TGVs, as seen in Figure 2(b).

These CBCPW transmission line traces, measuring 100 µm in width, are positioned alongside coplanar ground plates on both the top and bottom of the glass core (RDL1 and backside RDL), maintaining a spacing of 18 µm. TGVs establish connections between the signal lines on top and bottom of the glass core. A mesh of TGVs (pitch of 500 µm) also facilitates ground stitching between the ground plates on the top and bottom of the glass core, as seen in Figure 3(b).

Subsequently, the signal lines and ground plate constituting the backside RDL are linked to the BGA pads through microvias. These BGA pads are then soldered onto the PCB to enable the electrical characterization of the glass interposer. The glass interposer for electrical characterization consists of RDL1, TGVs, BRDL, microvias connecting BRDL-BGA pads and BGA pads. The length (L) of the RDL1 transmission line in the glass interposer is varied (3 mm, 4 mm, 5 mm, and 6 mm). The supplementary information (Table II in S2) provides details about the sizes of the different components in the glass interposer used for electrical characterization.

III. Assembly and Characterization of Thermal Test Vehicle

A. Assembly of Thermal Test Vehicle

The assembly of the thermal test vehicle includes the reference thermal chip, SAC 305 microbumps, glass interposer, Bi-Sn bumps, underfill and PCB. The glass interposer utilized measures 13×7 mm^2 and accommodates 25×14 BGA pads on the backside. Thermal performance analysis of the TGVs within the glass interposer is conducted using a reference thermal silicon chip measuring 5×5×0.5 mm^3 as the heat source [26].

To establish thermal/electrical contact between the reference thermal chip and the glass interposer, fifty SAC 305 solder balls (comprising 96.5% tin, 3% silver, and 0.5% copper) with a diameter of 50 µm are deposited onto the gold pads (measuring 100×200 $µm^2$) of the reference thermal chip using the SB^2 Pactech jet machine.

Following solder jetting; the subsequent step involves flip-chip bonding of the reference thermal chip to the glass interposer. The reflow process for this bonding is conducted at 250°C for 10 seconds, as elaborated in supplementary information (Figure 1 in S3). Figure 4(a) depicts the top view of the flip-chipped reference thermal chip on the glass interposer. Subsequently, this glass interposer subassembly shown in Figure 4(a) is prepared for bonding onto the PCB.

To facilitate DC electrical connection to the heater loopbacks on the reference thermal chip, a custom PCB is designed and manufactured using FR4 material with a thickness of 1.6 mm and featuring four routing layers. The BGA pads on the top side of the PCB are precisely aligned with those on the bottom of the interposer. Among these pads, 10 pairs of BGA pads (each with a diameter of 250 µm) are linked to the pads of the reference thermal chip for DC connection, while the remaining pads serve to provide thermal spreading and mechanical stability to the entire package.

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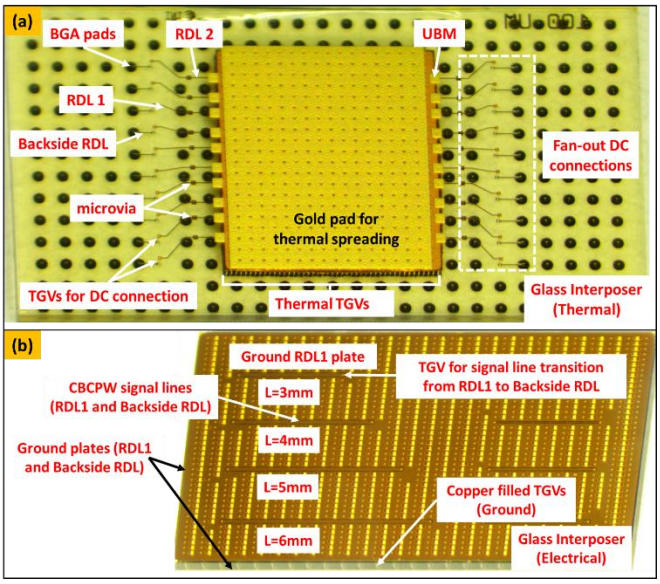


Fig. 3. Perspective view of the fabricated glass interposer for (a) thermal characterization with 100 µm pitch thermal TGVs in the interposer; (b) electrical characterization which includes CPW transmission lines on top and bottom of the glass surface which is interconnected through TGVs.

The connection between the interposer and the PCB is established using low-temperature-melting 250 µm diameter Bi-Sn solder balls, which are deposited onto the 250 µm diameter gold pads of the PCB using a stencil and tacky solder flux. This lower melting point solder is essential because the reflow temperature must be lower than that used for the flip-chip bonding of the reference chip onto the interposer earlier (Figure 4(a)). These solder balls undergo a primary reflow process to ensure a uniform solder surface for precise placement of the glass interposer subassembly.

Following the attachment of Bi–Sn solder balls on the PCB, a second reflow process enables the bonding of the subassembly (consisting of reference thermal chip and glass interposer) with the PCB. The same temperature reflow profile utilized for solder ball attachment on the PCB is applied (refer to Figure 2 in supplementary information S3).

The Bi-Sn solder balls on the PCB start to melt when the temperature reaches 155 °C, bonding to the glass interposer BGA pads during N_2 cooling. The set temperature is maintained higher than the actual melting temperature of Bi-Sn solder balls due to the temperature difference between the surface of the interposer and inside the oven temperature.

To further alleviate mechanical stress, an underfill epoxy (EPO-TEK 301-2) is applied between the chip and glass interposer, as well as between the glass interposer and the PCB. This final assembly is cured for 36 hours at room temperature. Figure 4(b) illustrates the top view of the cured final assembly of the thermal test vehicle, while the cross-section of this test vehicle is depicted in Figure 4(c&d). This cross-section shows the hourglass-shaped thermal TGVs in Figure 4(c) and the bonding of the reference thermal chip, glass interposer and PCB in Figure 4(d). The assembly process of the thermal test vehicle is also summarized in the supplementary information (Figure 3 in S3).

The FR4 PCB utilized for thermal characterization is 1.6 mm thick with a tolerance of ±10% and incorporates BGA bond pads with a pitch of 500 µm on the topside, aligning with the BGA pads at the bottom of the glass interposer.

B. Characterization of Thermal Test Vehicle

The heater loopbacks fabricated on the reference thermal chip serve as localized heat sources, generating hotspots on the chip's active surface. This chip is bonded onto the glass interposer, featuring varied pitches of the 50 µm diameter thermal TGVs at 100 µm, 200 µm, 300 µm and 400 µm. Activation of the heater loopbacks positioned along the two edges, as depicted in reference [26], facilitates the assessment of thermal characteristics across the glass interposer structure with distinct TGV pitches.

The heat generated by the heater loopback situated on the active surface of the chip is measured by infrared microscopy (FLIR X6540sc) at the topside of the flip-chip bonded reference thermal chip. This assessment involves the assembly described in Figure 4(b) situated on a copper block that remains at a consistent temperature of 20 ºC using a thermoelectric cooler (TEC). The reference thermal chip, featuring heater loopbacks along its edges, is powered through DC connectors at varying power levels (130 mW, 298 mW, and 500 mW). The reference thermal chip presented in this paper is being improved further to closely emulate higher thermal powers as well (5-50 W).

Figure 5 illustrates the temperature recorded at the topside of the chip for glass interposers with TGV pitches of 200 µm, 300 µm and 400 µm for a constant power of 500 mW. Temperature fluctuations correspond to the positioning of the heater loopbacks, with those at the chip edges generating higher temperatures compared to those at the chip center.

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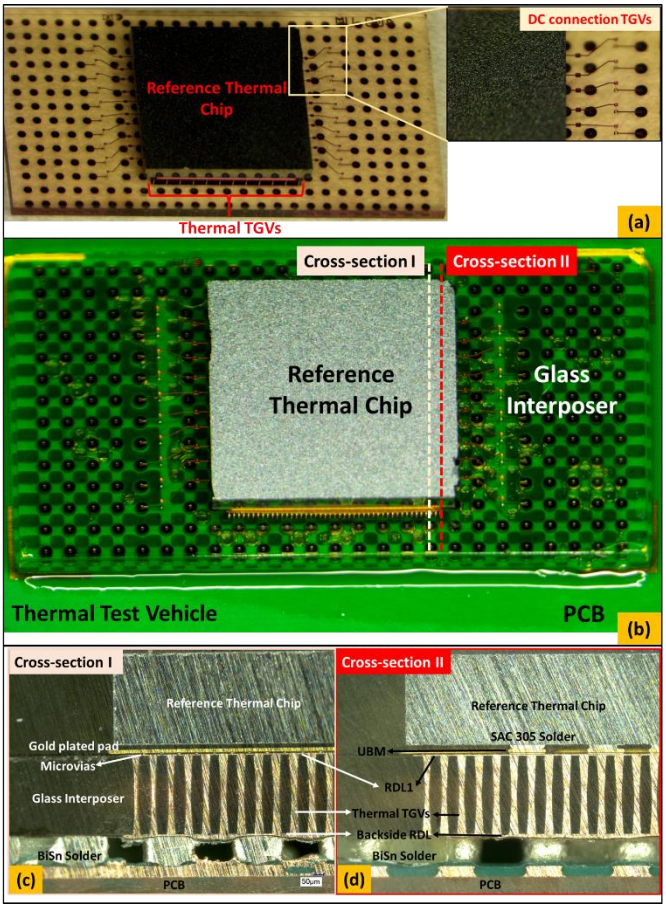


Fig. 4. (a) Perspective view of the subassembly containing flip-chip bonded reference thermal chip on glass interposer. (b) Top view of the thermal test vehicle showing assembled reference thermal chip and glass interposer (thermal TGV pitch of 100 µm) on PCB, with underfill between the reference thermal chip-glass interposer and glass interposer-PCB interfaces. The cross-sectional lines are specified in the figure. (c) Cross-sectional view of the thermal test vehicle along cross-sectional line 1. (d) Cross-sectional view of the thermal test vehicle along cross-sectional line 2.

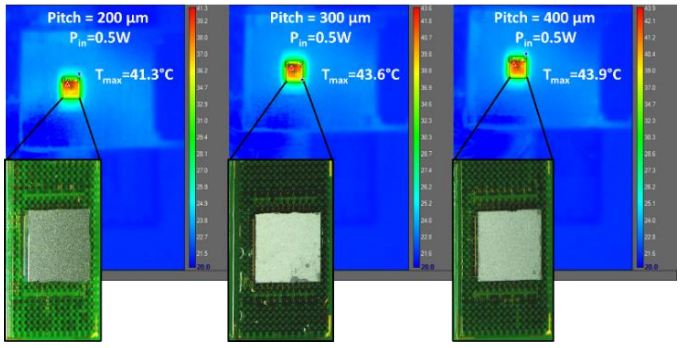


Fig. 5. Infrared thermal measurement showing surface temperature of the flip-chip bonded reference thermal chip on the glass interposer in thermal test vehicle exhibiting thermal TGV pitches of 200, 300 and 400 µm.

At elevated power levels, this disparity in maximum surface temperature between the corner of the chip's edge and the center of the chip's edge increases (±1ºC), attributed to edge effects as discussed in our previous work [26]. Figures 6(a & b) present measurements of the maximum surface temperature registered by a heater loopback situated at the chip's corner, showing a 2.9 ºC increase in temperature as the thermal TGV pitch is changed from 100 µm to 400 µm (at 0.5 W power). This increase in temperature is due to the decrease in the volume of copper in the region occupied by thermal TGVs (Table I). The reduction in copper volume results in elevated thermal resistance of the glass interposer. Consequently, the majority of heat disperses toward the top surface of the flip-chip attached reference thermal chip (Figure 6).

TABLE I. Table detailing the number of TGVs and the corresponding volume of copper in the glass interposer when the TGV pitch is increased from 100 µm to 400 µm)

Pitch of Thermal TGVs (µm)	Number of TGVs	Volume of Copper in Thermal TGVs under Chip (m^3)
100	2250	4.741×10^{-9}
200	575	1.211×10^{-9}
300	255	0.537×10^{-9}
400	156	0.328×10^{-9}

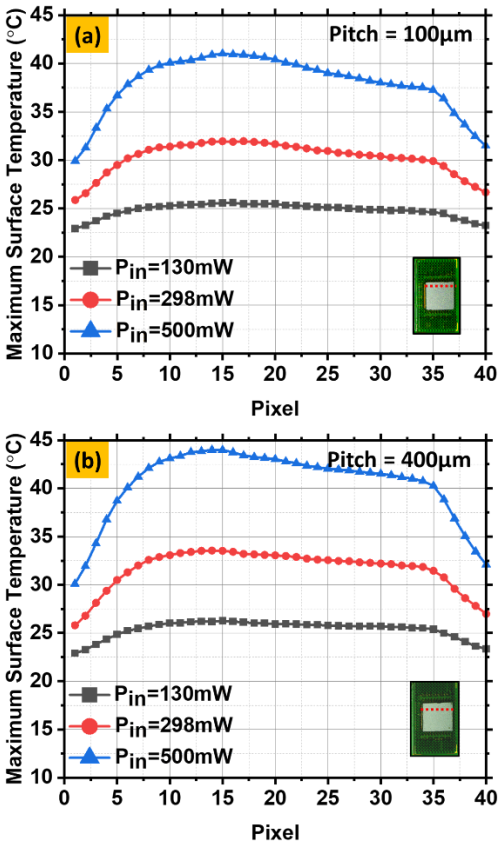


Fig. 6. Maximum surface temperature measurement across the topside of the flip-chip attached reference thermal chip (along the horizontal axis shown as dashed lines in the inset for (a)100 µm and (b) 400 µm pitch TGVs with increasing input powers of the heater loopback (P_{in}). The heater loopback at the corner of the chip is being operated in both (a) and (b).

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Moreover, the maximum surface temperature of the heater loopback positioned at the chip's corner is then simulated using Comsol Multiphysics®. The simulation parameters, along with simulation results, are provided in supplementary information (Table III and Figure 4 in S4). The simulation outcomes closely agree with experimental measurements, as shown in Figure 7. Despite a substantial 93% reduction in the number of thermal vias (as TGV pitch escalates from 100 µm to 400 µm), there is only a 2.9 °C increase in the surface temperature of the reference thermal chip. This observation is explained through simulations where the effective out-of-plane thermal conductivity of the volume occupied by the thermal TGVs and Bi-Sn solder bumps (with underfill) is varied from 1.2 W/m.K (glass) to 400 W/m.K (copper). The simulation results show that there is a notable practical advantage in utilizing thermal TGVs as compared to glass alone, evidenced by the steep decline in the chip's surface temperature with the incorporation of TGVs in Figure 8 and a 7% reduction in maximum temperature (at 0.5 W power) when a TGV pitch of 400 µm is integrated into the glass interposer (Figure 9). However, the change in chip's surface temperature becomes minimal (maximum temperature decrease of 1.5 °C) when the TGV pitch of 100 µm is substituted with copper (400 W/m.K). The stagnation in thermal performance observed in TGVs (as shown in Figure 8 (a&b)) is due to the low thermal conductivity and the larger volume of the PCB, which hinders efficient heat flow. This is also seen when the thickness of the glass interposer (with TGVs) is reduced from 460 µm to 110 µm in Figure 8. Existing studies indicate that variations in the thermal conductivity of the bump layer significantly impacts the overall thermal performance of the interposer, more so than the TGVs [22].

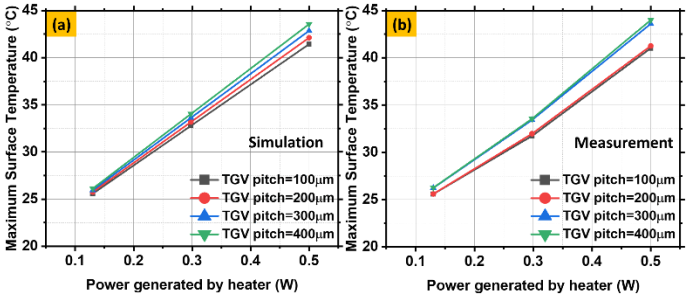


Fig. 7. Comparison of the (a) simulated and (b) measured maximum surface temperatures of the backside of the flip-chip attached reference chip in the thermal test vehicle using different TGV pitches in the glass interposer with increasing input power of the heater loopback in the chip.

While this holds true for Figure 8(b), this trend reverses when the volume of TGVs in the interposer is larger than that of the bumps (as seen in Figure 8(a)). In our case, the volume of TGVs (height= 460 µm) is larger than that of the Bi-Sn solder bumps layer (diameter= 250 µm), hence displaying a larger dip in the temperature of the chip as compared to the bumps. The chip's surface temperature is also lower in the case of TGVs for the 460 µm thick glass interposer as compared to the 110 µm thick glass interposer due to increased heat spreading. In order to achieve stagnation in the thermal performance of TGVs, a 460 µm thick glass interposer requires a slightly higher effective thermal conductivity value for TGVs as compared to the 110 µm thick interposer.

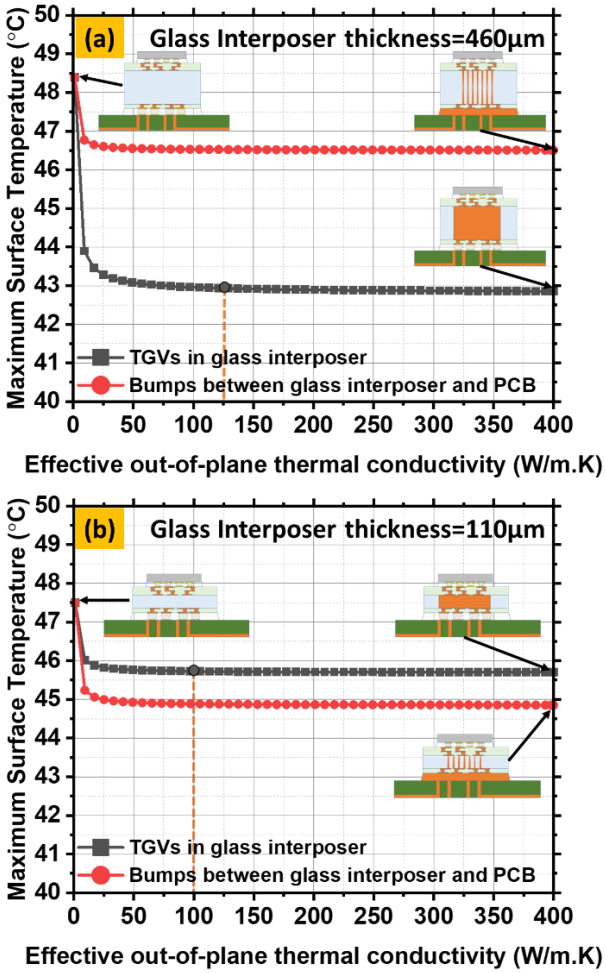


Fig. 8. Simulated variation in the chip's maximum surface temperature with the change in out-of-plane effective thermal conductivity of TGVs and bumps between glass interposer and PCB (with underfill) when the glass thickness/TGV height is (a) 460 µm and (b) 110 µm respectively. PCB (with underfill).

Thus, the incorporation of TGVs is crucial for establishing an effective thermal pathway, although increasing the TGV density (beyond the 100 µm pitch) and further enhancing the effective out-of-plane thermal conductivity of the glass interposer yields negligible impact on the chip temperature. This pitch relaxation of the thermal TGVs can also reduce the thermal stress in the TGVs [27].

The solution, hence, relies on improving the thermal conduction through the whole test vehicle stack by incorporating a heat dissipation mechanism in the PCB. For example, a copper heat sink in PCB offers a high thermal conductivity pathway through the PCB (it offers higher volume than TGVs and Bi-Sn bumps; because the PCB thickness is 1.6 mm). This is evident with an approximately 15 °C decrease in the chip's temperature with the incorporation of a heat sink

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contacting the TEC surface maintained at 20 ºC beneath the PCB (Figure 9). Consequently, integrating a heat sink or micro-thermoelectric cooler in the PCB can lead to efficient cooling of the chip within the package.

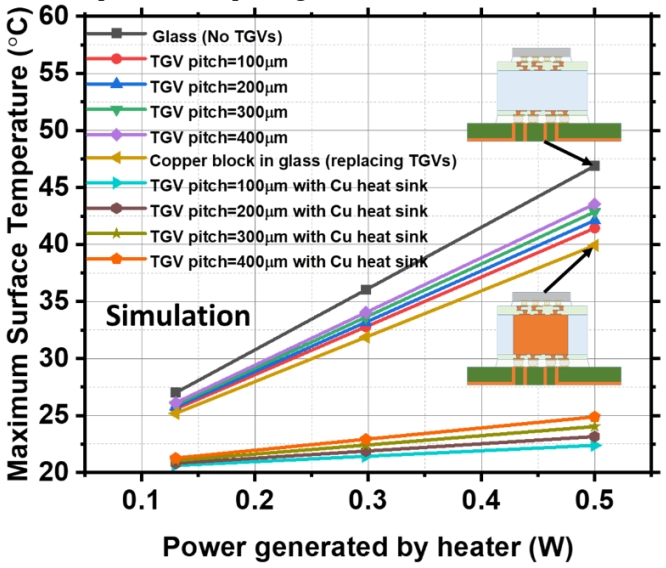


Fig. 9. Variation of the chip's maximum surface temperature with variation in the TGV pitch (100 µm, 200 µm, 300 µm and 400 µm). The figure also shows a significant decrease in maximum surface temperature with a heat sink embedded in the PCB, where the heat sink is the same size as that of the chip.

IV. Assembly and Characterization of Electrical Test Vehicle

A. Assembly of Electrical Test Vehicle

The electrical test vehicle is tailored for characterizing a packaged glass interposer and targeting a single-ended 50 Ω characteristic impedance. The assembly consists of four components: glass interposer, Bi-Sn solder bumps, underfill and PCB.

The assembly process starts with the attachment of 250 µm diameter Bi-Sn solder balls onto the BGA pads of the PCB, facilitated by flux and stencil. Subsequently, the glass interposer is carefully positioned over the Bi-Sn solder balls, and alignment adjustment between the interposer and the PCB is conducted under a high-resolution microscope. The attachment of the glass interposer to the PCB follows the same temperature reflow profile as the one used in the assembly of the thermal test vehicle. The underfill epoxy (EPOTEK 301-2) is applied between the interposer and PCB and cured at room temperature for 36 hours.

Figure 10(a) presents a side-view image of the Bi-Sn solder bonding between the interposer and the PCB (without underfill). To validate the attachment further, the entire assembly undergoes a high-resolution X-ray. The X-ray image in Figure 10(b) depicts the precise alignment and attachment of the BGA pads on the glass interposer to the corresponding bond pads of the PCB through the low-melting temperature solder balls (Bi-Sn), with no missing balls and no solder bridging observed in this process. The assembly process of the electrical test vehicle is also summarized in the supplementary information (Figure 5 in S5).

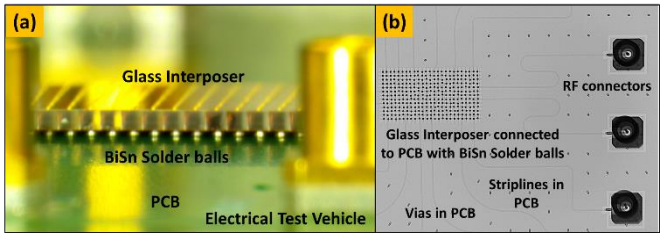


Fig. 10. (a) Side view of the electrical test vehicle showing the Bi-Sn solder balls bonding the glass interposer on the PCB for RF characterization. This side view is pictured after the Bi-Sn solder reflow and before epoxy underfilling. (b) X-ray imaging analysis of the electrical test vehicle.

A 1.6 mm±10% thick PCB for RF characterization is chosen, comprising a Rogers 4350B core, 4450F prepreg, and FR4 stack-up with plated through-hole vias and 50Ω impedance single-ended striplines. The Rogers 4350B PCB substrate has a dielectric constant (ϵr) of 3.66 (8 to 40 GHz) and a loss tangent of 0.0037 (10 GHz) [28]. The design of the BGA pads on the bottom side of the interposer is replicated on the top side of the PCB. The SMP connectors on the PCB enable electrical characterization of the electrical test vehicle.

B. Characterization of Transmission Lines on Glass

The interconnects between EIC and PIC are studied through electrical characterization of CPW transmission lines with varying lengths (3 mm, 4 mm, 5 mm, and 6 mm) of RDL1 lines on glass, without any backside ground (refer to Figure 12(b)). These CPW transmission line traces exhibit a width of 100 µm and signal-ground spacing of 18 µm. The characterization includes measurements of CPW transmission lines using a Vector Network Analyzer (VNA) employing 100 µm pitch GSG probes. Additionally, 3D simulations are executed in ANSYS High-Frequency Structure Simulator (HFSS).

For the CPWs, the S parameters are measured using two GSG air-coplanar probes (ACP) from Cascade (currently FormFactor), with a bandwidth of up to 67 GHz [29]. In order to de-embed the probes, a calibration is performed using an Impedance Standard Substrate (ISS) substrate. The one specific to these probes is the FormFactor 101-190D, which allows for calibration using the Short, Open, Load, Through (SOLT) standard [30].

The simulation outcomes closely correspond to the characterization results, except for the case of L= 4 mm, where deviations may be attributed to surface irregularities, such as scratches on the sample. Losses in the CPW transmission line structure are primarily attributed to slight deviations in characteristic impedance (approximately 51.5 Ω). The variation of characteristic impedance with frequency is depicted in Figure 12 for the CPW transmission line, CPW transmission line with backside ground (CBCPW), and CBCPW transmission line with backside ground and ground fence vias. The incorporation of backside ground and via fence

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surrounding the CPW transmission line serves to mitigate crosstalk and enhance suppression of higher-order modes, as detailed in [31].

The simulated and measured reflections for the transmission lines consistently remain below -15 dB for all lengths up to 40 GHz, as depicted in Figure 11. At 20 GHz, the simulated insertion loss for CPW lengths of 3 mm, 4 mm, 5 mm, and 6 mm is -0.242 dB, -0.325 dB, -0.404 dB, and -0.464 dB, respectively. Correspondingly, the measured insertion loss is -0.55 dB, -0.812 dB, -0.665 dB, and -0.632 dB, respectively. The slope of the S21 plot where the decay is monotonic, when normalized to the frequency and the length of the line, represents the dielectric loss from the glass substrate. For instance, for the 3 mm RDL1 line up to 10 GHz, the dielectric loss is around 0.0435 dB/GHz/cm, which is very close to the values obtained with FR4 material [32] (refer to Figure 6 in supplementary information S6). The slightly elevated insertion loss, especially at frequencies greater than 10 GHz observed in the measured samples compared to the simulated scenarios can be attributed to surface irregularities and the roughness of the copper on glass as the RMS surface roughness of copper is measured to be 12.7±0.3 nm [33].

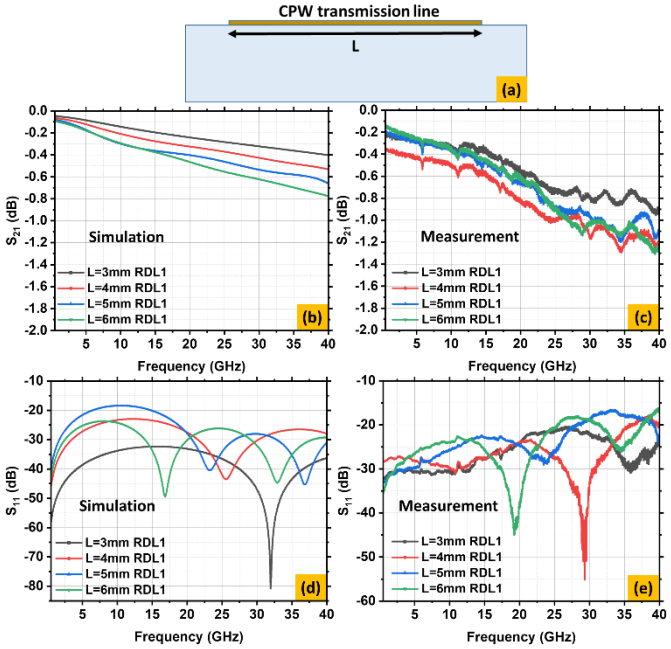


Fig. 11. (a) Schematic showing CPW transmission line on glass. (b) Simulated and (c) measured insertion loss for the CPW transmission line (RDL1) with varying lengths on glass. (d) Simulated and (e) measured return loss for CPW transmission lines on glass with varying lengths.

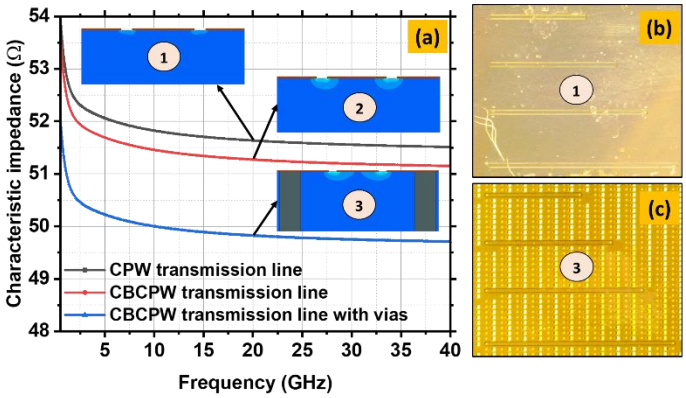


Fig. 12. (a) Variation of characteristic impedance with frequency for the CPW transmission line on glass, conductor backed CPW transmission line (CBCPW) and CBCPW transmission line with via fence connecting the side grounds to the backside ground on top and bottom of the glass interposer with their respective electric field distributions at 20 GHz. (b) shows the top view of the fabricated CPW transmission line on the glass interposer with no backside ground and TGVs and (c) shows the top view of the fabricated CBCPW transmission line with TGVs in the glass interposer.

C. Characterization of Glass Interposer

In addition to the interconnects on the glass interposer, we need to characterize the signal transmission through different components in the glass interposer. Thus, the glass interposer is characterized (Figure 13&14). A ground via fence encircles the signal transmission lines and signal TGVs with a ground via pitch of 500 µm. The characteristic impedance of the CBCPW structure with vias aligns well with 50 Ω, as evidenced in Figure 12.

For the characterization of the glass interposer, the same setup used for the previous sample is employed. The S parameters for the transmission lines are measured using two GSG |Z| probes from FormFactor with a bandwidth of up to 40 GHz [34]. In order to de-embed the probes, a calibration is made using an Impedance Standard Substrate (IIS) substrate. The one specific to these probes is the FormFactor CSR-4, which allows for calibration using the Short, Open, Load, Through (SOLT) standard [35].

Increased insertion losses in this structure, as compared to that in Figure 11, are attributed primarily to the geometrical dimensions of the TGVs, microvias and BGA pads. It also represents a collective impact of several factors: the roughness of the conductor surface between the copper-glass and copper-polyimide interface and the sidewall roughness of the TGVs [36, 37]. The change in the dielectric constant due to the polyimide layer atop the transmission line [38], and impedance discontinuities at the CPW-TGVs, TGV-microvias, and microvia-BGA pad structures [39-41] is included in the simulation model. Both simulation and measurement results demonstrate a good correlation in terms of insertion loss and return loss in the glass interposer structure (Figure 21 and Figure 22). The simulated 3 dB bandwidth for the glass interposer, where RDL1=3 mm, 4 mm, 5 mm, and 6 mm, is

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24.7 GHz, 21.9 GHz, 20.05 GHz, and 24.9 GHz, respectively. Meanwhile, the measured 3 dB bandwidth is 25.55 GHz, 21.63 GHz, 19.56 GHz, and 19.79 GHz, respectively.

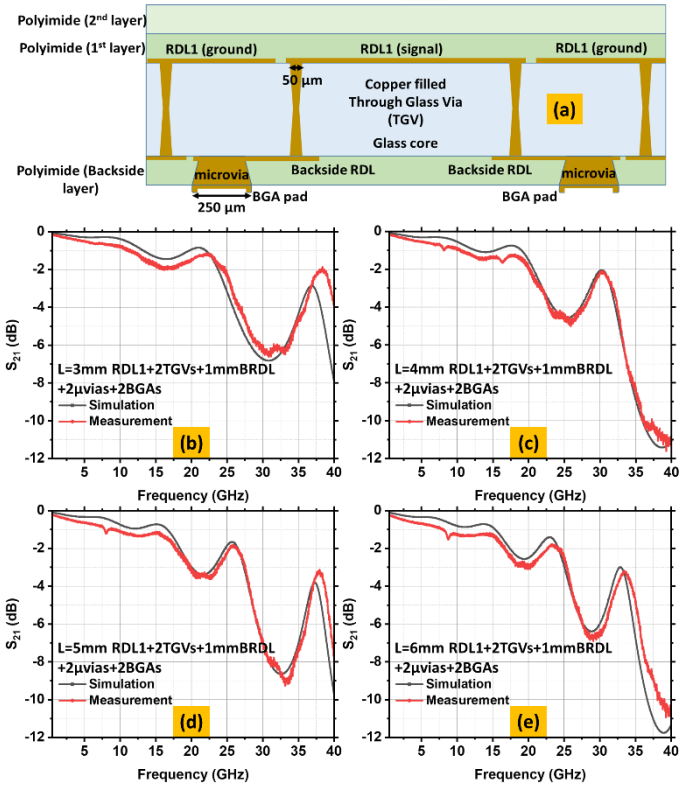


Fig. 13. (a) Schematic showing glass interposer for electrical characterization. Simulated and measured insertion loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

Likewise, the simulated return loss for the glass interposer is -1.964 dB, -0.867 dB, -1.485 dB, and -0.935 dB, respectively at 40 GHz. Meanwhile, the measured return loss is -5.16 dB, -0.962 dB, -2.22 dB, and -0.883 dB, respectively at 40 GHz. The return loss values and trends exhibit a close match, as demonstrated in Figure 14.

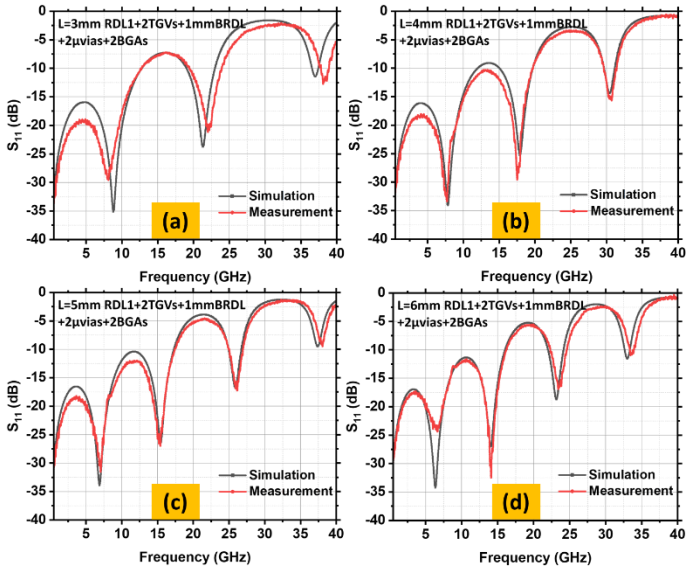


Fig. 14. Simulated and measured return loss results for the glass interposer with different lengths of the RDL1 line on top (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

D. Characterization of Electrical Test Vehicle

Thirdly, we characterize the packaged glass interposer test vehicle, illustrated in Figure 10(a). To measure the S parameters, the VNA needs to be calibrated first in order to transfer the reference plane to the ends of the cables coming out of the VNA. This is done using the electronic calibration kit specific for this VNA (ECAL) [42]. The ECAL module is connected between the ends of the VNA cables at ports 1 and 2, and we run the calibration routine. The results show a flat response up to 67 GHz, indicating good calibration. For the samples mounted on a PCB, the measurement does not need to use RF probes as the PCB is already equipped with miniature SMP connectors [43] with a bandwidth of 40 GHz. The measurements are conducted using RF connectors on the PCB connected to a 2.4 mm 3" cable, which is then linked to the coaxial cable of the VNA. The PCB also has a 2xTHRU [44, 45] structure, which is used to de-embed the effect of the launches and PCB transmission lines. The software used for de-embedding is called In Situ De-embedding by AtaiTec. By de-embedding the losses of the PCB from the losses of the electrical test vehicle, we determine the measured insertion loss for the packaged glass interposer with solder and underfill (Figure 15(a)). The simulation and measurement results follow a similar trend (refer to Figure 15); however, the degradation in the measurements stems from the uneven spread of the underfill between the glass interposer and PCB, which is leading to the resonances in the insertion loss measurements beyond 20 GHz (refer to Figure 7&8 in supplementary information S6). This is further confirmed by the measured return loss, which is lower as compared to the simulated return loss due to the presence of air pockets in the unevenly spread underfill layer(refer to Figure 9 in supplementary information S6).

As compared to the electrical losses in the glass interposer (Figure 13&14), the additional losses in the packaged glass

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interposer are attributed to impedance discontinuities induced by the inductive and capacitive parasitic effects of solder and underfill in the package. The EPO-TEK 301-2 underfill utilized between the interposer and PCB in this case features a dielectric constant and loss tangent of 3.8 and 0.012, respectively at 1 kHz. The Bi-Sn solder balls are cylindrical in shape with a diameter of 250 µm in the simulation model, leading to the underfill thickness between the glass interposer and PCB also being 250 µm in the simulation model.

To mitigate the impact of packaging losses on the glass interposer, especially at high frequencies, improvements in the design of TGVs and microvias are essential for impedance matching. Effective design changes would involve optimizing the diameter and pitch of TGVs, microvias, and BGA pads in the Ground-Signal-Ground (GSG) configuration, along with selecting underfill materials with lower dielectric constants and loss tangents [46, 47].

Hence, the next step is to optimize the electrical design for packaging. The design optimization is conducted for the loopback in the glass interposer, as the simulation and measurement results shown in Figure 15(a) exhibit very high losses. Several changes are implemented: the TGV, microvia, and BGA diameter are adjusted to 70 µm, 100 µm, and 100 µm, respectively. Additionally, the Bi-Sn solder ball diameter is reduced to 100 µm, and the grounding TGV/microvia/BGA pitch is modified to 250 µm. Consequently, the reduction in the Bi-Sn solder ball diameter results in a decrease in the underfill thickness to 100 µm. These alterations aim to minimize impedance discontinuity along the signal path, leading to a significant improvement in the electrical performance of the glass interposer, as demonstrated in Figure 16.

The insertion loss of the optimized design is notably reduced by approximately 11.83 dB (at 40 GHz) compared to the current design featuring the 3 mm long RDL1 line, along with TGVs, microvias, BGA pads, BRDL, solder, and underfill (as depicted in Figure 16(a)). Furthermore, the return loss for the optimized structure remains below -10 dB up to 40 GHz (Figure 24(b)). It is important to note that these improvements are achieved solely through geometrical parameter optimization, while the material properties remain unchanged.

The mechanical integrity of glass core substrates, however, needs to be explored. Due to the low lateral thermal conductivity of glass, non-uniform thermal gradients can lead to mechanical stress and potential failure. The thermal gradient in glass interposers needs careful management to prevent warping or cracking. The thickness of the glass interposer can impact its mechanical strength and pressure compliance. Thicker glass provides better mechanical integrity but may introduce challenges in signal routing. Non-uniform via density can create stress points, affecting the mechanical integrity of the interposer. Ensuring a balanced via distribution and balanced RDLs on both sides of the glass core substrate can help maintain structural integrity [15].

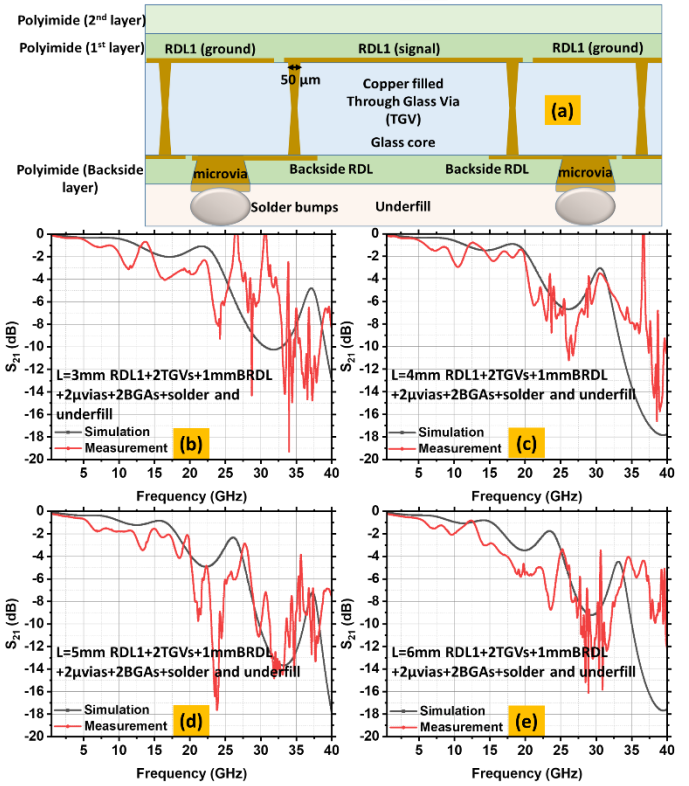


Fig. 15. Schematic showing the electrical test vehicle for characterization (with de-embedded PCB losses). Simulated and measured insertion loss results for the de-embedded test vehicle with different lengths of the RDL1 line (b) 3 mm, (c) 4 mm, (d) 5 mm and (e) 6 mm.

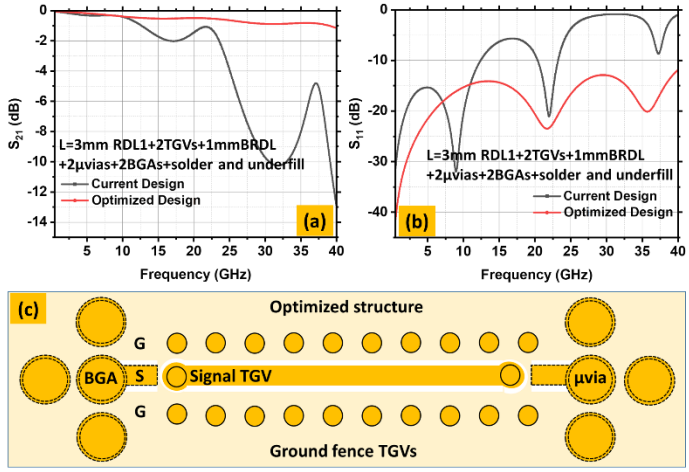


Fig. 16. Simulated insertion loss and return loss for the electrical test vehicle in (a) current design and (b) optimized design. (c) shows the optimized structure where the pitch of the ground fence TGV, microvias, BGA pads and solder are reduced to 250 µm, the microvia, BGA pad and solder diameter are reduced to 100 µm and the TGV diameter is increased to 70 µm to reduce impedance discontinuity along the signal path.

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CONCLUSION

This paper examines the heat dissipation and electrical performance in glass interposers, a vital technology for high-density electronic-photonic packaging. We investigated the effect of varying TGV pitch on the thermal performance of glass interposers and identified its impact on overall functionality. Furthermore, we investigated the electrical losses related to various interconnects in 2.5D glass interposer-based packages.

The heat dissipation in glass interposers is studied by varying the thermal TGV pitch from 100 µm to 400 µm in the thermal test vehicle. Thermal characterization with increasing TGV pitch from 100 µm to 400 µm reveals an increase of 2.9ºC in the chip's maximum surface temperature. The FEM simulation indicates that the incorporation of TGVs in the glass interposer leads to an improvement in its thermal performance, but the variation of TGV pitch lower than 100 µm has minimal impact on the heat dissipation of the reference thermal chip packaged on the glass interposer. This is because of the presence of the highly thermal-resistant PCB, which occupies a large volume, impeding heat conduction through it. Thus, the integration of a heat sink or micro-TEC in the PCB can reduce the thermal resistance incurred through the PCB.

Furthermore, electrical characterization of the packaged glass interposer reveals significant losses induced by impedance discontinuities along the signal path, including TGVs, microvias, BGA pads, solder, and underfill. Optimizing the design of TGVs, microvias, and BGA pads can result in lower electrical loss in the glass interposer. By minimizing impedance discontinuity, the signal transition from the narrower line/spacing of the glass interposer to the wider line/spacing of the PCB achieves an impressive reduction in insertion loss, bringing it closer to the performance of transmission lines on the glass.

The understanding of thermal management and signal transmission challenges related to electronic-photonic packaging using glass interposers can help in establishment of practical recommendations to improve performance and reliability in the future.

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