Electrically Active Interface Defects in the InGaAs MOS system

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Abstract

In this work we present experimental results examining the energy distribution of the relatively high (>1 × 10^{12}cm^{-2}.eV^{-1}) density of electrically active defects which are commonly reported at the interface between high dielectric constant (high-*k*) thin films and $In_{0.53}Ga_{0.47}As$. The interface state distribution is examined for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) system based on analysis of the full gate capacitance (C_g-V_g) of the surface *n*-channel $In_{0.53}Ga_{0.47}As$ MOS transistors. The experimental capacitance, recorded at -50°C and 1 MHz to minimize the contribution of interface state to the capacitance, is compared to the theoretical quasi-static C_g-V_g response to evaluate the interface state distribution across the $In_{0.53}Ga_{0.47}As$ energy gap and extending into the $In_{0.53}Ga_{0.47}As$ conduction band. To improve the accuracy of the fitting process, the Maserjian Y-function was used in the modeling of the interface defects and fixed oxide charge densities. The analysis reveals a peak of donor-like interface traps with a density of 1.5 × 10^{13} cm^{-2}.eV^{-1} located at ~0.36 eV above the $In_{0.53}Ga_{0.47}As$ valence band edge, a high density of donor-like states increasing towards the $In_{0.53}Ga_{0.47}As$ valence band. The analysis also indicates acceptor-like interface traps located in the $In_{0.53}Ga_{0.47}As$ conduction band, with a density of ~ 2.5 × 10^{13} cm^{-2}.eV^{-1} at 0.3eV above the $In_{0.53}Ga_{0.47}As$ conduction band minima. The reported interface state density is similar to reports for others oxides, suggesting that the recorded interface states originate from the $In_{0.53}Ga_{0.47}As$ surface.

1. Introduction

For several decades improvements in the performance of integrated circuits (IC's) has been based primarily on transistor miniaturisation. However, as minimum device dimensions reduced to below 50 nm, transistor miniaturisation no longer remained as the single driving force behind the development of nano-electronic integrated circuits. In the recent technology generations new materials have been

incorporated into the device to enhance transistor performance and to maintain or reduce the overall IC's power dissipation. High dielectric constant (high-*k*) materials have been introduced into the gate stack to minimise gate leakage current while maintaining capacitive coupling between the gate and the channel [1]. New device architectures have been implemented to induce strain into the transistor in order to boost the carrier mobility in the channel [2]. Looking beyond the 22 nm technology node there is a strong research interest in the heterogeneous integration onto a silicon platform of high mobility semiconductors, such as germanium [3] or GaSb [4] for *p* channel devices and III-V compound semiconductors for the complementary *n* channel devices.

Considering the *n* channel devices, many III-V substrate options have been reported including, GaAs [5], $In_xGa_{1-x}As$ [6,7], InAs [8] and InSb [9]. Indeed, the viability of using such high mobility materials has recently been given a new impetus for a number of reasons. Firstly, there has been significant progress in the integration of III-V onto a silicon platform [6,10]. Secondly, the use of atomic layer deposition [11] has been shown to lead to considerable improvements in the electronic properties of the high-*k*/III-V interface and the demonstration of true inversion in InGaAs MOS systems [12-14]. Thirdly, there have been very encouraging recent results indicating specific contact resistivity values to III-V compounds as low as ~2×10^{-9} Ω.cm^2 [15]. The combination of these three factors has revitalised the interest in III-V materials for high performance and low power *n* channel device applications.

For the successful incorporation of these alternative III-V channels into future MOSFET processes it is required to both quantify and control electrically active interface state defect densities (D_{it}), which are present at the high-*k*/semiconductor interface as well as fixed charges and electron or hole traps, which are located within the high-*k* oxide layer. Considering the case of the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system, interface state densities at around the mid-gap energy in the $In_{0.53}Ga_{0.47}As$ energy gap are typically reported to be in the range mid-10^{12} to 10^{13}cm^{-2} .eV^{-1} [16-19]. These densities remain too high for practical device applications. As well as the density of state at the mid-gap, it is important to characterise the distribution of interface defects throughout the energy gap, referred to here as $D_{it}(E)$. Knowledge of $D_{it}(E)$ is important as any specific features in the density of interface states distribution can be compared to theoretical models of defect energies [20] as a method to identify the physical origin of the interface states.

One approach to obtain the distribution of interface states across the band gap in the high-*k*/InGaAs MOS system is to obtain the true quasi-static C_g-V_g response of an MOS capacitor, and obtain $D_{it}(E)$ by a comparison to the theoretical response [21]. An alternative approach is to use both *n* and *p* type InGaAs MOS capacitor structures to examine $D_{it}(E)$ in the upper and lower portions of the InGaAs energy gap [22]. Ali et al. [23] reported a method to determine the $D_{it}(E)$ across the energy gap based on the frequency dependent gate to channel capacitance and conductance of an surface channel InGaAs MOSFET. In this work we extend on these studies to explore the use of the full gate capacitance of an InGaAs surface *n*-channel MOSFETs, in conjunction with the Maserjian Y-function, to profile the interface state density across the gap. The results are compared to other reports in the literature.

2. Sample Details

The experimental samples used in this study to investigate the interface state density profile are surface-channel MOSFETs fabricated on a 2-µm-thick Zn-doped (4×10^{17} /cm^3) *p*-$In_{0.53}Ga_{0.47}As$ layer grown on a

2-inch *p*+ InP wafer by metal-organic vapor phase epitaxy (MOVPE). The $In_{0.53}Ga_{0.47}As$ surface passivation prior to gate oxide deposition was an immersion in 10% $(NH_4)_2S$ at room temperature for 20 min, which was found to be an optimum in terms of interface state reduction and for the suppression of native oxide formation [22], [24]. The transfer time to the atomic layer deposition (ALD) reactor after surface passivation was less than 5 min. A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of $Al(CH_3)_3$ (TMA) and H_2O precursors at 250°C. The source and drain (S/D) regions were selectively implanted with a Si dose of 1×10^{14} /cm^2 at 80 keV and 1×10^{14} /cm^2 at 30 keV. Implant activation was achieved by rapid thermal anneal (RTA) at 600°C for 15 s in a N_2 atmosphere [25]. A 140-nm-thick SiO_2 field oxide was formed by electron beam evaporation and liftoff to minimize the gate pad capacitance. A 200-nm-thick Pd gate was defined by electron beam evaporation and liftoff. Non-self-aligned ohmic contacts were defined by lithography, selective wet etching of the Al_2O_3 in dilute HF and electron beam evaporation of a Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack [26]. A 300°C for 30 min forming gas (5% H_2/95% N_2) anneal was carried out in an open tube furnace. A schematic cross section of the device is shown in Figure 1 (a), with a TEM image of the gate stack region presented in Figure 1 (b), confirming the thickness of the ALD formed Al_2O_3 layer as 10 nm. The surface-channel $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs, featured a threshold voltage, V_T, of 0.43 V, an inverse subthreshold slope, *SS*, of 150 mV/dec., an I_{ON}/I_{OFF} of ~10^4 and a source/drain resistance, R_{SD}, of 103 Ω, Further details can be found in [27].

3. Experimental Results

3.1 Full gate capacitance of the $In_{0.53}Ga_{0.47}As$ MOSFET: Evaluation of the Integrated D_{it}

The full gate capacitance of the $In_{0.53}Ga_{0.47}As$ MOSFET as a function of the applied gate voltage (C_g-V_g) characteristic was obtained using a measurement configuration with the gate contact connected to the "high" of the impedance meter and the source, drain and substrate contacts shorted together and connected to the "low". In this measurement configuration, the inversion charge is provided through the source and drain for the condition of strong inversion at the Al_2O_3/ *p*-$In_{0.53}Ga_{0.47}As$ interface, and the full C_g-V_g response can be obtained [28].

Figure 2 shows an example of the full gate capacitance of the *n* channel MOSFET (W = 100 µm, L = 10 µm) measured at 20°C from 1 kHz to 1 MHz. The experimental C_g-V_g characteristic was corrected for parasitic capacitances using the method reported in [29]. The threshold voltage (V_T) is indicated on the Figure, and is in good agreement with the V_T value determined from the DC transfer characteristics of the MOSFET. The high level of dispersion of the capacitance with the ac signal frequency in the region corresponding to surface depletion of the Al_2O_3/ *p*-$In_{0.53}Ga_{0.47}As$ interface (V_g: -2.5 to 0.4V) is attributed to the capacitive contribution of interface defects and/or border trap response. The approach in this work is to minimize the interface defect and/or border trap capacitance response by an increase in the ac signal frequency and a reduction of the measurement temperature. It is noted that under such measurement conditions, interface traps are manifest primarily as a stretch out of the depletion part of the C_g-V_g

characteristic along the gate voltage axis. Ac signal frequencies higher than 1 MHz were avoided to prevent distortion of the inversion part of the C_g-V_g characteristic due to channel resistance effects [23]. [1]

The C_g-V_g measurements performed at an ac signal frequency of 1 MHz and a temperature of -50 °C are shown in Figure 3. Based on assumed interface defects capture cross sections of ~ 1×10^{-15} cm^2, the temperature of -50°C and ac signal frequency of 1 MHz should remove interface defect capacitance response from E_v + 0.17eV eV to E_v + 0.63 eV [30], where E_v is the valence band maxima. Also plotted in Figure 3 in the ideal theoretical C_g-V_g response at -50°C for the case no interface states, border traps or bulk oxide charges. The ideal C_g-V_g response was obtained by solving the Poisson equation in depletion [31] and the self-consistent Poisson-Schrödinger equations in inversion, including quantization in all valleys [32]. In the theoretical calculations, the work function of Pd on Al_2O_3, the Al_2O_3 film thickness and *k*-value, and the p-$In_{0.53}Ga_{0.47}As$ doping were set to 4.7 eV [33], 10 nm (from TEM in Figure 1(b)), 8.6 [27] and 3.3×10^{17} /cm^3 (obtained from measured minimum capacitance), respectively.

The comparison of the measured and theoretical response has a number of relevant features. Firstly, the experimental threshold voltage is shifted in a negative direction along the gate voltage axis, indicating the presence of positive fixed charge in the Al_2O_3, consistent with previous reports [34, 35]. The magnitude of the difference between the V_T from the modelled C_g-V_g characteristic to that of the experimental C_g-V_g characteristic (ΔV_T) corresponds to a positive oxide N^+, given by $N^+ = C_{OX} \times \Delta V_T / q$, where, $\Delta V_T = V_{T,theo} - V_{T,exp}$ and q is the charge of an electron. Based on the results in Figure 3, a positive charge density of $N^+ = 1.2 \times 10^{12}$ cm^{-2} located at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ is obtained, and this value is consistent with the density of positive charge determined from Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors [34]. It is noted that this value of N^+ is the equivalent positive oxide charge at the interface. The results in [34, 35] for a range of Al_2O_3 thicknesses indicate that the positive charge in the Al_2O_3 film is distributed throughout the bulk of the oxide layer.

From Figure 3, it is also evident that the experimental capacitance in inversion exceeds the theoretical value. This observation is consistent with other reports, where the experimental results indicate that interface states exist with energy levels aligned with the $In_{0.53}Ga_{0.47}As$ conduction band [21, 36, 37]. The interface states with energies above the $In_{0.53}Ga_{0.47}As$ conduction band minima (E_C) provide an additional capacitance in parallel with the inversion capacitance, which increases the measured capacitance towards the oxide capacitance, C_{OX}.

Finally, it is also evident from Figure 3 that the experimental characteristic from V_T towards the flat band voltage (V_{FB}) is stretched out in comparison to the theoretical response. This stretch is the results of charging Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface states located within the $In_{0.53}Ga_{0.47}As$ energy gap with the varying gate voltage. The experimental and modelled values of V_T and V_{FB}, as identified in Figure 3, can be used to estimate the integrated density of interface states across the $In_{0.53}Ga_{0.47}As$ energy gap in units [cm^{-2}]. For $In_{0.53}Ga_{0.47}As$ (E_g ~ 0.75eV) with a doping of $3.3 \times 10^{17}cm^{-3}$, the condition of flat band and inversion corresponds to surface Fermi level (E_f) positions of E_f-E_v = 0.04 eV and E_f-E_v= 0.71 eV, respectively. As a consequence, the conditions of V_{FB} and V_T in the C_g-V_g characteristic spans the majority of the $In_{0.53}Ga_{0.47}As$ energy gap. The approach reported here develops of the method reported in [34], where the

[1] It is noted that we have not confirmed that a temperature of -50°C and a 1 MHz ac signal frequency represents a true high frequency response. These conditions are used in this work as they represent a practical limit set by the probe station (-50°C) and an upper limit on the *ac* signal frequency set by the channel resistance effects.

experimental flat band conditions in *n* and *p* doped InGaAs MOS structures were used to evaluate the integrated D_{it} across the energy gap. The availability of a four terminal transistor allows the evaluation of the integrated D_{it} value with a single device structure. The additional gate voltage required to sweep from V_T to V_{FB} in the experimental curve compared to the theoretical (ideal) curve is directly related to the integrated $D_{it}(E)$ across the energy gap, as $D_{it} = C_{OX} \times (\Delta V_{FB} - \Delta V_T)/q$, where $\Delta V_{FB} = V_{FB,theo} - V_{FB,exp}$. From Figure 3, this yields a value of $D_{it} = 1.2 \times 10^{13}$ cm^{-3}, which is the integrated $D_{it}(E)$ from the flat band condition (E_f-E_v = 0.04eV) to the onset of strong inversion (E_f-E_v= 0.71 eV).

3.2 The Interface State Density Profile $D_{it}(E)$

The measurement of the experimental flat band and threshold voltages provides a value for the integrated $D_{it}(E)$ across the energy gap, but does not provide details of the interface state distribution. One approach to obtaining the energy distribution of the interface states is to introduce an interface state density profile into the simulated C_g-V_g response.

To assist with the process of matching the experimental and simulated characteristics we have used the Maserjian Y-function [38, 39], which is given by the following expression $Y = C_g^{-3} \cdot dC_g / dV_g$. The Maserjian Y-function highlights threshold voltage (V_T) and also aids in the determination of the flat band voltage (V_{FB}) and the substrate doping. Importantly, the Y-function is independent of the oxide capacitance, as the function is a derivative of the total gate capacitance and the constant oxide capacitance is removed. This is particularly useful in the analysis of the high-*k*/III-V MOS system as the low density of states in the conduction band together with issue of interface states with energies aligned with the conduction band, makes the extraction of the oxide capacitance problematic. An example of simulated Maserjian Y-function is shown in Figure 4(a) for a P_d/Al_2O_3(10nm)/*p* $In_{0.53}Ga_{0.47}As$/*p*-InP MOS structure, indicating the V_T, V_{fb} and the Y_{min} value which relates to the doping concentration in the semiconductor. The simulation in Figure 4 (a) is for the ideal case of no interface states or fixed oxide charges. The experimental and theoretical Maserjian Y-functions are shown together in Figure 4(b), indicating the threshold voltage shift (ΔV_T = 0.4 V) between the two responses due to the fixed oxide charge. There is also a difference between the experimental and ideal Y-functions over the gate bias range from 0.5 V to -2 V, which we attribute to the effect of interface states.

With the introduction of an interface state distribution into the energy gap in the theoretical (C_g-V_g) response, it is possible to induce the stretch out observed experimentally in the (C_g-V_g) characteristic at -50^{o}C and 1 MHz. This is shown in Figure 5 (a), with the corresponding Maserjian Y-functions in Figure 5(b). In the theoretical (C_g-V_g) response, a positive fixed oxide charge density of 1.2×10^{12} cm^{-2}, as determined from Figures 3 and 4, is also introduced to align the V_t values. It is noted that in the inversion region of the C_g-V_g characteristics the curves are still not aligned. In this region of the C_g-V_g response it is not possible to "freeze-out" the effect of interface states at 1 Mz and -50^{o}C. This is illustrated in Figure 6, and is consistent with interface defects with energies aligned with the conduction band. The method of using high frequencies and reduced temperatures to freeze-out interface states is based on a thermionic emissions term for emission of electron from the defects to the conduction or valence bands. For defects aligned with the conduction band there is no requirement to change energy to enter the InGaAs conduction band. While there could be a local potential barrier around the localised state at the interface,

the experimental results in Figures 6 (a) and (b) indicates that it is not possible to freeze out the interface defects response at -50ºC and 1 MHz. As a consequence, this portion of the curve is fitted with an interface state density profile extending into the conduction band and the quasi-static self-consistent Poisson-Schrödinger equations for the Al_2O_3/ *p*-$In_{0.53}Ga_{0.47}As$ interface in inversion.

The resulting experimental and theoretical C_g-V_g responses and the corresponding Maserjian Y-functions are shown in Figures 7(a) and 7 (b), respectively. The resulting interface trap density versus energy profile $D_{it}(E)$ is shown in Fig. 8 and presents three main features. There is a large density of donor traps extending from the $In_{0.53}Ga_{0.47}As$ valence band into the lower part of the $In_{0.53}Ga_{0.47}As$ energy gap. There is a feature peaking at 1.5×10^{13} $cm^{-2}.eV^{-1}$ and centred at 0.36 eV above the $In_{0.53}Ga_{0.47}As$ valence band edge. The fitting of the experimental and theoretical C_g-V_g responses can only be obtained by the use of donor like (+/0) interface defects within the $In_{0.53}Ga_{0.47}As$ energy gap. This is in agreement with the results reported in [21,34]. The density of interface states approaching the $In_{0.53}Ga_{0.47}As$ E_c is low (reducing below 1×10^{12} $cm^{-2}.eV^{-1}$), and is consistent with the steep transition towards strong inversion and low frequency dispersion observed in the gate to channel capacitance (Figure 6(a)). There is also a broad feature extending into the conduction band, acquiring a density of ~ 2.5×10^{13} $cm^{-2}.eV^{-1}$ at 0.3eV above the $In_{0.53}Ga_{0.47}As$ E_c. These defects are acceptor like (0/-) in agreement with [21], and the density values obtained of ~ 2.5×10^{13} $cm^{-2}.eV^{-1}$ at 0.3eV above the $In_{0.53}Ga_{0.47}As$ conduction band minima are in very close agreement with $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures reported in [21] and the case of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS with an $(NH_4)_2S$ surface preparation reported in [37].

4. Discussion

In relation to the interface state density profile presented in Figure 8, the presence of a peak in $D_{it}(E)$ around the mid-gap energy is in agreement with the work reported in [23] for $In_{0.53}G_{0.47}As$ *n* channel MOSFETs with an $LaAlO_3$ high-*k* gate dielectric. In this work, a peak $D_{it}(E)$ of around 4×10^{13} $cm^{-2}.eV^{-1}$ with a peak energy of E_v+0.45eV was evaluated. A peak in the $D_{it}(E)$ profile near the mid gap energy with a density ~ 2.5×10^{13} $cm^{-2}.eV^{-1}$ has also been reported for the $SrTa_2O_6/In_{0.53}Ga_{0.47}As$/InP MOS system [40]. The observation of a similar peak $D_{it}(E)$ position for a range of different high-*k* oxides suggests the dominant interface defects originate from $In_{0.53}Ga_{0.47}As$ surface. In relation to the physical origin of the interface states, the density and charge transition type are consistent with As_{Ga} antisite defects based on hybrid density functional calculations of point defects in III–V compounds [20].

The peak observed in the interface state density in this work and other publications [23], is not always reported. The $D_{it}(E)$ profiles reported in [21, 41, 41], show a monotonic increase in D_{it} from the $In_{0.53}Ga_{0.47}As$ conduction band towards the valence band edge. It is possible that, in these works, there is a broader distribution in the interface state density which increases towards the valence band energy, such that a clear peak around the mid-gap energy cannot be discerned. It is important to establish whether or not there are peak features in $D_{it}(E)$ distribution at the high-*k*/ $In_{0.53}Ga_{0.47}As$ interface, as it is of direct relevance to studies focussed on the understanding the atomic identification of interface states. In the case of the SiO_2/Si and high-*k*/Si interfaces, the use of electron spin resonance in conjunction with capacitance-voltage analysis has been successfully used to provide atomic identification of the primary interface defects, which are silicon dangling bonds [43, 44, 45]. In the case of high-*k*/ $In_{0.53}Ga_{0.47}As$ interfaces, the use of electron spin resonance will be complicated by the fact that the naturally occurring

isotopes of In, Ga and As all have a nuclear spin, the effect of which is to broaden the ESR signal associated with dangling bonds of In, Ga and As. In addition, the interface defects could be dimers or anti-site defects which may not have associated unpaired electrons. As a consequence, an approach being perused to gain insight into the atomic origin of the interface defects is through first principles calculations of defects energies and charge transitions [20, 46], and a comparison of these defects energy levels to experimental results. If there is no clear peaks in the $D_{it}(E)$ profiles from the experimental data, this closes off this approach to atomic identification. As a consequence, there is a need to further study the interface state density profile, and explore ways to characterise the interface with a higher energy resolution.

The relatively high density of interface defect around mid-gap (~1.5×10^{13} $cm^{-2}.eV^{-1}$) and the sharp increase in interface state density towards the valence band edge, as shown in Figure 8, can be reduced based on an optimisation of the surface preparation of the InGaAs surface prior to the ALD growth of the Al_2O_3 layer. A wide range of approaches have been explored to reduce the interface state density at the InGaAs/oxide interface , including: nitridation of the InGaAs surface [47], the deposition of Ga suboxides on an As decapped InGaAs surface [48], the use of As capping layers desorbed in the ALD reactor [49] and the use of undoped InP capping layers [6]. The use of an optimised $(NH_4)_2S$ surface preparation [22, 24], and a reduction of the transfer time from the $(NH_4)_2S$ solution to the ALD chamber (~ 3 minutes) has been demonstrated to results in surface inversion over both *n* and *p* type InGaAs [13], with mid-gap interface state density values in the range 6-9 $\times 10^{11}$ $cm^{-2}.eV^{-1}$. The observation of surface inversion for the *n*-InGaAs/Al_2O_3 interface also demonstrates that the high D_{it} values towards the valence band edge can be reduced using the optimised (10%, 20 minutes, 25^{o}C) $(NH_4)_2S$ surface preparation and minimum transfer time to the ALD reactor.

Finally, it is noted that further work is required to identify the true high frequency C_g-V_g response for the $In_{0.53}G_{0.47}As$ MOS system. This is important as the true high frequency C_g-V_g response is required both for D_{it} density evaluation and to relate the gate voltage to the energy position when evaluating the interface state density profile. The low frequency quasi-static C_g-V_g can also be employed, but this also has associated challenges [19]. In this work, we used -50^{o}C and 1 MHz to minimise the interface trap response, and based on [30] and an assumed interface state capture cross section of 1×10^{-15} cm^{-2}, this should achieve a true high frequency C_g-V_g for the majority of the energy gap. However, this is an area where further study is needed, and may require lower temperature measurements at liquid nitrogen (77K) or even < 77K using liquid helium, to identify the true high frequency C_g-V_g response needed to relate the gate voltage to the corresponding surface potential.

5. Conclusion

Electrically active interface defects have been examined for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ system using full gate capacitance measurements on surface *n*-channel $In_{0.53}Ga_{0.47}As$ MOS transistors. Poisson modeling in depletion and quasi-static self-consistent Poisson-Schrödinger modeling in inversion were used in conjunction with the experimental gate capacitance to obtain the interface state density across the $In_{0.53}Ga_{0.47}As$ energy gap and extending into the $In_{0.53}Ga_{0.47}As$ conduction band. To assist with the process of matching the experimental and simulated gate capacitance measurements, the Maserjian Y-function was used to highlight the threshold and flat band voltage conditions. The Maserjian Y-function is

particularly useful for the analysis of the high-*k*/InGaAs MOS system as the function is not dependent on the oxide capacitance, which can be difficult to obtain for high-*k*/InGaAs structures.

The analysis revealed donor-like (+/0) interface states within the $In_{0.53}Ga_{0.47}As$ energy gap, with a peak density of ~1.5×10^{13} $cm^{-2}.eV^{-1}$ and centered at 0.36 eV above the $In_{0.53}Ga_{0.47}As$ valence band edge. There is a sharp increase in electrical active defects in the energy range 0.1 eV to 0.2 eV above the valance band edge. These states are also donor-like, but it is not possible to discern if they are conventional interface states, border traps, or a combination of both defect types from the measurements and analysis performed. The analysis also indicates acceptor-like interface traps located in the $In_{0.53}Ga_{0.47}As$ conduction band, with a density of ~ 2.5×10^{13} $cm^{-2}eV^{-1}$ at 0.3 eV above the $In_{0.53}Ga_{0.47}As$ conduction band minima. The interface state density profile is broadly similar to reports for other high-*k* oxides, such as $LaAlO_3$, suggesting the interface defects originate from the $In_{0.53}Ga_{0.47}As$ surface.

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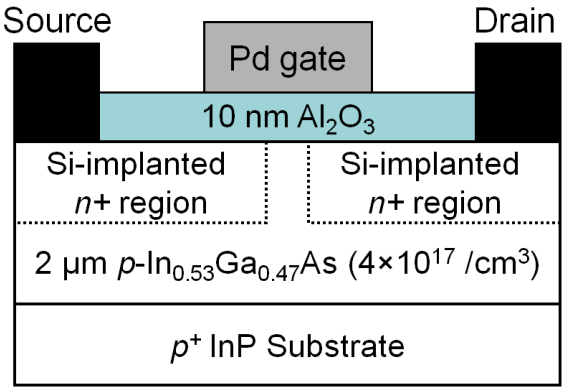

Figure 1 (a). Schematic cross-sectional diagram of a surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET with a 10-nm thick ALD Al_2O_3 gate dielectric.

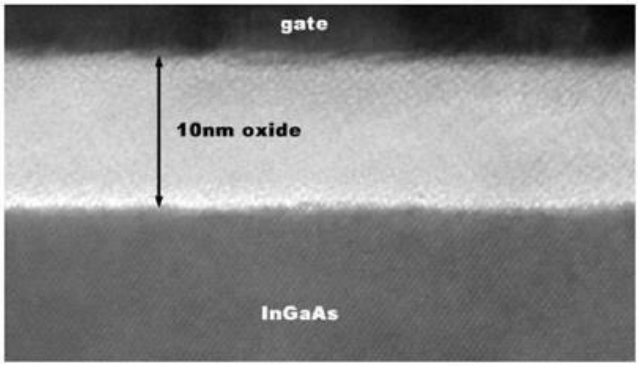

Figure 1 (b) Cross sectional TEM images through the gate stack region of the MOSFET. A C_{OX} of 7.6×10^{-3} F/m^2 was obtained based on the extracted Al_2O_3 *k*-value of 8.6 and the measured T_{OX} of 10 nm.

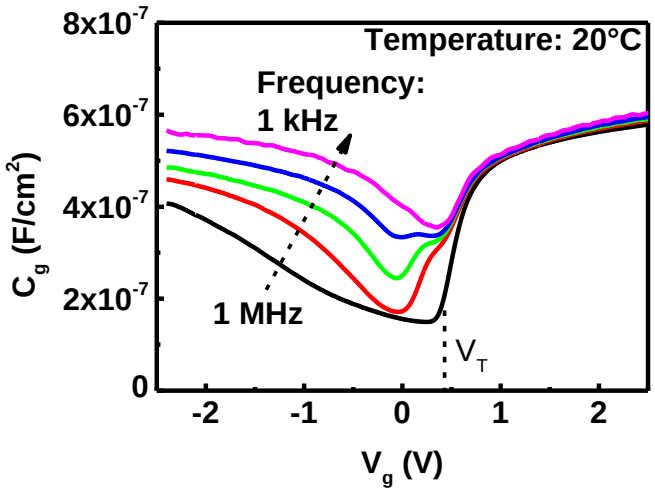

Figure 2. The full multi-frequency gate capacitance (C_g-V_g) response of the $In_{0.53}Ga_{0.47}As$ MOSFET recorded at room temperature for selected frequencies (1 kHz to 1 MHz). The C_g-V_g response was measured with the gate contact connected to the "high" of the impedance meter and the source, drain and substrate contacts shorted together and connected to the "low".

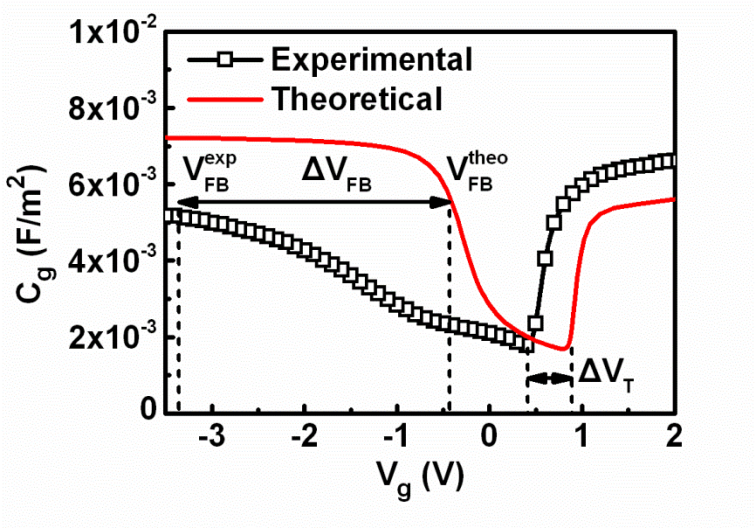

Figure 3. Comparison of the Cg-Vg characteristics, obtained for an *ac* signal frequency of 1 MHz and a temperature of -50°C, to the theoretical QS C-V characteristics at -50°C, obtained from a self-consistent Poisson Schrödinger simulation. An integrated D_{it} of 1.2×10^{13} cm^{-2} and a fixed positive oxide charge N^{+} of 1.4×10^{12} cm^{-2} are obtained from the from the difference between the experimental and theoretical values of the flat band voltages ΔV_{FB} and the threshold voltages, ΔV_T .

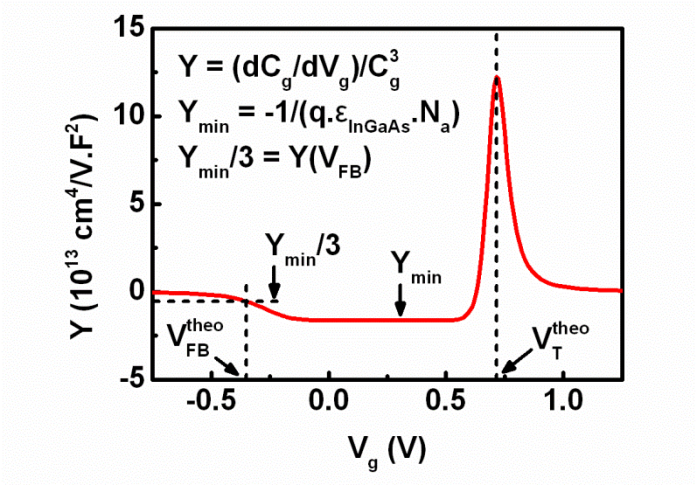

Figure 4 (a) Example of a simulated Maserjian Y-function for a Pd/Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ MOS structure, with 10nm of Al_2O_3 and a *p*- $In_{0.53}Ga_{0.47}As$ doping of $3.1x10^{17}$ cm^{-3}. This is for the ideal case of no interface and no fixed oxide charges.

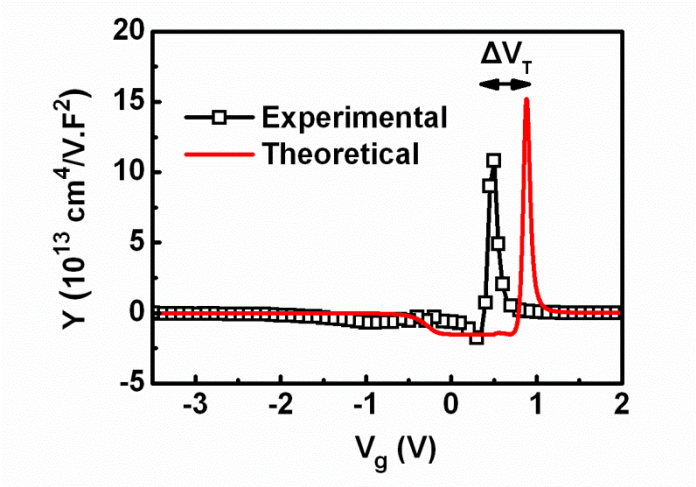

Fig 4 (b) Experimental and simulated (ideal) Maserjian Y-functions for a Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSFET structure (-50ºC). The simulated (ideal) response is for the case of no interface and no fixed oxide charges.

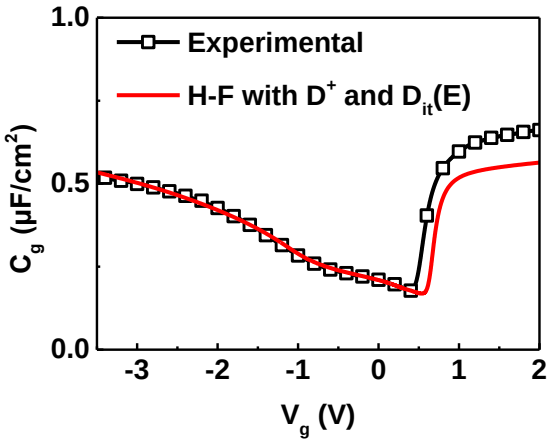

Figure 5 (a) Experimental and simulated high frequency C_g-V_g response (Poisson only) for a Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSFET structure (-50°C). An interface state density profile has been introduced into the simulated response to match the C_g-V_g stretch out in the bias range 0.4 V to -3.5 V. Note how the simulated C_g-V_g response (Poisson only) is below the experimental value in inversion.

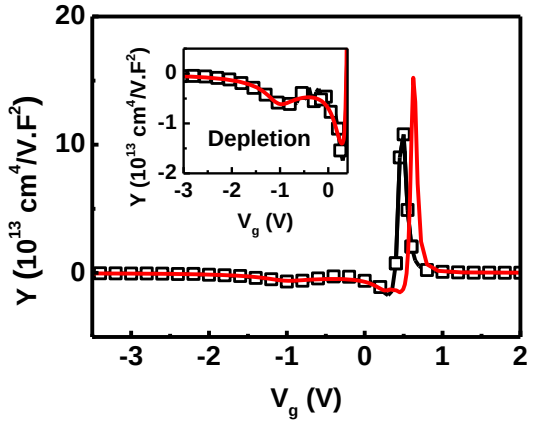

Figure 5 (b) Experimental and simulated Maserjian Y-functions for a Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSFET structure (-50°C), corresponding to Figure 5(a). An interface state density profile introduced into the simulated response is varied to match the simulated and experimental Maserjian Y-functions in the bias range of 0.4 to -3.5 volts. The inset highlighted this bias region. Note, even though the positive oxide charge ($1.2x10^{12}$ cm^{-2}) is introduced in the simulated Y function, the peak value (corresponding to V_T) is not fitted as the simulation is Poisson only. The self-consistent Poisson-Schrödinger solution in inversion introduces a further V_T shift (as seen in Figures 7(a) and 7 (b)).

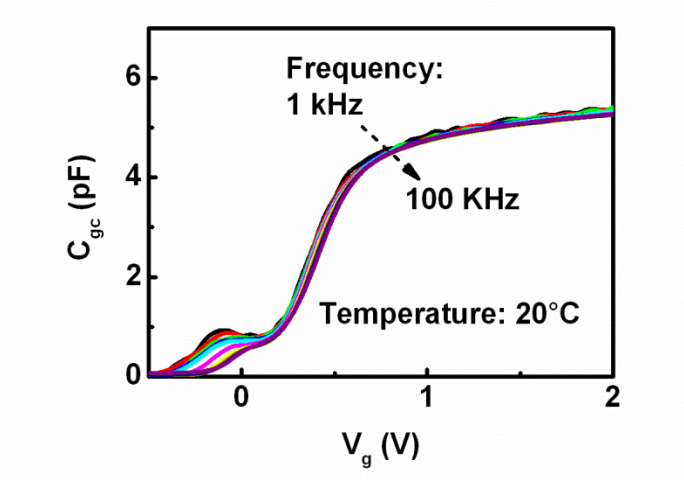

Figure 6 (a). Gate to channel capacitance of the *n*- $In_{0.53}Ga_{0.47}As$ MOSFET (W = 100 µm, L = 10 µm) from 1 kHz to 100 kHz at 20°C. The device V_T = 0.4V. Note the low level of frequency dispersion in inversion. The results suggest defects with energies within the $In_{0.53}Ga_{0.47}As$ conduction band have a minimal change in response over the frequency range 1 kHz to 100 kHz. The results indicate that the inclusion of interface states and a quasi-static solution are required to fit this region of the Cg-Vg characteristic. The effect of interface states within the $In_{0.53}Ga_{0.47}As$ energy gap is evident as the frequency dispersion in the bias range -0.5 to 0 volts.

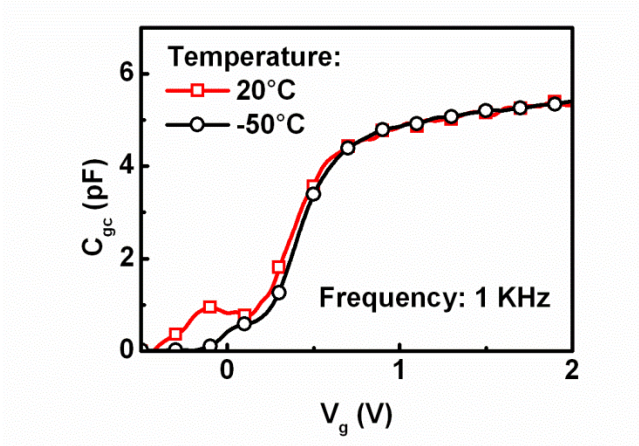

Figure 6 (a). Gate to channel capacitance of the *n*- $In_{0.53}Ga_{0.47}As$ MOSFET (W = 100 µm, L = 10 µm) at 1 kHz at -50°C and 20°C. The device V_T = 0.4V. Note the low level of frequency dispersion in inversion. The capacitance in inversion is not changing over the temperature range 20°C to -50°C. The effect of interface states within the $In_{0.53}Ga_{0.47}As$ energy gap is evident as the change of capacitance with temperature in the bias range -0.5 to 0 volts.

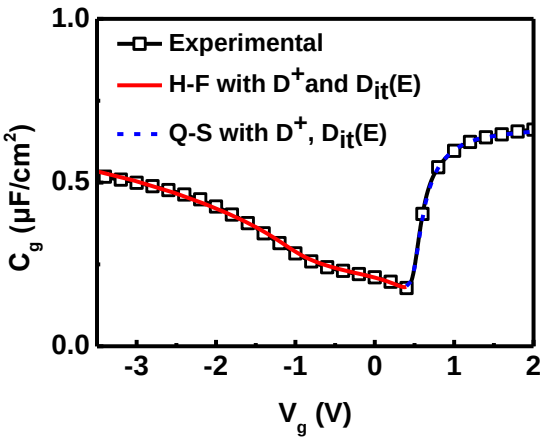

Figure 7 (a) Experimental and simulated high frequency C_g-V_g response for a Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOSFET structure (-50°C). An interface state distribution and fixed oxide charge is introduced into the simulated response. The depletion section of the characteristic (red curve) is modelled as a high frequency C_g-V_g response using Poisson only, where the interface states stretch out the curve along with gate voltage axis, but add no capacitance in the simulation. The inversion section of the characteristic (blue curve) is modelled as a self-consistent Poisson-Schrödinger solution, and is a low frequency solution, where the interfaces states within the $In_{0.53}Ga_{0.47}As$ conduction band both stretch out the C_g-V_g response and add a capacitance. This approach in inversion is based on the experimental results shown in Figures 6(a) and 6(b).

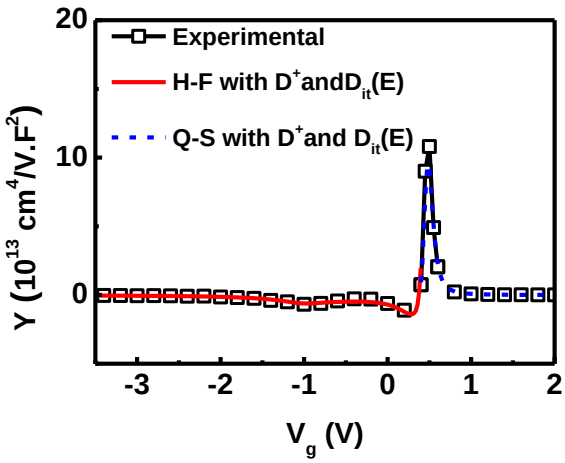

Figure 7 (b) Experimental and simulated Maserjian Y-functions for a Pd/Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ MOSFET structure (-50°C), corresponding to Figure 7(a). The use of the self-consistent Poisson-Schrödinger solution in inversion introduces a further V_T shift matching the peak values of the Maserjian Y-functions.

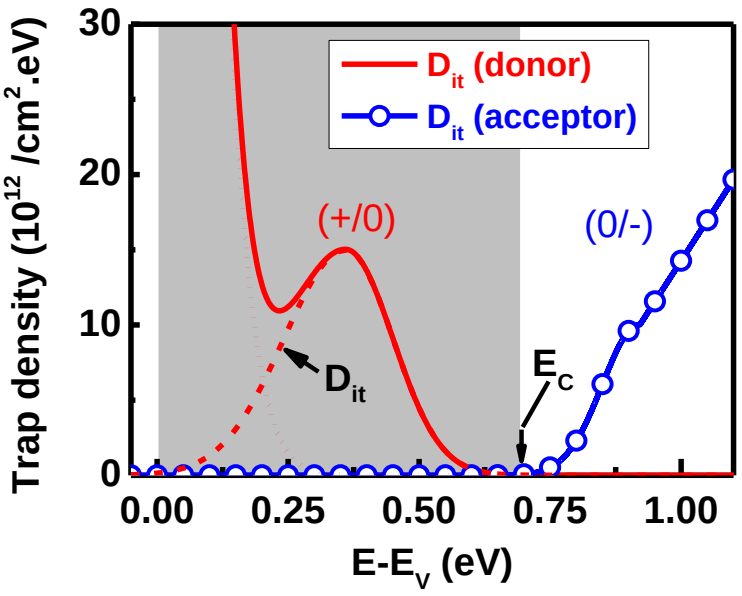

Figure 8. Interface state density versus energy profile ($D_{it}(E)$) at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface obtained from the modelling of the experimental C_g-V_g characteristic. The grey shaded area represents the $In_{0.53}Ga_{0.47}As$ energy gap. The defects located within the $In_{0.53}Ga_{0.47}As$ energy gap are donor type (+/0) and suggests the presence of two components, which are highlighted as two Gaussian distributions (red short dot lines). The interface state density is low near the conduction band edge (below $1x10^{12}cm^{-2}$), but increases into the $In_{0.53}Ga_{0.47}As$ conduction band edge. The interface states aligned with the $In_{0.53}Ga_{0.47}As$ conduction band edge are acceptor-type (0/-).