# Design of a Low Power, 14-Bit Continuous Time Delta Sigma Modulator for IoT Radio Receiver


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MCCI

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*Dedicated*

*To*

*My beloved Mother Collastique*

*Je t'aimerai toujours*

"In God, I believe him who gives meaning to all our thoughts.

# Abstract

Analog-to-Digital Converters are a fundamental building block of modern integrated RF radio transceivers. In the receiver signal chain, converting an analog baseband signal to the digital domain can consume a significant proportion of an integrated transceivers power budget. Coupled with this, the demand for flexible, low power, and robust ADCs to meet modern Internet of Things (IoT) wireless communication standards are ever increasing. Due to their oversampling nature, and inherent anti-aliasing filtering properties, Continuous Time Delta Sigma Modulator (CTDSM) ADCs are very well suited for low power IoT radio receiver architectures. However, CTDSM performance can suffer from clock jitter effects and inter-symbol interference (ISI) in the feedback DAC waveform which can significantly reduce SNR at the ADC output. The feedback DACs in CTDSM dictates the overall modulator's accuracy since any error introduced by this block appears directly at the output. In multibit CTDSMs the DAC mismatch greatly limits the modulator linearity. On the other hand, single bit CTDSMs are inherently linear and more area efficient compared to multibit counterpart, however they require higher order loop filters and oversampling ratio (OSR) to achieve similar performance. Also, variation in the rising and falling times of the DAC pulses in CTDSMs produce ISI. Previous works have shown that employing a Return-to-Zero (RTZ) feedback DAC pulse, the ISI issue can be mitigated at the expense of increasing clock jitter sensitivity. On the other hand, incorporating Finite Impulse Response (FIR) filter in the feedback DAC can reduce the clock jitter sensitivity.

This work will propose a $4^{th}$ order feedforward, single bit CTDSM with a return-to-zero (RTZ) feedback DAC that achieves state-of-the-art SNR in the presence of significant clock jitter by incorporating a FIR feedback DAC in the feedback path. The proposed single bit design combines the lower ISI sensitivity of the RTZ DAC with the lower jitter sensitivity of FIR DAC to produce a CTDSM suitable for IoT radio receiver and allows for an area efficient design that can meet the strict linearity and SNR requirements of a low power, high performance IoT based receiver architecture. The proposed CTDSM architecture was first modelled and simulated in MATLAB SIMULINK to demonstrate the feasibility of the adopted methodology of addressing DAC non-idealities in CTDSM. Time domain behavioral

simulation achieves a peak SNR of 89 dB without circuit thermal noise in presence of 4.2 ps rms jitter at 24 MHz sampling frequency over 250 kHz bandwidth. The circuit-level realization of the CTDSM in 65 nm CMOS process has a simulated power consumption of $1.407\,mW$ from a $1.2\,V$ supply. The Schreier figure of merit is $FoM_S = 169dB$. And the peak SNR of $84.8\,dB$ was achieved under the influence of circuit thermal noise.

# Declaration

I hereby declare that the dissertation entitled "**Design of a low power, 14-bit Continuous Time Delta Sigma Modulator for IoT radio receiver"** which is being submitted to the **School of Engineering, University College Cork**, in fulfilment of the requirement for the award of the **Degree of Master of Engineering Science**, is a bonafide thesis of the work carried out. The work described in this thesis contains no material which to a substantial extent has not been submitted to any University or Institution for the award of any degree, except where the due acknowledgment is made in the text.

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Ian Assom

August 2018

# Acknowledgment

Before any development of this dissertation writing, it seems appropriate to begin with thanks, those who support, help and encourage me throughout the completion of my research Master and contributed to make my time here at Microelectronic Circuit Centre Ireland (MCCI) a memorable and enjoyable experience.

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# Content

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# List of symbols and acronyms

| Notation | Description |
|---|---|
| $A_{dc}$ | Open Loop DC Gain |
| AAF | Anti-Aliasing Filter |
| AGC | Automatic Gain Control |
| ADC | Analog-to-Digital Converter |
| BBF | Base Band Filter |
| BW | Bandwidth |
| CIFB | Cascade Integrator Feedback |
| CIFF | Cascade Integrator Feedforward |
| CTDSM | Continuous Time Delta Sigma Modulator |
| DAC | Digital-to-Analog Converter |
| DEM | Dynamic Element Matching |
| DTDSM | Discrete-Time Delta Sigma Modulator |
| DR | Dynamic Range |
| ELD | Excess Loop Delay |
| ENOB | Effective Number of Bit |
| FDA | Fully Differential Amplifier |
| FIR | Finite Impulse Response |
| FoM | Figure of Merit |
| FS | Full Scale |
| IC | Integrated Circuit |
| IIT | Impulse-Invariant Transformation |
| ISI | Inter-Symbol Interference |

| | |
|---|---|
| GBW | Gain Bandwidth |
| GSM | Global System for Mobile communication |
| IBN | In-Band Noise |
| LSB | Least Significant Bit |
| MSA | Maximum Stable Amplitude |
| N-mos | N-type metal-oxide-semiconductor transistor |
| NRZ | Non-Return-to-Zero |
| OBG | Out-of-Band Gain |
| OSR | Oversampling Ratio |
| RF | Radio Frequency |
| RTZ | Return-to-Zero |
| RX | Receiver Signal of Interest |
| SNR | Signal to Noise Ratio |
| SNDR | Signal to Noise and Distortion Ratio |
| SJNR | Signal-to-Jitter Noise Ratio |
| STF | Signal Transfer Function |
| Op-amps | Operational Amplifier |
| P-mos | P-type metal-oxide-semiconductor transistor |
| PM | Phase Margin |
| PVT | Process Variation and Temperature |

# Chapter 1

# Introduction and Motivation

## 1.1 Introduction

The recent years have been marked by the rapid growth in applications such as wireless baseband receiver and smart sensors as well as battery-power consumer electronics. This has mainly been incited by the continuous downscaling of CMOS technology according to Moore's Law. While the cost of digital circuit has decreased thanks to Moore Law, the demand on analog circuit such as analog-to-digital converters (ADC) which provide the interface or liaison with these digital circuits is ever increasing. Indeed, in modern integrated circuit (IC) low power consumption and small cost/area are extremely critical, this makes the design of high-performance analog circuit more challenging.

Nowadays, there are billions of IoT sensors interconnect worldwide (e.g. in modern luxury cars where one can find various sensor nodes) and this trend is expected to double over the coming years. All these portable wireless sensors required a low power radio receiver to receive the information signal from the outside world. The ADC mandatory component in a receiver system, receives these signals whose bandwidth can be contaminated by large unwanted signals (blockers) from others adjacent transmitting channels. Therefore, the ADC should have high dynamic range and good linearity attributes to isolate and digitize the desired signal and achieve a cost-efficient design.

In fact, radio receivers are particularly susceptible to external blockers signals which can limit the overall receiver performances[1]. The traditional area intensive solution is to use significant front-end baseband filtering to attenuate

these interfering signals at the input of the ADC [2]. Put differently, the receiver can be considered as an intermediated step between the reception of the desired signal (at the antenna) and the extraction of information from this signal in the baseband. Therefore, to demodulate the information in presence of large interfering signals, the receiver should meet good linearity and dynamic range requirement. (. i.e. the range of signal levels over which it can operate). These requirements are often set by wireless communication protocol standards (explained in section in section 1.2) being used and the data rate in the receiver.

## 1.2 Background of IoT Radio Receiver

Many IoT applications require the RF transceiver to be able to support a combination of short-range communication standards within the same channel bandwidth while maintaining the same sensitivity and efficiency to optimize the usage of the radio spectrum. The receiver target by the current project can support the following range of packet-based IoT standard and technology:

### i. NB-IoT

The narrowband IoT (NB-IoT) is a low power wide area (LPWAN) radio technology standard that enables a wide range of devices to interconnect. NB-IoT operates in the cellular bands frequency at a data rate of $0.1 - 1\ Mb/s$ over several $km$ ranges. It also offers various benefits amount which; very power efficient, low cost, long battery life and high connection density and reliability

### ii. Bluetooth Low Energy (BTLE)

This is a proprietary open wireless standard for short range communication which was proposed to be low cost radio-based replacement for cable. It operates in the globally unlicensed $2.4\ GHz$ industrial, scientific and medical (ISM)-band. It has a data transmission rate of $1{,}2 - 1{,}3\ Mb/s$ over $10 - 100\ m$ range. BTLE has been

optimized to allow for a large amount of uncoordinated communication to take place in the same local area [9].

### i. ZigBee

ZigBee also known as IEEE802.15.4 is a short-range wireless standard operating at $2.4GHz$ (widely used frequency carrier) which is quite like Bluetooth. It's mainly targeted for industrial sensors, smart grids and low duty cycle operations. Compared to BTLE, it offers a lower data rate of about $up\ 250\ kbps$ and power consumption along with good flexibility and reliable communication [3]. The typical range is less than $100m$.

The communication system standards requirements for IoT radio applications are usually provided by the ETSI (European Telecommunication Standards Institute). These are summarized in Table 1.1.

Table 1-1:Summary of different range of packet based IoT technology

| WIRELESS TECHNOLOGIES AT A GLANCE | | | | | |
|---|---|---|---|---|---|
| **Technology** | **Frequency** | **Data rate** | **Range** | **Power** | **Cost** |
| 2G/3G | Cellular bands | 10 Mb/s | Several km | High | High |
| 802.15.4 | 2.4 GHz | 250 kb/s | 100 m | Low | Low |
| Bluetooth | 2.4 GHz | 1, 2.1, 3 Mb/s | 100 m | Low | Low |
| LoRa | < 1 GHz | <50 kb/s | 2-5 km | Low | Medium |
| LTE Cat 0/1 | Cellular bands | 1-10 Mb/s | Several km | Medium | High |
| NB-IoT | Cellular bands | 0.1-1 Mb/s | Several km | Medium | High |
| SIGFOX | <1 GHz | Very low | Several km | Low | Medium |
| Weightless | <1 GHz | 0.1-24 Mb/s | Several km | Low | Low |
| Wi-Fi (11f/h) | 2.4, 5, <1 GHz | 0.1-1 Mb/s | Several km | Medium | Low |
| WirelessHART | 2.4 GHz | 250 kb/s | 100 m | Medium | Medium |
| ZigBee | 2.4 GHz | 250 kb/s | 100 m | Low | Medium |
| Z-Wave | 908.42 MHz | 40 kb/s | 30 m | Low | Medium |

The system requirement of the radio receiver target by this project are summarized in Table 1.2. This is a high performance, low power, integrated radio transceiver supporting narrowband operation in $169.4\ MHz$ to $169.6\ MHz$ industrial, scientific and medical (ISM) band. A complete product data sheet can be found here:

http://www.analog.com/media/en/technical-documentation/data-sheets/ADF7030.pdf

Table 1-2: Target radio receiver system performance summary

| **Parameters** | **Values** |
|---|---|
| RF frequency range | $169.4\ MHz$ to $169.6\ MHz$ |
| Data rates | $2\ Gaussian\ frequecy\ key\ shifting\ (GFSK)\ Modulation$: $2.4\ kbps\ and\ 4.8\ kbps$ |
| Receiver (Rx) performance | $97\ dB\ blocking$[1] at $\mp 10\ MHz$ offset. |
| | $93\ dB\ blocking$ at $\mp 2\ MHz$ offset |
| | $66\ dB$ adjacent channel rejection |
| | $-122.8\ dBm$ sensitivity at bit error rate $(\mathrm{BER}) = 0.1\%$ |
| ▪ Accurate digital received signal strength indication (RSSI)<br>▪ Fast settling automatic frequency control (AFC) algorithm<br>▪ Autonomous automatic gain control (AGC) algorithm<br>▪ On-chip ARM Cortex-M0 processor for radio control, calibration and packet management | |

[1] Test the ADC rejection of undesired signals by applying a signal 97dB stronger than the desired signal at +/- 10MHz offset from the desired signal.

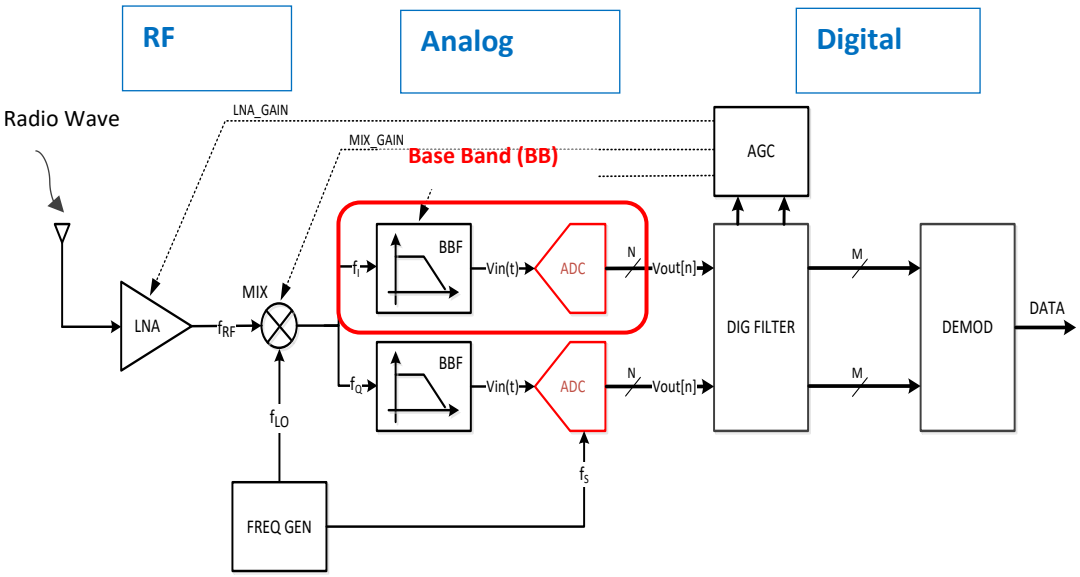



Figure 1-1: Overview of the radio receiver architecture in wireless communication

Figure 1.1 shows the architecture of a direct conversion radio receiver system that consists of an antenna, an analog signal pre-processing, an ADC and a digital processor part. The antenna receives the desired radio frequency signal (RX) and the surrounding –possible-strong –interferers. Then, a low noise amplifier (LNA), which is often designed to amplify the received signal without adding any extra noise nor distortion [4], along with automatic gain control (AGC) is used to boost the received signal. Moreover, the AGC loop controls the signal amplification so that the maximum aggregate input signal (. i.e. desired signal plus interfering signals) that will drive the ADC are within $6 - 10\,dB$ of its full-scale level to account for any sudden increase of the received signal level [5]. The output of the LNA is down-converted (. i.e. Frequency shifted) to baseband using a mixer. The mixer with a tunable local oscillator $f_{LO}$ translates the received signal from radio frequency (RF) into an intermediate frequency (IF). Subsequently, a second quadrature mixer is implemented to shift the IF baseband then split the signal into its in phase ($f_I$) and quadrature phase ($f_Q$) components for demodulation. The base band filter (BBF) is used to suppress unwanted interferer signals from neighboring channels and noise injected by the mixer. Then the I-Q signals are demodulated and digitized by the ADC into bit rate. The ADC has to be capable of providing

sufficient dynamic range (DR) more than $66\,dB$ as listed in Table 1.3 for the subsequent digital signal processing (DSP) stage along with good linearity to meet the performance metrics mandated by the wireless communication standard [6]

Since the ADC plays a crucial role in the receiver signal chain, its architecture topology is fundamental for the overall system performance. Indeed, an ADC that can isolate the wanted signal in a crowded RF environment will simplify the design of the radio receiver hence reduces the system cost and area.

CTSDM ADCs are the preferred ADC solution in many modern integrated radio receivers which often operate in multimode therefore more prone to interference signals from an adjacent channel. CTSDMs offers implicit anti-aliasing, coupled with the easy to drive resistive load making them a popular choice for low-cost receiver system [7]. Their feedback structure makes them independent of tight matching constraints resulting in high-performance ADCs that in general are lower power and have reduced area

## 1.3 CTDSM in Radio Receiver Environment

CTDSM ADC is the preferable solution for the IF digitization in radio receiver since beside from being capable of meeting the high DR ($> 66\,dB$) and linearity requirements set by various IoT standard, they also offer superior filtering of the large interfering signals from neighbouring channels. When a CTDSM with its built-in filter (its STF) is used as the ADC in the radio receiver architecture shown in Figure 1.1, the BBF can be eliminated resulting in a significant hardware saving and overall reduction of the receiver design cost.

As shown in [6], [1], [3], and [7] sigma delta modulators have proven their efficacy in various high performance wireless applications having to deal with strong blockers signals in noisy and crowded RF environment. In such a scenario, the dynamic range and linearity requirement of the ADC in receiver are no more defined by the in-band signal itself but also by the all these potential interfering signals which can sometimes be orders of magnitude larger than the signal of

interest. CTDSMs are therefore the compelling choice for implementing the ADC and sustain a full operation of the receiver.

This can be explained by the several advantages offered by this type of ADC topology. Indeed, the bestselling attributes and root causes of CTDSM popularity are:

- Their implicit anti-aliasing filtering inherited from the STF. In the CTDSM the sampling occurs after the loop filter ( see Figure 1.2), therefore the signal at the input of the quantizer is filtered and all the non-idealities inside the signal band are attenuated [5] by the continuous time loop filter. The loop filter STF thus acts as intrinsic low pass filter and should be designed to be flattened within the signal bandwidth to ensure that the nearest and far blockers do not fold-in with the bandwidth of interest as illustrated in Figure 2.6

- In the circuit realization, CTDSMs have a resistive input impedance, hence it is easy to drive and result in a simplified signal chain with reduced power dissipation [7].

Clearly, CTDSM ADC performance is a critical factor in radio receiver as it must convert the received in-band signal with high sensitivity while accommodating poorly-filtered adjacent blockers. Note that, often during the design phase the CTDSM is simulated standalone (as in this project) and not within the entire receiver module; hence, its own DR instead of the overall system is evaluated from which time to time may not fit the actual radio receiver specifications. Therefore as detailed explained in [7], it's recommended to design the modulator with a DR margin of about $10\ dB$ to guarantee its proper operation.

## 1.4 Motivation

The main objective of this work was to propose a high performance and low power ADC for IoT radio receiver. That could potentially reduce the level of signal integration at the receiver end resulting in a cost-efficient design. CTDSM ADCs

architecture is naturally well suited to meet the aforementioned performance requirements of IoT radio receiver because of their inherent anti-aliasing, attenuation of out-of-band blockers and excellent dynamic range which can significantly reduce the baseband filtering requirement in receiver signal chain as explained in section 1.3.

In this work, the focus has been placed on circuit innovation techniques to reduce the overall power, area, complexity and latency in the direct conversion of the receiver. The mains project research priorities are summarized in Table 1.3.

Table 1-3: ADC Target Specifications

| **Specification** | **Target** | **Comment** |
|---|---|---|
| Anti-aliasing | Aggressive | Design techniques to implement a robust & aggressive STF response to improve overall radio receiver figure of merit (. i.e. including BBF, Drivers & ADC in the Analysis) |
| Bandwidth | 250k – 500kHz | Flexible BW for IoT RX standards |
| ENOB \| SNDR | 14bits \| 86dB | High DR reduces RX complexity in BBF and AGC filter design |
| Power | < 0.1mW | Target FoM > 183dB highest reported |
| Area | < 100kμm$^2$ | Small area footprint achieved in CT-DSM designs |
| AVDD / DVDD | 1.2V / 1V | Target for 40nm/65nm ULP designs |

Thanks to continuous CMOS technology downscaling over the past years which has triggered the rapid improvement processing speed of the modern radio receiver module. This has paved the way for circuit innovation facilitating the development of new wireless IoT communication standards that provide higher data rates and ranges with improved energy-efficiency [8]. This has been enabled by the ability to infuse more on-chip integration of external components such as filters thus shifting the ADC toward the antenna side of the radio receiver which

has allowed the overall hardware and digital signal processing portioning of the receiver systems on the same chip. Moreover, using high performance, low power ADC such CTDSM in the radio receiver reduces the overall system size and cost which one of the practical motivations behind this project.

In the presented work, the total power consumption of the design was optimized at 3 levels in the top-down design approach adopted:

- Modulator architecture choice
- System modelling of the functional block
- Circuit level realization

## 1.5 Thesis Organisation

This thesis is divided into the following chapters:

**Chapter2:** An overview of analog to digital conversion in continuous time delta sigma modulator, the architectural choices and keys performance metrics of sigma delta modulator are also examined

**Chapter3** This chapter describes the system level modelling and simulation of the proposed 4th order single bit, feedforward CTDSM with RTZ DAC. The system level non-idealities excess loop delay (ELD), inter-symbol interference (ISI) and clock jitter which limit the performances of a single bit CTDSM are examined. Then an approach of reducing the clock jitter sensitivity on the proposed $4^{th}$ order CTDSM architecture using FIR DAC is presented. Lastly, the modulator behavioural modelling simulation results along with the effect of the non-idealities on the keys performances metrics are provided

**Chapter4** describes the complete circuit level realization of the proposed low power single bit CTDSM architecture. It also detailed the design consideration of the different modulator building blocks: op-amps, comparator, and return to common-mode DAC and FIR filter.

**Chapter5** presents the simulation results of the proposed $4^{th}$ order CTDSM that was implemented in TSMC's 65nm analog CMOS technology.

**Chapter6** concludes with an overall summary of the work carried out in the project, the sustainability of the results archived results, limitation and future work

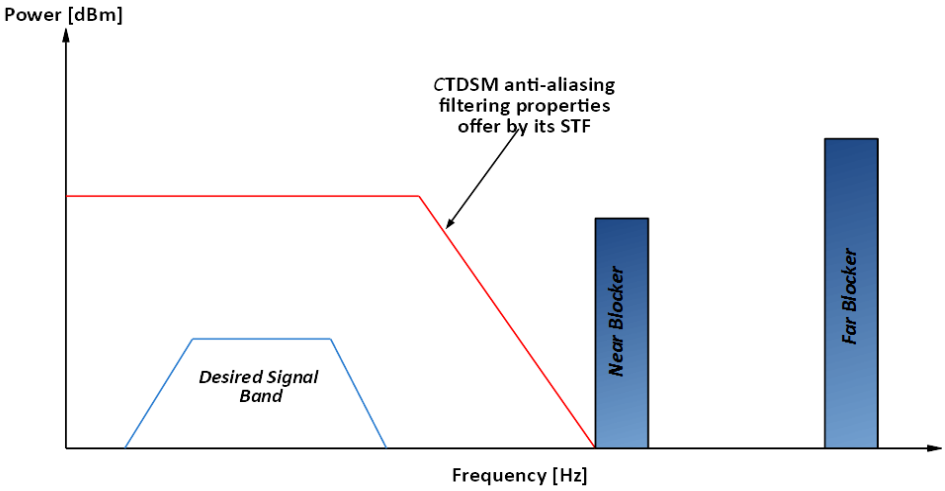



Figure 1-2: CTDSM implicit anti-aliasing filtering properties with in band flat STF to attenuate adjacent interferers

# Chapter 2

## Continuous Time Delta Sigma ADCs in IoT Radio Receiver

This chapter is intended to give an overview of analog to digital conversion in continuous time delta sigma modulator in section 2.1. Next the architectural choices and key performance metrics of sigma delta modulator are examined in section 2.2. Herein most of the term and definitions used in the rest of this thesis will be explained.

## 2.1 Overview of Continuous Time Sigma Delta Modulator

CTDSMs are oversampled data converters that offer several unique features to reduce the complexity in the design of ADC for IoT radio receiver that simultaneously requires medium conversion bandwidths, good linearity and higher dynamic range. An overview of some of the main characteristics such as, quantization, oversampling and noise shaping that make CTDSMs very attractive and popular ADCs architecture will be presented. More detailed analysis can be found in various literature [10] [1].

### 2.1.1 Sampling and Quantization in CTDSM

- **Sampling:**

Converting an analog signal to the digital domain requires two basic operations: sampling in time and quantization in amplitude.

The analog input signal $X(t)$ depicted in Figure 2.1 (a) is continuous in both time and amplitude. Sampling is mechanism in which the signal $X(t)$ is convert into

discrete time signal $X(nT_s)$, where n is an integer and $T_s$ is the sampling period. When translate in the frequency domain, this process introduces copies of the original spectrum $X(f)$ around integer multiple of the sampling frequency $f_s$ [10] as illustrate in Figure 2.1 (d) According to the Nyquist theorem, to prevent information loss it is necessary to use sampling frequency which is at least twice the bandwidth ($f_{Nyquist}$) of $X(f)$ in order to avoid aliasing [1], i.e the distortion of $X(f)$ due to the replica $X'(f)$ as shown in Figure 2.1 (e).

$$f_s = 2.f_{Nyquist} \tag{2.1}$$

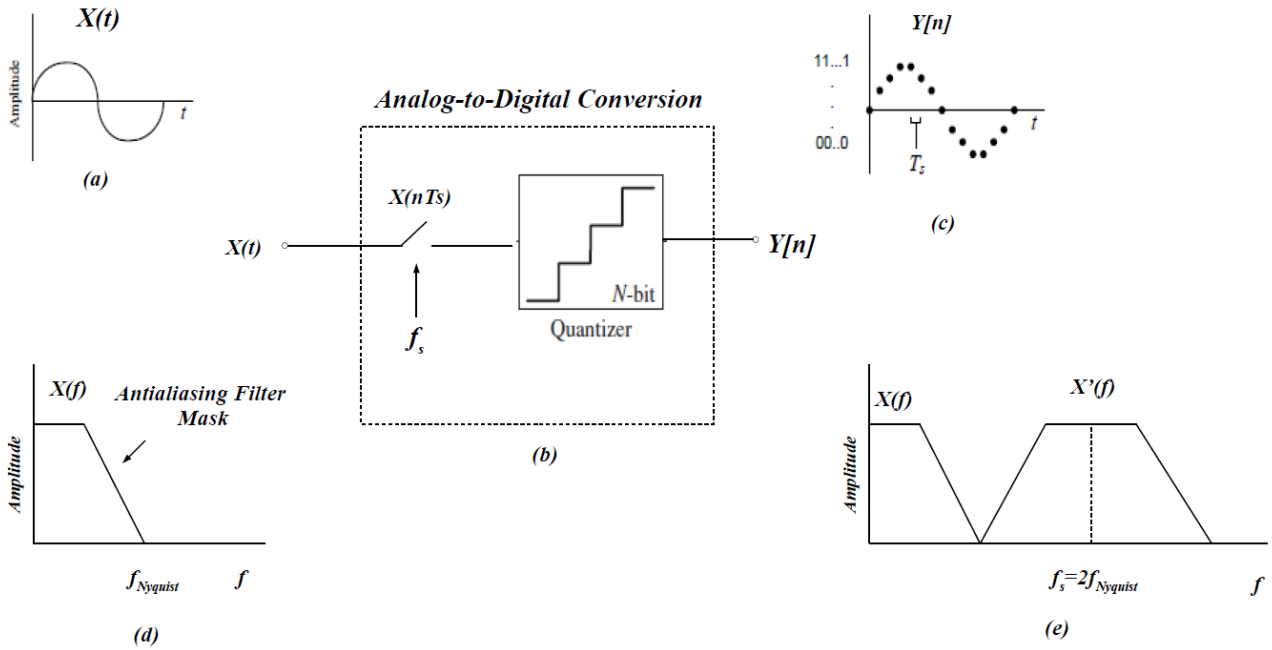



Figure 2-1: Analog-to-Digital Conversion Operation

In this way the signal $X(f)$ must be band limited, which is achieved by an antialiasing filter mask also illustrated in Figure 2.1 (d). ADCs which operated with a sampling frequency defined by equation 2.1 are usually referred to as Nyquist ADCs.

ADCs using a sampling frequency larger than the established by the Nyquist theorem are called oversampled ADCs and CTDSM belong to this category. In such ADCs the signal is sampled with a sampling frequency higher than that suggested by Nyquist theorem. Thus, the rate at which the signal is sampled by the converter is defined by the Oversampling Ration (OSR) given by:

$$OSR = f_s/2.f_{Nyquist} \tag{2.2}$$

One advantage of using oversampling is that it relaxes the anti-aliasing filter specifications [1] as it can be appreciated in Figure 2.2.

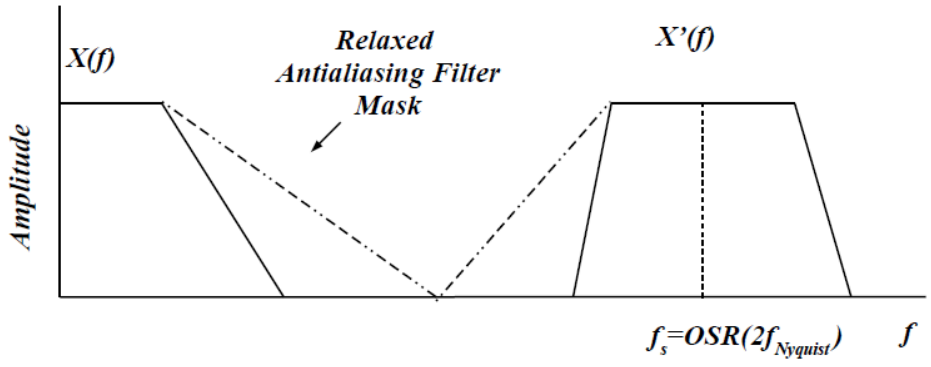



Figure 2-2: Oversampling and Relaxed Antialiasing Filter

- **Quantization**

Despite being discrete in time, the signal $X(nT_s)$ is still continuous in amplitude. Quantization is the process in which the sampled signal $X(nT_s)$ is discretized in amplitude and converted into $Y[n]$. In this process, the continuous amplitude $X(nT_s)$ are encoded into limited set of output amplitude levels defined by the number of bits, *N* in the quantizer. The number of quantization levels is equal to $2^N$. Thus, even the ideal quantization process inherently introduces errors to the signal commonly referred to as quantization error $q_e$, which is the amplitude difference between $Y[n]$ and $X(nT_s)$:

$$q_e = Y[n] - X(nT_s) \tag{2.3}$$

As described in [1] the quantization error has a rectangular probability density function. Thus, the power spectral density (PSD) of quantization error is constant over the entire sampling range frequency [1], [10]:

$$PSD = \frac{\Delta^2}{12 f_s} \tag{2.4}$$

Where Δ is the minimum quantization step defined by $2^N$. The quantization process is commonly modelled as an additive noise source as shown in Figure 2.3 often called quantization noise.

For the circuit designer, the advantage from modelling quantization error as an additive white noise is the Signal-to-Noise Ratio *(SNR)* i.e. ratio between the signal power and the quantization noise power [1], [3]. If one assumes that the input signal is a sinewave tone, the maximum *SNR* for Nyquist *N-bits* type ADC is given by [1]:

$$SNR_{Nyquist\ ADC} = 1.76 + 6.02N(dB) \tag{2.5}$$

From equation (2.2) and (2.4), the PSD of oversampled ADCs can be derived as:

$$PSD = \frac{\Delta^2}{12\ OSR\ 2f_{Nyquist}} \tag{2.6}$$

It's apparent from (2.6) that another advantage of oversampling is that that the quantization noise is spread in wider frequency band. Therefore, the quantization noise power is lowered in the signal band of interest, and the *SNR* is increased as shown in Figure 2.4.

Similarly, the *SNR* oversampled ADC such CTDSM is given by [1]:

$$SNR_{Oversampled\ ADC} = 1.76 + 6.02N(dB) + 3\,log_2(OSR) \qquad (2.7)$$

Clearly from (2.7) every time one's double the *OSR* the *SNR* is increased by $3dB$

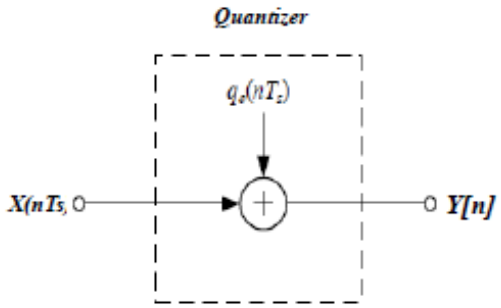



Figure 2-3: Quantizer Linear Model

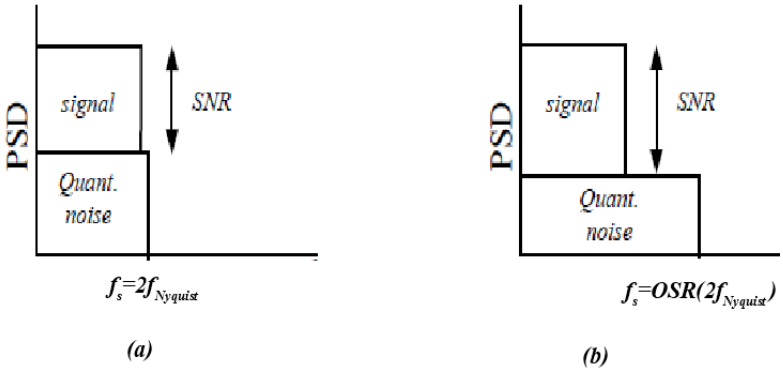



Figure 2-4: Quantization noise power in (a) a Nyquist ADC and (b) an oversampled ADC.

Assuming that the quantization noise from the *N-bits* ADC is an additive white noise, the power spectral density is spread uniformly in the Nyquist range [10] as shown in Figure 2.5 below. It is obvious that an increased OSR will reduce this in-band-noise *(IBN)* since the signal band occupies a smaller portion of the Nyquist interval. As derived in equation (2.7) every doubling in OSR will improves the signal to quantization-noise -ratio *(SQNR)* by $3dB$.

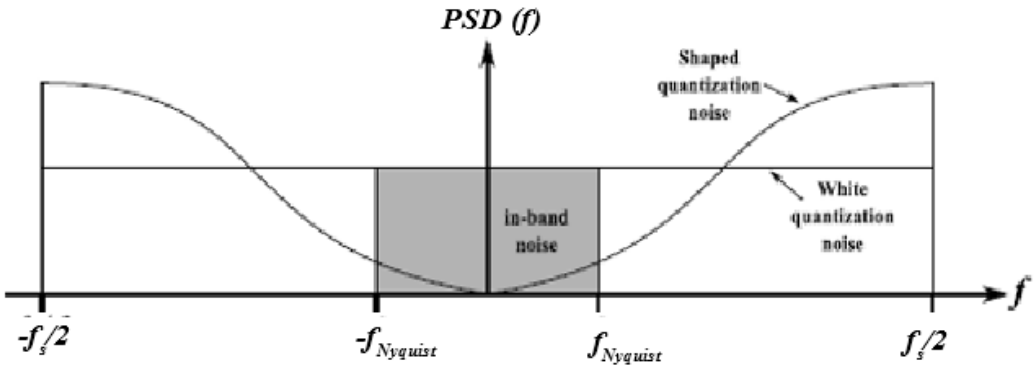



Figure 2-5: Quantization noise spectra with oversampling and noise shaping.

- **Noise Shaping**

Oversampling in ADC become more compelling if the *IBN* is further reduced by noise shaping. The noise shaped spectral also shown in Figure 2.5 where the quantization noise is shaped by an appropriate high-pass filter action. For example, if a first order high pass filter is used, every doubling of the OSR results in a *SQNR* improved of by $9dB$ [1] Consequently, the combination of oversampling and noise shaping inherently present in CTDSM topology offer the ability to reduce the IBN and push more noise toward higher frequencies (. i.e. out of the band of interest)

### 2.1.2 Signal Processing and Anti Alias Filtering in CTDSM

- **Signal Processing**

The principle of operation of a CTDSM can be explained as follows: if one considers the block diagram of the single loop CTDSM along with its corresponding linearized equivalent depicted in Figure 2.6, the loop filter output $H(s)$is sampled and quantized by the quantizer (. i.e. comparator) which injects quantization error $q_e[n]$ on the digital output. The output bitstream $Y[n]$ is then subtracted from the analog input $X(t)$ through the DAC pulse in the feedback path. The suppression or cancellation of this quantization noise is achieved by the oversampling of the signal bandwidth and noise shaping carried out by the loop filter. In other words,

the input $X(t)$ is low pass filtered by the modulator signal transfer function $(STF)$ and the quantization noise error $q_e(t)$ is high pass filtered by the modulators noise transfer function $(NTF)$.

This is summarized mathematically as follow; let consider the linearized model of the CTDSM shown in Figure 2.6 and if we assume that the N-bits quantizer can be model as an additive white noise (Figure 2.3).and that the feedback DAC can be modelled as unity gain stage, hence the transfer function of the CTDSM is expressed as:

$$\begin{aligned} Y(s) &= X(s)\frac{H(s)}{1+H(s)} + E_Q(s)\frac{1}{1+H(s)} \\ &= X(s)NTF(s) + E_Q(s)STF(s) \end{aligned} \tag{2.8}$$

$$\begin{aligned} STF &= Signal\ Transfer\ Fuction = H(s)/(1+H(s)) \\ NTF &= Noise\ Transfer\ Fucntion = \frac{1}{1+H(s)} \end{aligned} \tag{2.9}$$

Where *X* represent the input signal, $E_Q$ is the quantization noise and $H(s)$ the loop filter transfer function. It's clearly apparent from equation 2.8 the input signal and the quantization noise are subject to different transfer functions, which correspond to the signal transfer function *(STF)* and the noise transfer function *(NTF)* respectively.

To develop a basic understanding of the modulator behaviour, let's assume the loop filter to be a simple integrator i.e. $H(s) = 1/s$. Hence, the NTF and STF from equation (2.9) can be expressed as [1]:

$$\begin{aligned} NTF(jw) &= 1 - e^{-jwf_s} \\ STF(jw) &= \frac{1 - e^{-jwf_s}}{jw} \end{aligned} \tag{2.10}$$

Where $f_s$ is the modulator sample rate. It's apparents that we have $H(s) \to \infty$ at dc (i.e at $w = 0$), which means input signal near dc should be replicated faithfully in in the output bitstream $Y[n]$. Moreover, $|STF(jw)| = 1$ so one's should at

least expect the magnitude of an input at any frequency to be reproduced at the output. Likewise, $NTF(jw) \rightarrow 0$ at dc, and it increasase away from from dc; hence we say the quantization noise is ”shaped away from dc”.

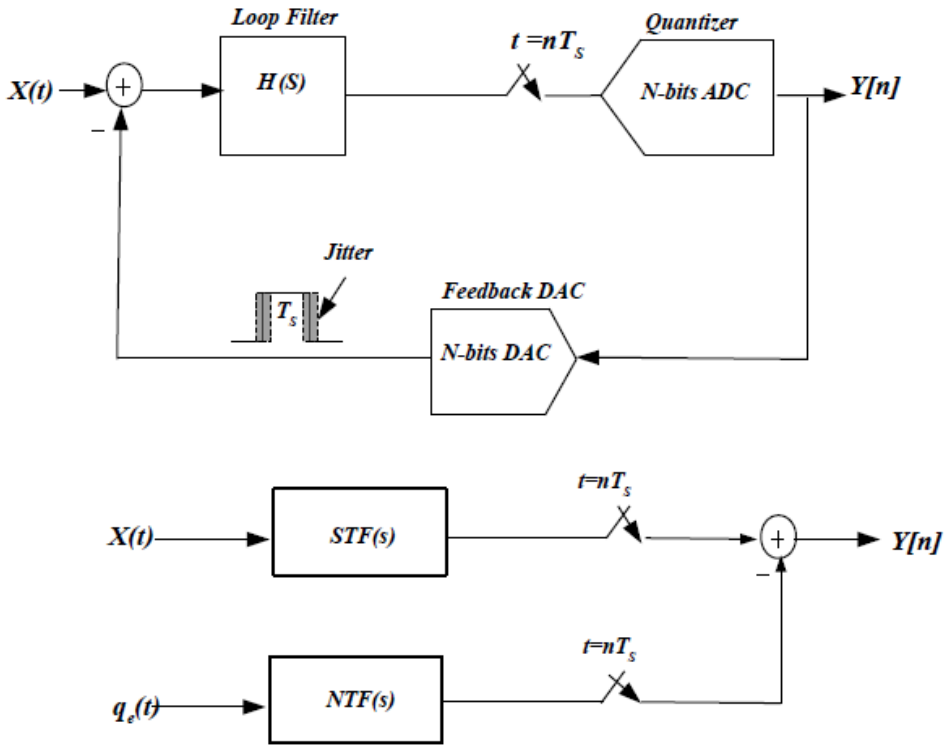



Figure 2-6: CTDSM data conversion overview and equivalent CTDSM linearized model

- **Anti-Alias Filtering**

One of the most important adavantage of a CTDSM is its inherent anti-alias filtering (AAF). As shwon in Figure 2.6, in CTDSM the sampling operation takes palce at the ouput of the loop filter and so any signals which my alias would be low-pass filtered by the loop filter. In other words, the AAF eliminates spectral components of the signal above half the sampling rate from the input siganl, in such way that the modulator input signal stay in-band and the subsequent sample operation does not alias input signals from higher frequency into the band of interest[3].

Figure 2.7, shows a plots of the magnitude response of the loop filter $L(jw)$, $NTF(jw)$ and $STF(jw)$ of the first order CTDSM (.i.e with $H(s) = 1/s$) discussed above. The STF's dc gain is unity and it has nulls at all nonzeros integral multiples of the sampling rate. This suggest that all the tones that could potentially be folded back to dc after sampling are inherently eliminated

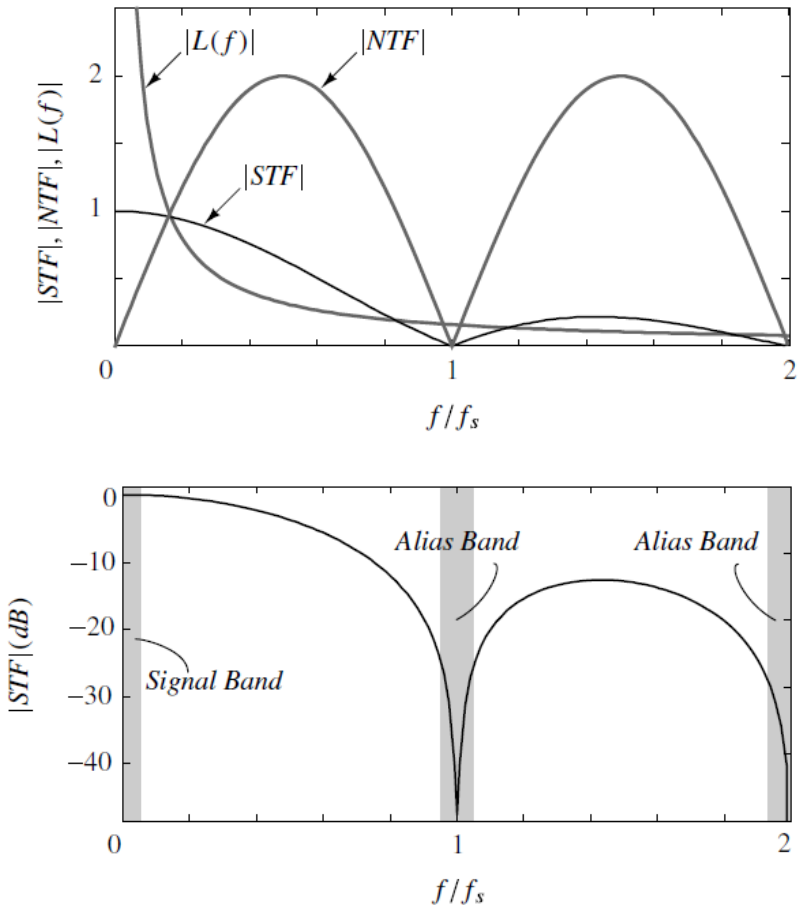



Figure 2-7:CTDSM Magnitude response of the loop filter, NTF and STF

### 2.1.3 Performance Metrics of CTDSM

Delta sigma modulator ADC keys characteristics are usually obtained from the frequency domain representation of the modulator output bitstream. In other words, dynamic performance metrics are directly measured from the modulator output power spectrum representation.

- **Linearity**

This is a crucial parameter in IoT receiver ADC. Because non-linearity in the circuit implementation will introduce distortion components within the system such as offset, strongest distortion component, intermodulation (IM3) etc. Ideally, to sustain the modulator functionality, these distortion components should be weaker than the minimum detectable input signal power.

- **Dynamic range (DR)**

Probably the most important parameter of any data converter. This is the ratio of the biggest input signal that can be converted by the ADC to the smallest Note that the maximum input power is often limited by non-linearity while the minimum input power is limited by noise. Moreover, it's a good practice to design the modulator considering the DR range requirement of the overall receiver system

The conversion efficient oversampled ADCs is often specified in term of Schreier FoM given by:

$$FoM_S = DR\ (dB) + 10log_{10}\left(\frac{BW}{P}\right) \tag{2.11}$$

Wehere $P$ denotes the power needs by the ADC; $BW$ is the signal bandwidth and $DR$ is the ADC dynamic range.

- **Signal to Noise Ratio (SNR)**

As discussed in section 2.1.1, this the ratio between the input signal power and the sum of noise power within designed bandwidth. This is a key and widely used metric to evaluate the performance of CTDSM.

- **Effective Number of Bits (ENOB)**

This is the actual resolution of the modulator. It's usually given by $ENOB = (SNDR - 1.76)/6.02$. Where *SNDR* is the signal to noise ratio plus any distortion inject in the modulator.

- **Spurious-Free Dynamic Range (SFDR)**

This is the difference between the power of the wanted signal and the power of the highest or strongest distortion component within the signal bandwidth.

### 2.1.4 CTDSM Architectural Consideration

When defining a CTDSM architecture, various design trade-offs must be made to optimize the modulator performance for a specific application. This begins with the modulator architectures choice.

#### i. Single bit vs Multibit Quantizer

The number of bits of the quantizer will significantly impact the total area and power consumption of the entire modulator. Both single bit and multibit design offer some advantages and disadvantages so what type quantizer one should use is really application-specific.

| **Single bit quantizer** | **Multi-bits quantizer** |
|---|---|
| Inherently linear feedback DAC → Two-level (simple comparator) | More prone to circuit imperfections |
| Single feedback DAC required → less area, less layout parasitic, and power saving | Requires Multibit feedback DAC → Each DAC introduce mismatch due to PVT hence overall linearity is limited |
| Relaxes integrator design constraint in the loop filter→No DEM required | Required extra circuitry (DEM) and calibration →Increases complexity and stability of the modulator |

| | |
|---|---|
| Reduced ELD in the feedback path → high sampling rate & SQNR can be obtained [5] | Introduce extra ELD from the DACs, DEM logic, and calibration circuitry |
| Higher OSR which will require more amplifier bandwidths. Also, they require higher order loop filters that are difficult to stabilize. | Lower OSR and modulator order compared to a single bit CTDSM |
| The maximum allowed band gain (OBG) equal to 1.5dB above this the modulator becomes unstable | Can tolerate OBG up to 2.5dB |

From the above, for a power and area point of view, the single bit quantizer seems to be best suited for the project. However, single bit CTDSM required higher OSR and higher order loop filter which can result in stability and ELD issues if not properly addressed in the circuit design

### ii. Cascade Integrator with Feedforward vs Feedback Distribution

The two widely used architecture in CTDSM is feedforward and feedback loop filter topologies. Figure 2.2 is an illustration of the feedback and feedforward the loop filter structure of a 4th order CTDSM. Each loop filter structure offers some advantages and disadvantages summarized below.

| **Cascade Integrator Feedforward (CIFF)** | **Cascade Integrator Feedback (CIFB)** |
|---|---|
| Requires a single DAC in the feedback path. However, it requires a multi-input summing amplifier | Multiples DAC to feedback each integrator stage output → Area hungry but not summing amplifier required. |
| Contrary to the CIFB structure, feedforward loop as seen in Figure 2.2 | High integrator swing required. Because the output of each integrator |

| | |
|---|---|
| apart from the first integrator, the integrator outputs do not contain a significant part of the input signal. Put differently, the loop filter only processes the error signal and as a result, the integrator's output will content an attenuated replica of the input signal. Thus, the design requirement of the 2nd and subsequent integrating stages are much relaxed. | contains, besides filtered quantization noise, a substantial part of the input signal. This can be explained as follow: since the integrator input signals are controlled to be zero over time, the summed single bit DAC signal and the integrator output are the same over time. Because in CTDSM the feedback signal continuously tracks the input signal, the output of the integrators must carry a significant portion of the input signal. Therefore the integrators need to have a high output swing to avoid signal clipping and overload[11]. |
| High effective open loop gain of the loop filter due to the smaller output swing of the first integrator. | Low open loop gain in the loop filter [12]. |
| Power efficient and self-recover from overloaded Input [11]. | Power-hungry. |
| Suffers from out-of-band peaking which can potential leads to instability and compromises the ADC dynamic range in the presence of large out-of-band interferers. | Immune to gain peaking and the STF doesn’t present any issue in the overall design. |

From the above, clearly, there is a design trade-off consideration regarding which type of loop filter topology architecture to use knowing that this is the most critical block of any CTDSM. In this work, we have opted for the feedforward topology to meet the low area and power target of this project. Therefore, we will only present the system level design of the feedforward loop filter architecture.

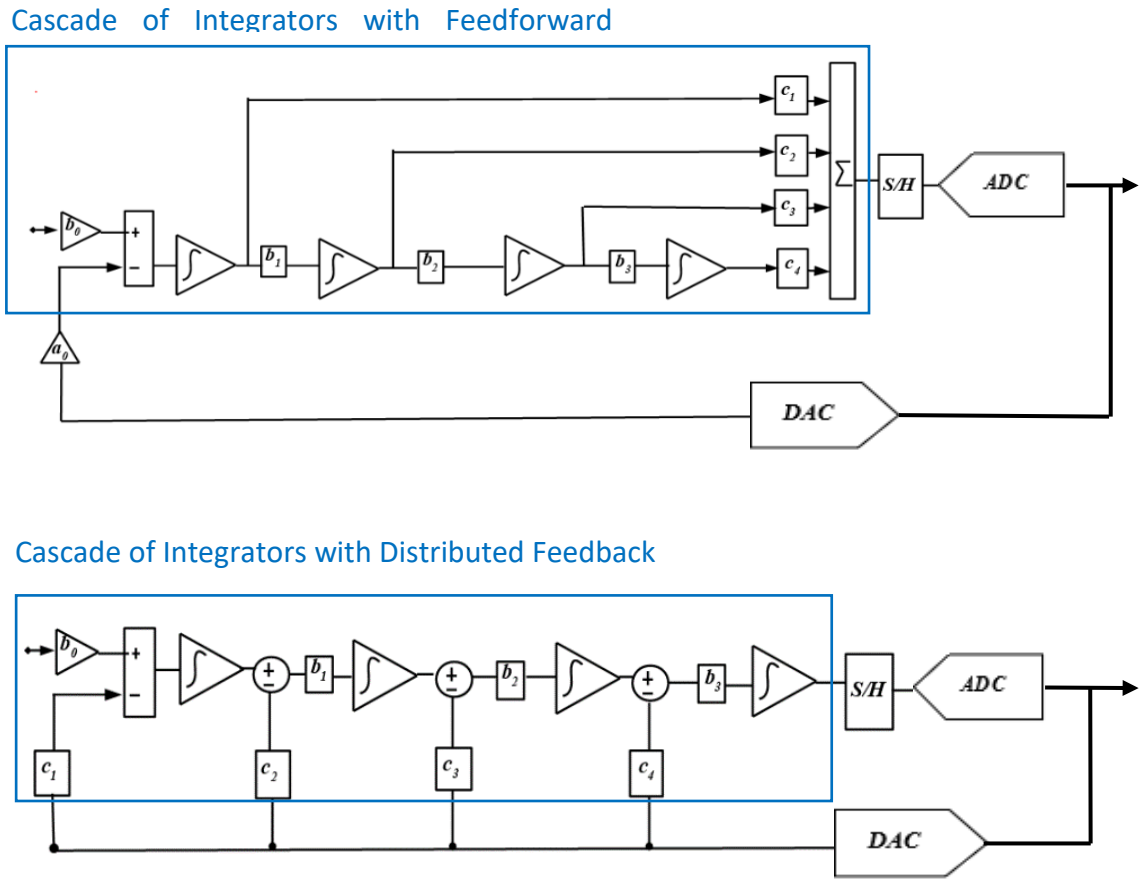



Figure 2-8: 4th order CTDSM with (a) Cascade of Integrators Feedforward (CIFF) and (b) Cascade of Integrators Feedback

Figure 2.7 shows the CTDSM with a feedforward loop filter structure. This is a fourth-order loop filter. A details description of the CTDSM loop filter transfer function and its mathematical derivation can be found in [1].

The general form of $n^{th}$ order integrator path is given by:

$$L_n(s) = \left(\frac{W_u}{s}\right)^n \tag{2.12}$$

where $w_{\square}$ is the unity gain frequency of the integrator. The transfer function of the loop filter is

$$L_0(s) = L_1(s) = \frac{w_{u4}C_4}{s^4} + \frac{w_{u3}C_3}{s^3} + \frac{w_{u2}C_2}{s^2} + \frac{w_{u1}C_1}{s^1} \tag{2.13}$$

And the signal transfer function is given by:

$$\begin{aligned} STF\ (s) &= \frac{L_0(s)}{1 + L_1(s)} = \frac{L_1(s)}{1 + L_1(s)} \\ and\ letting\ w_{ui}C_i &= k_i \\ STF\ (s) &= \frac{k_4 + k_3 s + k_2 s^2 + k_1 s^3}{k_4 + k_3 s + k_2 s^2 + k_1 s^3 + s^4} \end{aligned} \tag{2.14}$$

Equations (2.6) and (2.7) indicate that the *STF* can roll-off only as $1/f$ at high frequencies. This is the price to be paid/limitation when adopting the cascade integrators with a feedforward structure. Both feedback and feedforward structure can provide the same noise transfer function the main differentiation is observed on the signal transfer function. Considering the $STF$ described by (2.7), it is straightforward to see that it has four poles and three zeros. Therefore, the feedforward STF acts as a first-order lowpass anti-aliasing filter while an equivalent feedback (CIFB) structure will behave as a fourth-order lowpass filter thus providing much stronger anti-aliasing filtering at high-frequencies. However, CIFB structure is not power efficient, as the gain of the first integrator is small in the signal band. Thus, the noise and distortion from succeeding integrating stages can be significant when referred to the input. Using a CIFF structure avoid this problem, since the gain of the first integrator is large in the signal band. However, the STF of CIFF structure tends to peak outside the signal band of interest. This is shown in Figure 2.10 where the CIFF STF (blue curve) elicits a peaking around $350\ kHz$ which implies that at this frequency the maximum stable input amplitude is reduced by the out-of-band gain which about $\approx$ $7.6\ dB$

However, this out-of-band gain peaking can be reduced or attenuated by incorporating a direct feedforward path from input to the summing node. This is covered in the circuit realization chapter 4. Also, it should be pointed out that by combining feedforward structure with local feedback $d_1$ and $d_2$around the two-

loop integrators (Figure 2.9) enables us to move the NTF zeros away from dc and spread them over the signal band NTF (Figure 2.10). Consequently, the in-band noise (IBN) and DR are improved a detailed analysis regarding the performance gain from the addition of local feedback is provided in [6]. This design trade-off between CIFF and CIFB topology was taken into account in this work to combine the advantage of both structures.

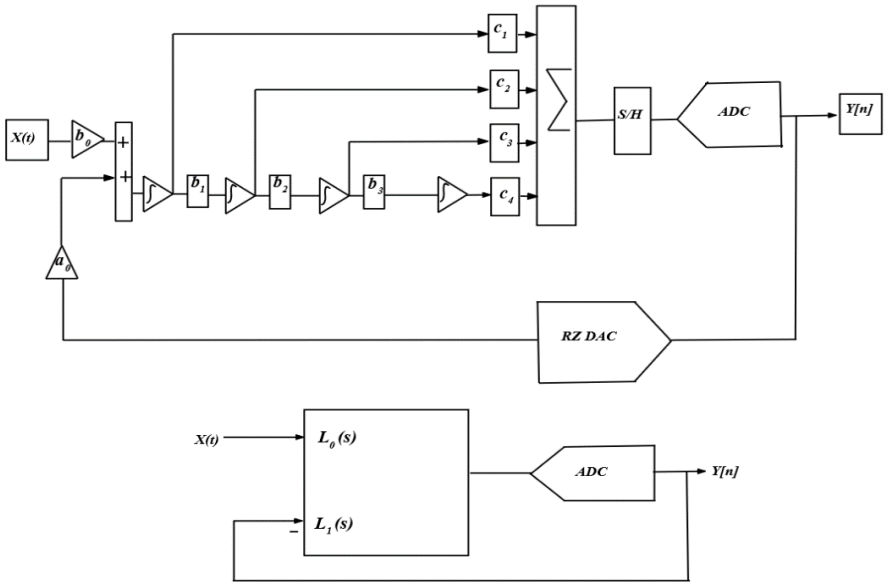



Figure 2-9: 4th order CTDSM with feed-forward loop filter structure and the modulator block diagram representation

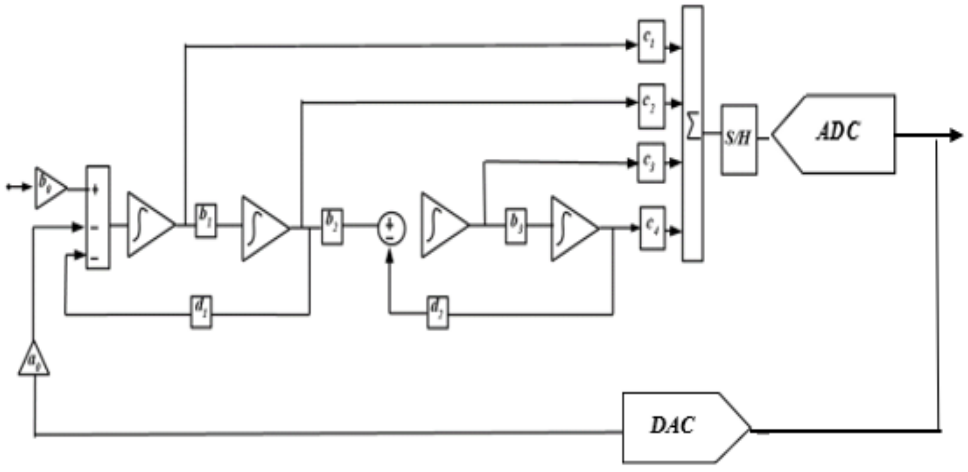



Figure 2-10: 4th order CTDSM feedforward loop filter with local feedback paths

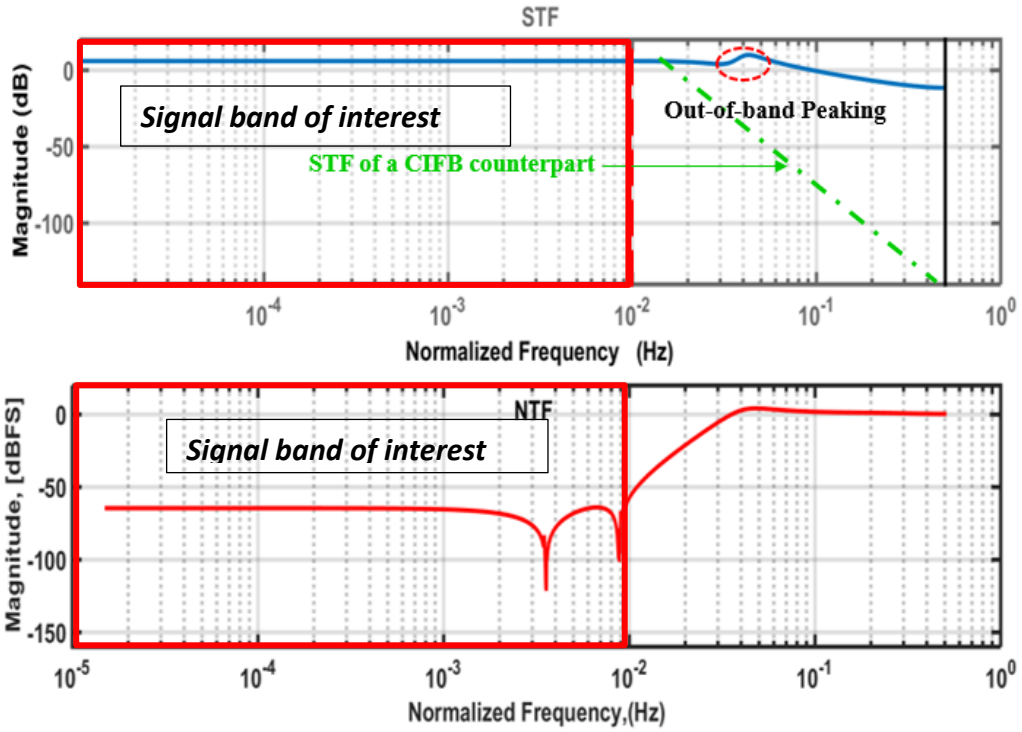



Figure 2-11: Simulated 4th order CTDSM feedforward loop filter structure STF and NTF.

## Summary

This chapter provides an overview of IoT radio application wireless communication standard with an emphasis on NB-IoT, BTLE and LoRa technology since they are the protocol currently supported by the receiver module target in this project. Some of the key performance specifications for CTDSM ADC in the receiver system have been distinguished along with their superior advantages. It was shown that ADC's DR and linearity requirement within the receiver is not only defined by the in-band signal of interest level but by the adjacent interferer signals which can be much stronger in signal power.

# Chapter 3

## Prototype Continuous Time Delta Sigma Modulator Implementation

This chapter describes the system level modelling and simulation of the proposed 4$^{th}$ order single bit, feedforward CTDSM with RTZ DAC that can achieve the 14-bits ENOB and high linearity design target for IoT radio receiver (shown in Figure 1.1). In section 3.1, an overview of the system level architecture modelling will be presented. Section 3.2 will discuss the main feedback DAC non-idealities: excess loop delay (ELD), inter-symbol interference (ISI) and clock jitter. Then section 3.3 will illustrate how clock jitter was modelled and simulated in the proposed modulator architecture. Section 3.4 presents a method of reducing the clock jitter sensitivity on the proposed 4$^{th}$ order CTDSM architecture. The last section provides the modulator behavioural modelling simulation results along with the effect of the non-idealities on the keys performances metrics

### 3.1 Architecture Modelling

As already mentioned, the target application of this project is IoT radio receivers, where both high DR and excellent linearity are required to allow the detection of small desired signals in presence of large blockers [13]. For this reason, a single bit CTDSM with RTZ feedback DAC architecture has been adopted, in order to mitigate ISI issue described in section 3.2.2 which if not addressed can deteriorate the modulator linearity. The targeted existing radio receiver module uses a $24\ MHz$ clock as low-cost crystal oscillators are available at 24MHz. This means that for a signal bandwidth of $250\ kHz$, the OSR is restricted to a value of *48*. Thus, to achieve an $86\ dB$ ADC SNR along with meeting linearity requirement of low

power IoT receiver, a 4$^{th}$ order, single bit, CIFF loop filter with RTZ DAC CTDSM is adopted, this is depicted in Figure 3.1.

One of the design challenges in sigma delta modulator is to identify an architecture that will best meets the intended application requirements. Since there are a plethora of different possible sigma delta design choices. From the target DR and signal bandwidth of interest as well with the sampling frequency, one's can rapidly visualize and assets the performance of different sigma delta modulators using the *Sigma –Delta online tool* available at *(http://www.sigma-delta.de/).* This is an interactive web-based design tool for CTDSM developed by [15]. It allows the direct acquisition of the modulator design coefficients that will meet the user's intended design goal without any need for the DT to CT transformation as largely reported in the literature. Once satisfactory modulator design coefficient was obtained the proposed CTDSM shown in Figure 3.1 was implemented in MATLAB® Simulink® environment where extensive behavioural simulation was performed, the objective is to investigate the effect of common non-idealities and fully characterize the proposed CTDSM.

Figure 3.1 also shows the loop filter coefficient used to implement and stabilized the 4 order CTDSM. Note that the local feedback loop coefficient a relatively small due to the higher-order nature of the modulator. This implies that the resistors value use to implement these resonators at the circuit level will be sensitive to process and temperature variation and will require optimization to maintain the stability of the modulator. Further details on how this is achieved can be found in [1].

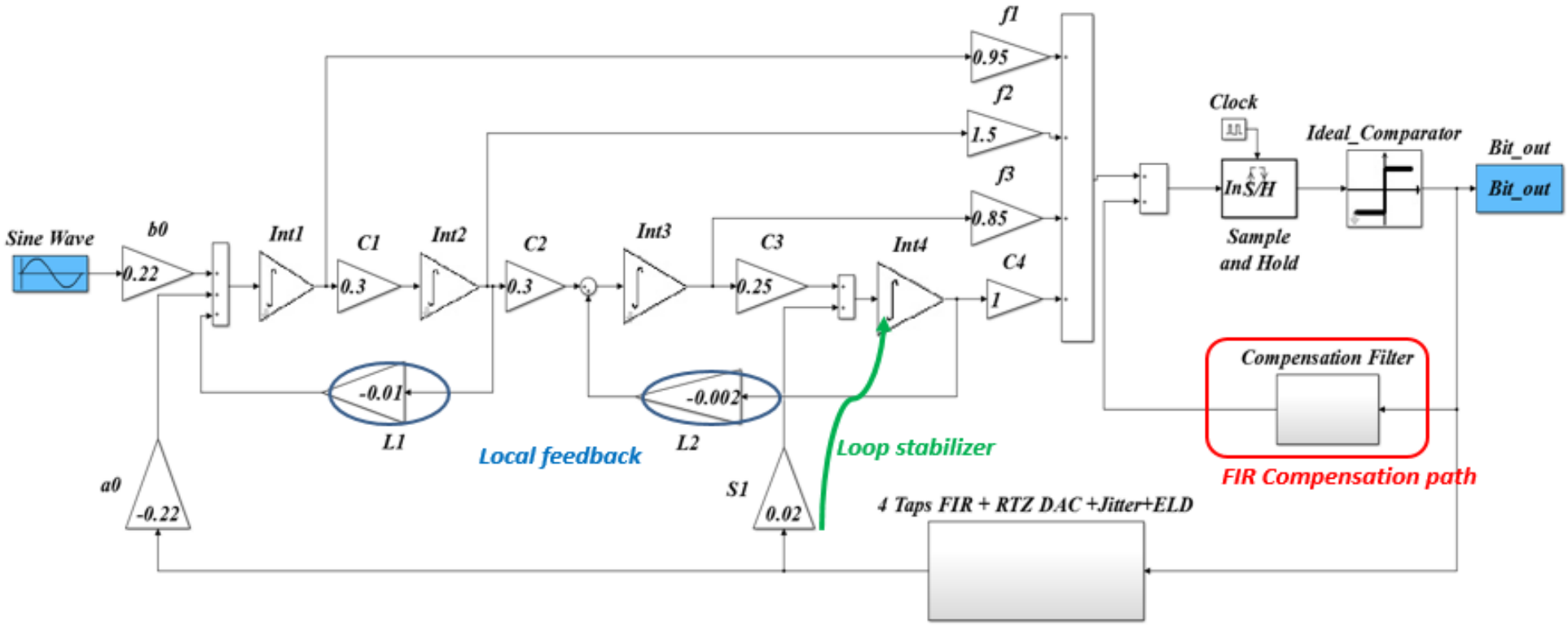



Figure 3-1: System level architecture overview of the proposed 4th order CTDSM in in MATLAB® Simulink® environment. It consists of the loop filter's coefficients values that required to stabilize the modulator, a behavioural model of the continuous time integrator with amplify unity gain use in the integrating stage CTDSM; an ideal comparator is used to model the 1-bit quantizer. Compensation path is required to re-stabilize the CTDSM from delay introduced by the FIR filter

## 3.2 Feedback DAC Non-idealities

In CTDSMs any deviation from the ideal DAC pulse severely affects the performance of the modulator, since the waveform is continuously integrated at the front-end of the modulator. ELD, ISI interference and clock jitter are the main limiting factors in the adequate representation of square-shaped DAC waveforms, and the fundamental causes of performance degradation in single bit CTDSM architectures [2].

### 3.2.1 Excess Loop Delay (ELD)

In [16] timing variation in feedback pulse which is assumed to be a constant delay $T_d$ between the ideal and implemented feedback DAC is commonly reffered to as excess loop delay.ELD is a problematic issue in CTDSMs and has a detrimental effect on their performance [17]. ELD mainly arises because of the following: in an ideal CTDSM, the feedback DAC current responds immediately to the quantizer (comparator) decision instant. However, in practice, there exists an inherent delay between comparator decision time and DAC response due to non-zero switching time within the DAC.

Excess loop delay causes the DAC pulse edge to begin after the sampling clock edge. Therefore, its detrimental effect on the modulator will highly depend on the type of DAC pulse used in the feedback path as depicted in Figure 3.2 for an NRZ and Return-To-Zero (RTZ) feedback waveforms where both DAC pulses are shifted by $Td < Ts$ from theirs supposed ideal position.

For an RTZ DAC with ELD less than half a clock cycle (i.e. $Td < 0.5\,Ts$), it's clear that the DAC pulse remains inside the clock period and a constant amount of feedback quantity (assumed to be a current charge) is integrated per sampling period. By contrast, for an NRZ DAC Figure 3.2, any loop delay will shift the pulse into the next sampling period causing an error in the amount of integrated charge over one period. Therefore, CTDSMs using an NRZ DAC will require an ELD compensation path around the quantizer to restore the modulator stability [18], [19]

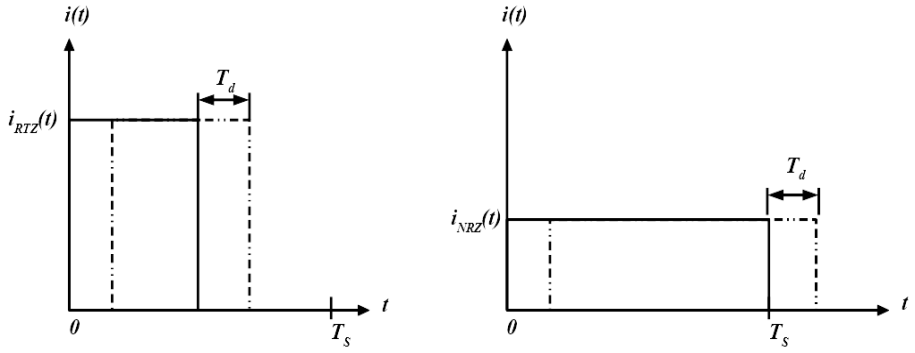



Figure 3-2: Loop delay effect on an RTZ and NRZ DAC

### 3.2.2 Inter-Symbol Interferences (ISI)

In CTDSMs the implementation of the feedback DAC waveform suffers from asymmetrical rising time and falling time. This nonideality causes additional errors that directly add to the modulator input and tend to degrade its performance, unless they are small enough.

For the case of CTDSM employing an NRZ DAC large different between the rise and fall times of the DAC pulse introduce inter-symbol interference resulting in harmonic distortion within the loop filter that compromises the modulator linearity along the achievable *SNR*. ISI can be thought of as a dependence of the modulator feedback energy content on an output bitstream pattern [20]. Figure 3.3 shows two output data patterns for NRZ and RTZ DAC pulses. Due to the non-zero rising and falling times, it can be seen that the amount of feedback quantity (assumed to be a charge) being integrated into a CTDSM depends on the output data sequence. In order words, when using an NRZ DAC mismatch between rise and fall times makes the pulse area is different if the preceding pulse one. Therefore, the resulting errors in the feedback charge will depend on the output sequence and thus giving rise to signal-dependent distortion [21]. As illustrate in Figure 3.3 RTZ DAC can be using to avoid ISI, so that, in spite of different rise and fall times in DAC response, the error remains constant in every clock period (Figure 3.3).

Figure 3.4 illustrates the output spectrum of a 4th order single bit CTDSM under the presence of ISI, for an NRZ and an RTZ DAC pulses, where the superior performance of the RTZ DAC is clearly seen.

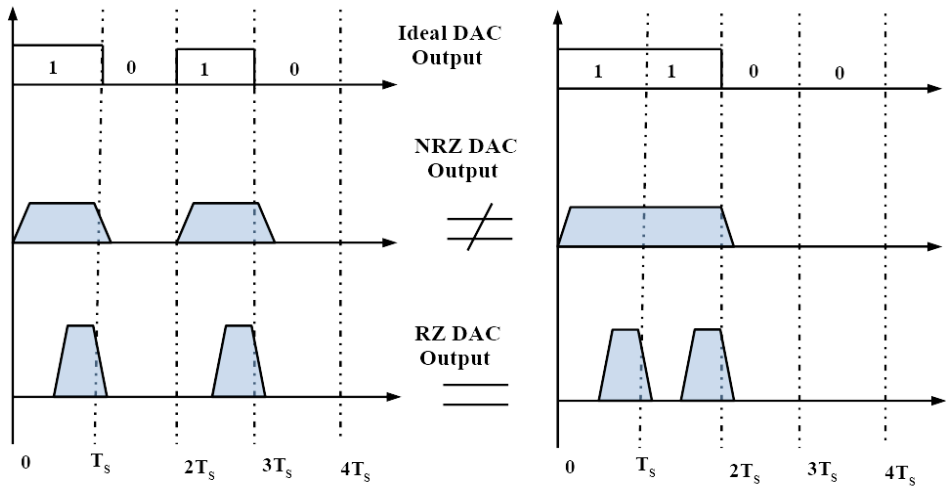



Figure 3-3: Inter-symbol interference on the feedback DAC waveform

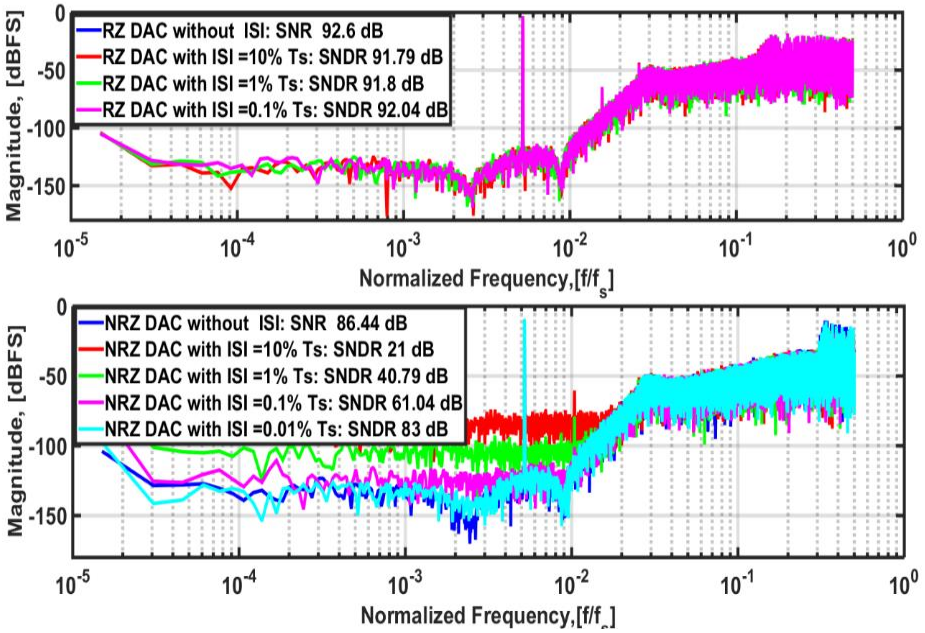



Figure 3-4: PSD of the 4th order single-bit CTDSM modulators with NRZ and RTZ feedback DACs under the influence of ISI—the same architecture is used in both cases

### 3.2.3 Clock Jitter

Clock jitter is a random timing deviation of a clock signal edge from the ideal clock edge. In a CTDSM this effect introduces random variations in the amount of feedback charge in the modulator per clock period [22]. Thus, the ability of the CTDSM to tolerate timing jitter will depend on the type of DAC waveform used in the feedback path. Figure 3.5 shows the typical structure of a CTDSM with the jitter error at DAC pulse edges being introduced in the feedback signal

Due to the continuous time integration of the feedback waveform, the DAC pulse width, which dictates the amount charge transfer per period, will also be modified by any errors in the sampling instant [23]. Figure 3.6 shows an illustration of an NRZ and RTZ DAC under the influence of clock jitter. It's apparent that RTZ pulse will be more affected by clock jitter error due to the occurrence of two switching of the DAC pulse within every clock period. As a result, the amount of charge error integrated at the front-end of the modulator is doubled when using an RTZ DAC

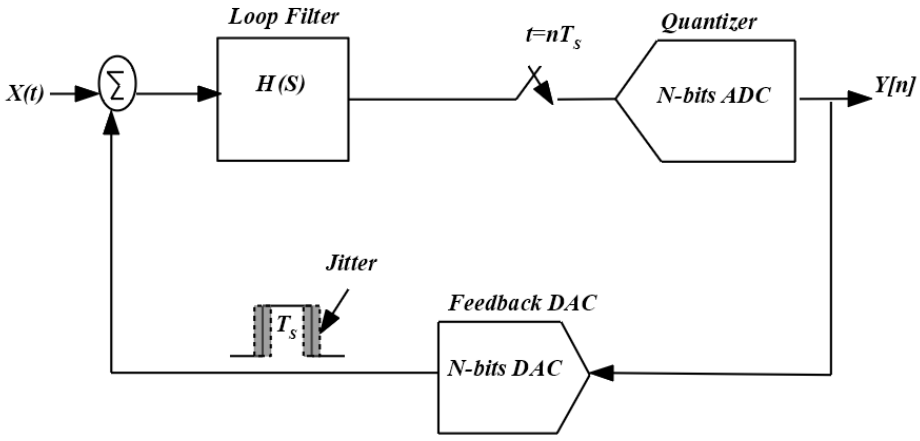



Figure 3-5: CTDSM with jittered feedback DAC Pulse

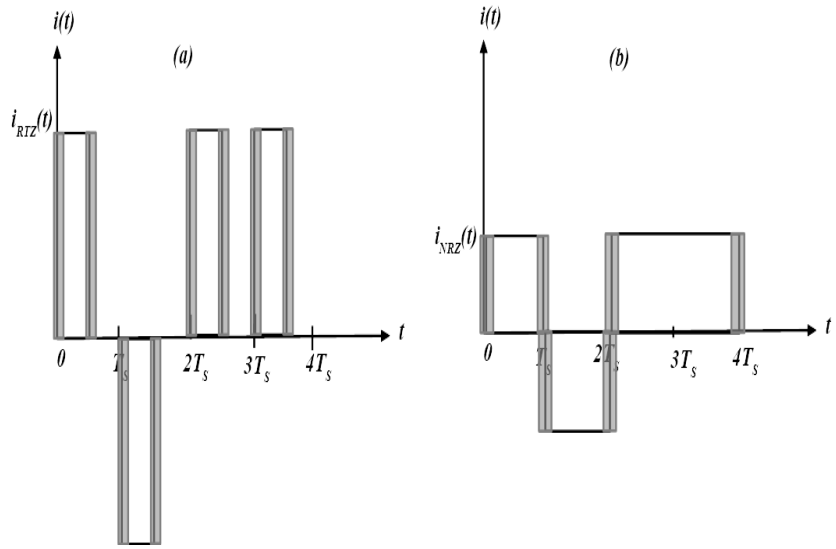



Figure 3-6: (a) RTZ and (b) NRZ feedback DAC pulses under Clock Jitter Noise Influence.

## 3.3 Clock jitter modelling

To ease the analysis, clock jitter is assumed to follow a Gaussian distribution, thus allowing us to model the jitter as uncorrelated additive white noise on the DAC pulse edges as shown in Figure 3.6. Here, jitter error is defined as the difference between the jittered feedback DAC pulse and the ideal DAC pulse at every sampling instant as shown in Figure 3.7. These variations of the DAC pulse width directly modulate the amount of feedback charge per clock cycle in the CTDSM.

The integrated in-band noise due to jitter for an NRZ feedback DAC (IBNJ) is given by [23]:

$$IBNJ_{NRZ} = \left(\frac{\sigma_t}{T_s}\right)^2 \frac{4p}{OSR} \tag{3.1}$$

where $p$ denotes the probability of the modulator output to make a transition (should be high) and standard deviation of the jitter error sequence

For a CTDSM using a RTZ DAC, it's been demonstrated in [16] that the total integrated in-band noise due to jitter is:

$$IBNJ_{RTZ} = \left(\frac{\Delta}{2}\right)^2 \left(\frac{K_{i,RTZ}}{K_{i,NRZ}}\right)^2 \left(\frac{\sigma_t}{T_s}\right)^2 \frac{A_{RTZ}}{OSR} \tag{3.2}$$

where Δ is the DAC step size, $A_{RTZ}$ is the DAC pulse activity factor, $k_i$ is the feedback path scaling coefficient, $\sigma_t$ is the standard deviation of the jitter error sequence, $T_s$ is the sampling period and $OSR$ is the oversampling ratio.

Considering the adopted single bit modulator with RTZ DAC pulse topology, the activity factor is $A_{RTZ} = 2$, due to the occurrence of two switching events of the DAC pulse within every clock period, hence two edges of the DAC pulse are always jittered per period.

Additionally, the amplitude of the RTZ DAC pulse $I_{RTZ}$ (Figure 3-6a) is determined by the feedback scaling coefficient and the DAC step size. For a single bit CTDSM this given by [10], $I_{RTZ} = K_{i,RTZ}\Delta/2$. Note that in the case of an NRZ DAC pulse, jitter affect the transferred feedback charge only if the feedback signal varies its sate. In other words, the jitter noise only depends on the difference between two adjacent feedback pulses. Consequently, the above-mentioned activity factor is reduced to 1. Likewise, if a transition occurs in the NRZ feedback DAC, the step is always a complete step-width Δ rather than $\Delta/2$ in the RTZ case

As a result, the induced IBN due to jitter for the RTZ implementation is derived as [10]:

$$IBNJ_{NRZ} = \left(\frac{\sigma_t}{T_s}\right)^2 \frac{8}{OSR} \tag{3.3}$$

In many publications, to easily compare the impact of clock jitter on these two widely used rectangular feedback pulse, a jitter suppression efficiency $n_{\square}$ was introduced [2] Using (3.2), to evaluate the INBJ for RTZ and equation (3.1) for NRZ feedback DAC assuming that the probability $p = 0.8$ as recommended by [23] for good in-band noise due to jitter estimation, the efficiency $n_j$ equal to :

$$n_j = 10\log_{10}\frac{IBNJ_{RTZ}}{IBNJ_{NRZ}} = 10\log_{10}\frac{A_{f,RTZ}}{A_{f,NRZ}} \approx 4\ dB \tag{3.4}$$

Therefore, for a single bit CTDSM an RTZ DAC performs about $4\ dB$ worse than the NRZ counterpart for the same amount of clock jitter. To illustrate the effect of clock jitter, on the adopted a 4$^{th}$-order, single bit CTDSM architecture, an uncorrelated additive white noise was injected on the DAC pulse edges as described in [11] and illustrated in Figure 3.7. The clock jitter effect over the proposed CTDSM output power spectral density (PSD) with an RTZ DAC pulse is depicted in Figure 3.8, where it can be seen that even a small σjitter of 0.01% Ts can lower the SNDR by about 11dB.

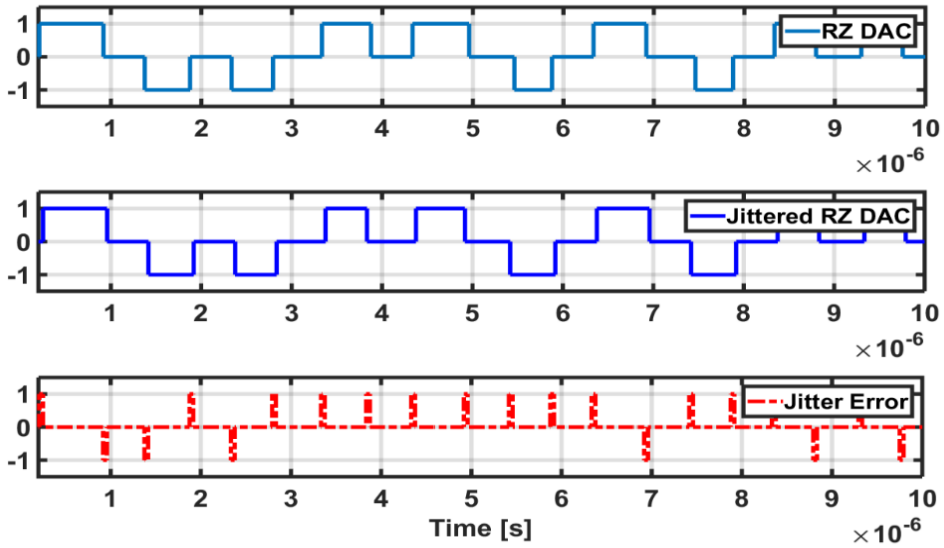



Figure 3.7: Simulated timing jitter error across few cycles on a 4th order single-bit CTDSM with RTZ DAC pulse

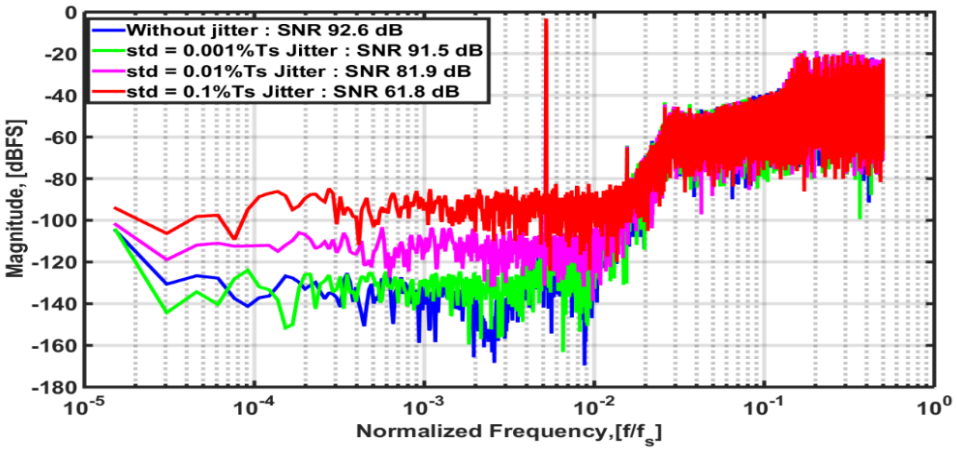



Figure 3.8: Simulated PSD for the 4th order CTDSM under clock jitter influence ($f_s$ =24 MHz & input amplitude= 0.35 V)

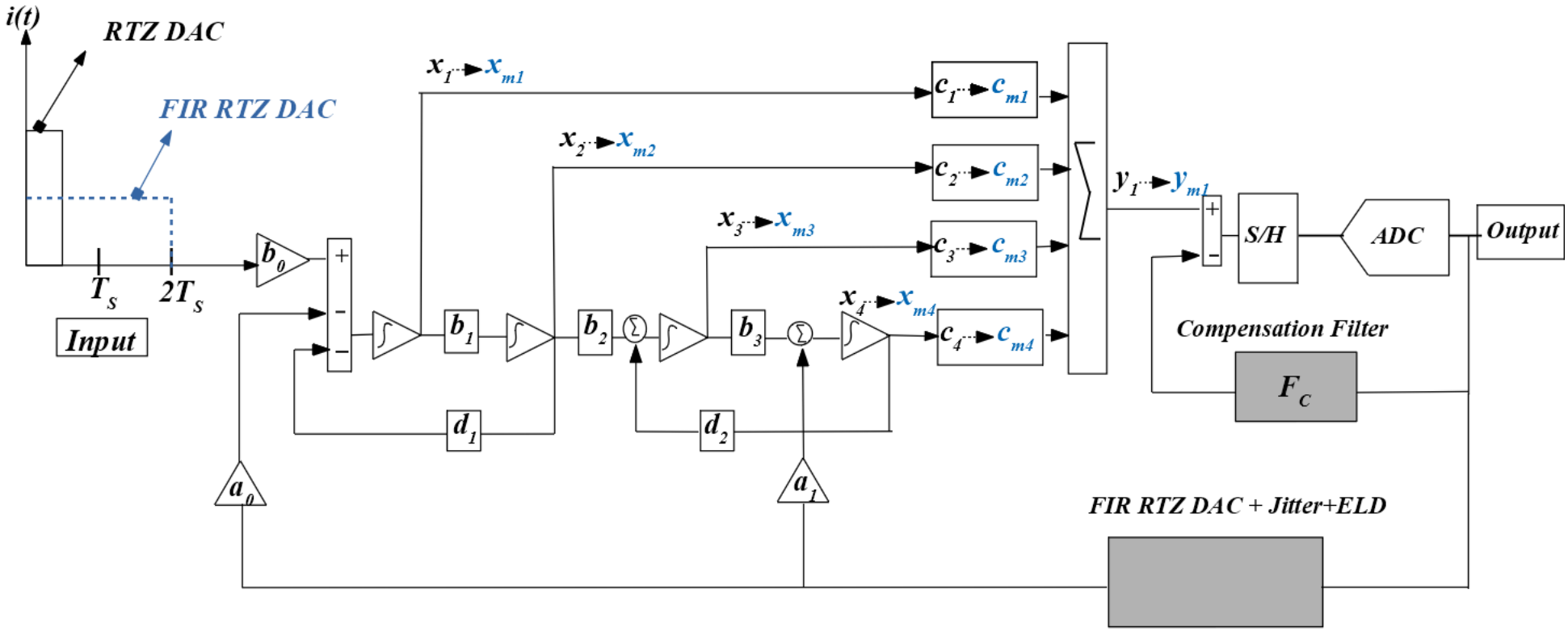



Figure 3.9: 4th Order CTDSM Architecture Overview. The original modulator with an RTZ DAC loop filter pulse response is referred to as $y(t)$ and the proposed CTDSM i.e. with the FIR RTZ DAC loop response is denoted by $y_m(t)$

## 3.4 Clock Jitter Alleviation in CTDSM through RTZ FIR DAC

Various exiting methods of reducing the effect of clock jitter in CTDSM have been presented in the literature. Multi-bits design has been proposed in [24] to reduce the sensitivity of CTDSM to clock jitter since the step size of the feedback pulse is reduced hence the amount jitter error also (based on the number quantizer level). However, multi-bit feedback DACs introduce mismatch in the circuitry due to devices process variation and temperature [22], which limit the overall linearity of the modulator. Additionally, using a multibit DAC requires extra calibration circuitry know as dynamic element matching resulting in an overall increase in complexity and instability of the CTDSM coupled with power and area budget. Similarly, switched-capacitor DAC pulse has been suggested in [20] to mitigate the influence of jitter in CTDSM since they exhibit low charge variation in the presence of jitter. However, the actual circuit level implementation of such DAC switching pulse can be challenging.

In the proposed CTDSM architecture, to reduce RTZ DAC clock jitter sensitivity, we have incorporated a FIR filter in the feedback path, which is illustrated in Figure 3.9. Adding this FIR filter to the feedback DAC attenuates the high-frequency content of the clock jitter before it is feedback to the input of the modulator, reducing its negative impact in the modulator's accuracy. On the other hand, the FIR filter introduces an additional delay in the feedback path, which compromises the stability of the overall modulator. This additional delay is compensated via a compensation filter $F_c$ around the quantizer as depicted on the right side of Figure 3.9. This allows the modified loop filter with FIR RTZ DAC impulse response to match the original loop filter impulse response

The synthesis of the modified CTDSM feedforward coefficients denoted by $c_{m1} \dots c_{m4}$ that will restore the original CTDSM loop filter impulse response is achieved using the method of moments described in [25]. Considering again Figure 3.9, the loop filter pulse output can be expressed as:

$$Y(t) = c_4x_4 + c_3x_3 + c_2x_2 + c_1x_1 \,. \tag{3.5}$$

By incorporating the FIR DAC into the loop, the individual modulator loop paths $x_1 \ldots x_4$ will be modified and the resulting loop filter pulse output is modified to:

$$Y_m(t) = c_{m4}x_{m4} + cx_{m3} + c_{m2}x_{m2} + c_{m1}x_{m1} \,. \tag{3.6}$$

By using the method of moments of [25] and [26], the pulse response of the $\frac{1}{S^N}$ integrating path denoted by $x_{\square}(t)$ is given by:

$$\begin{aligned} x_N(t) &= \frac{t^{N-1}}{(N-1)!}\,\mu_l(t) * p(t) \\ &= \frac{1}{(N-1)!}\int_0^t p(\tau)(t-\tau)d\tau \end{aligned} \tag{3.7}$$

where *p(t)* is the total area of the DAC pulse response (ideally equal to one after one sample period) and $u_{\square}(t)$ is $l^{th}$ moment of the DAC pulse $\mu_l = \int_0^t \tau^l p(\tau)d\tau$ with *p(t)=1* and $0 \le t \le T_s$.

Substituting the moments of the RTZ DAC pulse into equation (3.7) and after simplification, the original 4th order CTDSM loop filter's individual path pulse responses are:

$$\begin{aligned} x_4(t) &= \frac{1}{6}\mu_0 t^3 \; - \frac{1}{2}\mu_1 t^2 + \frac{1}{2}\mu_2 t^1 \; - \frac{1}{6}\mu_3 \\ x_3(t) &= \frac{1}{2}\mu_0 t^2 - \mu_1 t + \frac{1}{2}\mu_2 \\ x_2(t) &= \mu_0 t - \mu_1 \\ x_1(t) &= \mu_0 \end{aligned} \tag{3.8}$$

A similar method is used to derive the individual path response ($x_{m1} \ldots x_{m4}$) of the modified CTDSM with a 4-tap FIR filter. The amplitude of $y_1(t)$ with RTZ DAC will be reduced from 2 to $2/(Number\ of\ FIR\ taps)$. Thus, the FIR RTZ DAC can now

be interpreted as a pulse amplitude $p(t) = 0.5$ from $0 \leq t \leq 2T_s$ as illustrated in Figure 3.10 (blue). The $l^{th}$ moment of this DAC pulse is given by $\mu_{ml} = \int_0^t \tau^l(0.5)d\tau$ and, after substitution into (3.7), it can be shown that the modified CTDSM pulse responses of the loop filter paths are given by:

$$\begin{aligned} x_{m4}(t) &= \frac{1}{6}\mu_{m0}t^3 - \frac{1}{2}\mu_{m1}t^2 + \frac{1}{2}\mu_{m2}t^1 - \frac{1}{6}\mu_{m3} \\ x_{m3}(t) &= \frac{1}{2}\mu_{m0}t^2 - \mu_{m1}t + \frac{1}{2}\mu_{m2} \\ x_{m2}(t) &= \mu_{m0}t - \mu_{m1} \\ x_{m1}(t) &= \mu_{m0} \end{aligned} \tag{3.9}$$

As shown in Figure 3.10 the loop filter pulse response of the original CTDSM (blue curve) will be identical to that of the proposed loop filter pulse response with a 4-tap FIR

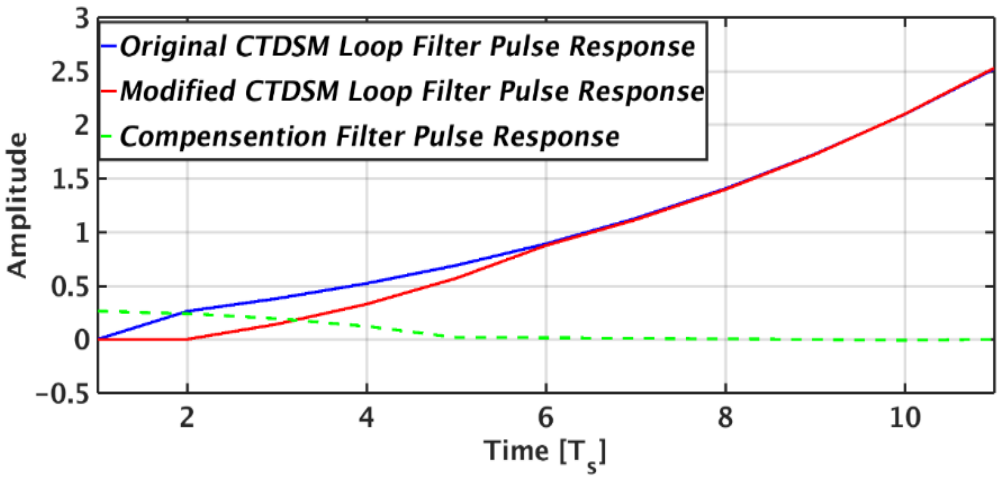



Figure 3-7: Illustration of the 4th order CTDSM loop filter response with RTZ DAC (red), the modified CTDSM with a 4 taps FIR RTZ DAC and the responses of the $F_c$ compensation filter.

The new re-scaled loop filter feedforward coefficients that will enable the loop filters described by equations (3.5) and (3.6) to align after $t_{delay}$ = number of filter taps are as follows:

For $y(t) = y_m(t)$ and $\mu_{m0} = \mu_0 = 1$ :

$$c_{m4} = c_4\,;\; c_{m3} = c_3 + (\mu_{m1} - \mu_1)c_4$$
$$c_{m2} = c_2 + (\mu_{m1} - \mu_1)(c_3 + c_4\mu_{m1}) - \frac{c_4}{2}(\mu_{m2} - \mu_2)$$
$$c_{m1} = c_1 - c_2\mu_1 + \frac{c_3\mu_2}{2} - \frac{c_4\mu_3}{6} + c_{m2}\mu_{m1} + \frac{c_{m4}\mu_{m3}}{6} - \frac{c_{m3}\mu_{m2}}{2}$$

Thus, the $F_c$ compensation filter coefficients can be found as the difference between the original loop filter response (blue) and the modified CTDSM pulse response (red) shown in Figure 3-7. Although not included in the previous coefficient derivations, the NRZ DAC can tolerate excess loop delay (ELD) up to 0.5Ts without any extra step in the coefficient derivation [1].

The proposed 4th order single bit CTDSM with a 4-tap FIR RTZ DAC was simulated in the MATLAB® Simulink® environment. With a sampling frequency of $24\ MHz$ over a signal bandwidth of $250\ kHz$, and including a clock jitter error sequence of $4.2\ ps\ rms$ the designed CTDSM achieves a maximum SNDR of $89.2\ dB$ which is illustrated in Figure 3.11. This plot validates the reduced jitter sensitivity of the proposed 4th order CTDSM with RTZ + FIR DAC and shows its improved robustness in the presence of clock jitter. Moreover, it is apparent that increasing the number of filter taps results in improved immunity to clock jitter effects. This is illustrated in Figure 3.12, where a clock jitter parametric analysis for 4-tap and 8-tap FIR DAC filtering is plotted. It is clear that 8-tap filtering outperforms the 4-tap one by about 3 dB at $\sigma_{jitter}$ = 4.2 ps, but it comes at the expense of an increased hardware complexity in both the FIR filter and the $F_c$ filter, leading to increased power consumption, silicon area and loop filter stability concerns. Therefore, a 4-tap FIR RTZ DAC represents a better trade-off to achieve a low area and cost-efficient design. Finally, it is worth mentioning that to achieve similar SNDR performance without the proposed FIR RTZ DAC method, a clock source of $0.5ps, rms$ clock jitter would have been required.

## Summary

This chapter has highlighted the influence of some of the common DAC non-idealities namely ELD, ISI and clock jitter in single CTDSM ADCs and their effect on modulator output *SNR*. Based on this, it was proposed to combine the use of an RTZ and FIR DAC to have inherent ISI immunity and reduced clock jitter sensitivity. The derived loop filter coefficients and mathematical assumptions were validated though MATLAB® simulations, showing that the proposed approach and architecture can simultaneously meet SNR and clock jitter specifications for IoT radio receiver applications.

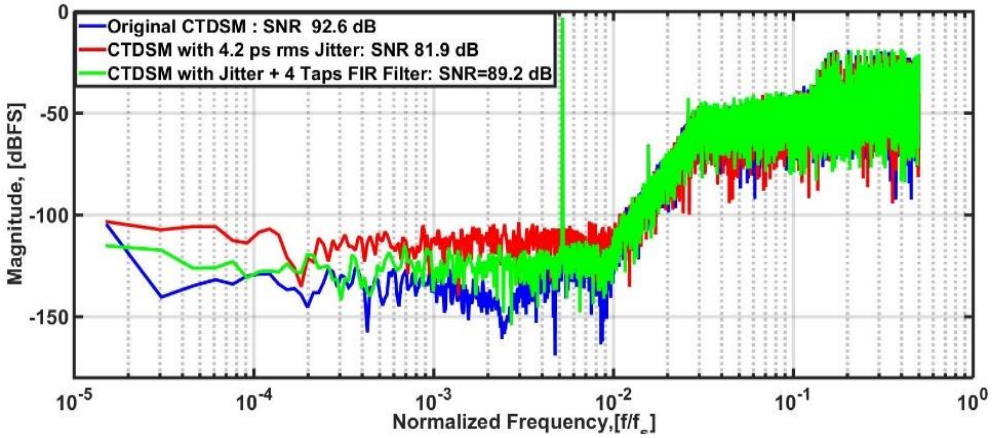



Figure 3-9: Simulated PSD with clock jitter, assumed white (σjitter = 0.01% Ts and fs= 24MHz). The jitter free spectrum is shown in blue. The CTDSM power spectral densities with 4 taps FIR filter in feedback paths is illustrate in green.

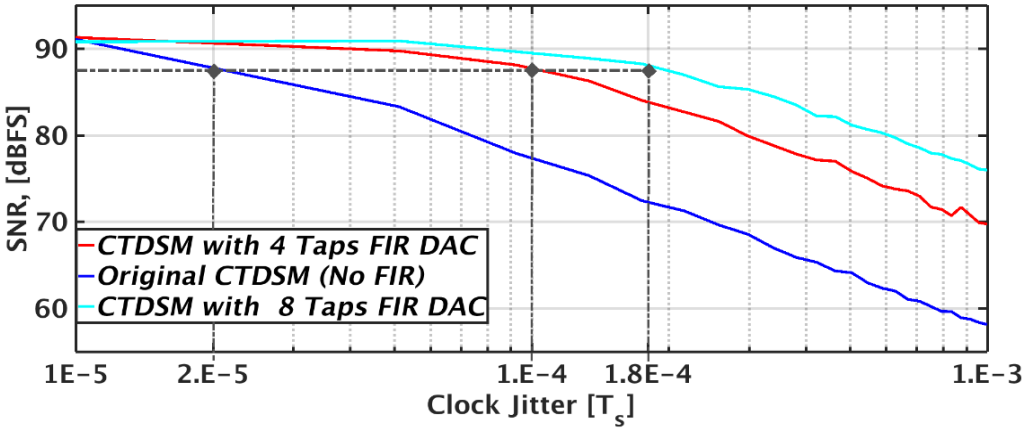



Figure 3-9: Comparison of the modulator SNR under clock jitter influence with a 4-tap and 8-tap FIR RTZ DAC.

# Chapter 4

## Circuit Design of a Low Power Continuous Time Delta Sigma Modulator

From the system level analysis detailed in the previous chapter, using an RTZ FIR DAC can significantly reduce the impact of clock jitter and ISI which are the main causes of performance degradation in high order CTDSM. This chapter will describe the circuit realization of the proposed $4^{th}$ order, single bit CTDSM targeting14-bit resolution along with meeting the strict linearity, power and area requirement of low power IoT radio receiver. The proposed single bit design is implemented in 65nm CMOS process using a supply voltage of 1.2 V. The modulator operates at $24MHz$ sampling rate over a bandwidth of $250KHz$. The following *top dow*n design flow was used: the MATLAB® Simulink® model described in chapter 3 was initially implemented using ideal components from the *AnalogLib* in cadence in order to validate the system level performance results obtained in chapter 3. Next each of the modulator building blocks i.e. RC integrator, OTA, quantizer, analog summer and DAC were gradually replaced with their transistor level counterparts.

### 4.1 Loop Filter Design

Single loop filter topology is not only advantageous in being area-efficient but also puts less constraint on the integrators design and coefficients matching which are the main building blocks of the loop filter as explained in [27]. Before diving into the design of the various modulator constituents, it is very important to analyse the different contributing noise sources within the adopted modulator

architecture in order to be able later to correlate the simulation results with theoretical expectation. This was done by performing a noise budget analysis as summarized in Table 4.1 and the companion pie chart where one should properly allocate the total modulator in-band noise (IBN). Since the current design target a 14-bit ENOB, we designed for an SQNR to be around $94\ dB$, which means that the total IBN power should be around $7\ dB$. This IBN power was proportionally shared amount the various noise contributor. For a single bit CTDSM architecture, these noise sources are mainly:

- Shaped quantization noise.
- Thermal noise mainly dominated by the first integrating stage, the input resistor, the feedback DAC resistor and the local feedback or notch resistor.
- Clock Jitter noise from the feedback DAC pulse.
- Non-linearity resulting from potential circuit mismatch and other noise sources coming from the power supply and conditioning circuit such as the current biasing, voltage references and buffer circuit

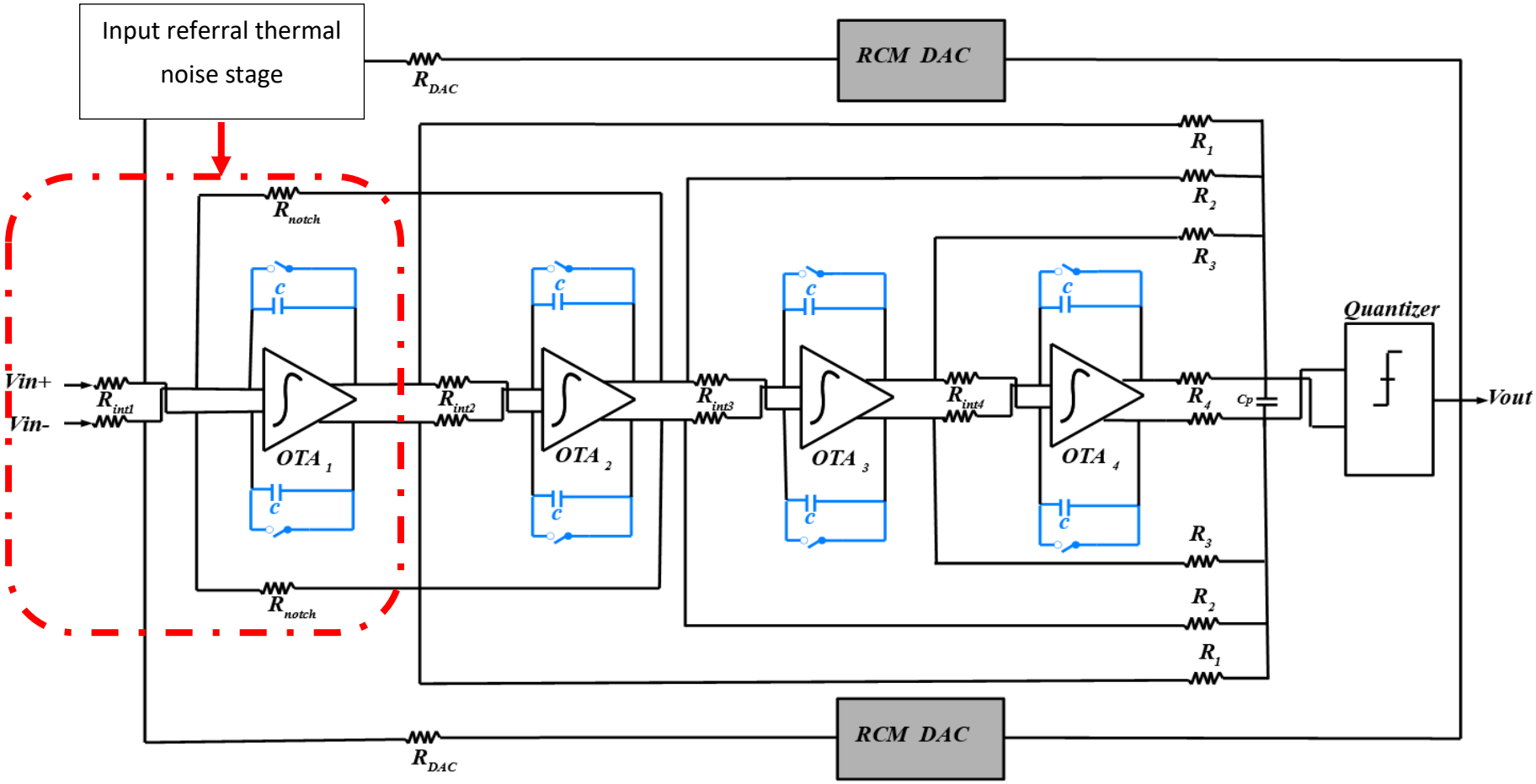



Figure 4-1: Implementation of the fully differential fourth-order, single bit quantizer, feedforward CTDSM

Table 4-1: Noise Budget

| Noise Contributor | Noise Budget | SNR for the noise source |
|---|---|---|
| Thermal Noise | 70 % IBN | 88 dB |
| Jitter Noise | 10% IBN | 92 dB |
| Quantization Noise | 10% IBN | 93 dB |
| Circuit Limitation | 10% IBN | 93 dB |

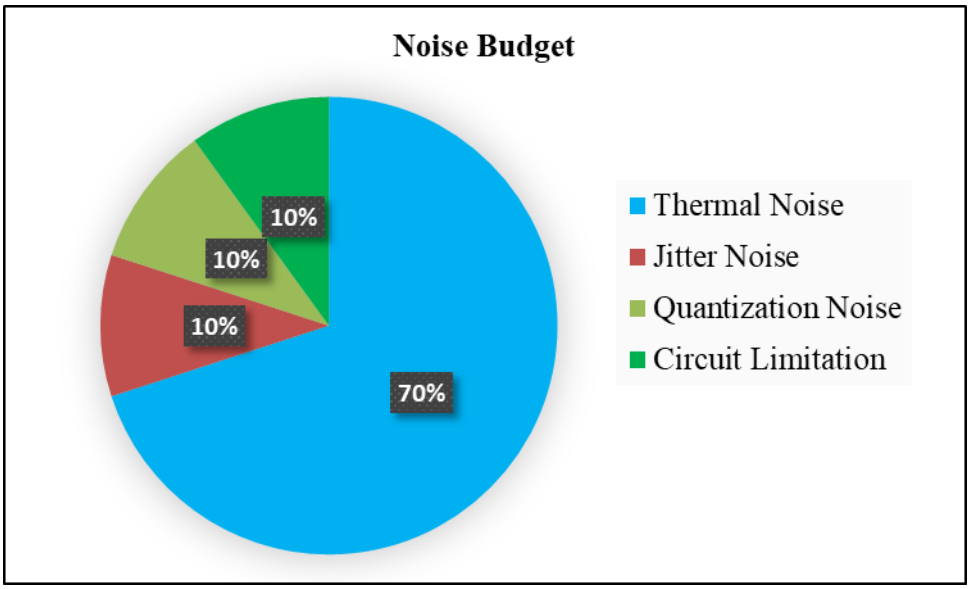



Figure 4-2: Noise Budget of the 4th order single-bit CTDSM

The overall circuit implementation of the 4th order modulator is depicted in Figure 4.1. The loop filter consists of four active RC-integrators. Note, the switch around each integrator is required to set the initial condition when powering up the modulator; they stay close for *2.5* $\mu s$ after the modulator turn on time then open afterward. The next major block of the loop filter is the analog passive resistive feedforward summer.

The first step in the loop filter design is to translate the loop filter coefficients shown in Figure 3.1 (cf. chapter 3) into practical realizable resistor and capacitor

values. Thus, the choice of the absolute input resistors values denoted by $R_{in1}$ and $R_{DAC}$ is dictated by the modulator input referred thermal noise which is mainly dominated/dictated by the first integrating stage. [17]

Focusing only on the first stage amplifier (OTA 1) highlighted in red (Figure 4.1), the main thermal noise contributors are from: the input resistors, DAC resistors, and local feedback resistor, $R_{notch}$ . Note, in the subsequent noise analysis we assumed that the amplifier noise contribution is negligible as in [27] and this was further validated by simulation results.

Therefore, the total input referred thermal noise power of the modulator taking into account the differential nature of adopted topology is given by [17]

$$\overline{v_n^2} = 2(\overline{v_{Rint1}^2} + \overline{v_{RDAC}^2}\frac{R_{\text{int1}}^2}{R_{DAC}^2} + \overline{v_{Rnotch}^2}\frac{R_{\text{int1}}^2}{R_{notch}^2} \tag{4.1}$$

Note that the two-scaling factor in the above equation is due to the fully differential characteristic of the first stage integrator.

And the thermal noise power generated by each resistor is:

$$\frac{\overline{v_{Rin1}^2}}{\Delta f} = 4KTR_{\text{int1}};\ \frac{\overline{v_{RDAC}^2}}{\Delta f} = 4KTR_{DAC};\ \frac{\overline{v_{Rnotch}^2}}{\Delta f} = 4KTR_{notch} \tag{4.2}$$

Hence the total input referred thermal noise yields:

$$\overline{v_n^2} = 8KT\left(R_{\text{int1}} + R_{DAC}\frac{R_{\text{int1}}^2}{R_{DAC}^2} + R_{notch}\frac{R_{\text{int1}}^2}{R_{notch}^2}\right)\Delta f \tag{4.3}$$

In CTDSM only the in-band noise components are considered since the high-frequency part of the noise is subsequently filtered by the decimator filter. Therefore, the induced in-band thermal noise power is given by:

$$P_N = \int_{-f_B}^{f_B} \frac{\overline{v_n^2}}{\Delta f} df \tag{4.4}$$

$$v_n^2 = P_N = 16KTf_B \left( R_{\text{int1}} + R_{DAC} \frac{R_{\text{int1}}^2}{R_{DAC}^2} + R_{notch} \frac{R_{\text{int1}}^2}{R_{notch}^2} \right)$$

Observing that $R_{in1} = R_{DAC}$ and assuming that $R_{notch} \gg R_{int1}$, (4.4) results in:

$$P_N = 32KTf_B R_{\text{int1}} \tag{4.5}$$

Using the total input referred noise power giving by (4.5) and for a target resolution of $B - bits$, over a certain bandwidth $f_B$ the maximum tolerable input resistance $R_1$ can be derived as [17]:

$$R_{\text{int1}} \leq \frac{V_{in}^2/2}{32KTf_B 3 \times 2^{2B-1}} \tag{4.6}$$

By using the current design specification this results to $R_{in1} \leq 10.2\ k\Omega$.

Thus, fixing the input resistor $R_{in1} = R_{DAC} = 10k\Omega$ the corresponding integrating capacitor $C_1$ value can be solved from the loop filter scaling coefficient $b_1$: and the sampling frequency $f_s$

$$C_1 = \frac{1}{b_1 R_{\text{int1}} f_s} \tag{4.7}$$

Equation (4.7) can be re-used to translate the loop filter coefficients into corresponding $R$ & $C$ for the subsequent integrating stages (int. 2-4)

The implementation resistor and integration capacitor values of the loop filter coefficients derived in chapter 3 are summarized in Table 4.2.

Table 4.2: CTDSM loop filter passive R & C components calculations

| System Level | Circuit Realization | Coefficient | Circuit Value | Sampling Freq | Integrator Capacitor |
|---|---|---|---|---|---|
| $a_1$ | $R_{DAC}$ | 0.22 | $10k\Omega$ | $24MHz$ | $18.39pF$ |
| $b_1$ | $R_{in}$ | 0.22 | $10k\Omega$ | $24MHz$ | $18.39pF$ |
| $c_1$ | $R_2$ | 0.3 | $7.33k\Omega$ | $24MHz$ | $18.39pF$ |
| $c_2$ | $R_3$ | 0.3 | $7.33k\Omega$ | $24MHz$ | $18.39pF$ |
| $c_3$ | $R_4$ | 0.25 | $8.8k\Omega$ | $24MHz$ | $18.39pF$ |
| $l_1$ | $R_5$ | 0.01 | $220k\Omega$ | $24MHz$ | $18.39pF$ |
| $l_2$ | $R_6$ | 0.02 | $440k\Omega$ | $24MHz$ | $18.39pF$ |

## 4.2 Fully Differential OTA Amplifier Design

In CTDSM with feedforward loop filter topology, the first integrator does not only determine the overall modulator noise and linearity but also, it's the most power-hungry block in the entire loop filter. As the noise contributions from subsequent stages are progressively attenuated by the loop filter. Thus, the bias current (and hence power dissipation) can be gradually reduced from the first stage to last stage [28]. Therefore, when designing the first stage integrator, one should ensure that it has a low input referred noise. The employed continuous time integrators were realized using operational transconductance amplifier (OTA) topology as it offers superior insensitivity to parasitic capacitances, speed and good load driven strength when compared to other amplifier structure (Op-amps-RC & Gm-C) as further explained in [29]

In[27] and [30] it was shown that for low power CTDSM, the strictest requirement on the integrating stage amplifier design is the gain bandwidth product i.e. $GBW \approx 3f_s$ and good output swing voltage [22]. The amplifier swing requirement can be explained as follows: the 4$^{th}$ order CTDSM has four states whose values at the sampling instant completely define the modulator operation. The output voltages of integrators at the sampling instant within the loop filter

correspond to these modulator states. Therefore, the amplifier within the integrator needs to have large output voltage swings to produce the correct output voltage value and avoid signal clipping otherwise the entire modulator functionality will be altered. On the other hand, the requirement on the amplifier slew rate are only minor constraint, especially because in CTDSM the signal is oversampled i.e. the input signal is slower compared to the sampling rate thus slew rate limitation of the amplifier signal will have little effect as long as the outputs signal are close enough to the correct values after a clock cycle making CTDSM tolerant to slew rate imperfection [22].

These design requirements were chosen because low power consumption as mentioned in the introductory chapter is one of the main design targets of this project since as it will be shown in the simulation results chapter 5, the loop filter is the most power-hungry

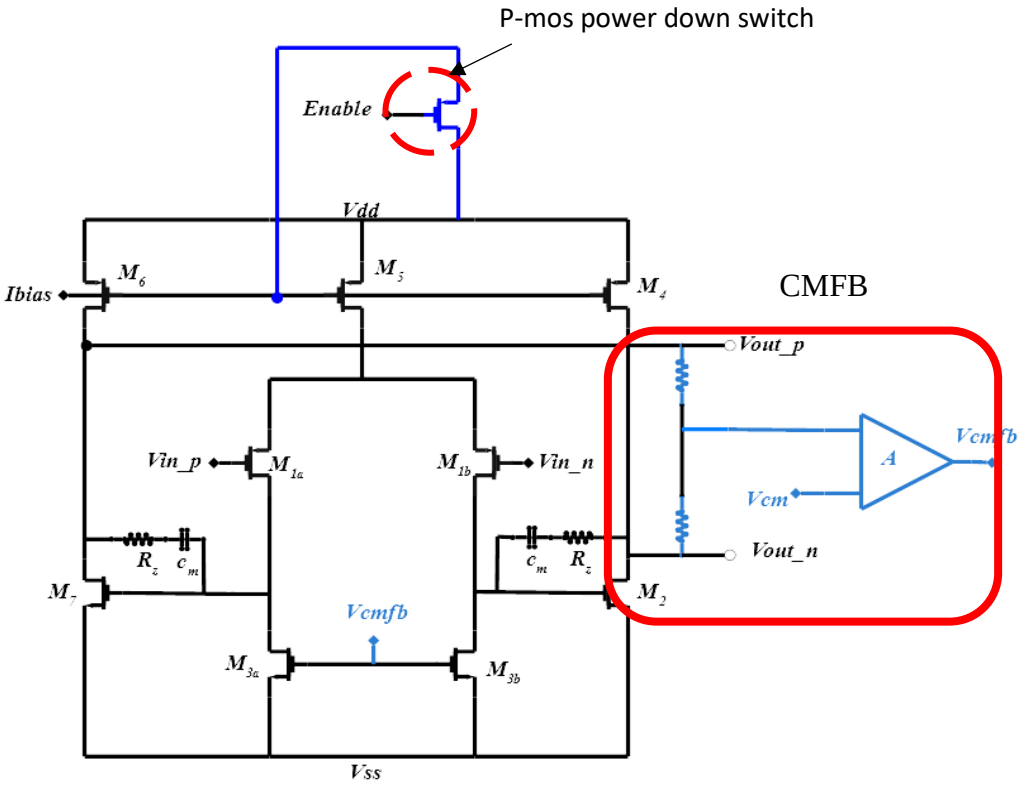



Figure 4-3: Fully differential two stage miller compensated OTA with CMFB circuit used in loop filter integrators

Figure 4.3 shows the circuit of the fully differential Miller OTA used in the integrating stage of the modulator loop filter. The Miller OTA consists of two cascades stages: a P-mos1 differential input represent by transistor M1a & M1*b;* the second stage is N-mos common-source gain stage M2. The current generated by the input differential pair is converted to a voltage by current mirror transistors M3a & M3b. The input bias current at each stage is controlled via M4 & M5 while pole splitting is achieved through $C_m$. In fact, the two stages Miller OTA is a second order system as it shows two dominant poles, thus the purpose of the Miller capacitance is to split these poles apart, pushing the second pole far beyond the unity gain frequency and the first pole too low frequencies. This turns the two stage OTA into a first order or dominant pole system [31]. However, the Miller capacitance introduces a right half plane zero which is cancelled out by connecting a resistance $R_z$ in serie with $C_m$ which value is given by $R_z = 1/g_{m2}$ . Furthermore, the compensation capacitance $C_m$ set the gain bandwidth product as derived from the expression: $GBW = g_{m1}/2\pi C_m$ and the non-dominant pole frequency is given by $f_{nd} = g_{m2}/2\pi C_L$ where $C_L$ is the load capacitance. Both of these two quantities set the stability requirement of the two stages amplifier. Thus, the non-dominant pole is often pushed a very high frequencies to ensure that the amplifier is stable.

The fully differential topology implementation was adopted to maximize the amplifier output swing and minimized common mode noise. Therefore, a common mode feedback (CMFB) circuit was required to fix the output voltage to the common value $V_{cm}$. The CMFB circuitry (shown in figure 4.10) consists of resistive divider that detect the output common mode voltage of the OTA. A sense amplifier is used to compare the detected output voltage with the common mode reference $V_{cm}$ and finally any common mode error voltage $V_{cmfb}$ is fed back to current mirror transistors M3a & M3b to adjust the output common mode voltage. The transistor level schematic of the CFMB sense amplify is shown in Figure 4.10. Power down *P-* guarantee that zero current flows in the amplifier when it's "OFF" thus no power is dissipated

The Gm/Id sizing methodology for low voltage CMOS circuit design described in [32] was used to find the sizes of the optimum transistors to use in Miller OTA that

will meet the prescribed design target such gain bandwidth product, low power consumption and dc gain.

Since the amplifier is one of the most critical elements of in the loop filter, it's crucial to fully characterize its behaviour by running various test bench as shown in the subsequent section.

### i. Output Swing

This is essential for low voltage design. The maximum fully differential amplifier output swing can be estimated as follow assume a common mode voltage of $V_{cm} = 0.6\,V$:

- **Positive output node swing**

$$\begin{aligned} V_{swing_p} &= (V_{dd} - V_{M6_{dsat}}) - (V_{ss} + V_{M7_{dsat}}) \\ &= (1.2\ - 0.14026) - (0 + 0.0543) \\ V_{swinp} &= 1.005\text{V} \end{aligned} \tag{4.8}$$

- **Negative output node swing**

$$\begin{aligned} V_{swing\_n} &= (V_{dd} - V_{M4_{nsat}}) - (V_{ss} + V_{M2_{nsat}}) \\ &= (1.2\ - 0.14876) - (0 + 0.0485) \\ V_{swing\_n} &= 1.003\text{V} \end{aligned} \tag{4.9}$$

- **Fully differential amplifier output swings**

$$\boldsymbol{V_{swing} = V_{swing_p} + V_{swing_n} = 2.008V} \tag{4.10}$$

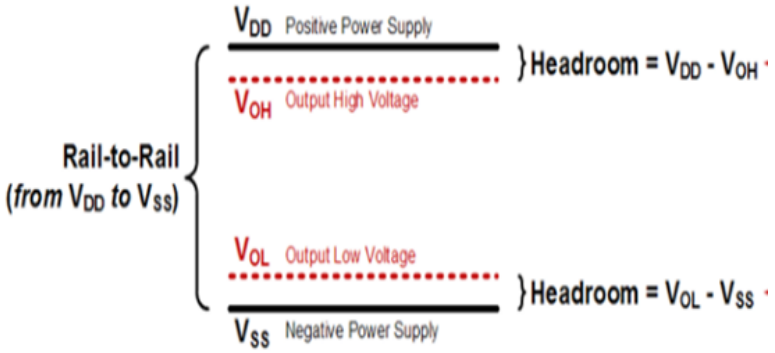



Figure 4-4: Amplifier output swings illustration

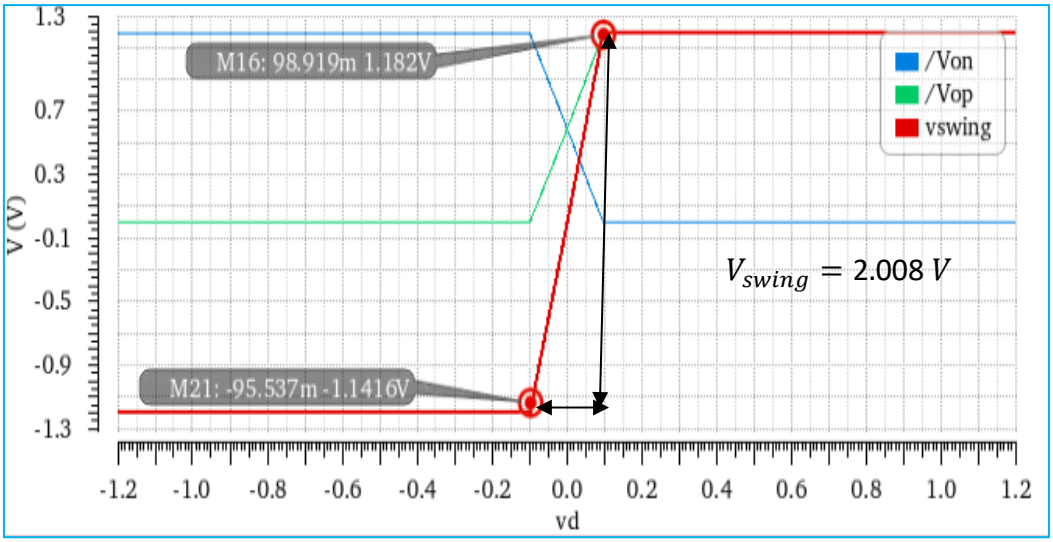



Figure 4.5: Amplifier voltage output swings

### ii. **Small Signal Open Loop Gain, Phase Margin and Gain bandwidth** product

While good linearity of the first amplifier in loop filter is very important to meet the ADC, specification mentioned in introductory chapter. An open loop gain DC gain $A_0 \geq 60\ dB$ is sufficient gain to ensure that the first integrator stage has enough gain to drive the load from the next stage and performs the input signal amplification. The design target for the unity gain bandwidth and phase margin

were respectively $GBW \approx 3f_s = 72\,MHz\;and\;PM = 50°$ to ensure that the amplifier is stable. The setup used to measure the loop gain is shown in Figure 4.6.

The simulated magnitude and phase response of the fully differential OTA is shown in Figure 4.7. The DC open loop gain is about $A_0 = 63dB$, the unity gain bandwidth frequency $GBW = 90.72\,MHz$ and the $PM = 52°$. The total power consumption is about $P_w = 410\,\mu W$

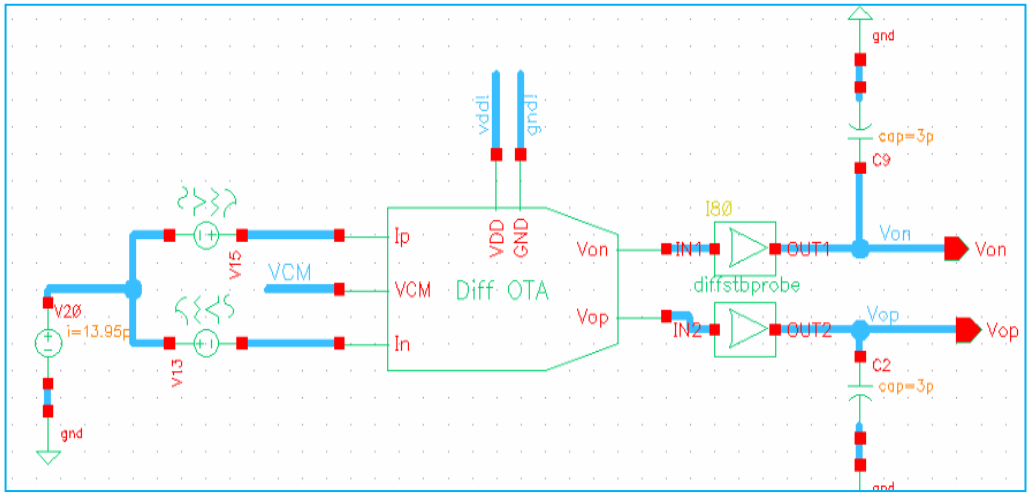



Figure 4.6: Setup to simulate the amplifier gain

$$\begin{aligned} GBW &= f_{-3dB} \times Open\;loop\;Gain \\ &= 59.6639k \times 1520.54 \\ &\boldsymbol{GBW = 90.72\,MHz} \end{aligned} \tag{4.11}$$

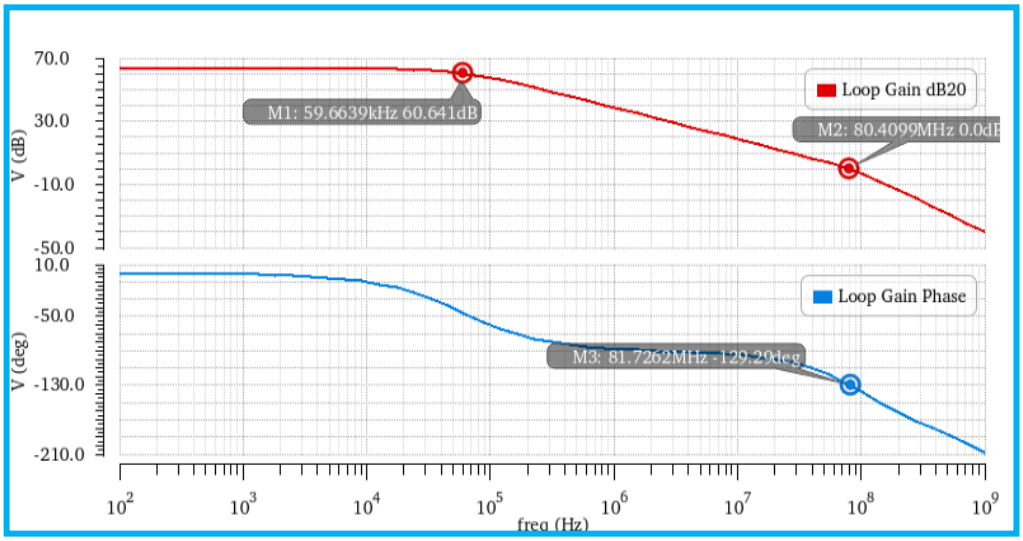



Figure 4.7: Magnitude and phase plots of the OTA used in the first integrator.

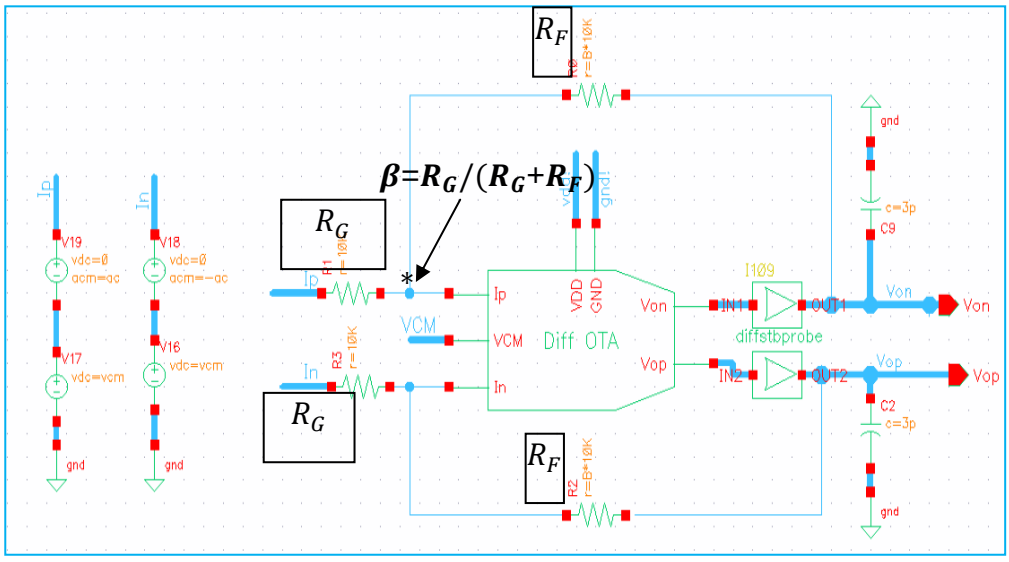



Figure 4.8: Setup to simulate the stability of the amplifier in feedback configuration

### iii. Amplify feedback configuration stability

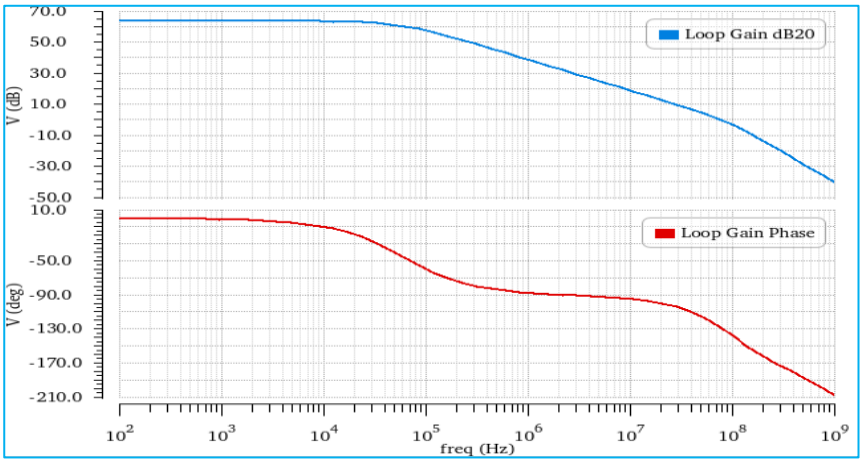
The ***stb*** algorithm in Cadence Spectre simulator can be used to test the stability of an amplifier. This analysis linearizes the circuit about DC operating point and computes the loop gain, phase margins of the amplifier. The *diffstbprobe* available in the *AnalogLib* is used to handles unbalanced differential circuits and is placed in the feedback loop to be measured. Figure 4.8 shows the setup used to check the stability of the fully differential amplifier in the feedback configuration. The *diffstbprobe* is place at the output to virtually break the feedback loop and has an internal setting to selects the differential-mode gain being measured.

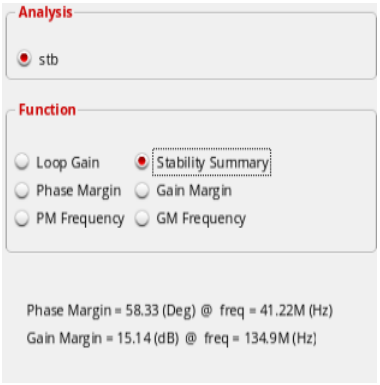
- Sample feedback gain calculation illustration

Assuming an input signal $V_{ip} = V_{in} = 10uV_{pp}$ & Common input $V_{CM} = V_{DD}/2$

- Signal gain is, $= \frac{\Delta V_{OUT}}{\Delta V_{IN}} = -\left(\frac{R_F}{R_G}\right) = \frac{20K}{10K} = 2$
- Close loop gain is $A_{cl} = \frac{A_0}{1+A_0\beta}$ as $A_0 \rightarrow \infty$, $A_{cl} = 1/\beta$ and $Noise\ Gain = 1/\beta = 1+\frac{R_F}{R_G}$
- Therefore $A_0\beta \rightarrow \boldsymbol{Loop\ gain}$ and $\boldsymbol{Noise\ Gain \neq Signal\ Gain}$.

The *stb* simulation results are summarized in Figure 4.9. One's should note that the discrepancy observed on the GBW computed in eq 4.11 and that shown in Figure 4.9 is caused by the effect of the non-dominant pole, equation 4.11 is an implication that assumes a single pole roll-off




| | |
|---|---|
| **Results** | $I_{dc} = 5\mu A$<br>$V_{dd} = 1.2V$<br>$C_{Load} = 3pF$ |
| **Gain** | $A_0 = 63dB$ |
| **Phase** | $PM = 58°$ |
| **GBW** | $PM = 90.7MHz$ |

Figure 4.9: Loop gain and phase of the stability analysis along with the stb summary

### iv. CMFB circuit stability

The CMFB circuit is an essential part of any differential amplifier. Since it's used to amplify the difference between the average of the differential OTA output and the reference bias voltage $V_{cm}$. Thus, the CMFB needs to have enough loop gain to minimize the error voltage (. i.e. makes the average output voltage to be very close to $V_{cm}$). Moreover, since the CMFB is only used to adjust the DC level, one should ensure that it does not limit the amplifier signal swing and that it's stable and more important that the loop gain has a higher $GBW$ for better rejection of any common mode signal. Therefore, a separate set up as shown in Figure 4.10 was used to test the stability of the CMFB loop as standalone. The *stb analysis*[2] in

[2]The spectre stb analysis provide a way to simulate continuous time loop gain, phase and gain margin with breaking the feedback loop. It uses the i*probe* placed in the feedback path to be measured

cadence was used to break the feedback loop from resistive divider output to the sense amplifier input using the *iprobe* as also illustrated in Figure 4.10. The CMFB simulated DC gain was $A_{CMFB} = 10.72\ dB$, the $GBW = 20.48\ MHz$ and the phase margin $PM = 82$ °.

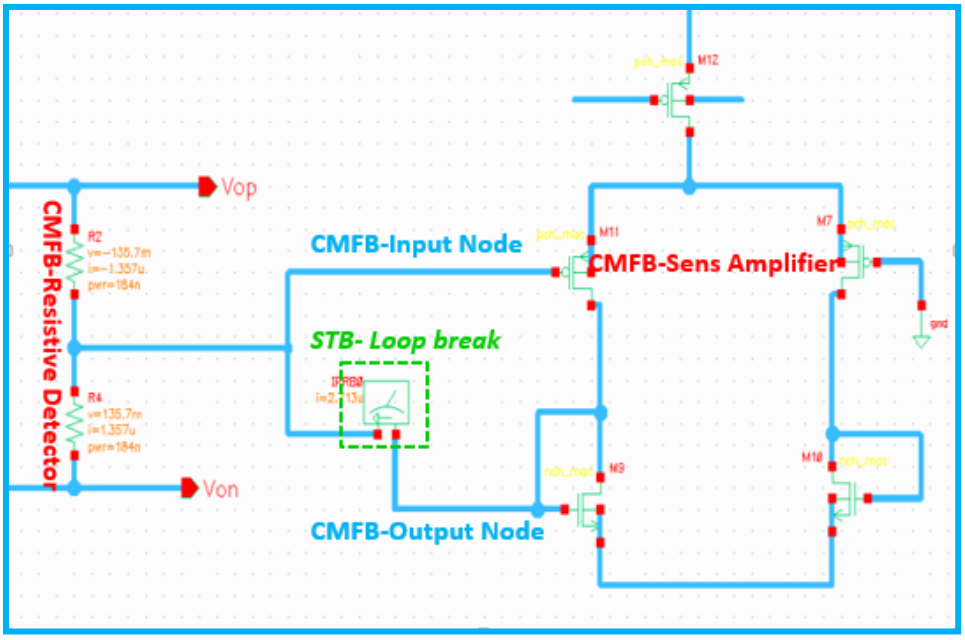



Figure 4.10: CMFB loop stability test setup

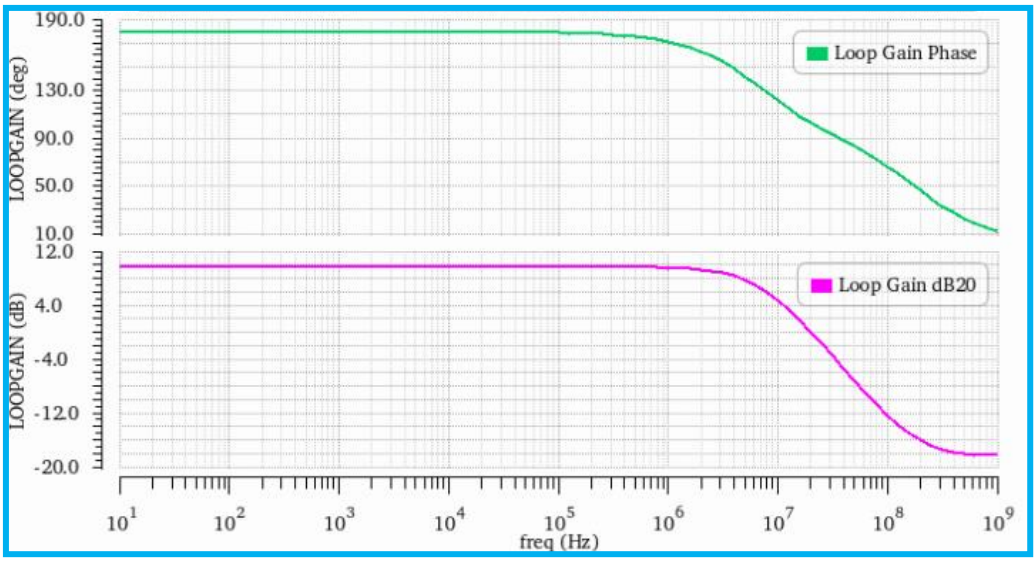



Figure 4.11: CMFB magnitude and phase response:

One very important point that worth mentioning, in the amplifier design is the dc gain non-linearity. Figure 4.12 exemplarily shows the simulated open loop gain. The maximum dc gain of *63* $dB$ is obtained at the common mode output voltage and fade rapidly as the output voltage reaches the maximum output swing voltage as illustrate by the bell blue curve. Hence for best results, one should ensure that the amplifier often operates within the correct input common mode range. This is often omitted when implementing gain boosting technique for the amplifier, while this can potentially increase the dc gain by $X$ $dB$ this amount of dc gain will only be available if the amplifier operated at the common voltage any slight offset from this value will significantly reduce this dc gain. So, generating plots as those illustrate Figure 4.12 is a great way of having a better insight of the amplifier functionality across output swing range.

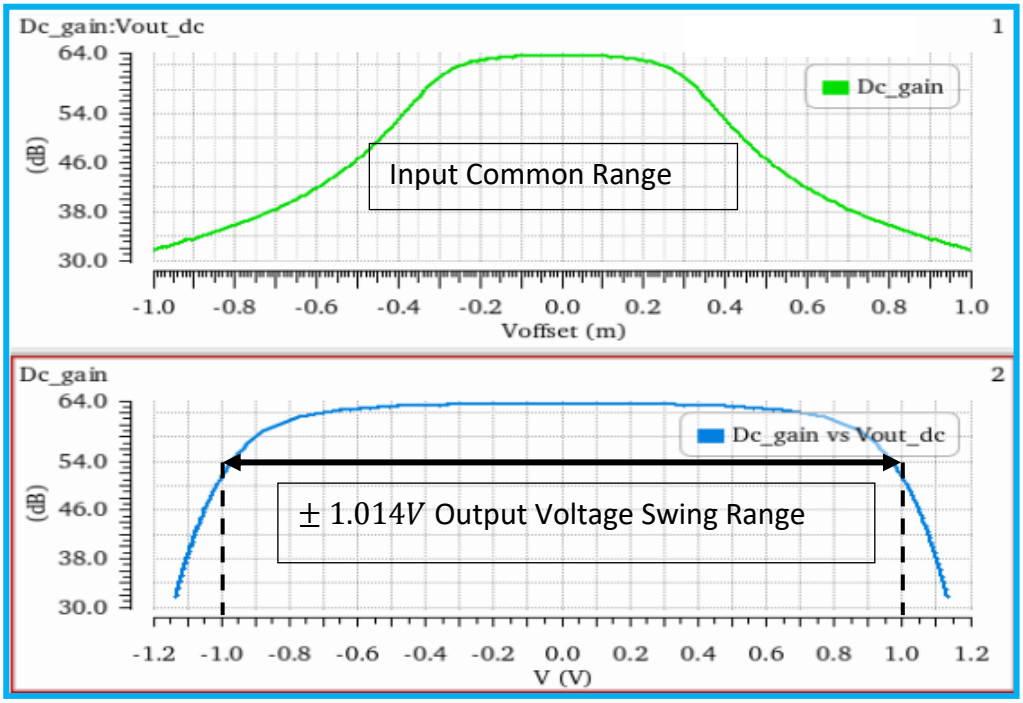



Figure 4.12: Amplifier differential gain variation over the output swing range

The designed fully differential amplifier seems to meet the low power design target specifications of the CTDSM and thus can be embedded into the first integrating stage. The same OTA topology was re-used in the subsequent stages (2-4) of the loop filter by down scaling the unity gain bandwidth frequency accordingly taking advantage of the fact that in CIIF loop filter topology, the innermost loop must have a larger unity gain bandwidth frequency than the outermost loop. Hence the amplifier $GBW$ can be approximately halved in each integration stage resulting in significant power saving. However, one of the bottlenecks of the CIFF structure is the implementation of the feedforward coefficients summation node. This will be discussed in the next section

## 4.3 Feedforward Analog Summation

As mentioned in chapter 2, CIFF loop filter topology is more power and area efficient and easier to implement than their CIFB counterparts. However, CIFF modulator requires a feedforward summer at the output of the loop filter which

can be arduous to implement especially in the analog domain due to the noisy nature of the signal being added together. With that in mind let's have look at the different types of summing network circuits commonly used to add several signal/voltages together.

### 4.3.1 Active summation

Most of the reported CTDSMs with CIFF loop filters are implemented using active summation. Figure 4.13. is a schematic of the active summing network circuit. It requires a high dc gain and bandwidth product (*GBW*) operational summing amplifier to produce a precise output voltage signal which is the sum of the individual input voltages, scaled by the corresponding resistors. The summation node will work perfectly only if the amplifier has a high gain especially at high frequencies, with low common mode input noise. The high gain requirement of the active summing amplifier can be explained as follows. The transfer function of the inverting amplifier depicted in Figure 4.13 can be expressed as:

$$\frac{V_{out}}{V_{in}}(s) = -a_i \frac{A(s)}{1 + A(s)} \tag{4.12}$$

where $a_i$ is the scaling coefficient and $A(s)$ is the amplifier transfer function.

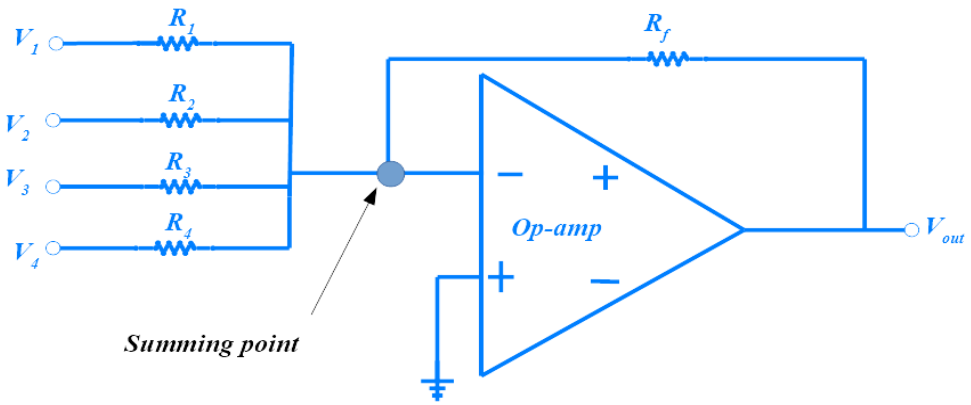



Figure 4.13: Illustration of the active feedforward summation

It can easily be shown the weighted output summing voltage is giving by:

$$-V_{out} = V_1\left(\frac{R_f}{R_1}\right) + V_2\left(\frac{R_f}{R_2}\right) + V_3\left(\frac{R_f}{R_3}\right) + V_4\left(\frac{R_f}{R_4}\right) \tag{4.13}$$

The next step is to find the input resistors values that will produce the correct loop filter output weighted voltage signal based on the loop filter feedforward coefficients. This is given by:

$$\begin{aligned} |V_{out}| &= V_1 f_1 + V_2 f_2 + V_3 f_3 + V_4 f_4 \\ &= V_1\left(\frac{R_f}{R_1}\right) + V_2\left(\frac{R_f}{R_2}\right) + V_3\left(\frac{R_f}{R_3}\right) + V_4\left(\frac{R_f}{R_4}\right) \end{aligned} \tag{4.14}$$

Hence by fixing $R_f$ to a known value (e.g. 10 kΩ), the summing node inputs resistors are:

$$R_1 = \frac{R_f}{f_1};\ R_2 = \frac{R_f}{f_2};\ R_3 = \frac{R_f}{f_3};\ R_4 = \frac{R_f}{f_4} \tag{4.15}$$

One of the bottlenecks and performance limitation of active summation in CIFF loop filter architecture is high dc gain and gain bandwidth product requirement of the summing amplifier. It's shown in [33], that the summing amplifier requires a minimum $GBW \approx 5f_s$ and gain of $A_0 = 70 \sim 80\ dB$ to ensure overall loop filter stability since the limited bandwidth of the summing amplifier acts as an additional pole in the loop filter and degrades its phase margin which defines the modulator stability. Therefore, for $MHz$ sampling rate design applications such as the current project, active summation is not the most efficient approach in terms of power and area consumption. In fact, simulation results showed that if one was to use active summation, the total power consumption of the summing block will be greater than the entire modulator power dissipation.

### 4.3.2 Passive Summer Network

This is a great alternative to overcome the limitation imposed by the active summation in CIFF loop filter topology. Passive feedforward summation is more power and area efficient than their active counterpart since it does not require a summing amplifier thus consume any active power. The two variances of passive summing are presented below.

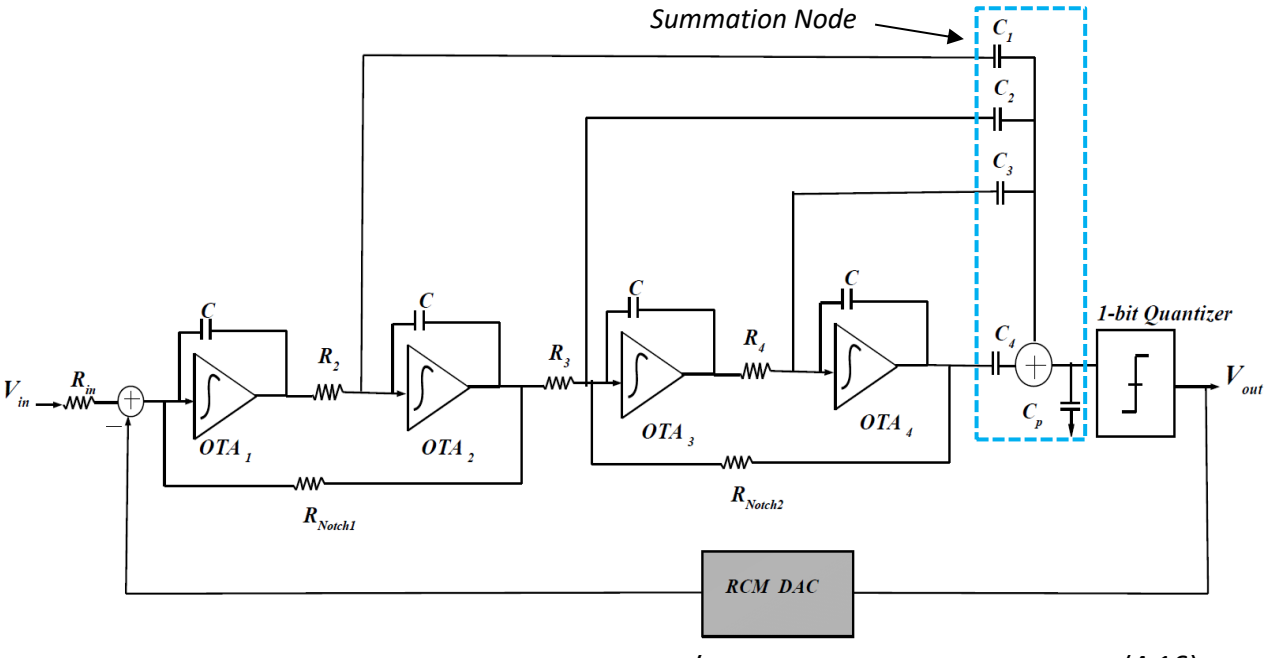



Figure 4.14: Single ended schematic of the CTDSM with feedforward capacitive summing

where $c_{Total} = c_1 + c_2 + c_3 + c_4 + c_Q + c_{Par}$. And the capacitance summation node must guarantee the following: $(f_1 + f_2 + f_3 + f_4) = 1 - (c_Q + c_{Par})/(c_{Total})$.This important criterion can be achieved by appropriately chosen the capacitances values used at the summation node.

The setup depicted in Figure 4.15 was used to test the feedforward capacitive summing around the last integrator with 4 inputs differential voltage signal $V_1 \ldots V_4$ oscillating around a common mode voltage $V_{cm} = 0.6$ with a peak to peak amplitudes respectively scaled by the capacitances $c_1 \ldots c_4$ ratio as derived in equation (4.16). It was thus observed the output voltage amplitude shows in red

(Figure 4.16) is the precise sum of the individual input voltage but does not oscillate around the common mode voltage.

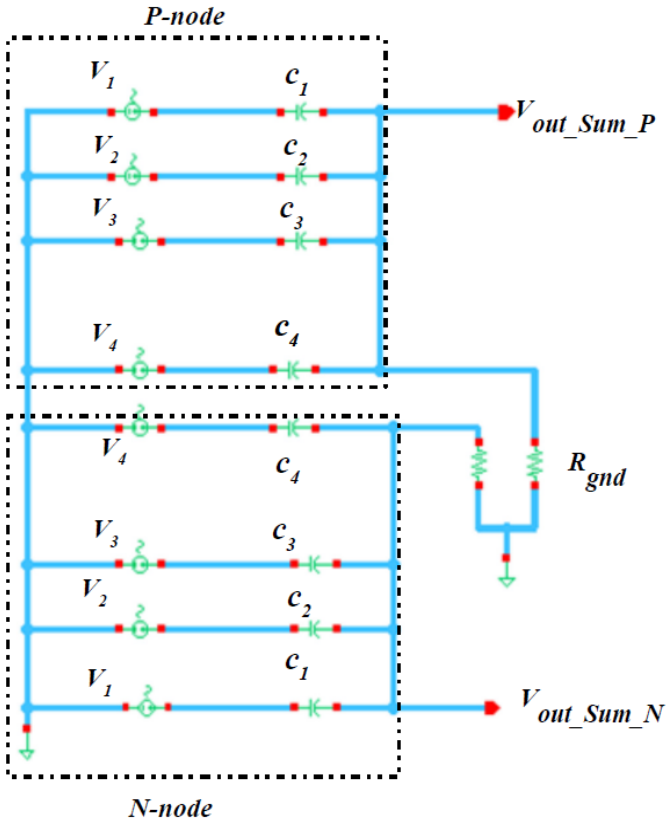



Figure 4.15: Feedforward capacitive summing test bench setup

Capacitive feedforward summation overcomes the performance limitation observe with its active counterpart. In fact, since the summation network is implemented only with passive components (capacitors), it alleviates the need for summing amplifier resulting in significant power consumption and area saving. However, capacitive summing has a high pass filter type characteristic and attenuates low frequency signals this is commonly referred to as ac coupling, illustrated in Figure 4.17.

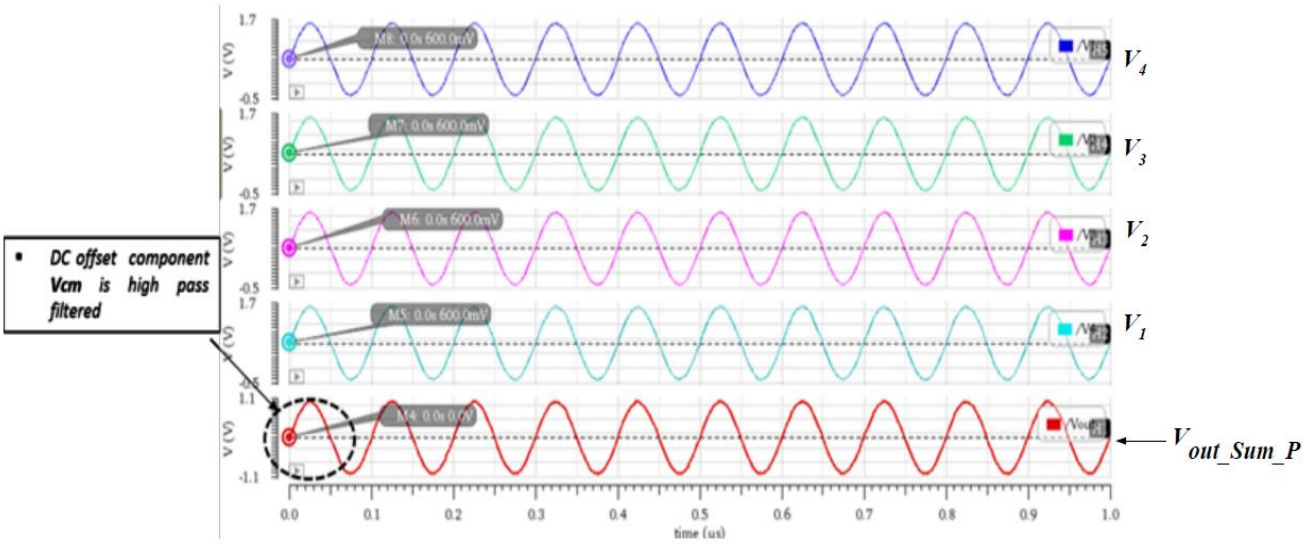



Figure 4.16: Illustration of capacitive summing showing the effect of ac coupling of ac coupling

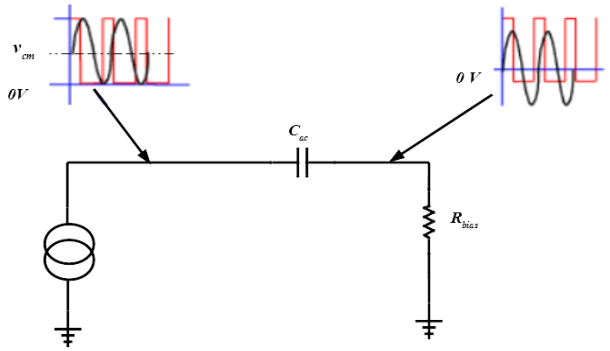



Figure 4.17: AC coupling illustration. The $C_{ac}$ capacitor blocks the dc components of the input signal.

- **AC coupling**

Capacitive coupling is when only ac component of a signal is allowed to pass through a node and the low frequencies corposants of the signal are rejected or high pass filtered. Figure 4.18 illustrates the ac coupling phenomena where clearly the dc offset has been removed by the high pass network $C_{ac}$ in series with $R_{bias}$ which has to be quite large to ensure the stability of the loop filter.

In essence, each of voltages $v_1$ … $v_4$ at the output of each integrator are ac signals oscillating around the common mode voltage, thus capacitors $c_1$ … $c_4$.at the summing node will block any dc components present within each signal. As results the quantizer will need to be dc bias at the common mode voltage $v_{vm}$. Alternatively, one's could overcome the ac coupling issue by implementing the passive summing network using resistors. This is described in the next section

#### *4.3.2.2 Feedforward resistive summing*

Passive resistive summing at the input of the quantizer was used as illustrated the modulator circuit realization as highlighted in Figure 4-1. To ease the analysis, a simplified version of the resistive summing network is only considered as shown in Figure 4.18.

Before going through the analysis of the summer network, it's important to state ***Daisy's theorem[3] which states that "sum of all voltage gains at the summing node should equal to 1"***. This assertion will be used to describe the operation of the passive resistive summer.

Figure 4.19 depicts the parallel voltage summer, the output voltage from each integrator in the loop filter is connected in parallel through resistors to the same point referred to as "summing node". At this point, each input voltage/signal will attempt to modify the total output voltage by blowing the current trough/from its. The resistors are necessaries to ensure that every input at the summing network has an influence on the total output and more importantly ensuring that *Daisy's theorem* holds at this node. The choice of the resistor value is based on the loop filter feedforwards coefficients and the derivation of presented below.

Looking to each input, the summing node can be regarded as a voltage divider composed by two sets of resistances: input resistances $R_1$ … $R_4$ and the equivalence remaining resistances $\{(R_1 \,//\, R_2 \,//\, R_3)\}$ and $\{(R_2 \,//\, R_3 \,//\, R_4),\ (R_1 \,//\, R_3 \,//\, R_4),(R_1 \,//\, R_2 \,//\, R_4),$

[3]Daisy's Theorem states that the sum of ALL voltage gains must be equal to one

From *Daisy's theorem,* the sum output voltage is given by:

$$V_{out} = \alpha_1 V_1 + \alpha_2 V_2 + \alpha_3 V_3 + \alpha_4 V_4 \ and \ \alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = 1 \quad (4.20)$$

where $\alpha_1 \dots \alpha_4$ represent the input voltage scaling coefficients. These will correspond to the normalized version of the loop filter feedforward coefficients ($f_1 \dots f_4$) mentioned previously and which value is listed in Table 4.2. Hence voltage scaling the coefficients are derived as:

$$\alpha_1 = \overline{f_1} = \frac{V_{out}}{V_1} = \frac{(R_2 \,//\, R_3 \,//\, R_4)}{(R_2 \,//\, R_3 \,//\, R_4) + R_1}$$

$$\alpha_2 = \overline{f_2} = \frac{V_{out}}{V_2} = \frac{(R_1 \,//\, R_3 \,//\, R_4)}{(R_1 \,//\, R_3 \,//\, R_4) + R_2}$$

$$\alpha_3 = \overline{f_3} = \frac{V_{out}}{V_3} = \frac{(R_1 \,//\, R_2 \,//\, R_4)}{(R_1 \,//\, R_2 \,//\, R_4) + R_3}$$

$$\alpha_4 = \overline{f_4} = \frac{V_{out}}{V_4} = \frac{(R_1 \,//\, R_2 \,//\, R_3)}{(R_1 \,//\, R_2 \,//\, R_3) + R_4}$$

And normalized feedforward coefficients are:

$$\overline{f_1} = \frac{f_1}{f_T};\ \overline{f_2} = \frac{f_2}{f_T};\ \overline{f_3} = \frac{f_3}{f_T};\ \overline{f_4} = \frac{f_2}{f_T};$$

$$f_T = f_1 + f_2 + f_3 + f_4$$

$$(\ original\ loop\ filter\ feedforward\ coefficients\ )$$

The passive resistive feedforward was implemented and a similar setup as the one used in section 4.3.2.1 with the capacitive summer was used to test the summer network. The simulation results are illustrated in Figure 4.19.

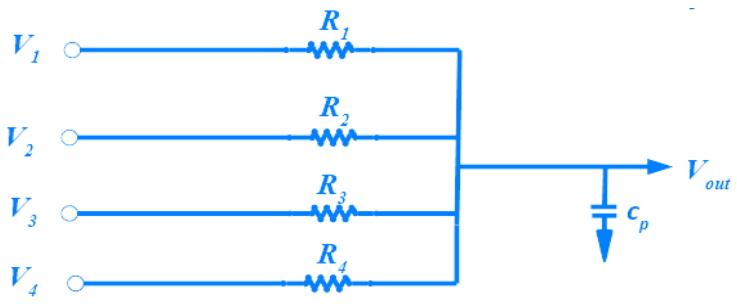



Figure 4.18: Passive Resistive Summing Network

Clearly, resistive passive summing seems to overcome the AC coupling limitation found on its capacitive counterpart since the output voltage (red curve in Figure 4.19) is the sum of each integrator output signals and oscillates around the reference common mode voltage. Moreover, it's highly efficient in terms of area and power and does not require any re-biasing of the quantizer.

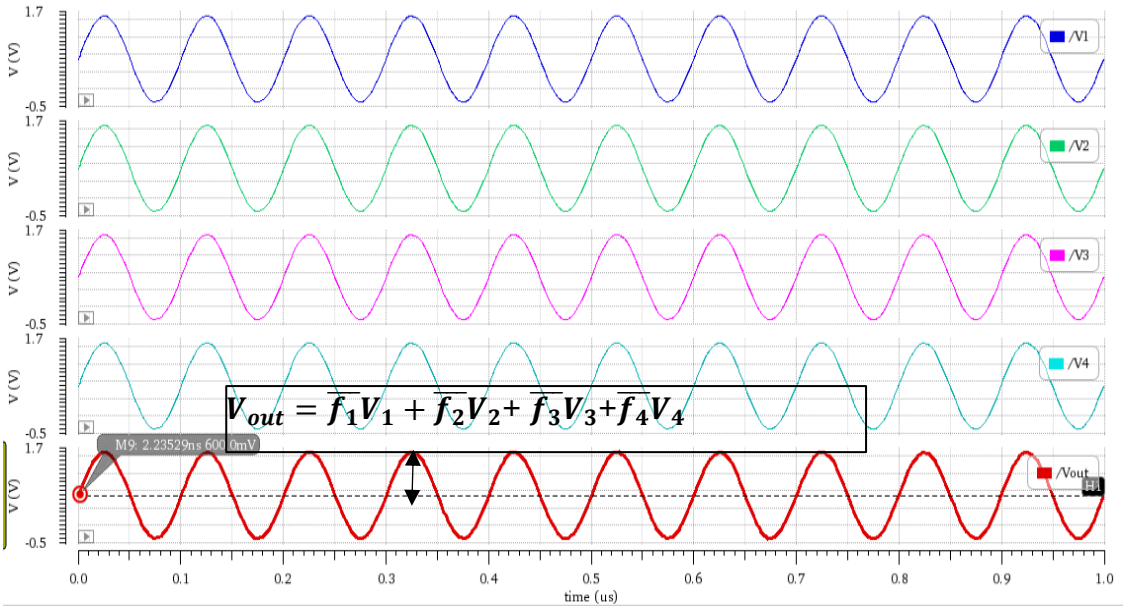



Figure 4.19: Illustration of the feedforward passive resistive summing

## 4.4 Quantizer: Strong Arm Comparator

The quantizer is used to converter the loop filter output to digital bits-stream is another non-linear element in CTDSM. In order to achieve a low power, small layout area design a single bit quantizer topology has been adopted as it offers an inherent linear feedback DAC and does not require DEM or calibration circuitry found in multibit design, moreover single quantizer reduced the overall ELD in the feedback path and lastly single quantizer results in better energy-efficiency and reduced area design compared to multibit quantizer.[34]

In the current CTDSM architecture implementation, the quantizer should complete the quantization of the loop filter output (assumed to be voltage) in half a clock cycle (approx. $21\ ns$) to avoid ELD. This requirement was considered in the choice of quantizer architecture. The adopted Strom Arm Latch comparator shown in Figure 4.20 was adopted due to its fast operation with a decision time of $450\ ps$. Other comparator errors such as offset, hysteresis and nonlinearities were not addressed because they are usually attenuated, and noise shaped by the loop filter. Nevertheless, quantizer especially multibit implementation can still be responsible of performance degradation in a CTDSM due to timing induced errors such as propagation delay within the quantizer.

The strong-arm latch comparator consists of the following: an integrating stage, a latch stage, and a tail current source. Note in the latch stage the current source was sized slightly large to achieve fast latching. The comparator operates as follows [35]:

- Reset phase $\boldsymbol{Clk = 0}$

When the clock signal is low, the P-mos devices $M_7$ & $M_5$ are ON in triode. This respectively pull the positive and negative integrating stage output voltage $v_{op}$ & $v_{on}$ to the supply.

- Regeneration phase $\boldsymbol{Clk = 1}$

When the clock signal goes high, the tail current transistor $M_1$ is turned ON. Subsequently $M_2$ & $M_3$ turn ON initially in saturation. And $v_{op}$ & $v_{on}$ nodes start discharging from $V_{dd}$ to ground. Note that these nodes are discharged to ground at different rates based on the applied input signal. As a result, there is an imbalance voltage created between $M_2$ & $M_3$, when the voltage at the input of the SR latch $v_{op}$ $or$ ( $v_{on}$) goes below $V_{dd} - V_{th,M3}$ the P-mos transistors $M_{12}$ & $M_{13}$ turn ON. And nod e $f_p$ & $f_{on}$ are no longer discharging to ground and the N-mos transistors $M_6$ & $M_9$ are turned OFF. Hence $f_p$ & $f_{on}$ begin to be pulled toward $V_{dd}$ at different and regeneration phases starts. Further details on the strong arm latch comparator operation are provided in [35]

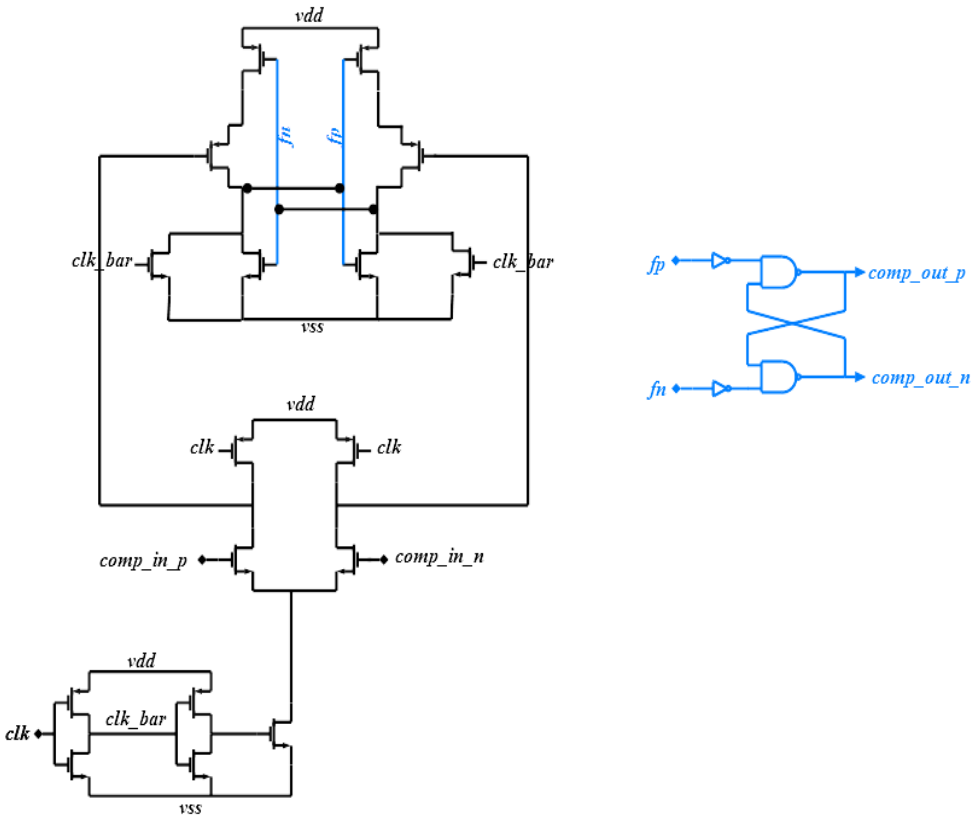



Figure 4.20: Strong Arm Latch Comparator used in the single bit quantizer

## 4.5 Return to Common Mode DAC

The feedback DAC must meet the matching, low noise, linearity along with low power area consumption requirement of the CTDSM. The DAC element can be implemented in various ways such as: current steering DACs, switched capacitive DACs, and resistive DACs. Each DACs architecture has its one merit and trade-off has examined in[29] The return to common mode DAC (RCM) was used in this CTDSM architecture due to its inherent immunity to ISI and reduced sensitivity to ELD (cf chapter3). The RCM DAC was implemented using switched resistive DAC topology because it tends to be very power efficient and it offers low input referred thermal noise contribution than current steering DAC [29]. Moreover, as discussed in chapter 3, RZ DAC is inherently linear with reduced distortion caused by nonlinearities in the loop filter when compared to NRZ DAC. The resistive DAC offers an additional benefit in that it has voltage to current conversion via a feedback resistor $R_{DAC}$ which is the same as the first integrating stage input resistance $R_{int1}$. Since the value these two resistances can be perfectly matched the gain of the feedback DAC path will equal that of the input signal path and potential errors due to non-ideal amplify virtual ground will be reduced [17].

Figure 4.21a shows how the switch resistive DAC is connected to the first integrator. Let's denote by $D_{out}$ the quantizer output bitstream (thermometer code). Each thermometer code bit drives the DAC resistor $R_{DAC}$ and depending on the bitstream state (i.e. $D_{out} = 0\ or\ D_{out} = 1$) the DAC resistor is connected to the positive or negative references voltages ($V_{ref,p}\ or\ V_{ref,n}$) The bitstream state is held for half the clock period and during the remaining half clock cycle ($tlck_{DAC}$) the DAC resistor is connected to the common mode reference voltage $V_{cm}$, causing the feedback quantity (assumed to be current without loss of generality with a peak value $i_{max} = I_o = V_{dd}/\ 2R_{DAC}$) to return to common mode for the latter half clock period this results in RCM DAC pulse shape.

The feedback DAC current waveforms are illustrated in Figure 4.21b; the main observation is that there is an error in the amount of current being fed back in the loop filter denoted by $i_{err}$ from the supposed ideal value. This is due to the ON-resistance of the DAC switches and their parasitic capacitance $c_p$. Hence the

switches in the DAC should be carefully designed taking into account their non-zero switching resistance. However due to the occurrence of two transition per clock cycle, the RCM DAC type pulse ensures that a constant or fixed amount of current is fed back in the modulator at every clock period thus attenuating the impact of the error current $i_{err}$ But the price paid for this is the increased sensitivity clock jitter (cf. chapter 3). That said, by incorporating an FIR filter in the feedback path one could reduce the adverse effects of jitter on the modulator performance as shown in section 4.6.

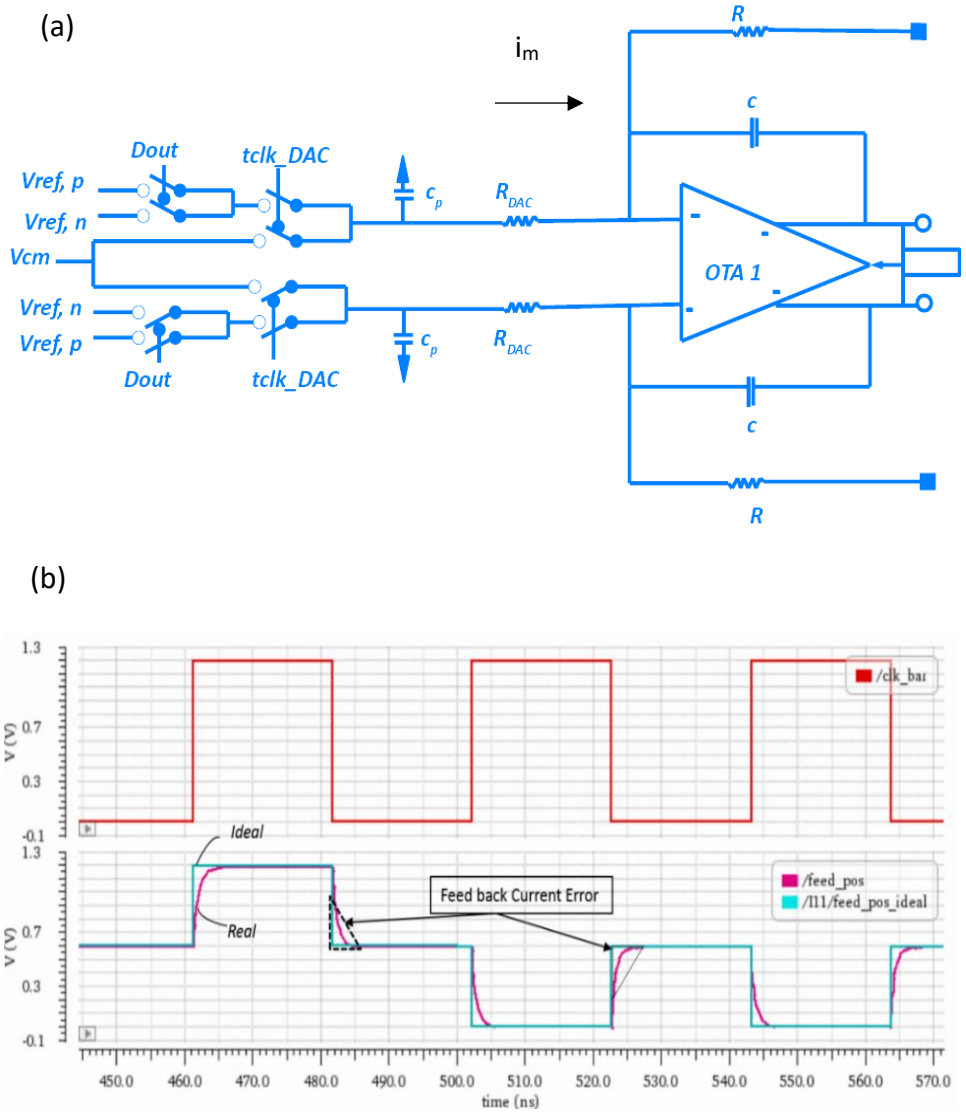



Figure 4.21: (a) Single bit stitched resistor return to common mode DAC.

(b) Current waveform

- **Switch ON-resistance**

The DAC switches are implemented as CMOS transmission gate by connecting an N-mos devices switch in parallel with P-mos devices switch (Figure 4.22) in order to be able to pass both positive and negative reference voltage based on the output bitstream. The most import design specification is its ON-resistance which is the parallel combination of the On-resistance of the P-mos and N-mos stitches ($. i. e.\ R_{ON} = r_{ON,p} II\ r_{ON,n}$). The ON-resistance value can be reduced by increasing the aspect ratio (W/L) of both P-mos and N-mos transistors. However, this increases the transistor area and consequently their corresponding drain/source capacitances, with subsequent impact on switching operation. Therefore, when sizing the T-gate switch, one should ensure that the ON-resistance of both P-mos device and N-mos device are approximately equal ($r_{ON,p} \approx r_{ON,n}$) as also illustrated in Figure 4.22

Moreover, since ON-resistance peak at the circuit dc bias voltage operating point ($V_{cm}$), the sizing of the T-gate transistors needs to be methodically adjusted bearing in mind that making the length of the device to large will result in a slower switching operation compromising the DAC functionality. On the other hand, using minimum channel length devices will increase the ON-resistance causing harmonic distortion. Therefore, the designer must find the optimal device's size (design trade-off).

While CTDSM with an RCM DAC offers all the above-mentioned advantages, unfortunately, it is particularly sensitive clock jitter. However, embedding a FIR filter in the feedback reduces the impact of clock jitter. The circuit implementation of the FIR filter is presented in the next section.

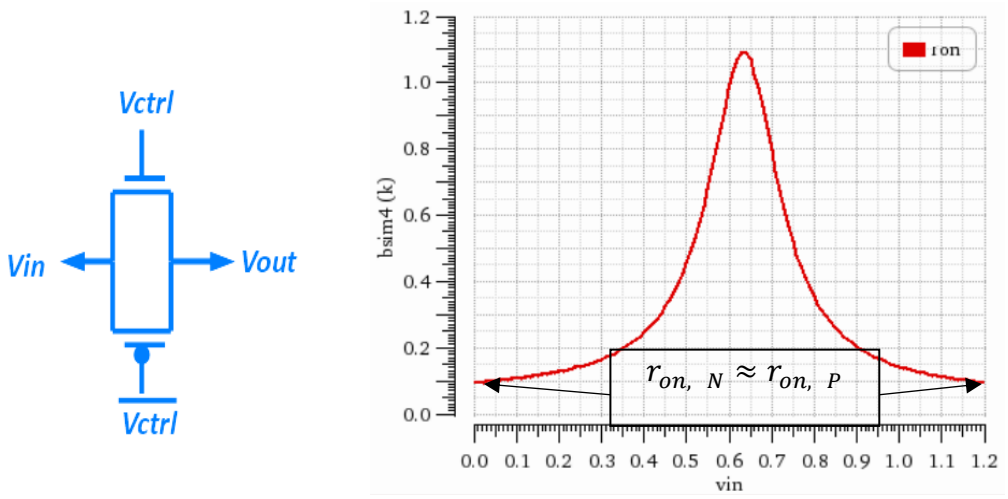



Figure 4.22: Transmission gate On-resistance Illustration

## 4.6 FIR Return to Common Mode DAC

Incorporating an FIR filter in the feedback path somewhat addresses clock jitter limitation often associates with RZ DAC pulse type. The operation principle of the FIR RZ DAC was described in chapter 3, this section will present that actual circuit realization of the FIR filter.

The FIR filter is implemented in a semi-digital fashion using a resistor and d-type latch as shown in Figure 4.23. Recalling the transfer function of the four taps FIR $F(Z) = a_0 + a_1Z^{-1} + a_2Z^{-2} + a_3Z^{-3}$, the filter taps coefficient $a_0 \dots a_4$ are realized via resistors $R_0 \dots R_4$ ( to ease the implementation, the four taps weight all equal to 0.25) and the period delay $Z^{-1}$ is materialized by the d-latch that acts like a shift register.

The FIR filter operates as follows: quantizer output bitstream $V[n]$ is fed into d-latch (shift register) that holds the bit status for one clock period then is shorten to the resistor for the associated weight. Put differently, one can think of the FIR filter in time domain as a single bit feedback DAC which average adjacent output bitstream sample (e.g.$V[n], V[n-1]\ V[n-2]$) and reduce the step size from sample to sample, thus mimicking a multi-bit feedback (multibit quantizer) operation.

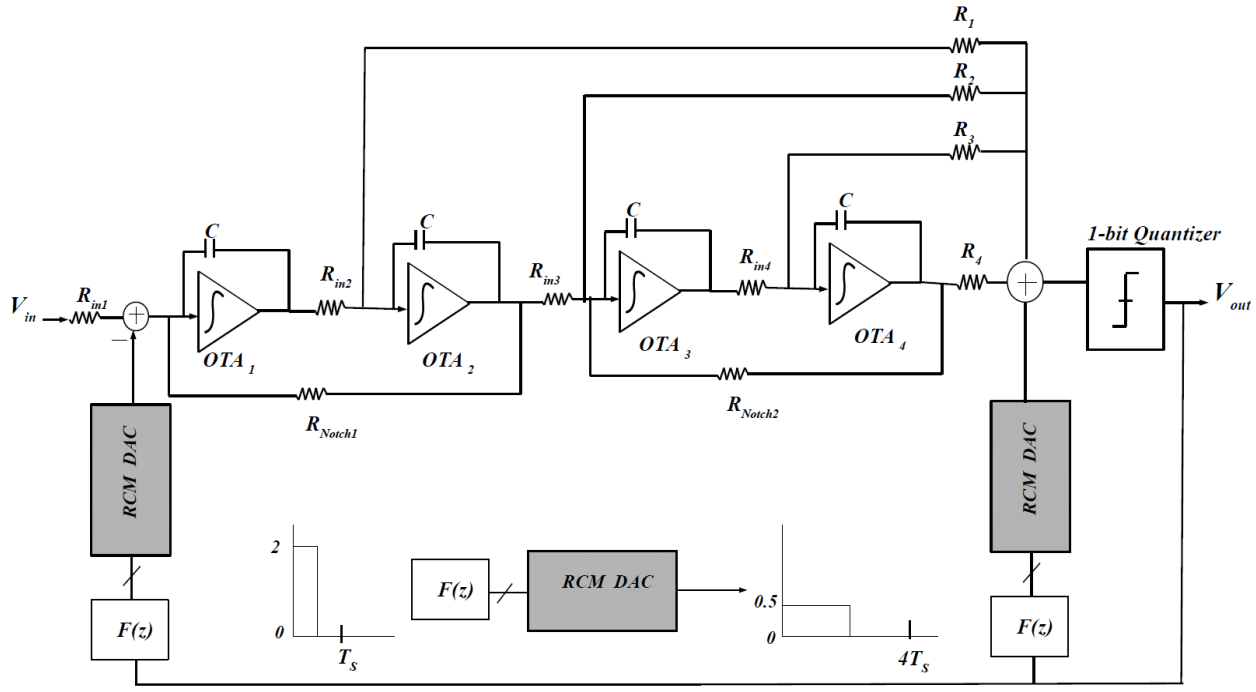



Figure 4.23: Simplified Single ended schematic of the CTDSM with a FIR filter in the feedback path.

## Summary

This chapter presented the circuit level realization in CMOS 65nm process of the 4th order, single bit CTDSM sampling at *25MHz* using *a 1.2V* supply. A details description of the modulator main building was provided. Also, noise analysis of the design was derived and its influence on the achievable SNR was discussed.

The integrating stage implementation uses a two stage fully differential Miller OTA topology. It was shown that this amplifier architecture allows to meet the DC gain, bandwidth and linearity requirements of the CTDSM. Additionally, it was also shown that one of bottleneck of CIFF loop filter topology is the implementation of feedforward coefficients summation. In this regard, passive and active summation were analysed. The active analog summation is area and power hungry, hence this work opted for the passive resistive summation due to its flexibility and ease of implementation when compare to the capacity summer counter that suffer from AC coupling as described in section 4.3.2. This work uses a single bit quantizer that was implemented via strong arm comparator. Finally, the return to common mode

resistive DAC used in the feedback paths was discussed along its the advantages and limitations. It was shown that the switch in feedback DAC can be particularly sensitive to clock jitter, one approach proposed to reduce this jitter impact was to incorporate a FIR in the feedback paths.

The simulation results of the circuit level relegalization of the $4^{th}$ order CTDSM are presented in chapter 5.

# Chapter 5

## CTDSM Simulation Results

This chapter presents the simulation results of the proposed 4th order CTDSM that was implemented in Tsmc 65nm analog CMOS technology showed in Figure4.1 chapter 4. The nominal supply voltage is 1.2 V. With the fully differential realization, the analog ground is chosen to be $V_{cm} = 0.6\,V$ to maximize the integrator's swings. Furthermore, the positive and negative reference voltages ($V_{ref,p}$ $V_{ref,n}$) are set to ($1.2\,V$ $and$ $0\,V$) respectively. All the simulation results present in this chapter were obtained from the 4th order CTDSM schematic shown in Figure 4.1. The modulator was designed in Cadence Virtuoso and Spectre simulator was used to test the design functionality. Firstly, we focus on the modulator maximum input amplitude (MSA) and ELD simulation results. Secondly, the CTDSM single tone test result is presented. Thirdly the loop filter anti-aliasing filter properties of the simulated circuit will be presented followed by the modulator the dynamic range and transient noise performances.

### 5.1 Maximum Stable Amplitude

This is the largest input signal level the modulator can tolerate for stable operation. To determine the modulator MSA we use similar methods as described in [22]: we applied a low –frequency ( $57KHz$) input sine wave whose amplitude was stepped and we ran the simulation for hundreds of thousands clock cycles. For each amplitude, the in-band SQNR was computed. We keep increasing the amplitude and repeated the simulation and calculation until the maximum amplitude for which the modulator remain stable was found. Figure 5.6 in section 5.5 shows a

plot of the SQNR as a function of the input amplitude. From this graph, it's apparent that the MSA is about $-10.5\ dBFS\ or\ 0.36\ V$.

While this method of estimating the MSA give a satisfactory result, it should be noted that it is demanding in simulation time as long simulation has to be run for each amplitude. An alternative technique used in [37] is to excite the modulator with a stepped ramp over millions of clock period and record the quantizer input magnitude until the modulator becomes unstable.

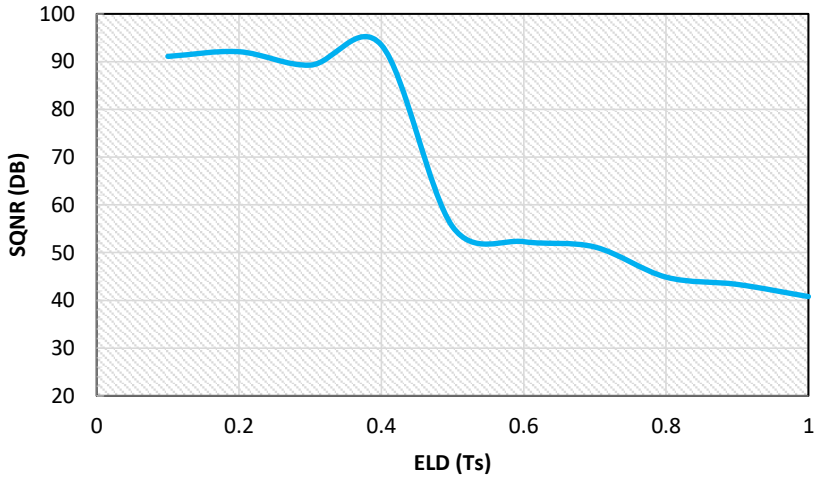



Figure 5-1: CTDSM SQNR vs Excess Loop delay (ELD)

## 5.2 ELD vs SNR

Local ELD was added in the feedback loop to account for the delay between the quantizer decision instant and the DAC output switching time as described in chapter 3. Hoes does one estimate the maximum amount of ELD that the modulator can tolerate? To answer this question a parametric analysis was performed where we varied the amount of local ELD being introduced and computed the corresponding output SNR of the modulator. Figure 5.1 shows the simulation results that illustrate the effect of ELD on the proposed $4^{th}$ order CTDSM. It's apparent that the current architecture can tolerate up to $0.4\ T_s$ local loop delay. Any ELD beyond this value will cause the modulator to become unstable.

Moreover, performing this parametric analysis was very useful in that it allows us to identify the root cause of the performance degradation that was observed during the simulation circuit level implementation of the proposed CTDSM. As previously mentioned a top down design methodology was adopted in this project so initially, we attempted to replicate the system level modulator topology described in chapter 3 with *0.5* $T_s$ ELD. Clearly using that amount of local ELD in the circuit level counterpart degrades the modulator in-band SQNR. Therefore, in the circuit implementation of the proposed CTDSM, we used $0.25\ T_s$ local ELD since it offers the optimum SQNR

## 5.3 Single tone test

Figure 5.2 shows the $2^{14}$ power spectral density of the 4th order CTDSM output for a *57* $KHz$ signal tone with a *0.72* $V_{PK-PK}$ and third harmonics distortion which mainly occurs as a results of non-linearity of the voltage to current (V/I) conversion element at the input of the loop filter which in case of the CTDSM correspond to the input resistance $R_{in}$ and feedback DAC resistance $R_{DAC}$ .

The in-band flatness is due to the noise shaping characteristic of CTDSM. As described in section 2.1.1, the noise shaping will be effective from dc to $f_{BW}$ while next to the bandwidth the noise will rapidly increase. The addition of local resonators around the integrating stage allows the spreading of the NTF zero over the signal band. In order to improve the *IBN* and DR the *NTZ* zero was optimized fall close signal bandwidth $f_{BW}$ by tuning the resistor value in the feedback resonators. (note there is design trade-off between performance gain and NTF zero placement optimization)

Clearly, from Figure 5.2, the third harmonic is the main dominant non-linearity with about $HD3 = -108.4\ dBFS$. Due to the fully differential nature of the implemented CTDSM as explained in [11], the modulator should have no even order harmonics which explains why the second harmonic $(HD3)$ is not present on the output spectrum shown in Figure 5.2.The simulated modulator has a spurious-free dynamic range $SFDR \approx 98.7\ dBFS$ which meets the radio receiver linearity requirement mentioned in chapter2.

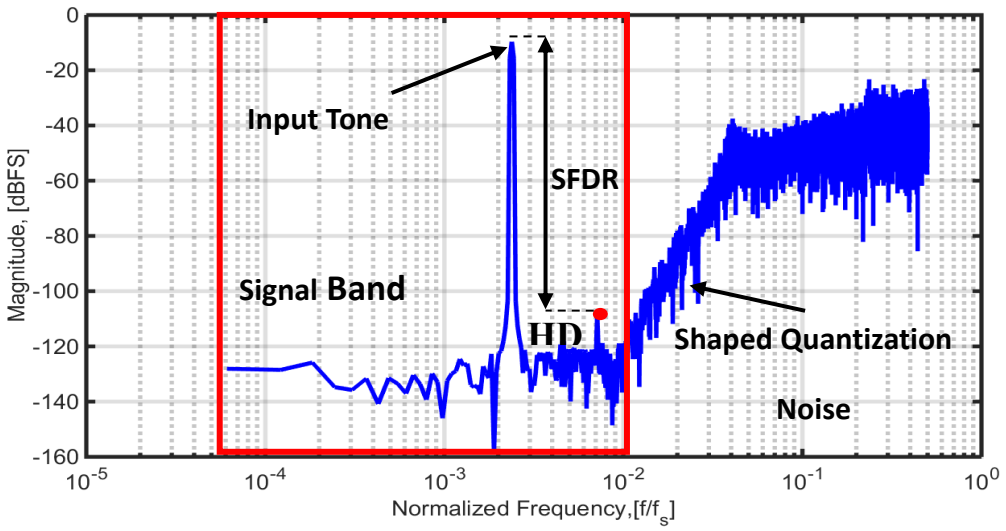



Figure 5.2: Simulated CTDSM output PSD for 57KHz input tone.

CTDSMs performances are usually measured from theirs power spectrum estimation, but it worth mentioning how this spectrum is obtained i.e. the type of signal processing analysis applied on the modulator output bitstream since this point often not specified when sharing sigma delta modulator performance results in the literature. The Fast Fourier Transform FFT is a widely used method to estimate CTDSM power spectral density. However, in order to avoid misleading results, it's important to clarify the type of windowing, scaling and averaging is applied to the modulator output data during the FFT analysis. Without going into too many details on FFT mathematical background which can be found in various textbooks, we used a Hann window periodograms[4] with $N = 16384$ points to simulate the CTDSM as it offers superior protection against signal leakage which sometimes reduced the effective modulator output SNR. The input tone frequency was chosen to be $kf_s/N$ where $k$ should ideally be an even number. In the simulation results presented in Figure 5.2 a value of $k = 39$ was used which

[4] Method of estimating the PSD of a process via the discrete-time Fourier transform of the samples of the process (usually done on a grid with an FFT) and appropriately scale the magnitude squared of the result

coupled with the Hann window minimized the power leakage of the input sine's signal.

## 5.4 Loop Filter Anti-Aliasing Performance

Due to the sampling process in CTDSM, any input signal with frequency $f_{in}$ equal to multiple of the sampling frequency $f_s$ can potential be reflected in the modulator bandwidth. This problem is usually referred to as aliasing and this is the real bottleneck in radio receiver application. A key attribute of a CTDSM is its inherent anti-aliasing filtering offered by the loop filter, thus the STF should elicit or have notches around multiples of $f_s$ to suppress the alias component. The simulated modulator signal transfer function (STF) is shown in Figure 5.3. The modulator STF has a low pass filter characteristic and has nulls at non-zero integral multiple of the sampling frequency $f_s$ therefore potential alias tone will be attenuated. Furthermore, the STF exhibits a peaking at $350\ kHz$ this inherent to CIFF loop filter topology if not address this could amplify any nearby interferers sitting at this frequency thus compromising the modulator AAF properties. The adopted approach to reduce this out-band peaking was to add a direct feedforward from the input stage to the feedforward summer. More importantly, the STF shows a flat in-band response which good for AAF.

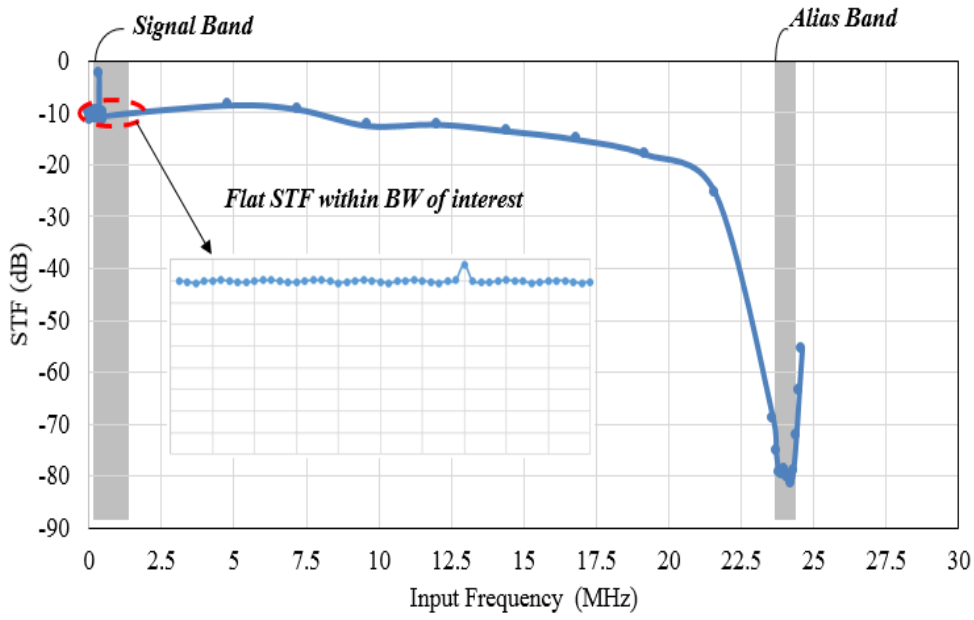



Figure 5.3: Simulated Modulator Signal Transfer Function

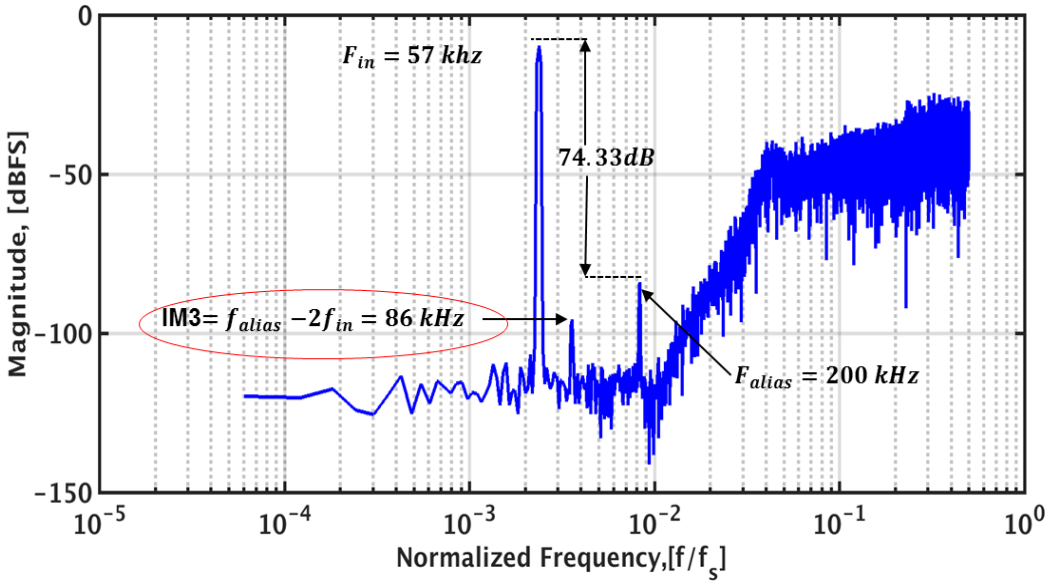



Figure 5.4: Simulated Modulator Anti-Aliasing Test

The amount of alias suppression that the current CTDSM implementation can achieve was investigated by running an alias test with the following set up:

- The modulator was excited with an input sine with tone located at $F_{in} = 57\ kHz$
- The alias signal tone was placed at $F_{alias} = 24.2\ MHz$
- $\boldsymbol{Expected\ alias\ f_{2A} = |f_s - F_{alias}| = |24\ MHz - 24.2\ MHz| = 200\ kHz}$

The simulated output spectrum in Figure 5.4 shows the presence of an alias signal around $200\ kHz$ which is attenuated by $74\ dB$ ( $P(f_{in}) - P(f_{2A}) = 74.33\ dB$).The higher order out of bandwidth harmonic distortions and alias signal which are not filtered by the NTF nor attenuated by the SFT will be removed or attenuated by the decimator filter (not covered in this thesis) in the digital domain.

Finally intermodulation test was performed to test the receiver's ability of receiving a desired signal in the presence of unwanted signal by simulating the modulator with two input signals with tones located at $F_{in1} = 160\ kHz\ and\ F_{in2} = 120\ kHz$, thus one would expected the third intermodulation tone at $\boldsymbol{IM3 = 2(f_{in1}) - f_{in2} = 200kHz}$ **&** $\boldsymbol{IM2 = 2(f_{in2}) - f_{in1} = 80kHz}$. The two tones intermodulation test simulation result from Figure 5.5 shows that the modulator has an $94\ dB$ attenuation of the IM3 tone at $200\ kHz$.

Overall the modulator exhibits good linear behaviour which very crucial for IoT radio receiver.

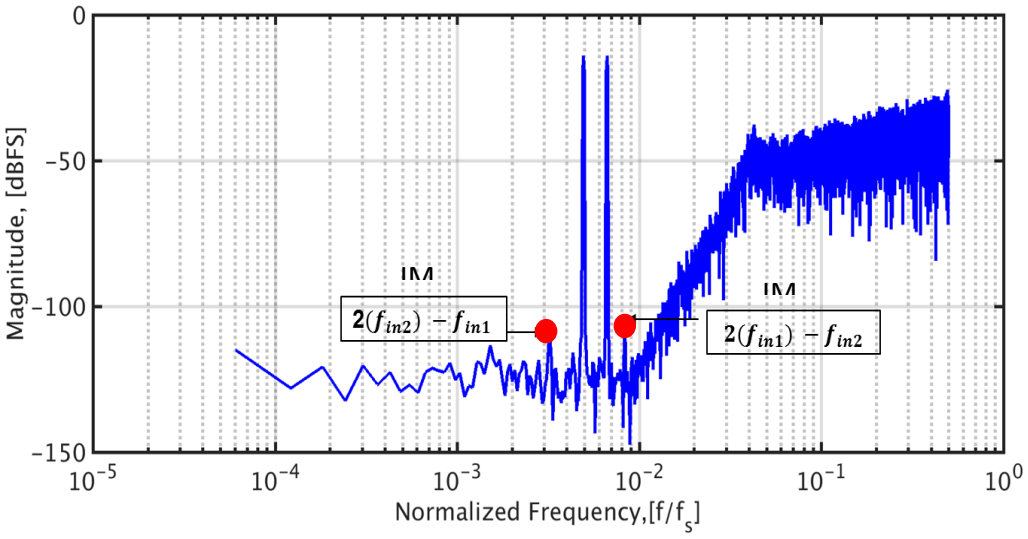



Figure 5.5: Simulated Modulator Intermodulation Distortion Test

## DR and Noise Simulation Results

- **Dynamic range**

The simulation results in Figure 5.6 shows that the modulator can achieve a maximum SNR of $93\ dB$ for an input amplitude (single ended) of $-10.5\ dBFS$. The corresponding $DR\ > 90\ dB$ meets the high dynamic range requirement for an ADC in low power IoT radio receiver architecture.

- **Transient Noise Simulation**

To assess the influence of devices on circuit behaviour, a small signal approximation of the noise is most commonly used with the assumption that these device noise contributions are small enough and does not alter the circuit operating point. Spectre simulator (in Cadence Virtuoso) offers a transient noise analysis that was used to evaluate the effect of devices noise on the 4$^{th}$ order CTDSM. Transient noise can be thought of as injecting random Gaussian noise at each sampling instant. Details on the noise modelling can be found in [38].

Figure 5.7 shows the transient noise simulation result; the main observation is that there is about $9\ dB$ lost in SNR when the transient noise is enabled. However, the

modulator still meets the DR and linearity (reduced harmonics distortion) requirement of an ADC in IoT radio receiver.

Last point to note is that, there are various available noise analysis tool such the Analog Fast Spice (AFS) simulator from Mentor Graphic, when deciding to use one this simulator it's very important to understand how with is being modelled as this could lead to potential misleading results. For instance, some discrepancy has been observed between transient simulation results obtained from AFS this was due to a burg in the device noise modelling algorithm with AFS. Therefore, it's often good to use Spectre since it's the widely adopted noise simulation tool.

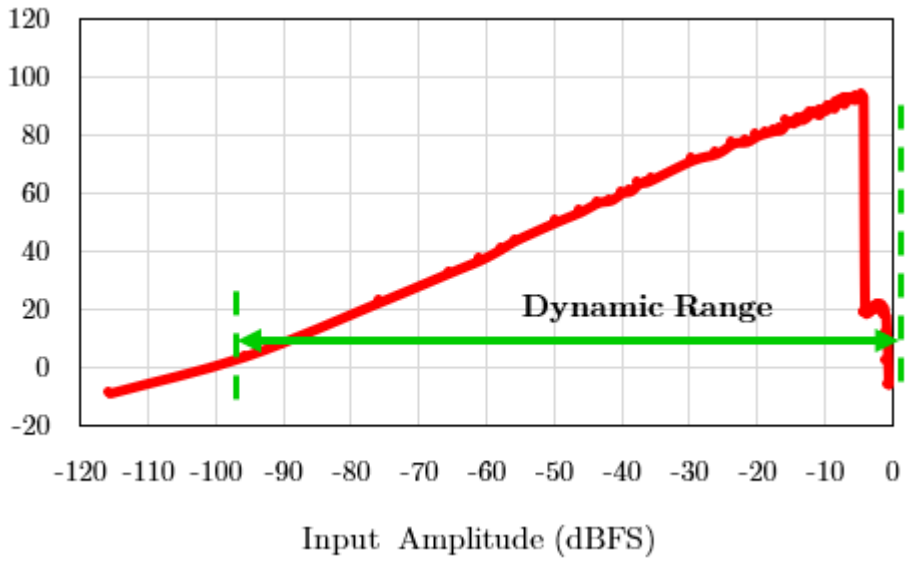



Figure 5-4: Modulator Output SNR vs. Input Amplitude (fin=57 kHz).

A summary of the simulated modulator performance is given in Table 5.1. From Table 5.1 the designed modulator consumes only *1.407 $mW$* from a *1.2 $V$* supply. The figure of merit for the designed CTDSM is $\text{FoM}_S = 169dB$. The peak SNR of *84.8 $dB$* was achieved under the influence of transient noise. This is about *2 $dB$* less than the theoretical expectation from the noise budget in section.4.1.1. The main reason could be the input referral noise from the second stage RC integrator which was not considered in noise budget.

The total power consumption breaks down across the CTDSM building block is illustrate on pie chart below. The loop filter is main contributor of the entire power dissipation. As expected, the first input stage input is the most power-hungry block consuming about *33%* of the overall power. However, there several suggestions on how one could further reduce the power consumption and hence improve the modulator figure of merit. These power optimization techniques will be discussed in chapter 6.

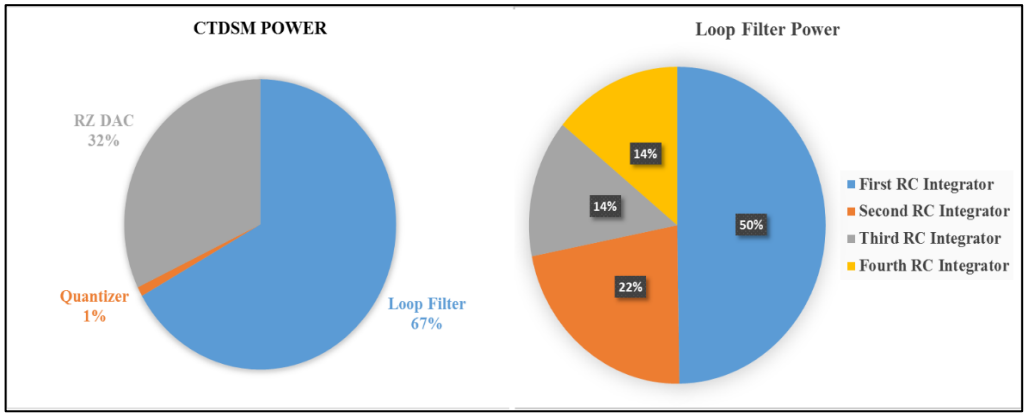



Figure 5.8: Distribution of the Power Consumption of the Modulator

Table 5-1: Modulator Performance Summary

| | VALUES | UNIT |
|---|---|---|
| $V_{DD}$ Supply Voltage | 1.2 | V |
| $f_B$ Signal Bandwidth | 250 | kHz |
| $f_S$ Sampling Frequency | 24 | MHz |
| MSA Maximal Stable Input Amplitude | 0.36 | V |
| DR Dynamic Range | 93 | dB |
| IBN In-Band Noise Floor | -109 | dBFS |

| | | |
|---|---|---|
| Spurs Free Dynamic Range for a 57 kHz input tone and third harmonic in-band distortion | 98.7 | dBFS |
| Alias Attenuation | 74.33 | dBFS |
| SNQR Peak Signal to noise ratio | 94 | dBFS |
| $SNR_{Trans}$ Peak Signal to noise ratio with transient noise | 84.8 | dBFS |
| Pwr Average Power Consumption | 1.407 | mW |
| $FoM_S$ Schreier Figure of Merit | 169 | dB |
| Technology | 65 nm CMOS process | |

## Summary

This chapter presented the simulations results of the proposed 4$^{th}$ order CTDSM that was implemented in Tsmc 65nm analog CMOS technology 1.2 V supply. The designed CTDSM operates at *25MHz* and has a bandwidth of *250kHz.* The modular achieved a peak SNR of 84dB; this is 5dB lower when compared system level simulation in chapter 3. The discrepancy is due to the fact the thermal noise was not model in system level simulation in chapter 3. Also, because this work didn't take into account noise contribution of each integrator as it was assumed that the input referred thermal noise of the first integrating stage was the dominant noise contributor in the noise analysis. For future improvement one's should consider all the noise sources. Moreover, the results achieved with the current CTDSM implementation meet the design specification target by this project in terms of dynamic range and loop filter anti-aliasing filtering characteristics. However, the first integrating stage is the main power hungry (50% of the total power) block in the presented design, this suggest that with further circuit optimization the overall power consumption can be reduced below the $1.40\ mW$ achieved in this works.

# Chapter 6

# Conclusion and Future Work

## 6.1 Conclusion

The aim of this project was to propose a high performance, area and power efficient ADC coupled with superior linearity and good anti-aliasing filtering properties for IoT radio receiver system. Oversampled converter, especially continuous time sigma delta modulators (CTDSMs) offer various advantage such as an inherent anti-aliasing filtering property which relaxed the base band filtering (BBF) requirements at the input of conventional radio receiver signal chain. The quest for good linearity and high dynamic range along low power which the goal of this work is, brings with it question about stability and sustainability of the CTDSM in radio receiver subject to strong nearby interfering signals and how the DR performances of the modulator as standalone could fit in the overall receiver system to achieve a truly cost-efficient design.

This thesis has presented a $1.47mW$, 14-bits, CTDSM in $65\ nm$ CMOS with $94\ dBFS$ peak SNR, $84.8\ dBFS$ SNDR, SFDR $98.7\ dBFS$ and $74.33\ dBFS$ attenuation of alias signals. First, a system level of the prototype modulator was model in MATLAB®SIMULINK where it's proven that incorporating a FIR filter with an RTZ DAC in the feedback path reduce the sensitivity of the 4$^{th}$ order CTDSM to ISI and clock jitter. Then, the circuit realization of this protype modulator was implemented. The most power-hungry element of the modulator is the loop filter and it was realized using the feedforward topology. Despite all the advantages offered by this loop filter structure, it's often limited by the requirement of analog summer. It's been shown that using a resistive passive summer was an area and power efficient approach to overcome the summation limitation in feedforward loop filter architecture.

## 6.2 Future Enhancement

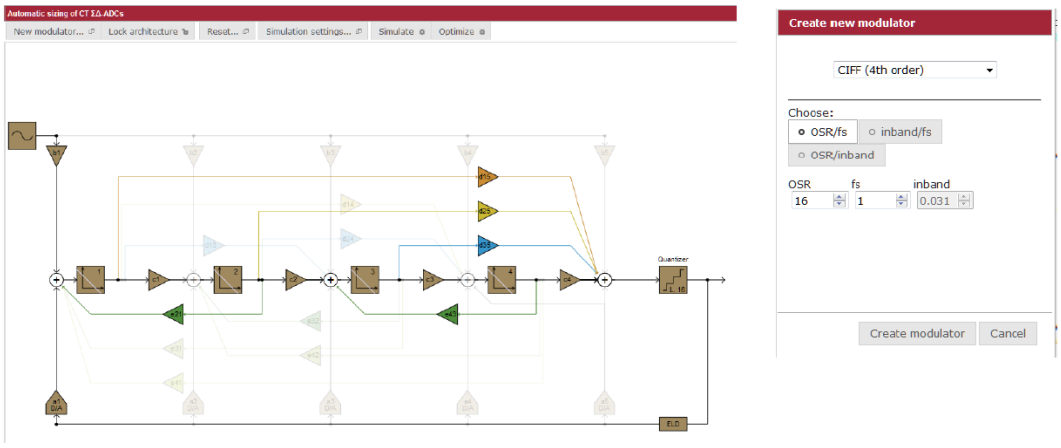
Based on the insight gained from the work covered in this dissertation, extensions in the following areas of the project could be implemented or investigated to further reduced the power consumption and improved the overall performance of the CTDSM, several architecture development and circuit techniques could be considered:

- The two stages Miller OTA was used to implement the loop filter RC-integrators. However, multistage feedforward compensated OTA offer high dc gain over a wider bandwidth in power efficient manner. Therefore, designing the integrator with feedforward amplifier structure would have resulted in further power saving.
- Return-to-zero (RTZ) DAC has been adopted to alleviate ISI error in the modulator. However as shown in chapter 3, this was the expense of worsen jitter tolerance. Moreover, for large input amplitude the op-amps will require extra power. Different alternative such as dual return-to-zero DAC and dynamic element matching with ISI error shaping could lead to better reduction of the ISI error as advocated in [39].
- The idea of using a multi-input comparator can be an interesting approach to overcome the feedforward summation at loop filter provided the loop filter outputs voltages amplitudes are not large.
- Some power saving can be achieved by optimizing the switch resistive DAC design. For instance, using a three input nand gate with a bit digital logic in figure 41a could reduce the number of T-gate in switching scheme. Hence, more are and power dissipation saving.

# Appendix

## CTDSM Automatic sizing online tool usage

We used the "UniUlm Sigma Delta Synthesis Tool" available at: [www.sigma-delta.de](http://www.sigma-delta.de). This is a powerful design tool, allows for quick comparison and analysis of possible architectures.



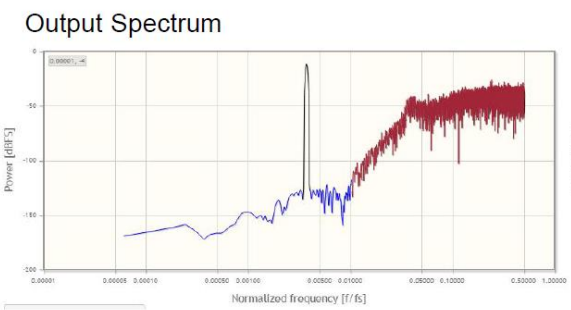

| Coefficient | Value | Last value |
|---|---|---|
| a1 | -0.22000 | -0.22000 |
| b1 | 0.22000 | 0.22000 |
| c1 | 0.30000 | 0.30000 |
| c2 | 0.30000 | 0.30000 |
| c3 | 0.25000 | 0.25000 |
| c4 | 1.00000 | 1.00000 |
| d15 | 0.95000 | 0.95000 |
| d25 | 1.50000 | 1.50000 |
| d35 | 0.85000 | 0.85000 |
| e21 | -0.01000 | -0.01000 |

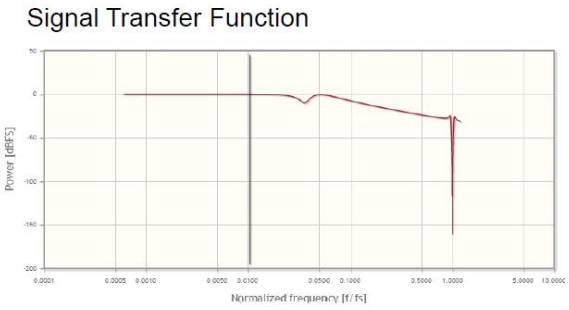
| Integrator | DC gain | GBW | Prop. path value | Last prop. path value |
|---|---|---|---|---|
| 1 | 1000 | 2.915339708328247 | - | - |
| 2 | 1000 | 1.009602665901184 | - | - |
| 3 | 1000 | 1 | - | - |
| 4 | 1000 | 1 | - | - |

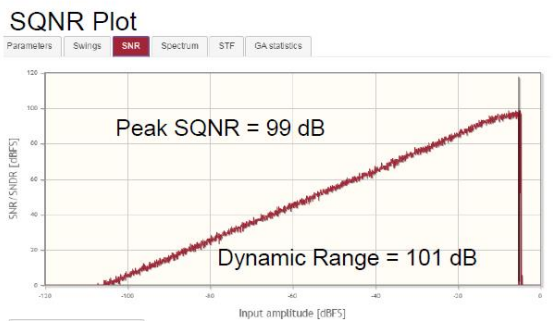
- **User interface**

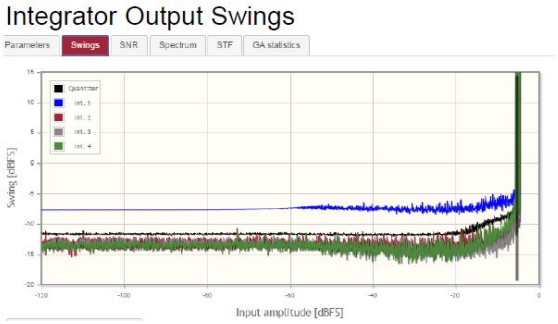
**Desired Modulator Specifications**: *4thOrder CT CIFF modulator*; *Single loop architecture*

*1-bit quantizer*; *Resistive feedback with RZ DAC*; *BW = 250 kHz*; $fs$= 24 MHz; *ELD*




*= 0.5Ts*

**Formula for determining Resistor and Capacitor values:**

$$k_{\square} = \frac{1}{f_s RC}$$

***Sample calculation of Ctaking $R1$=$10k\Omega$and $fs$=$24MHz$:***

$$C = \frac{1}{(24\text{MHz})(10\text{k}\Omega)(0.22)} = 18.$$

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