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Authors	Chang, Tongwei;Mathewson, Alan;Kennedy, Michael Peter;Greer, James C.
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Heterodimensional FET With Split Drain

Tongwei Cheng, A. Mathewson, *Senior Member, IEEE*, M. P. Kennedy, *Fellow, IEEE*, and J. C. Greer, *Senior Member, IEEE*

***Abstract*—A modification to heterodimensional field effect transistors (HDFET) is introduced and demonstrated to provide novel switching capabilities. The modification consists of introducing a split drain into the HDFET structure allowing the transistor to operate as a single pole–double throw switch. By extension, multiple pole–multiple throw switches can be made within a single transistor structure by introduction of multiple split drains or sources. If the device is fabricated on silicon germanium substrates, compatibility of the structure with conventional CMOS processing is achievable, allowing for new applications in digital, mixed signal, and high voltage switching.**

***Index Terms*—Heterodimensional field-effect transistor (HDFET), semiconductor relay, silicon germanium.**

I. Introduction

HETERODIMENSIONAL field-effect transistors (HDFETs) are comprised of a side gated two-dimensional electron (2-DEG) or hole gas (2-DHG) connecting source and drain contacts [1]. Voltages applied to side gates cause the depletion regions formed at the gate-channel junctions to spread, displacing charges in the 2-D gas region. HDFETs were originally introduced for III-V technologies, but their operation on silicon germanium (SiGe) substrates has recently been shown [2]. A simple change to the device layout allows for novel switching capabilities [3].

If reverse bias is applied, the channel remains isolated from the gates due to the depletion regions formed, while electrical contact between source and drain is maintained. Increasing reverse bias at either of the side gates results in the channel being pinched off. Before pinchoff, the 2-D Fermi gas is squeezed down to a quantum wire, and the position of the wire can be manipulated by appropriate selection of gate bias voltages [2]. The modification to the basic HDFET device with a deep trench structure splitting the drain is shown in Fig. 1; the trench is filled with an insulator such as SiO_2. Splitting the drain allows for new switching applications with only minor modification to the layout and fabrication process. For example, fabrication of SiGe heterostructure field effect transistors (HFETs) is a mature technology, and HDFETs require no top gate or gate oxide, substantially simplifying process requirements. The trench isolation in the drain is significantly less difficult to process, than say deep trench structures for memory. For a split drain structure, a multiple output device is achieved in contrast to multiple side gate HDFETs [4].

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T. Cheng, A. Mathewson, and J. C. Greer are with the NMRC, University College Cork, Ireland (e-mail: Jim.Greer@nmrc.ie).

M. P. Kennedy is with the Department of Microelectronic Engineering, Enterprise Centre, University College Cork, Ireland.

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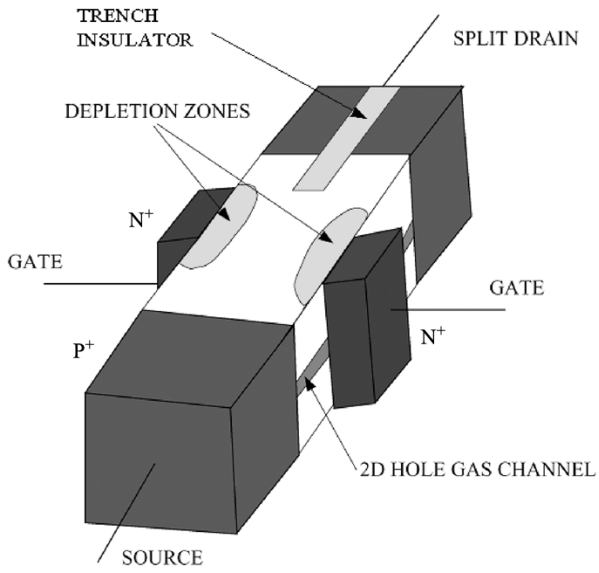


Fig. 1. HDFET with split drain modification.

II. Simulation Details

The simulations are performed for a p-type Si–SiGe HDFET. The side gates are n-type diffusion contacts. A transistor with drain-source length of $L_{\mathrm{DS}} = 3.0\ \mu$m and a gate-to-gate length of $L_{\mathrm{G1\text{-}G2}} = 0.5\ \mu$m has been studied. An energy balance model with appropriate selection of materials parameters [2], [5] allowing simulation of a 2-D quantum well formed within a SiGe substrate is used. The substrate design used in [2] with the 2-D hole gas located in a $Si_{0.4}Ge_{0.6}$ quantum well of 4.5-nm width in the growth direction is considered. The valence band offset ($\Delta E_V \approx 300$ meV) is maximized to capture a large hole density in the quantum well. Different dopant concentrations with carrier density $n = 4.8 \times 10^{21}/\mathrm{cm}^3$ and $n = 4.0 \times 10^{21}/\mathrm{cm}^3$ are introduced in the left- and rightside gate regions, respectively, permitting sensitivity to doping variations to be studied.

III. Results and Analysis

The charge density in the 2-DHG at zero gate bias is undisturbed except for the equilibrium depletion regions formed at the side gates. In this mode, both drains are in electrical contact with the source as the 2-DHG extends around the trench region on both sides. In Fig. 2, a cut-plane through the 2-DHG is shown with side gate voltage V_{G1} at ground and the V_{G2} chosen to deplete the charges connecting source to Drain2, allowing current to pass to Drain1, with only leakage currents to the side gates and Drain2. For a symmetric device structure, exchange of the gate biases results in switching whereby the

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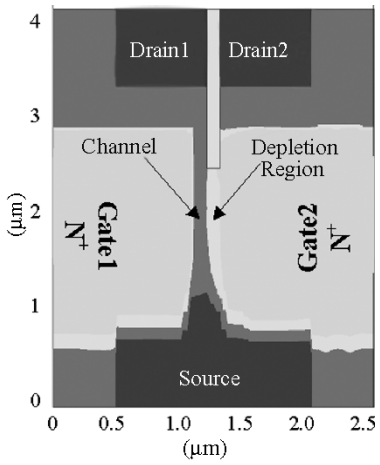


Fig. 2. Cross section of the HDFET structure cut through the 2-D quantum well region. The leftside gate (Gate1) is at ground voltage and the rightside gate (Gate2) voltage at 4.0 V forming a depletion region, cutting off the conducting channel to Drain2.

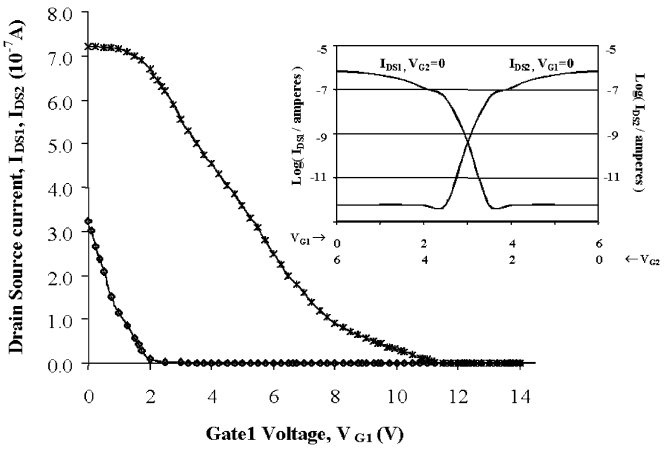


Fig. 3. Inset: Switching operation for a symmetric device structure with drain-source bias of -0.1 V. The combined plot is for $I_{\rm DS1}$ versus $V_{\rm G1}$ with $V_{\rm G2}$ fixed at ground, and $I_{\rm DS1}$ versus $V_{\rm G1}$ with $V_{\rm G2}$ fixed at ground. Main figure: Drain current as a function of gate voltage with drain-source bias of -0.1 V and drain-source currents $I_{\rm DS1}$ and $I_{\rm DS2}$ with $V_{\rm G2} = 0$ and $V_{\rm G1}$ is varied and asymmetric gate doping ($\diamond I_{\rm DS1} * I_{\rm DS2}$).

source is brought into electrical contact with the Drain2, but without current being passed to Drain1. Hence, a single pole (the source) can be switched by application of gate voltages between two positions (the drains). The transistor is more flexible than a conventional single pole–double throw switch, in that either none, one, or both of the source drain regions can be brought into electrical contact with the source by suitable selection of side gate voltages, and further division of the drain and/or source regions allows for multiple pole–multiple throw switches.

In the inset of Fig. 3, switching behavior for an ideal symmetric device with side gate doping $n = 4.8 \times 10^{21}/\text{cm}^3$ has been extracted from three-dimensional (3–D) simulation. Switching is demonstrated by sweeping one of the gate voltages, with the opposing gate at ground. The ratio of on/off current is on the order of 10^6. For lower values of gate voltage, $I_{\rm DS1}(I_{\rm DS2})$ is approximately independent of $V_{\rm G2}(V_{\rm G1})$ as the gate voltage clears only half the channel, pinching the conducting path to one of the drains. As the depletion region continues to spread, the gate voltage then begins to pinch off the conducting path to second drain region.

Modeling of the 2-DHG as a thin semiconductor plane allows for estimates of the side gate capacitance, which for the geometry considered is approximately 0.1 fF/μm. This leads to an estimate for a threshold frequency f_T of 326 GHz (channel length 0.1 μm and gate width 1.0 μm). A single silicon FET with comparable geometry displays f_T of the order 160 GHz and as is known from III–V HDFET technology, this improved frequency response is due to the low capacitance associated with the thin cross section of the 2-DHG.

The terminal output currents for varying gate voltages are displayed in Fig. 3 for a device structure with 20% variation in side gate doping (an extreme case for most processes.) As voltage $V_{\rm G1}$ increases with $V_{\rm G2}$ at ground, current to the Drain1 is lowered until it is pinched-off with $I_{\rm DS1} < 1$ pA at voltages above 2.4 V. The current at $I_{\rm DS2}$ is relatively insensitive to the application of $V_{\rm G1}$ up to the point where the first half of the channel is depleted. As $V_{\rm G1}$ is further increased, the depletion region spreads and removes charge from the channel connecting source and Drain2. As the depletion region spreads across the channel with increasing gate bias, both drain regions become isolated from the source. The nearly linear reduction in both drain currents with application of the side gate voltage as the depletion region first sweeps past across the channel region conducting charge to Drain1, and then continues to deplete charge in the channel until isolating Drain2, is a consequence of the linear dependence of the depletion width with reverse bias in p-n junctions formed between 3-D contacts and a charged plane [6]. Note the asymmetry in the currents between Drain1 and Drain2. Differing doping concentrations at the gates lead to different equilibrium depletion widths $W_1 = 0.1\,\mu$m and $W_2 = 0.03\,\mu$m, and a smaller percentage of the channel is open for conduction for source-Drain1 compared to source-Drain2. Strong variation of the depletion width with side gate doping is related to the small volume of charge contained within the quantum well. To insure a low current to the side gates, a reversed bias between gate and channel is required, and the resulting depletion widths set a fundamental limit to gate-gate spacings. Fluctuations in side gate doping must take into account that the sum of the side gate depletion widths must be smaller than the gate-gate spacing (i.e., for the asymmetric doping case, $L_{\rm G\text{-}G} > 0.13\,\mu$m, for the symmetric case $L_{\rm G\text{-}G} > 0.06\,\mu$m). The effect of varying $V_{\rm G2}$ has also been considered in the asymmetric device while holding $V_{\rm G1}$ at ground. Similarly, it is possible to manipulate the 2-DHG gas allowing for the current to be pinched-off for $I_{\rm DS2}$, while maintaining roughly constant current to $I_{\rm DS1}$. As the depletion width spreads from gate to gate, both drain currents are in an off-state.

IV. Conclusion

A split drain HDFET structure enables operation as a semiconductor relay. As demonstrated previously, HDFETs have a large reverse bias breakdown (> 20 V) at the gate-channel junction, and the depletion width spreading at these bias voltages is on the order of microns [2]. This enables the channel region to be freely positioned; hence switches with larger trench

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structures separating the drain regions can be designed with better drain-drain isolation. Sensitivity of the device to side gate doping has been examined. Finally, introduction of several drain regions enables switching of the source to multiple drains, and similarly the source region may be split allowing for multiple input terminals into the device.

REFERENCES

[1] M. S. Shur, W. C. B. Peatman, M. Hurt, R. T. Ytterdal, and H. Park, "Heterodimensional technology for ultralow power electronics," in *Proc. NATO Adv. Res. Workshop*, Ilde Bendor, France, 1995, pp. 263–268.

[2] T. Cheng and J. C. Greer, "Side gating in silicon germanium heterodimensional field effect transistors," *Microelectron. Eng.*, vol. 71, pp. 197–208, 2004.

[3] T. Cheng, A. Mathewson, M. P. Kennedy, and J. C. Greer, "Irish Patent Application 2003/0167, NATI29/P/IE," US patent filed, 2004.

[4] J.-Q. Lu, M. J. Hurt, W. C. B. Peatman, and M. S. Shur, "Heterodimensional field effect transistors for ultra low power applications," in *GaAs IC Symp. 20th Annu. Tech. Dig.*, Atlanta, GA, 1998, 98CH36260, pp. 187–1990.

[5] M. Lundstrom and R. Shuelke, "Numerical analysis of heterostructure semiconductor devices," *IEEE Trans. Electron Devices*, vol. 30, pp. 1151–1159, 1983.

[6] B. Gelmont, M. Shur, and C. Moglestue, "Theory of junction between two-dimensional electron gas and p-type semiconductor," *IEEE Trans. Electron Devices*, vol. 39, pp. 1216–1222, Oct. 1992.

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