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Supporting Information

Large-Area Growth of MoS₂ at Temperatures Compatible with Integrating Back-End-of-Line Functionality

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Note 1: BEOL Thermal Budget Limit Discussion

In the introduction section of the main manuscript, the vagueness associated with the present description of the BEOL thermal budget limit for monolithic heterogeneous 3D integration is mentioned, and we discuss it further here. At present, it is known that, a processing temperature of 550 °C for a process time of 2 hours (regime 1), and a processing temperature of 500 °C for a process time of 5 hours (regime 2), are both within the BEOL thermal budget limit for monolithic heterogeneous 3D integration, and in fact are considered to be very close to the limit, although we do not have a strictly defined limit value that is a function of process temperature and process time [1]. As a result, it is difficult to compare against when, for example, other works have used different process temperatures and different process times. If a single caloric value, in terms of a heat transfer energy equation, and as a function of the process temperature and process time could be found, the BEOL thermal budget regime limit could potentially be specifically defined for easy comparison and guidance. We explore this possibility in more detail here.

There have been significant advances in the thermal analysis of the BEOL 3D integration of chip components, and this includes very significant and dedicated theoretical and/or

experimental studies. The thermodynamics of the BEOL 3D integration of chip components is extremely complex, and no simple heat transfer equation describes the systems, which require a specialised modelling regime very different to the BEOL process in our study [2, 3, 4]. Direct materials integration at the BEOL, heterogeneous or otherwise, appears extremely challenging experimentally given the paucity of reports in the literature, although theoretical studies of the BEOL 3D integration also paint a complex thermodynamic picture [5, 6, 7]. There is very limited thermodynamic analysis of the monolithic heterogeneous BEOL 3D integration process, or of the effect on the underlying CMOS circuitry.

Caloric equations of state do exist for material systems, for generic thermodynamic processes of materials [8, 9], and for silicon dioxide [10], but all the focus has been on the thermodynamics of material phases as a function of temperature and pressure in mostly high energy processes, which are not characteristic of our BEOL system, nor easily applied.

Therefore, the above assessment summary has not provided an easily-applied literature solution to providing a caloric value to describe the thermodynamic heat transfer of the generic BEOL monolithic heterogeneous 3D integration process. Nevertheless, basic thermodynamic theory provides a case study on heat transfer for integrated circuits that may present a starting point for determining a caloric value [11].

This formulation in [11] uses the conservation of energy, in that the rate of heat transfer, that is the heat current, $H = dQ/dt$, must be equal to the electrical power, P , dissipated. Since power P is equivalent to H , then $T_{IC} = T_{amb} + (R_{IC} P) = T_{amb} + (R_{IC} H)$, where T_{IC} is the temperature of the integrated circuit, T_{amb} is the temperature of the surrounding ambient, and R_{IC} is the proportionality constant for the integrated circuit. Therefore, applying an equivalent BEOL proportionality constant, say R_{BEOL} , to a simplified model of a generic BEOL system and rearranging the equation in terms of H , we get, $H = (T_{BEOL} - T_{CMOS})/R_{BEOL}$. Given that $H = dQ/dt$, then $Q = H t$, leading to the caloric value equation, $Q = t (T_{BEOL} - T_{CMOS})/R_{BEOL}$, where T_{BEOL} is the BEOL process temperature, T_{CMOS} is the underlying CMOS circuitry temperature (taken as 25 °C at the start of the process), t is the total process time in seconds, and Q is the total heat transfer energy in joules. Note that if the BEOL system were to have multiple steps for creating diverse device functionalities, then the total heat transfer energy limit, Q_{lim} , could be considered the sum of each step, n , and Q_{lim} could be described in terms of n : $Q_{lim, n} = \Sigma (H_n$

t_n). Reducing the process temperature and/or time of each step, n , would then permit more BEOL processing within the thermal budget limit, $Q_{lim, n}$.

Applying this simplified case study expression to the BEOL thermal budget limit [1] for heterogeneous 3D integration, a rearrangement under the conservation of energy would give, $Q R_{BEOL} = \Delta T t = (T_{BEOL} - T_{CMOS}) t$. Two thermal budget regimes are shown experimentally to be within the BEOL thermal budget limit, but are considered to be very close to the maximum limit. These regimes are: (1) 550 °C for 2 hours (7,200s), and (2) 500 °C for 5 hours (18,000s). If the simplified model considered here, using the unknown R_{BEOL} , is correct, both of the regimes (1) and (2) should provide a similar BEOL thermal budget heat energy transfer value Q . Applying the simplified model equation to each of these regimes in turn, we obtain, (1) $Q R_{BEOL} = 3,780,000 \text{ K s}$, and (2) $Q R_{BEOL} = 8,550,000 \text{ K s}$. Given that the proportionality constant, R_{BEOL} , should be a constant in the model, the observation of very different values for the product of Q and R_{BEOL} for regimes (1) and (2) implies very different caloric values Q , thus proving that the simplified model fails to describe the overarching BEOL thermal budget limit. We plot the two regimes in Fig. S1. The values derived from [1] are indicated by the red stars, with regime (1) in green, and regime (2) in both green and cyan, described by the constant area that is mapped by varying the process temperature difference, $\Delta T \text{ [K]}$, and the process time, $t \text{ [s]}$. We can clearly see that the two regimes do not describe the same BEOL thermal budget area, confirming that the simple thermodynamic model, based on a single proportionality constant, R_{BEOL} , fails.

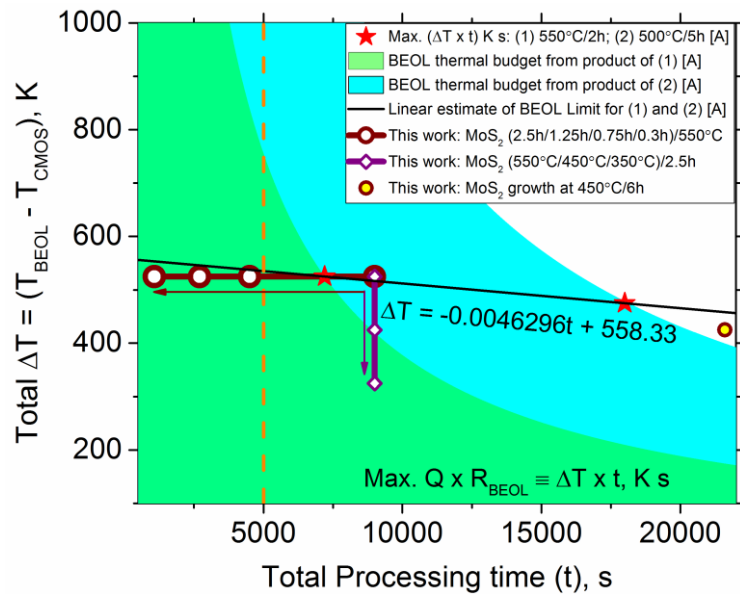


Figure S1: (red stars) The two BEOL thermal budget limit points experimentally verified from reference [1], which is termed as reference [A] in the legend, and gives the two BEOL thermal budget regimes: (1), in green; and (2), in both green and cyan. Since these two regimes describe different areas, the simple thermodynamic product model fails. The experimentally verified BEOL thermal budget limit points (red stars), are fitted to by the black line, giving a next best estimate of the thermal budget limit within the approximate range of $\sim 5,000$ s (vertical orange dashed line) and $\sim 22,000$ s. Within this mapping is plotted the thermal budget points of this work, which are estimated to be approximately at and below the next best linear estimate to the BEOL monolithic heterogeneous 3D integration thermal budget limit (black line).

While this simple model fails to describe the BEOL thermal budget system, we recognise that the two conditions represented by the red stars are experimentally verified as being within the BEOL thermal budget, and are in fact close to the maximum limit of this thermal budget. Hence we know that these two points are correct. By taking a simple line going through these two points, we arrive at a next best estimate of the BEOL thermal budget limit over a limited process time range. This is indicated by the black line in Fig. S1. While very approximate, this estimate may give us a guide to where the limit of the combined temperature difference, ΔT , and the process time, t , may possibly be for the BEOL thermal budget limit. We restrict our assessment to the $\sim 5,000$ s (vertical orange dashed line in Fig. S1) to $\sim 22,000$ s process time range, as outside of this range, it is likely to be even less applicable. It is within this context that we plot the thermal budget points of this work, showing that they are approximately at and below this estimated BEOL thermal budget limit, as indicated by the black line. Note that further thermal stability advances to the underlying silicon circuitry [12], as well as to the intermediate BEOL, such as the metal interconnect and ultra-low k -value interlayer dielectric thermal stability developments in [13], may provide some flexibility in the BEOL 3D monolithic heterogeneous integration thermal budget limit, although limitations remain due to the low thermal stability of NiPt silicidation [14]. Hence, our work appears to be approximately at and below the required thermal budget limit for the BEOL.

This is as far as we can go in the search for a caloric value, Q , and we believe that a dedicated study would be required to determine an accurate caloric equation that describes the BEOL monolithic heterogeneous 3D integration process system, given that the simple model we investigate, relying on a single proportionality constant R_{BEOL} , fails, indicating that the heat transfer energy of the system has a variety of complex dependences. Therefore, a dedicated study encompassing both experimentation and simulation would be required to advance this topic further, which is beyond the scope of our work.

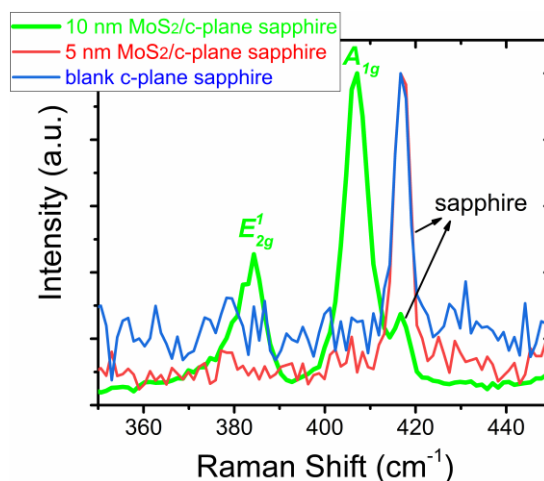


Figure S2: Raman spectra of nominally 10 nm MoS₂ on c-plane sapphire, nominally 5 nm MoS₂ on c-plane sapphire, and blank c-plane sapphire. The Raman mode on the 5 nm MoS₂ is lost due to the large Raman signal from c-plane sapphire.

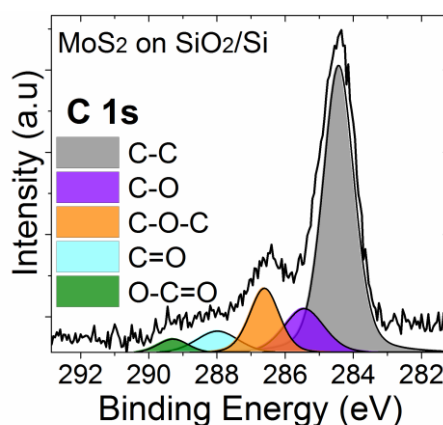


Figure S3: *Ex-situ* monochromatic XPS (C 1s) of MoS₂ (550 °C, 10 sccm 1% H₂S, 2.5 hours) grown on SiO₂/Si substrate, indicating the existence of various carbon/oxygen bonding configurations. It is not known if these are mostly distributed within the MoS₂ film, at the grain boundary regions for example, or if they are concentrated on the surface of the MoS₂ as a result of atmospheric exposure for example. It is also possible that there is a combined contribution from these sources to different concentration levels.

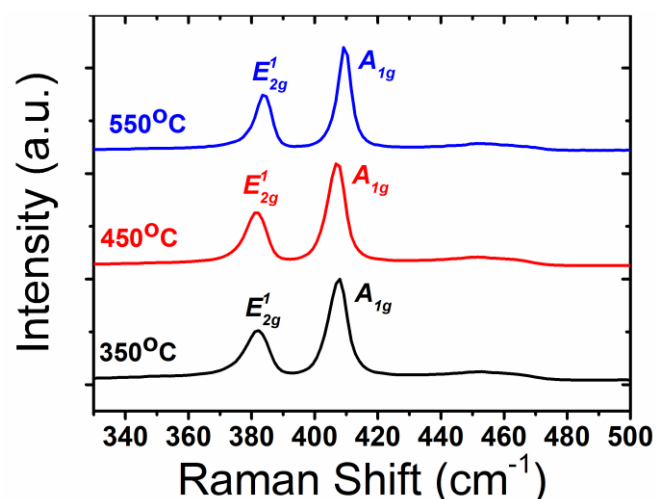


Figure S4: Comparison of the Raman response of the MoS₂ grown at 550 °C (top, blue line), at 450 °C (middle, red line) and at 350 °C (bottom, black line), all on SiO₂/Si substrates. Importantly, the presence of these signature peaks confirms that MoS₂ has been formed during the depositions at 350, 450 and 550 °C. The Full Width at Half Maximum (FWHM) of the E'_{2g} and A_{1g} peaks are shown in table S1.

Table S1: A Lorentzian fitting is used to acquire the FWHM values for the E'_{2g} and A_{1g} peaks from figure S4. The FWHM increases as the growth temperature decreases providing evidence that disorder increases as the growth temperature reduces.

Growth temperature	E' _{2g} (cm ⁻¹)	A _{1g} (cm ⁻¹)
350 °C	9.01	6.76
450 °C	7.51	6.33
550 °C	5.94	4.81

Note 2: Spatial Mapping of Raman Spectroscopy

For the spatial mapping by Raman spectroscopy, 66 measurements were performed over an area of 15 µm x 15 µm, on three macroscale separated sites, for each sample. For each mapping, the baseline was subtracted and set to zero. Then, for a mapping image, an intensity range was set. For these mappings, the A_{1g} peak was chosen because in general it was the more distinct peak of the two main Raman modes of 2H-phase MoS₂, and therefore easier to set to a specific Raman shift. The colour on the images varies from black to red which corresponds to lowest to highest intensity. Hence, the higher the intensity at the set Raman shift, the brighter the red colour. The intensity range differed for each sample due to different Raman settings including laser power and integration time for each measurement. For the nominally 10 nm and 3 nm on glass, it can clearly be seen that MoS₂ is present throughout all sites, with only slight changes

in the intensity. For the nominally 1.2 nm on glass, the colour is a darker red. One of the challenges with this set was that the A_{1g} peak was not as well defined, therefore, picking one Raman shift was more difficult. Another challenge was subtracting the baseline. The intensity range set was not from zero but instead taken from a rough estimate to where the base of the A_{1g} peak lay. The set intensity range is included in the table S2 below.

Table S2: Raman spatial mapping details.

MoS₂ thickness / substrate	Intensity Peak (cm⁻¹)	Intensity Range
10 nm/glass	407.1	0 – 7996
3 nm/glass	405.9	0 – 760
1. 2 nm/glass	404.5	1100 – 1600
10 nm/a-Al ₂ O ₃ /glass	407.2	0 – 6328
10 nm/c-plane sapphire	407.1	0 – 3540
10 nm/a-Al ₂ O ₃ /c-plane sapphire	407.2	0 – 4900
10 nm/SiO ₂ /Si	407	0 – 11450

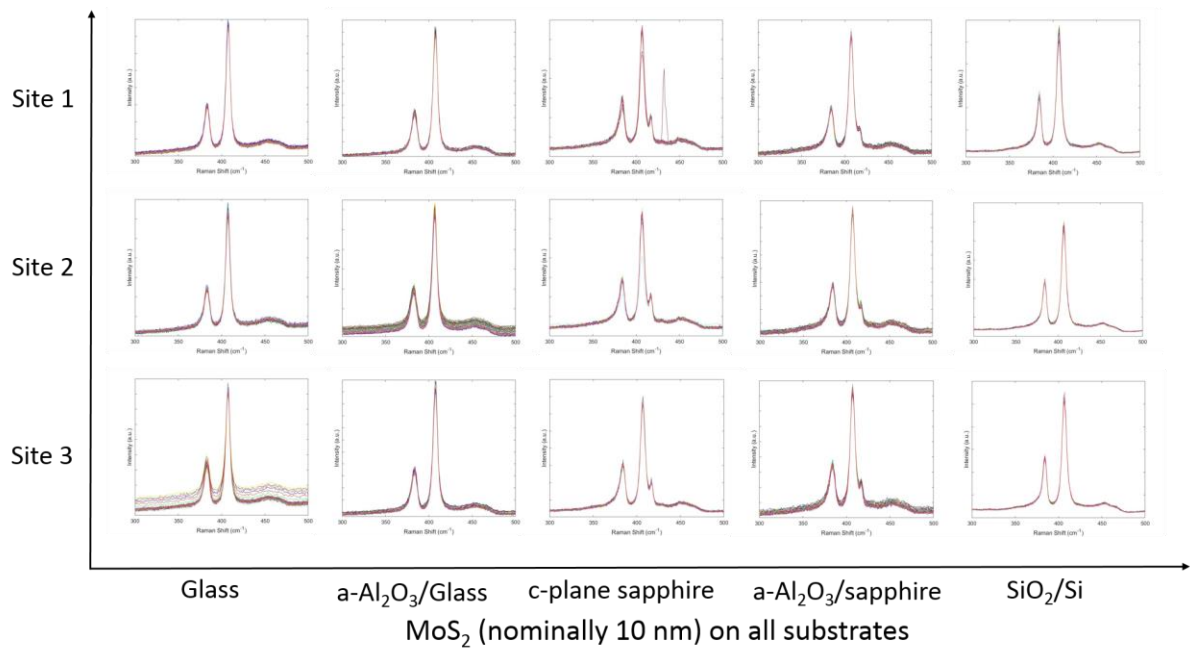


Figure S5: Raman microscale statistical spectra (66 spectra across 15 μm x 15 μm at each macroscale separated site) on nominally 10 nm MoS₂ on all the substrates under investigation.

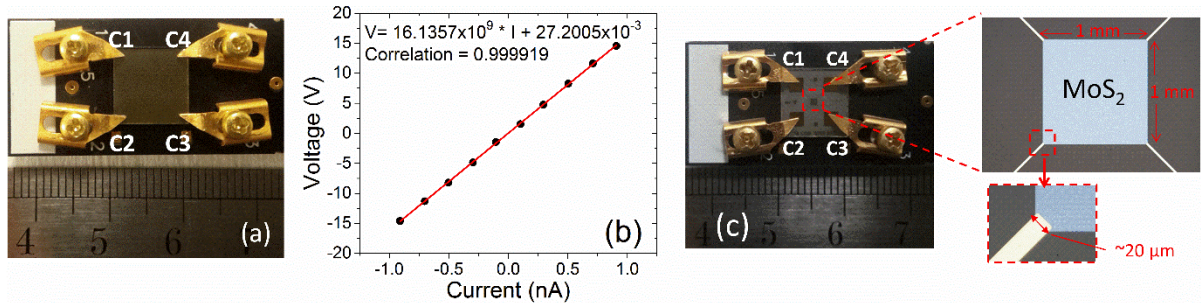


Figure S6: (a) Example image of unpatterned MoS₂ film on sapphire or a-Al₂O₃/sapphire (1 cm $\times$ 1 cm) contacted for room temperature Hall-effect/4-point resistance (Hall/4P) measurements in a Van der Pauw (VdP) configuration. (b) Excellent ohmic behaviour is achieved for MoS₂/sapphire as measured in the Hall/4P system. The 2-point (2P) resistance including a high contact resistance is extracted from the slope. (c) Example image of patterned MoS₂ (1 mm $\times$ 1 mm) on a sapphire or a-Al₂O₃/sapphire (1 cm $\times$ 1 cm) substrate with Ni/Au metal tracks running out to four contact pads (see zoomed-in inset images to the right of (c)) to form the VdP structure for room temperature Hall/4P measurements.

Note 3: Figure S6 and Table 1 (Main Paper)

Figure S6: The measurements were performed in a LakeShore Model 8404 DC/AC Hall-Effect Measurement System fitted with a high-resistance unit (part number 84031; up to 200 G Ω in

DC mode with electrometer-grade buffer load minimisation and guard-signal current-leakage minimisation). Consistent ohmic behaviour is obtained across all two-point contact options. Similar results are also observed on MoS₂/a-Al₂O₃/sapphire (not shown). The Hall results for the MoS₂ on SiO₂ (85 nm)/Si(*p*++) substrates are excluded, as it is observed that Hall/resistance results can be affected, or even dominated, by the underlying *p*-type Si substrate. The resistance of the MoS₂ is in the GΩ range but has ohmic behaviour, and the Hall system can apply current to a maximum voltage of ±100 V to achieve a maximum set current (1 pA to 0.1 A range). As a consequence, significant leakage through the 85 nm SiO₂ to the underlying Si substrate can be observed. See for example figure S6 (b), where a current of 5 nA would correspond to an applied voltage of 80 V, close to or exceeding the breakdown voltage of 85 nm SiO₂. At lower voltages, stress induced leakage currents in SiO₂ can still contribute, or dominate, the Hall analysis [15, 16]. To avoid this coupling to the Si substrate, all the Hall/4P results presented in this paper are obtained from MoS₂ grown on sapphire or a-Al₂O₃/sapphire substrates.

Table 1 (main paper): AC magnetic field Hall-effect measurements were unsuccessful across all samples due to a consistently poor signal-to-noise ratio. We have consistently observed this phenomenon in general for CVD/ALD TMD thin films and the origin of the dominant noise is as yet unknown. The effect is not observed for natural and synthetic TMD crystals, nor for TMD layers formed by thermally-assisted conversion of the metal in a sulfur flux. These results point to instabilities in the CVD/ALD TMD layers with time constants comparable to the period of the AC magnetic field variation (i.e., around 10 seconds). An investigation of the interesting phenomenon is beyond the scope of this work.

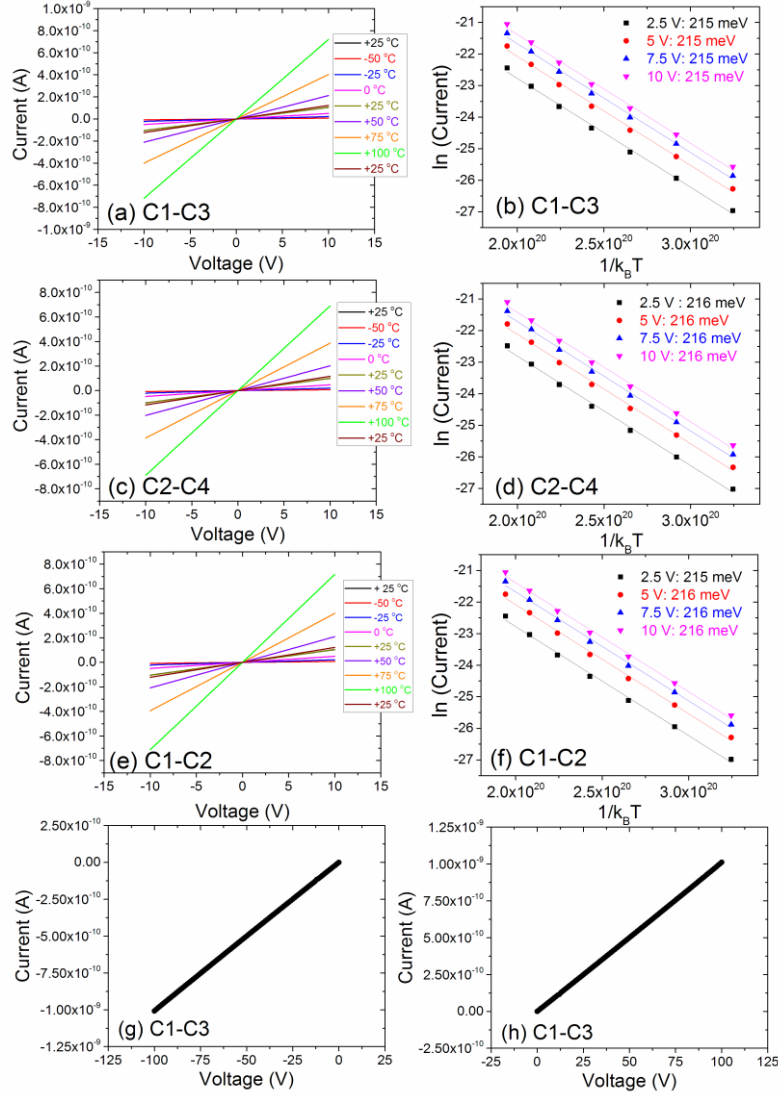


Figure S7: Current-voltage (I-V) characteristics of patterned MoS₂ (550 °C, 10 sccm 1% H₂S, 2.5 hours) on a-Al₂O₃/sapphire substrate. (a), (c) and (e) show I-V characteristics measured at different contact (C) options (C1-C3, C2-C4 and C1-C2) of the patterned MoS₂ between -50 °C and +100 °C. The temperatures from top to bottom in the legend show the sequence of the measurements. Extraction of activation energy at selected voltage values is shown in (b), (d) and (f), and the values of 215–216 meV are consistent with the presence of oxygen in the MoS₂. Activation energy is also extracted at other voltage values which all exhibit similar results (not shown). (g) and (h) show that ohmic behaviour is preserved up to a voltage range between ±100 V at room temperature.

Note 4: Mobility Comparison, Figure 6 (Main Paper)

Hall mobility is related to majority carriers in a longitudinal (in-plane) electric field resulting from a Lorentz force induced by an electric current and a magnetic field. Field-effect mobility is related to either minority or majority carriers (depending on device type) in both a longitudinal and a transverse (out-of-plane) electric field [17, 18]. They are correlated through the conductivity mobility (via the Hall factor), the drift mobility (when minority and majority carriers are equivalent), and the effective mobility. The drift mobility and the effective mobility are equivalent at low transverse electric fields [19-21]. The field-effect mobility is obtained when the transverse electric field is increased, which results in a reduced mobility value compared to the effective mobility [19, 21]. Hence, comparing a field-effect mobility obtained at a low transverse electric field with a Hall mobility gives the best relative assessment.

Table S3: Process details of various ALD-grown MoS₂ from the literature. The first column refers to the ALD growth temperature, which is generally lower than CVD growth temperature. Annealing temperatures/durations are included in the second column where applicable.

ALD growth temperature	Growth/Annealing/Comments	Ref.
175-200 °C	Mo(CO) ₆ + H ₂ S plasma, on SiO ₂ /Si wafer, GaN and sapphire substrates	Jang <i>et al.</i> [22]
300 °C	Mo(thd) ₃ + H ₂ S, on a large variety of substrates including SiO ₂ /Si, glass and sapphire, etc	Mattinen <i>et al.</i> [23]
350-450 °C	MoCl ₅ + H ₂ S, on SiO ₂ /Si, electron mobility of 1 cm ² V ⁻¹ s ⁻¹ from a back-gated FET.	Browning <i>et al.</i> [24]
450 °C	MoCl ₅ + H ₂ S, on SiO ₂ /Si.	Liu <i>et al.</i> [25]
155-175 °C	Mo(CO) ₆ + H ₂ S, on SiO ₂ /Si wafer, improved crystallinity and chemical composition by post-deposition rapid thermal annealing from 500°C to 900 °C (5 minutes) in H ₂ S/Ar.	Pyeon <i>et al.</i> [26]
100 °C	Mo(CO) ₆ + CH ₃ SSCH ₃ , on SiO ₂ /Si or bare Si wafers, MoS ₂ is crystallised after annealing at 900 °C (5 minutes) in Ar atmosphere.	Jin <i>et al.</i> [27]
300 °C	MoCl ₅ + H ₂ S, on sapphire wafers, a post-annealing at 800 °C (30 minutes) under saturated sulfur vapor.	Tan <i>et al.</i> [28]
Up to 475 °C	MoCl ₅ + H ₂ S, on SiO ₂ /Si and quartz substrates following an annealing in sulfur environment at 600-900 °C (30 minutes)	Valdivia <i>et al.</i> [29]
As low as 60 °C	Mo(NMe ₂) ₄ and H ₂ S, a-Al ₂ O ₃ substrates, MoS ₂ is crystallised by annealing in sulfur vapor at 1000 °C (5 hours).	Jurca <i>et al.</i> [30]

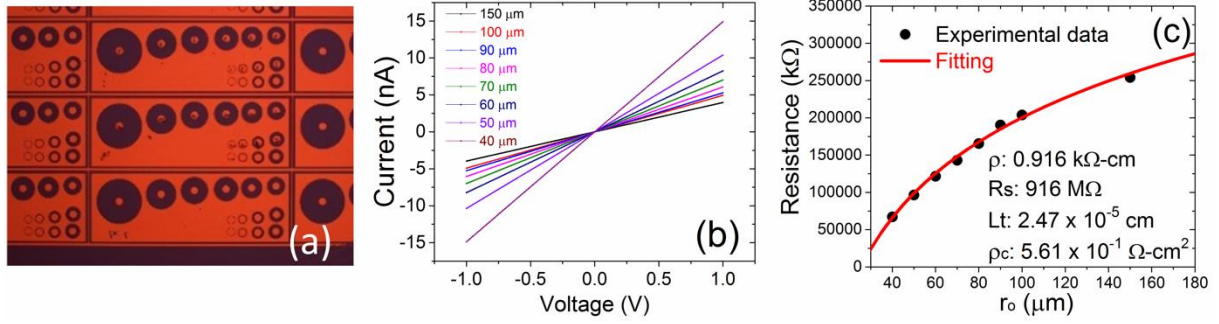


Figure S8: (a) c-TLM structures fabricated on ~ 10 nm MoS_2 (550 $^\circ\text{C}$, 10 sccm 1% H_2S , 2.5 hours) grown on a SiO_2/Si substrate. (b) c-TLM structures exhibit linear current-voltage characteristics at room temperature (outer radius r_o : 40–150 μm of 8 devices used). (c) The total resistance versus outer radius (r_o). This non-linear data can then be linearised (not shown) to extract resistivity (ρ) via sheet resistivity, R_s or ρ_s , (when the MoS_2 thickness is known), transfer length (L_t) and specific contact resistivity (ρ_c).

Note 5: Figure S8 in Comparison to the Hall Results of Table 1 (Main Paper)

The c-TLM measurements in figure S8 are independent measurements to the Hall/4P/2P measurements described in table 1 of the main paper, but each method can determine the sheet resistivity (R_s or ρ_s) of the MoS_2 directly (and thus resistivity ρ when the thickness is known), albeit in the micro-scale for the c-TLM patterned measurements, and in the macro-scale for the Hall-based 4-point VdP measurements. Given the Hall/4P/2P system is performing at the limit of its high-resistance-unit capability, comparing the c-TLM results to the Hall/4P/2P results is a valuable exercise. We see a quantitative correlation between the ρ values obtained from the two different resistance measurement techniques.

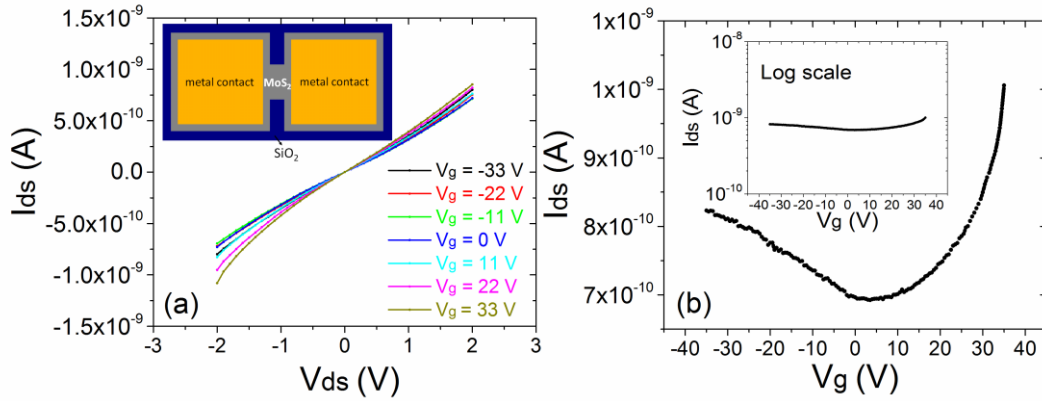


Figure S9: Room temperature (a) output characteristics and (b) transfer characteristics at $V_{ds} = 2$ V of back-gated lateral (in-plane) transport CVD-MoS₂ junctionless MOSFETs. Negligible field modulation is observed, which can be attributed to the large density of grain boundaries and related carrier-trapping defects. Inset in (a) is an illustration of the real device that was measured.

Note 6: Transistor (FET) Measurements, Figure S9, for Logic Applications

Back-gated junctionless transistors are fabricated using ~ 10 nm MoS₂ (550 °C, 10 sccm 1% H₂S, 2.5 hours) on SiO₂ (85 nm)/Si (p^{++}) substrates to explore field-effect modulation of the lateral (in-plane) conduction. The Si (p^{++}) is used as the back-gate. The transistors are annealed in forming gas (5% H₂ + 95% N₂) at 400 °C for 1 hour as a standard step to reduce source/drain contact resistance. Output characteristics and transfer characteristics (at $V_{ds} = 2$ V) of a transistor with a channel length (L) of 10 μm and a channel width (W) of 25 μm are shown, where I_{ds} is the drain-source current, V_{ds} is the drain voltage and V_g is the back-gate voltage. These responses are representative of the general response of transistors as we vary L (4 μm to 60 μm), W (15 μm to 50 μm), V_{ds} (-2 V to +2V) and V_g (-50 V to +35 V) in our large number of transistor measurements (not shown). Negligible field modulation is observed, which can be attributed to the large density of defects within the MoS₂ energy gap, which restrict the movement of the Fermi level in the MoS₂ through the application of a back-gate voltage. This situation is very similar to the case of amorphous or polysilicon thin film transistors without reduction/passivation of defects within the energy gap.

Charge trapping at grain boundaries

An assessment of the charge trapping density can be calculated using figure S9 as follows: if the Fermi level movement in the MoS₂ film is pinned by gap state defects in the MoS₂, then

the effective density of gap states must be sufficient to prevent Fermi level movement over the applied gate voltage range of ± 35 volts, which is the maximum back-gate voltage range applied in the transfer characteristics in figure S9. Considering the case of a positive back-gate voltage and an oxide capacitance C_{ox} (85 nm of SiO_2) of $4.06 \times 10^{-8} \text{ F cm}^{-2}$, the density of trapped charge ($Q_t \text{ cm}^{-2}$) required to restrict Fermi level movement in the MoS_2 is estimated to be $Q_t \geq C_{ox} \times \Delta V/q \approx 1 \times 10^{13} \text{ cm}^{-2}$, where q is the elementary charge and $\Delta V = 35 \text{ V}$. For a grain size of only 10 nm (i.e. 10^{-6} cm), which is a good estimation of the CVD-grown MoS_2 in this work, this corresponds to a volume trap density of $\geq 1 \times 10^{19} \text{ cm}^{-3}$ (i.e. $1 \times 10^{13} \text{ cm}^{-2} / 10^{-6} \text{ cm}$).

FET current Levels in Comparison to Hall Data

While the I_{ds} current in figure S9 (b) shows negligible variation with the back-gate voltage V_g , it is noted that the magnitude of I_{ds} and the associated total resistance (post-anneal) is in reasonable agreement with the measurements in the Hall/4P system on the non-patterned (and non-annealed) films. For a given back-gate voltage (V_g), where carrier concentration (n) and mobility (μ) are constant, the gradient of the I_{ds} vs V_{ds} relationship is proportional to $(n \times \mu)$. The value of $(n \times \mu)$ at $V_g = 0 \text{ V}$ is $\sim 9.1 \times 10^{14} \text{ cm}^{-1} \text{ V}^{-1} \text{ s}^{-1}$, and the Hall/4P results predict a similar $(n \times \mu)$ value in the range 1.9×10^{15} to $3.2 \times 10^{15} \text{ cm}^{-1} \text{ V}^{-1} \text{ s}^{-1}$. It is noted that the comparison is made on the value of $(n \times \mu)$ between the Hall analysis and FET data, through the obtained current I_{ds} . This shows broad agreement between the current levels from the Hall analysis and the back-gated FETs.

FET-based resistivity correlated with c-TLM, in comparisons to the resistivity from Hall/4P system

We can assess the source/drain transistor structures as equivalent to linear-bar TLM structures, and use this definition along with the transfer length L_T from the c-TLM results to estimate the resistivity ρ . If we calculate the slope of any I_{ds} - V_{ds} plot for any V_g in figure S9 (a), given that V_g has minimal modulation capability, we get the total resistance R_t from the inverse of the slope $s \sim (8 \times 10^{-10} - 3 \times 10^{-10}) / (2 - 1) \sim 5 \times 10^{-10}$, giving $R_t \sim 2 \times 10^9 \Omega$. We know from bar TLM theory [19] that $R_t \sim (\rho_s/Z) \times (L + 2L_T)$ where ρ_s is the sheet resistivity, Z is the width (25 μm) of the channel (= metal width), L (10 μm) the channel length, the transfer length $L_T = 2.47 \times 10^{-5} \text{ cm}$ from the c-TLM results in figure S8 (c), and given the condition $L \geq 1.5L_T$ ($1 \times 10^{-3} \geq \sim 3.5 \times 10^{-5}$) is true. Hence, rearranging in terms of ρ_s we get $((25 \times 10^{-4}) \times (2 \times 10^9)) / (10 \times$

$10^{-4} + (2 \times 2.47 \times 10^{-5}) \Omega/\text{sq.} \sim 2.382313... \times 2 \times 10^9 \Omega/\text{sq.} \sim 4.8 \times 10^9 \Omega/\text{sq.}$ The resistivity $\rho \sim \rho_s \times t \Omega \text{ cm}$, where t is the thickness (10 nm) of the MoS_2 , giving $\rho \sim 4.8 \text{ k}\Omega \text{ cm}$. This approximate resistivity agrees very well with the resistivity (2.0 to 3.3 $\text{k}\Omega \text{ cm}$) determined by the 4P measurements in the Hall system as shown in table 1 in the main paper. The transistor results, along with the findings of the c-TLM analysis, provide independent support to the 4P resistivity and Hall results.

Table S4: Comparison of our room temperature CVD-grown MoS_2 thin-film-based gas sensor results with the literature room temperature CVD-grown MoS_2 thin-film-based NO_2 gas sensor results.

No.	Material Description	Method/precursors/ growth temperature	Response % @ LLOD	LLOD (Lowest limit of detection)	Response/ recovery time	Selectivity	Ref.
1.	Atomic layer MoS_2	Deposition of MoO_3 and sulfurisation of MoO_3 using sulfur source, on sapphire, at 850 °C	1%	1.5 ppm	No recovery at room temperature.	Not shown	[31]
2.	3D Hollow MoS_2 nanoflakes	Prior to CVD, 5, 10, 15, 20-tetrakis(4-hydroxyphenyl)-21H, 23H-porphyrin (p-THPP) thin films deposition on Si/SiO ₂ substrate as organic promoter layer, at 550 °C to 800 °C	3%	150 ppb	Less than 50% recovery	Not shown	[32]
3.	Atomic layer MoS_2	Pre-deposited MoO_3 (Thermal Evaporator) and sulfur as source, on Si/SiO ₂ , at 900°C	35%	120 ppb	Thermal annealing at 100 °C to recover the baseline.	Not shown	[33]
4.	Vertically aligned MoS_2 nanoflake network	Precursor MoO_3 and sulfur, on Si/SiO ₂ , at 1000 °C	3.4%	1 ppm	98s/ No recovery at room temperature.	Highly selective against NH_3 , H_2S , H_2 , CH_4 , CO_2	[34]
5.	2D MoS_2	$\text{Mo}(\text{CO})_6$ (at 35 °C) and H_2S (5 sccm) as the Mo and S precursors, on plastic, at 200 °C	97%	25 ppm	180 s / 480 s	Not shown	[35]
6.	Resistive CVD grown monolayer MoS_2 sensor	Standard CVD process, MoO_3 and S as precursor, at 850 °C	9.5%	10 ppm	Poor recovery (< 50%), External energy (Photoexcitation) for complete recovery	Not shown	[36]
7.	In plane and edge enriched	Modified APCVD, MoO_3 and sulfur as	10.36%	10 ppm	8.51 s / No recovery at RT.	Selective against	[37]

	MoS ₂ nanoflakes	precursors, on Si/SiO ₂ , 800 °C			UV assisted recovery - 146.49 s Recovery @ 125 °C – 19.6 s	NH ₃ , H ₂ S, H ₂ , CO ₂	
8.	2D MoS ₂	Conventional CVD, on Si/SiO ₂ substrate, MoO ₃ and sulfur 550 to 870 °C	15.28%	5 ppm	40% recovery at RT, Recovery observed at 100 °C and using UV treatment	Selective against NH ₃ , H ₂ S, H ₂ , CO ₂	[38]
9.	Bilayer MoS ₂	Two-step process-deposition of MoO ₃ and sulfurisation using sulfur source, on Si/SiO ₂ substrate, at 650 °C	2.6%	1 ppm	678 s / 318 s	Selective against NH ₃ , CH ₄ , H ₂ , O ₂	[39]
10	MoS ₂ optoelectronic gas sensor	Conventional CVD, on sapphire substrate, MoO ₃ and sulfur, at 650 °C	300%	25 ppb	Recovery using red light illumination	Not shown	[40]
11	Vertically Aligned MoS ₂ layers	Mo deposited Si/SiO ₂ with elemental sulfur introduced in furnace, at 770 °C	0.2%	100 ppb	30% recovery only	Not shown	[41]
12	2D MoS ₂	Commercially available MoS ₂ (synthesised using CVD), on Si/SiO ₂ substrate	5%	1 ppm	Recovery using UV-LED illumination	Not shown	[42]
13	Single layer MoS ₂	Standard CVD process, MoO ₃ and sulphur, on flexible PET, at 800 °C	40%	20 ppb	480 s / > 1200 s for < 50% recovery. Fully recovered using red light illumination	Not shown	[43]
14	MoS ₂	CVD	1%	300 ppb	238 s / 300 s @ 300 ppb	Ultra-selective against H ₂ , H ₂ S, NO, CO ₂ , CH ₄ , SO ₂ , Acetone	[Our work]

Note 7: MoS₂ sensor thickness considerations

For sensors, the thickness has a significant role to play in the gas sensing performance, since a sensor is a surface phenomenon. In particular, the electron confinement in two-dimensional space deeply affects the gas sensing capabilities. This translates as a remarkable enhancement in the sensor response when the thickness is reduced into the regime of quantum confinement [44]. The quantisation of electrons favourably alters the transport properties of charge carriers, mainly due to the reduced density of states (DOS) for 2D semiconductors, thus making them more susceptible to surface phenomena [45]. In one study on self-assembly for transition metal oxides [46], the potential of ultra-thin transition metal oxides nanosheets, such as ZnO, WO₃,

Co₃O₄, in various electronic applications, is discussed. They demonstrated the thickness of these nanosheets between 1.6 nm and 5.2 nm, corresponding to 2–7 stacking layers of the monolayer and stated that all the thicknesses of these 2D nanosheets in this range are thin enough to present quantum confinement effects, demonstrating their potential applications in some novel electronic devices. In another study [47], single and multilayer (4L) MoS₂ based gas sensors for NO detection at room temperature are fabricated, and similar responses were reported for 2 to 4L (1.5 to 2.9 nm). On the other hand, although the single layer MoS₂ based device showed the better performance, unfortunately, the response was unstable. Hence, the focus of our work, in regard to gas sensors, was to develop thinnest possible film in the range of 2 nm to 5 nm to exploit the maximum surface to volume ratio for the intended gas sensing application, but at the same time, maximise the possibility of a successful processing of devices. Due to the fabrication challenges, we could not advance a gas sensing study on 3 nm MoS₂ films.

Reference

- [1] Fenouillet-Beranger C *et al* New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI *IEEE International Electron Devices Meeting (IEDM) (San Francisco, CA, USA, December 15-17, 2014)* 27.5.1-27.5.4
- [2] Colgan E G, Polastre R J, Knickerbocker J, Wakil J, Gambino J and Tallman K Measurement of back end of line thermal resistance for 3D chip stacks *29th IEEE Semiconductor Thermal Measurement and Management Symposium*, San Jose, CA, 2013, pp. 23-28
- [3] Wakil J, Colgan E G and Chen S Back-End-of-Line and Micro-C4 Thermal Resistance Contributions to 3-D Stack Packages *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 7, pp. 1007-1014, July 2011
- [4] Kikuchi S, Suwada M, Onuki H, Iwakiri Y and Nakamura N Thermal characterization and modeling of BEOL for 3D integration *2015 IEEE CPMT Symposium Japan (ICSJ)*, Kyoto, 2015, pp. 97-100
- [5] d'Alessandro V, Magnani A, Codecasa L, Rinaldi N and Aufinger K 2016 Advanced thermal simulation of SiGe:C HBTs including back-end-of-line *Microelectronics Reliability* **67** 38-45
- [6] El Helou A, Raad P E, Venugopal A and Kande D Thermal characterization of Si BEOL microelectronic structures *Proceedings of the ASME 2018 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems. ASME 2018 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*. San Francisco, California, USA. August 27–30, 2018. V001T03A002. ASME.

- [7] Cheng C C *et al* Monolithic heterogeneous integration of BEOL power gating transistors of carbon nanotube networks with FEOL Si ring oscillator circuits *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, pp. 19.2.1-19.2.4
- [8] Coleman B D and Mizel V J 1964 Existence of Caloric Equations of State in Thermodynamics *J. Chem. Phys.* **40** 1116-1125
- [9] Lomonosov I V, Bushman A V, Fortov V E and Khishenko K V 1994 Caloric equations of state of structural materials *AIP Conference Proceedings* **309** 133-136
- [10] Fortov V E 1972 Caloric equation of state of silicon oxide and of a silicone liquid *Combust Explos Shock Waves* **8** 346-350
- [11] “*University Physics*”, Young H D and Freedman R A, 9th Ed., Addison-Wesley, New York, USA, 1996. See: Heat and calorie definitions on pp.470-471; Equations 15-27 and 15-28 on p.486, part of Section 15-9, Integrated Circuits: A case study on heat transfer, pp.485-487.
- [12] Shulaker M M, Hills G, Park R S, Howe R T, Saraswat K, Wong H S P and Mitra S 2017 Three-dimensional integration of nanotechnologies for computing and data storage on a single chip *Nature* **547** 74-78
- [13] Fenouillet-Beranger C *et al* Guidelines for intermediate back end of line (BEOL) for 3D sequential integration *2017 47th European Solid-State Device Research Conference (ESSDERC)*, Leuven, 2017, pp. 252-255
- [14] Andrieu F *et al* A review on opportunities brought by 3D-monolithic integration for CMOS device and digital circuit *2018 International Conference on IC Design & Technology (ICICDT)*, Otranto, 2018, pp. 141-144
- [15] Yamada R-I and King T-J 2003 Variable stress-induced leakage current and analysis of anomalous charge loss for flash memory Applications *IEEE International Reliability Physics Symposium (IRPS) (Dallas, TX, USA, March 30 - April 4)* 491-496
- [16] Ishida T, Tega N, Mori Y, Miki H, Mine T, Kume H, Torii K, Yamada R-I and Shiraishi K 2014 Mechanism of state transition of a defect causing random-telegraph-noise-induced fluctuation in stress-induced leakage current of SiO₂ films *Jpn. J. Appl. Phys.* **53** 08LB01
- [17] Sze S M and Ng K K 2007 *Physics of Semiconductor Devices* 3rd Ed. (John Wiley & Sons Inc., Hoboken, New Jersey, USA)
- [18] Colinge J P, Lee C W, Akhavan N D, Yan R, Ferain I, Razavi P, Kranti A and Yu R 2011 *Junctionless Transistors: Physics and Properties*, Chapter 10 of “*Semiconductor-On-Insulator Materials for Nanoelectronics Applications*” (Eds: Nazarov A, Colinge J P, Balestra F, Raskin J P, Gamiz F and Lysenko V S) (Springer, Berlin, Germany)
- [19] Schroder D K 2006 *Semiconductor Material and Device Characterization* 3rd Ed. (John Wiley & Sons Inc., Hoboken, New Jersey, USA)
- [20] Van Zeghbroeck B 2011 *Principles of Semiconductor Devices*, available online only at <http://ecee.colorado.edu/~bart/book/>; USA
- [21] Muller R S, Kamins T I (with Chan M) 2003 *Device Electronics for Integrated Circuits* 3rd Ed. (John Wiley & Sons Inc., New York, USA)
- [22] Jang Y, Yeo S, Lee H-B-R, Kim H and Kim S-H 2016 Wafer-scale, conformal and direct growth of MoS₂ thin films by atomic layer deposition *Appl. Surf. Sci.* **365** 160-165

- [23] Mattinen M, Hatanpää T, Sarnet T, Mizohata K, Meinander K, King P J, Khriachtchev L, Räisänen J, Ritala M and Leskelä M 2017 Atomic layer deposition of crystalline MoS₂ thin films: new molybdenum precursor for low-temperature film growth *Adv. Mater. Interfaces* **4** 1700123
- [24] Browning R, Padigi P, Solanki R, Tweet D J, Schuele P and Evans D 2015 Atomic layer deposition of MoS₂ thin films *Mater. Res. Express* **2** 035006
- [25] Liu L, Huang Y, Sha J and Chen Y 2017 Layer-controlled precise fabrication of ultrathin MoS₂ films by atomic layer deposition *Nanotechnology* **28** 195605
- [26] Pyeon J J, Kim S H, Jeong D S, Baek S-H, Kang C-Y, Kim J-S and Kim S K 2016 Wafer-scale growth of MoS₂ thin films by atomic layer deposition *Nanoscale* **8** 10792
- [27] Jin Z, Shin S, Kwon D H, Han S-J and Min Y-S 2014 Novel chemical route for atomic layer deposition of MoS₂ thin film on SiO₂/Si substrate *Nanoscale* **6** 14453-14458
- [28] Tan L K, Liu B, Teng J H, Guo S, Low H Y and Loh K P 2014 Atomic layer deposition of a MoS₂ film *Nanoscale* **6** 10584-10588
- [29] Valdivia A, Tweet D J and Conley Jr J F 2016 Atomic layer deposition of two dimensional MoS₂ on 150 mm substrates *J. Vac. Sci. Technol. A* **34** 021515
- [30] Jurca T, Moody M J, Henning A, Emery J D, Wang B, Tan J M, Lohr T L, Lauhon L J and Marks T J 2017 Low-temperature atomic layer deposition of MoS₂ films *Angew. Chem. Int. Ed.* **56** 4991-4995
- [31] Cho B *et al* 2015 Charge-transfer-based gas sensing using atomic-layer MoS₂ *Sci. Rep.* **5** 8052
- [32] Kang M A, Han J K, Cho S Y, Bu S D, Park C Y, Myung S, Song W, Lee S S, Lim J, and An K S 2017 Strain-gradient effect in gas sensors based on three-dimensional hollow molybdenum disulfide nanoflakes *ACS Appl. Mater. & interfaces* **9** 43799-806
- [33] Cho B *et al* 2015 Bifunctional sensing characteristics of chemical vapor deposition synthesized atomic-layered MoS₂ *ACS applied materials & interfaces* **7** 2952-2959
- [34] Kumar R, Kulriya P K, Mishra M, Singh F, Gupta G and Kumar M 2018 Highly selective and reversible NO₂ gas sensor using vertically aligned MoS₂ flake networks *Nanotechnology* **29** 464001
- [35] Zhao Y *et al* 2018 Low-temperature synthesis of 2D MoS₂ on a plastic substrate for a flexible gas sensor *Nanoscale* **10** 9338-45
- [36] Goel N, Kumar R and Kumar M 2018 Enhanced sensing response with complete recovery of MoS₂ sensor under photoexcitation *AIP Conference Proceedings* **1942** 050060
- [37] Agrawal A V, Kumar R, Venkatesan S, Zakhidov A, Yang G, Bao J, Kumar M and Kumar M 2018 Photoactivated mixed in-plane and edge-enriched p-type MoS₂ flake-based NO₂ sensor working at room temperature *ACS Sens.* **3** 998-1004
- [38] Kumar R, Goel N and Kumar M 2017 UV-activated MoS₂ based fast and reversible NO₂ sensor at room temperature *ACS Sens.* **2** 1744-1752
- [39] Xu T, Pei Y, Liu Y, Wu D, Shi Z, Xu J, Tian Y and Li X 2017 High-response NO₂ resistive gas sensor based on bilayer MoS₂ grown by a new two-step chemical vapor deposition method. *J. Alloys Compd.* **725** 253-259

- [40] Pham T, Li G, Bekyarova E, Itkis M E and Mulchandani A 2019 MoS₂-based optoelectronic gas sensor with sub-parts-per-billion limit of NO₂ gas detection *ACS Nano* **13** 3196-3205
- [41] Cho S Y, Kim S J, Lee Y, Kim J S, Jung W B, Yoo H W, Kim J and Jung H T 2015 Highly enhanced gas adsorption properties in vertically aligned MoS₂ layers *ACS Nano* **9** 9314-21
- [42] Kang Y, Pyo S, Jo E and Kim J 2019 Light-assisted recovery of reacted MoS₂ for reversible NO₂ sensing at room temperature *Nanotechnology* **30** 355504
- [43] Guo J, Wen R, Zhai J and Wang Z L 2019 Enhanced NO₂ gas sensing of a single-layer MoS₂ by photogating and piezo-phototronic effects *Science Bulletin* **64** 128-135
- [44] Nah J, Kumar S B, Fang H, Chen Y-Z, Plis E, Chueh Y-L, Krishna S, Guo J and Javey A 2012 Quantum size effects on the chemical sensing performance of two-dimensional semiconductors *The Journal of Physical Chemistry C* **116** 9750-9754
- [45] Neri G 2017 Thin 2D: The new dimensionality in gas sensing *Chemosensors* **5** 21
- [46] Sun Z, Liao T, Dou Y, Hwang S M, Park M S, Jiang L, Kim J H and Dou S X 2014 Generalized self-assembly of scalable two-dimensional transition metal oxide nanosheets *Nat Commun.* **5** 3813
- [47] Li H, Yin Z, He Q, Li H, Huang X, Lu G, Fam D W H, Tok A I Y, Zhang Q and Zhang H 2012 Fabrication of single- and multilayer MoS₂ film-based field-effect transistors for sensing NO at room temperature *Small* **8** 63-67