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The effect of a varied NH_3 flux on growth of AlN interlayers for InAlN/GaN heterostructures

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The effects of AlN interlayer growth conditions on InAlN/AlN/GaN heterostructures are investigated, with interlayers imaged as they would appear prior to InAlN barrier layer deposition using surface atomic force microscopy scans undertaken immediately after growth. Surface morphologies and subsequent heterostructure conductivity suggested minimum on-resistance can be achieved by balancing the underlying GaN channel decomposition and interfacial roughening when deciding AlN interlayer growth parameters on a sapphire substrate of a given miscut. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4818645]

GaN-based devices are a promising candidate for applications requiring robust, reliable heterostructure field effect transistors (HFETs) operating at high frequencies,[1] and with good power handling capabilities.[2] The two-dimensional electron gas (2DEG) formed in the unintentionally doped GaN channel layer by the polarization and band gap discontinuities at an AlGaN/GaN or InAlN/GaN heterointerface[3] offers a high density of charge carriers with a high mobility, as the electrons are nominally isolated from potential alloy scattering effects in the barrier layer. This structure is exploited to fabricate HFETs. Substrates used in nitride HFET metal-organic vapour phase epitaxy (MOVPE) include SiC and silicon (111), although sapphire is commonly used for its low cost and despite its poor thermal conductivity and lattice mismatch with GaN.[4]

The inclusion of an optimised ~1 nm AlN interlayer (IL) between the GaN and the barrier layer has been experimentally proven to increase channel mobility.[5] AlN has the highest bandgap in the III-nitride system, so the inclusion of a thin strained layer acts to further confine the carriers to the undoped GaN and minimize the electron wavefunction overlap with the barrier layer, reducing alloy-related scattering and hence improving mobility and overall device characteristics. It can also act as a growth barrier in MOVPE preparation of InAlN/GaN heterostructures, by protecting the underlying GaN from potential decomposition when the growth conditions are switched to those required for good quality InAlN growth.[6]

If the AlN IL is grown too thin, its effects are too weak, i.e., there is no measurable difference in 2DEG mobility.[7] However, if it is grown too thick, channel mobility is reduced that undermines the inclusion of the IL, which is speculated to be due to roughening at the interface.[8] Optimization of the AlN IL is therefore a critical growth parameter for minimizing the channel resistance and hence maximising subsequent HFET performance.

This study aims to characterise the ~1 nm AlN surface as it would appear immediately prior to the deposition of an InAlN barrier layer. The effect of substrate miscut and V/III ratio on heterostructure conductivity are analysed. Tapping mode AFM was used to image AlN surfaces; and Van der Pauw measurements to extract sheet resistance, mobility and 2DEG concentration from the subsequent samples. Correlation of heterostructure performance with AlN surface morphology and growth parameters provides insight into the scattering mechanisms that reduce conductivity in InAlN/AlN/GaN HFET devices.

All samples were prepared using a 3×2 in. Close Coupled Showerhead AIXTRON MOVPE system. The literature suggests the optimal thickness of a single AlN layer to be ~1 nm,[5,7,8] which was the nominal thickness used in this assessment, assuming a linear growth rate based on bulk (~1 μm) AlN calibration layers. A nominal 1 nm AlN/10 nm GaN superlattice grown under similar conditions was analyzed using X-ray diffraction (XRD), indicating the AlN thickness may be slightly thinner than that estimated from growth rates, at around 0.7 nm. A slightly thinner AlN layer will act to enhance the decomposition mechanisms discussed later in this paper. The temperature during the AlN deposition is fixed to be the same as that of GaN (1060 °C); higher temperature is preferable for good quality AlN, but an increase whilst the GaN surface remains exposed risks channel decomposition,[8] varying the sheet resistance uncontrollably.

Two remaining growth parameters are the V/III ratio (the ratio of incoming group V and group III precursor gases) and the substrate miscut, i.e., the angle between the surface of the sapphire substrate and the (0001) growth plane. 1 nm AlN /2 μm GaN layers were grown, with V/III ratios 100, 500, and 25 000 utilized during AlN deposition. c-plane sapphire substrates were used, miscut by either 0.1° or 0.4° toward the m-plane.

GaN samples were prepared on sapphire substrates of each miscut and used as templates for subsequent growth of the GaN channel, AlN interlayers, and InAlN barrier layers. Assuming no major electrical degradation from incorporated regrowth impurities at the buried interface, the GaN template

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surfaces may be regarded as exposed channel layers in a nitride HFET.

Figure 1(a) shows a $1 \times 1\ \mu m^2$ AFM scan of a GaN template grown on sapphire with a miscut of 0.4°. It is typical of a MOVPE GaN-on-sapphire surface[9]—step flow growth is observed, characteristic of the moderate surface diffusion length of GaN and the initial stepping on the sapphire. Screw and mixed type dislocations terminate steps and manifest as nm-scale pits at a density of around $10^9\ cm^{-2}$, estimated from XRD ω-2θ scans. The rms surface roughness is around 0.8 ± 0.3 nm.

After the AlN layers were deposited, the wafers were brought back to room temperature in a N_2 ambient atmosphere with an ammonia flow mimicking that of InAlN barrier layer deposition (detailed in Table I). Figures 1(b)–1(d) show AlN interlayer AFM scans for various V/III ratio and substrate miscut configurations. AlN is known to exhibit "step-bunching" when grown via MOVPE on GaN (the accumulation of AlN adatoms at step eges due to their low surface diffusion length), exaggerating the step flow pattern on the underlying GaN. Figures 1(b) and 1(d) provide some insight into the genesis of this process as a function of growth parameters—increasing the V/III ratio from 500 to 25 000 on samples on substrates with the same miscut appears to encourage the step bunching, evidenced by the loss of regularity in step spacing and direction and resulting in bunches of step edges occurring more frequently in Figures 1(d) than 1(b). This is due the reduction of the surface diffusion length with increasing ammonia concentration, where AlN adatoms accumulate at step edges, thus departing from the underlying morphology of the GaN channel layer.

Samples grown on 0.4° miscut sapphire are expected to show more step-bunching behaviour than those on the 0.1° miscut substrates due to the geometry dictating an increased number of initial steps on the former; Figures 1(b) and 1(c) demonstrate this. Roughness measurements across the AlN surfaces were made in areas excluding the large pits (see next paragraph), and did not suggest any variation in step height with increased V/III ratio, with all samples having an rms surface variation of between 0.6 and 1.4 nm.

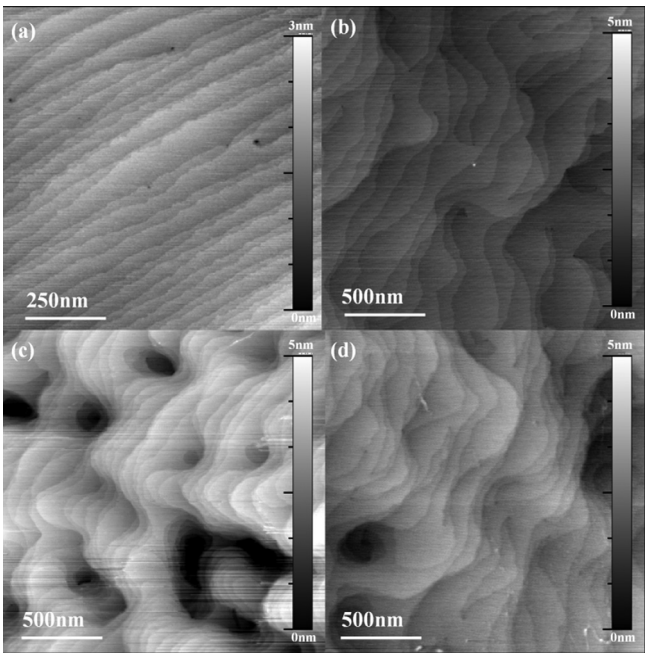


FIG. 1. (a) AFM surface image of a GaN surface. (b) 1 nm AlN on GaN at V/III ratio = 500 on 0.4° miscut sapphire. (c) 1 nm AlN V/III ratio = 500 on 0.1° miscut sapphire. (d) 1 nm AlN V/III ratio = 25 000 on 0.4° miscut sapphire.

TABLE I. Deposition and cool down growth parameters utilized for the AlN layers.

Substrate miscut	1 nm AlN NH_3 flow (mmol/min)	1 nm AlN V/III ratio	Cool down NH_3 flow (mmol/min)
0.4°	2.6	500	2.6
0.4°	13	2500	13
0.4°	0.52	100	56
0.4°	2.6	500	56
0.4°	130	25 000	56
0.1°	0.52	100	56
0.1°	2.6	500	56
0.1°	130	25 000	56

The ammonia flow during the post-growth cooldown is a crucial parameter; without this stage, we observe large pits upon AFM surface analysis (~200 nm across and at least 20 nm deep). Figure 2 displays such surfaces on 0.4° miscut sapphire substrates with different AlN V/III ratios utilized during growth—the pits extend well into the GaN through the partially deposited AlN layer. Their depth suggests they are the result of the GaN decomposition in an ammonia-poor environment, as does their decrease in number from $\sim 12\ \mu m^{-2}$ to $\sim 3\ \mu m^{-2}$ for V/III = 500 and 2500 in Figures 2(a) and 2(b), respectively.

The corresponding sample with V/III = 25 000 (Figure 2(c)) had fewer pits at around $\sim 1\ \mu m^{-2}$, and had a roughness comparable to the surface in Figure 1(d), which was grown identically except for the inclusion of the ammonia cool down phase. This supports the hypothesis that the pits may be suppressed by ensuring there is sufficient ammonia present during the cool down. We may attribute the large pit features in Figures 1(b) and 1(c) to the same effect, i.e., decomposition of exposed GaN during the cool down phase prior to wafer extraction. Such roughness would be detrimental to HFET performance, and GaN decomposition must be considered when speculating on the quality of a heterojunction channel.

Heterostructure DC performance across the series is displayed in Figure 3. The growth process is identical to that of the exposed AlN IL samples with the inclusion of 10 nm of nominally lattice matched InAlN capping the structure acting as a barrier layer. ~1 cm^2 samples were prepared and tested using the Keithley 920 series Hall test equipment.

The samples grown on 0.1° miscut sapphire show a clear increase in channel mobility and consequential reduction in sheet resistance at room temperature with increased V/III ratio, attributed to a higher quality GaN channel and uniform AlN interlayer. Structures grown on the 0.4° sapphire show a room temperature sheet resistance of ~590 Ω/□ at V/III = 500 (roughly the same as on the 0.1° miscut substrate) but

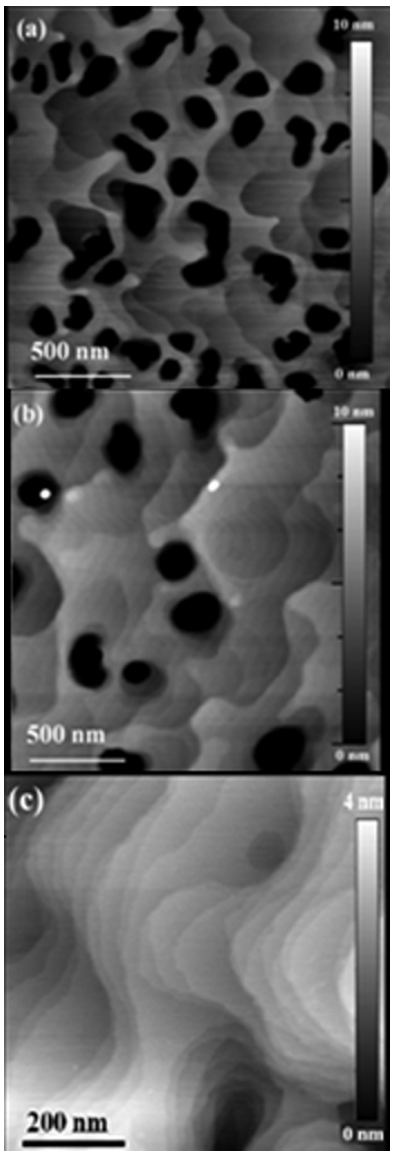


FIG. 2. AlN IL on GaN with (a) V/III ratio = 500, (b) V/III ratio = 2500, and (c) V/III ratio = 25 000, deposited at 1060 °C with IL nitrogen and ammonia flows maintained during the cool down stage.

an increase up to ~640 Ω/□ at V/III = 25 000; in this configuration interfacial scattering caused by AlN step-bunching inhibits the channel mobility, overcoming the benefits of the high quality underlying GaN and representing the importance of considering the multiple physical mechanisms active in AlN interlayer deposition. Notably, there is a clear reduction in sheet resistance with V/III ratio for the samples on the 0.1° miscut sapphire without any significant variation in the surface rms roughness, but with a clearly visible change in step spacing and direction. This result was confirmed with 77 K Hall measurements, also displayed in Figure 3, where phonon scattering is suppressed and the roughness scattering mechanisms are more dominant. The 2DEG concentration was found not to vary significantly across either series. The similarity of the 77 K and room temperature mobility measurements confirms the channel resistances are dominated by interfacial roughness and not thermal phonon scattering, which suggests further optimisation is still required.

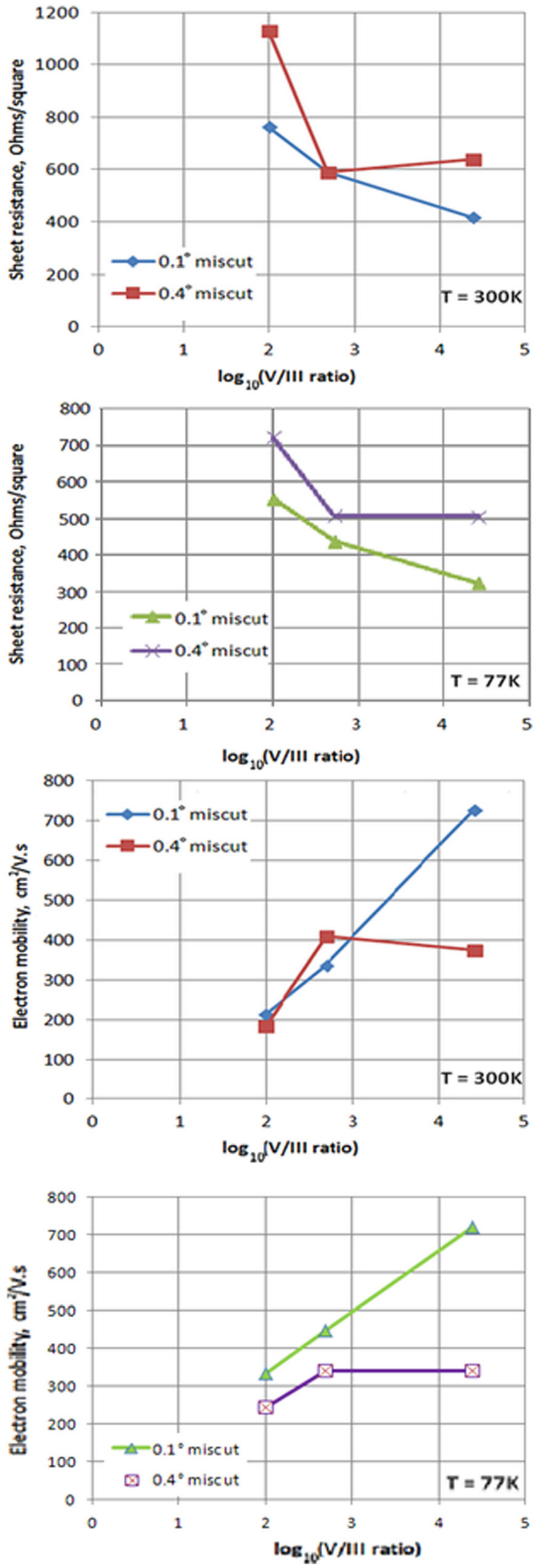


FIG. 3. Sheet resistance and electron mobility of InAlN/AlN/GaN heterostructures at 300 K and 77 K as a function of AlN interlayer growth conditions.

In conclusion, AlN interlayers for InAlN/GaN HFET epistructures were grown on sapphire substrates of different miscuts and with different V/III ratios and directly imaged using atomic force microscopy. Subsequent heterostructure

conductivity suggests minimal on-resistance may be achieved by balancing GaN channel decomposition and interfacial roughening when considering AlN interlayer growth conditions on a sapphire substrate of a given miscut. AlN surfaces that most closely resemble the underlying GaN reference sample produce samples with the lowest sheet resistance, as these layers have the most uniform thickness and hence the least amount of roughness scattering. Further improvements to optimise a narrow AlN thickness window may be required.

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