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4.48GHz Fractional-*N* Frequency Synthesizer with Spurious-Tone Suppression via Probability Mass Redistribution

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***Abstract*—A 4.48GHz type-II charge pump fractional-*N* PLL implemented in a 0.18μm BiCMOS process is presented. The divider controller's output is processed using a novel block, the Probability Mass Redistributor, which statistically reconfigures the modulation noise such that fractional spurs are minimized. Measurements demonstrate in-band fractional spurs of -80dBc. The solution, which is a drop-in modification of a conventional MASH structure, incurs a modulator area increase of 22%, and can be used in conjunction with other linearization strategies.**

***Index Terms*—BiCMOS, frequency synthesis, digital delta-sigma modulation, phase lock loop, spurs.**

I. Introduction

Fractional-N frequency synthesizers are widely used, particularly in communications applications, to produce frequencies which are rationally related to precise reference frequencies. The instantaneous divide value of the multimodulus divider in the feedback path of a fractional-N PLL is determined by a divider controller, which is commonly implemented as a digital delta-sigma modulator (D$\Delta\Sigma$M).

A disadvantage of the fractional-N PLL is the presence of fractional spurs which result from interaction between the signal introduced by the D$\Delta\Sigma$M and nonlinearities in the loop. When fractional spurs lie inside the loop bandwidth, they cannot be attenuated by filtering, and tend to dominate the overall phase noise spectrum. For this reason, the worst-spur amplitude is an important performance metric.

A number of techniques have been developed to reduce the amplitudes of in-band fractional spurs. These include linearization strategies such as bleed current and phase noise cancellation [1], [2] and reshaping of noise introduced by the divider controller through modulator redesign [3], [4]. Using a combination of cancellation and reshaping, Familier and Galton have reported a worst-case in-band spur of -72dBc at 3.35GHz and a -79dBc reference spur with a third-order 16-stage divider controller based on a successive requantizer (SR) [5]. This paper presents a novel noise reshaping block, called a Probability Mass Redistributor (PMR) [6], which is inserted between a conventional MASH D$\Delta\Sigma$M-based divider controller and the feedback divider. It modifies the probability mass function (PMF) of the modulation noise introduced by the divider controller, yielding a -72dBc worst-case fractional spur at 4.485GHz and -110dBc reference spur. Normalizing for output frequency, this represents an improvement of 2.5dB in the in-band spur performance compared to [5].

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II. Reducing nonlinearity noise via PMR

The contribution of PLL nonlinearities to the output phase noise spectrum (hereafter termed *nonlinearity noise*) depends on the shape of the nonlinearity and the probability distribution of the modulation noise arising from feedback divider modulation [7]. In addition to linearizing the inevitable PFD/CP nonlinearity, one way to minimize spurs is to modify the statistical properties of the modulation noise signal so that it produces smaller spurs, if any, when it encounters that nonlinearity. Swaminathan *et al.* introduced the SR-based divider controller which does not produce spurs in the presence of specified polynominal nonlinearities [4]; the most recent implementation of an SR-based divide controller was reported in [5]. We achieve better performance by modifying the probability mass function (PMF) of the accumulated divide ratio controller output, which is proportional to the modulation noise [8]. The finite state machine which reshapes the PMF is called a Probability Mass Redistributor (PMR) [6].

Fig. 1 shows two different modulation noise signals: (a) the accumulated output of a MASH modulator and (b) the same signal post-processed by a PMR. The time-domain waveform, hereafter denoted $\Delta\phi_{\mathrm{mod}}$, is proportional to the time difference between the clock edges presented at the input of the PFD. Note that the PMF of the MASH divider controller has a Gaussian shape while that of the PMR, which has been designed to produce smaller spurs, is non-Gaussian.

The time-domain signal $\Delta\phi_{\mathrm{mod}}$ is applied to the PFD/CP, which has a nonlinear transfer characteristic. We remove the linear component from this transfer characteristic and consider the residual nonlinearity, which can be thought of as equivalent to the INL of a data converter. For illustration, consider a theoretical nonlinearity which is stronger at the centre of the noise range. Fig. 2 shows how the distribution of the input signal is distorted by the residual nonlinearity.

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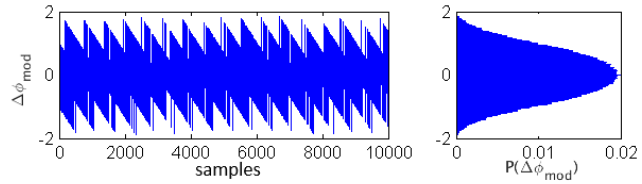
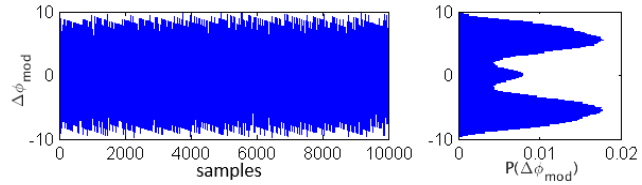


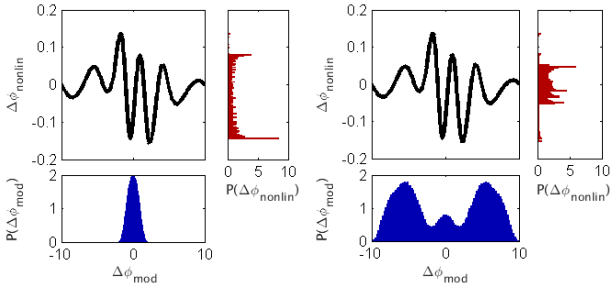
(a) MASH



(b) MASH + PMR

Fig. 1: Time-domain plot (left) and PMF (right) of the modulation noise $\Delta\phi_{\text{mod}}$ from (a) MASH and (b) MASH+PMR divider controllers.

The (blue) PMF of the PFD/CP input is mapped through the residual nonlinearity (black) to produce the (red) PMF of the output. Note that, by modifying the input PMF so that the signal spends less time around the stronger elements of the nonlinearity, the amplitude of the output's nonlinear component is reduced. This in turn reduces the amplitudes of spurs that are caused by the nonlinearity.

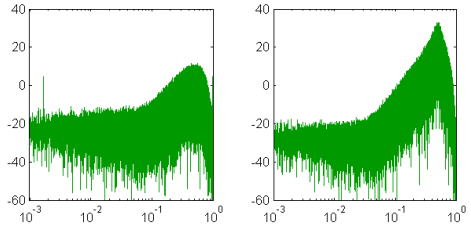


(a) MASH (b) MASH + PMR

Fig. 2: Modifying the modulation noise PMF (blue) to reduce the amplitude of the nonlinearity noise PMF (red) in the presence of a simulated residual nonlinearity (black).

Fig. 3 contrasts the output noise spectra in the two cases, where it can be seen that the fractional spur at 1.66 mrads^{-1} in the MASH's normalized spectrum (a) has been reduced below the noise floor in the case of the MASH+PMR (b). In general, given a residual nonlinearity function with a specified shape, the output PMF of the divider controller can be optimized so as to minimize the contribution of the nonlinearity to the output phase noise spectrum. This PMF modification can be accomplished by inserting a reconfigurable PMR in cascade with a conventional MASH-based divider controller, programmed so as to optimize the PMF for a given nonlinearity.

The role of the PMR is to modify the PMF of the divider controller's output while leaving the spectral shaping properties unchanged. If the probability mass is distributed such that the nonlinearity appears more linear, as shown in



(a) MASH (b) MASH + PMR

Fig. 3: Phase spectral densities at the PFD/CP output, using each modulator configuration.

Fig. 2(b), then the nonlinearity noise power will be reduced, and consequently the amplitudes of the associated spurs. This is achieved by using a second modulator to add a noise component with a similar spectral profile to a basic MASH divider controller, but whose PMF is programmable. If the PMF of the MASH's accumulated noise is given by $P_{\text{MASH}}(x)$, and the PMF of the PMR's accumulated noise is given by $P_{\text{PMR}}(x)$, then the PMF of the accumulated output signal can be approximated by:

$$P_{\text{mod}}(y = x) = P_{\text{MASH}}\,(2x) * P_{\text{PMR}}(x), \tag{1}$$

where $*$ denotes convolution. The influence of the PMR on the PMF is maximized by preceding it with the low-amplitude MASH modulator.

III. PMR Implementation Details

The PMR, shown in Fig. 4 is qualitatively similar to a single SR stage [4]. The modulation noise spectrum is high-pass shaped by means of the difference stages, while the PMF of its accumulated noise can be modified using a Transition Matrix stored as a lookup table [9]. The Transition Matrix and the order of the stage are both programmable.

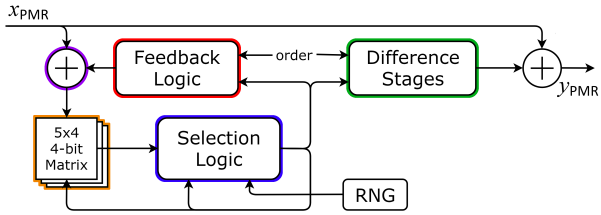


Fig. 4: PMR block diagram.

Fig. 5 shows the implementation in greater detail. In order to facilitate noise-shaping up the third order, a 5×5 Transition Matrix is required. The matrix is stored as a $5 \times 4 \times 4$-bit look-up-table. This is possible because the Transition Matrix is a stochastic matrix where the entries in each row sum to unity; hence, the values of the final column are implied. The Transition Matrix can be described using seven variables, where two pairs are correlated and the remaining three are independent, due to the restrictions placed on the matrix [5]. Considering the minimum and maximum value of each variable results in 72 matrices, each representing a corner case.

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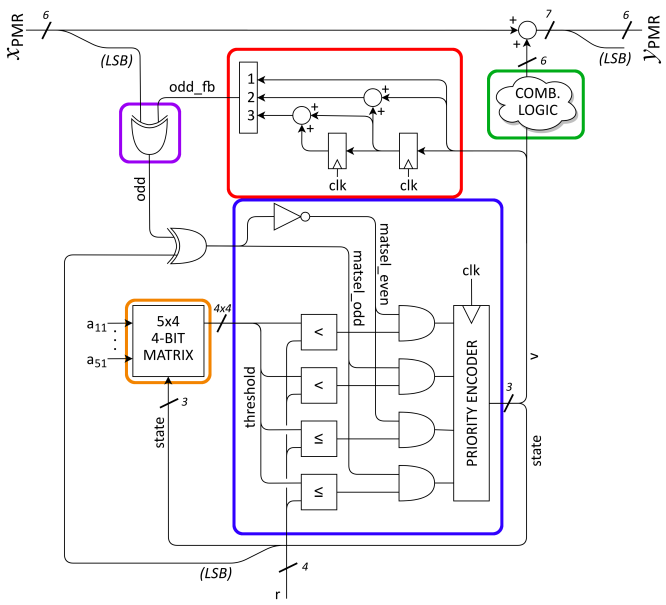

Fig. 5: PMR implementation details.

The selection logic (blue) operates as follows. There are five possible outputs, denoted v_1 to v_5. Four threshold values, corresponding to the possible output choices v_1–v_4, are extracted from the Transition Matrix (orange) according to the previous selection logic output. These values are compared to a random number, generated using an LFSR-based Random Number Generator (RNG), to produce a vector of binary decisions, where a 1 indicates that the corresponding output choice may occur. The LSB of the previous selection logic output is also processed (red) and compared to the LSB of the PMR input (purple) in order to determine the required parity such that the $\langle x_{\text{in}} + v \rangle_2 = 0$. Based on this information, some of the decisions may be set to 0 if the corresponding output would produce the wrong parity. Finally, a priority encoder determines the lowest output choice for which the decision is 1; if all the decisions are 0, then the 5$^{\text{th}}$ choice, v_5, is output.

The selection logic output is accumulated a number of times equivalent to the chosen order (green), before being added to the input. First-, second- and third-order shaping can be chosen, as determined by the value of the order control signal. The selection logic ensures that the LSB of the summation is 0, so that the LSB can be discarded, thereby performing lossless 1-bit quantization.

IV. Synthesizer Implementation Details

The PMR was validated in a type-II charge-pump PLL with a switched divider controller implemented in a 180nm SiGe BiCMOS process. The synthesizer architecture is shown in Fig. 6. A binary-weighted bipolar charge pump (CP) is used, which implements bipolar variable bleed current to allow the performance to be evaluated across a range of operating points and local nonlinearities. The VCO is a quad-core pseudo-differential Colpitts design supporting frequency selection from 4GHz to 8GHz. Output dividers and multipliers with tracking filters further extend the PLL's output frequency

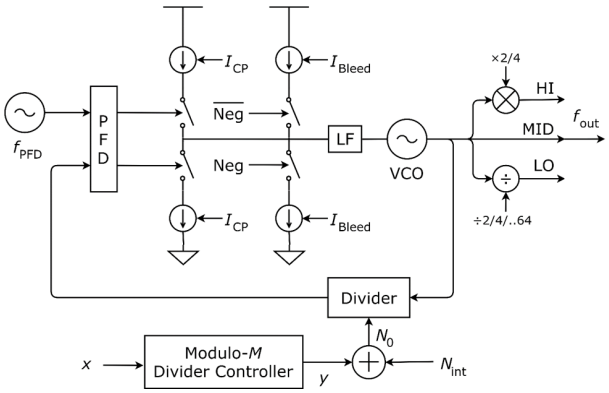

Fig. 6: Frequency synthesizer architecture. The programmable CP has optional bleed current. Dividers and multipliers are present in the LO and HI paths, but are not used in this paper.

range, however, all measurements presented in this work are taken at the VCO output, denoted MID.

The Modulo-M divider controller implements a fraction x/M so that $f_{\text{out}} = (N_{\text{int}} + x/M)f_{\text{PFD}}$. The complete controller is shown in Fig. 7. Two variants are implemented to facilitate a side-by-side comparison. The EN signal is used to switch between a 25-bit MASH 1-1-1 and a nested hybrid comprising an effectively 24-bit MASH and a PMR.

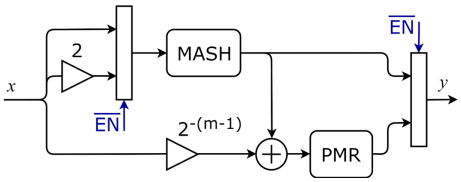

Fig. 7: Implemented divide ratio controller, switchable between MASH and MASH+PMR.

A photomicrograph is shown in Fig. 8. The PMR increases the area of the digital by 22% compared to the MASH alone.

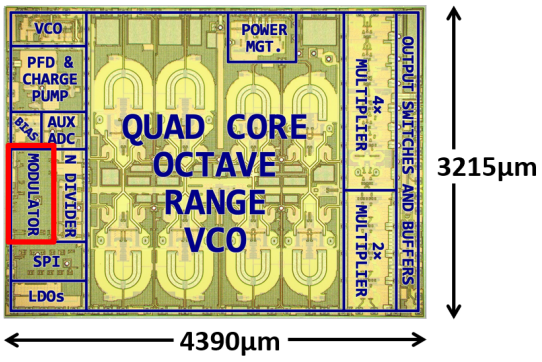

Fig. 8: Micrograph of fabricated silicon.

V. Measured Performance

For each constant input x corresponding to an offset from an integer multiple of f_{PFD}, the fractional spur with the largest amplitude was recorded. Fig. 9 shows the spur amplitudes for

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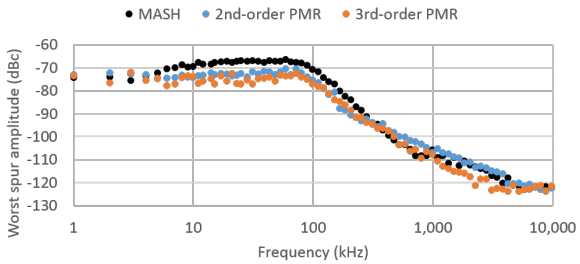

Fig. 9: Worst-case spur versus offset from carrier.

the MASH and MASH/PMR hybrids over a range of modulator inputs. As x is increased, the spur frequency increases with it, until it leaves the passband of the PLL response and is attenuated; variation in the height of spurs is expected to be influenced only by the loop response. In the passband, the spur amplitude remains relatively constant, with minor variations attributable to uncertainty in the measurement of the amplitudes of very weak spurs. The MASH plus third-order PMR has the best in-band spur performance.

Fig. 10 shows spectra corresponding to the best-case spur performance, both with and without the PMR. Manual bleed current optimization has been carried out in order that the best-case performance, in each case, is represented. The use of the PMR has reduced the worst-case spur amplitude, offering a performance improvement of 7dB in this case. An increase in the passband noise floor can also be seen, with a corresponding spur-free jitter increase from 166fs to 209fs (1kHz–100MHz); this is due to the wider spread of the input to the PFD/CP. The PMR accounts for less than 2% of the power consumption of the digital block.

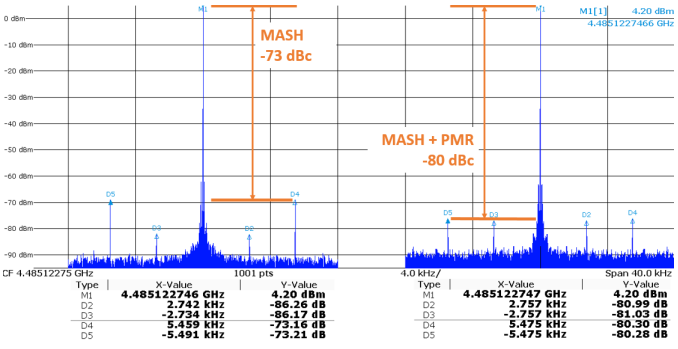

Fig. 10: Spectra showing best-case spur performance after bleed current tuning, both with and without use of the PMR.

Table I compares the part's performance to the previous state-of-the-art. Our solution advances the state-of-the-art spur performance normalized to output frequency.

TABLE I: Comparison of spur performance with previous work. A single spur measurement is given for comparison with [11] because a full sweep was not presented in that paper. FOM = In-Band Phase Noise $-10\log_{10}(f_{\text{PFD}})-20\log_{10}(N_0)$

Reference	[10]	[11]	[12]	This work
Year	2015	2017	2017	2018
Technology [nm]	65	14	65	180
f_{VCO} [GHz]	2.0	2.69	3.35	4.0–8.0
f_{PFD} [MHz]	26	26	26	64.44
Loop Bandwidth [kHz]	1500	N/A	48	100
P_C [mW]	9.1	13.4	19.52	118
Supply [V]	1.0/2.0	N/A	1.0/1.2	1.2/3.3/5
Worst case fractional spur [dBc]				
sweep	**–70**	—	**–72**	**–72**
single measurement	—	**–78.6**	—	**–80**
In-band Noise [dBc/Hz]	−91.1	−113.6	−87.5	−96
3MHz Noise [dBc/Hz]	−105	−137	−137	−145
Reference Spur [dBc]	−87	−87.6	−79	−114
FOM	−223	−228	−204	−211.2
Area [mm^2]	0.046	0.257	0.341	13.2
Architecture	Analog PLL	ADPLL	Analog PLL	Analog PLL

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