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Bandwidth Enhancement to Continuous-Time Input Pipeline ADCs

Daniel O'Hare, *Student Member, IEEE*, Anthony G. Scanlan, Eric Thompson, *Member, IEEE* and Brendan Mullane, *Member, IEEE*

***Abstract*—This work presents design analysis and insights for a new Continuous Time Input Pipeline (CTIP) ADC architecture that has enhanced bandwidth. An all pass filter based analog delay in the signal path allows bandwidth extension to Nyquist signal bandwidths. A resetting integrator gain stage provides a signal path delay helping to increase the bandwidth while reducing the power cost. The noise filtering property of the resetting integrator gain stage preserves the medium resistive input benefit of CTIP ADCs. The resetting integrator allows the architecture to be implemented with a Feed-Forward compensated op-amp using low voltage CMOS processes. This work has been verified by simulation results of a CTIP ADC with 1.2V supply voltage designed in TSMC's 65nm CMOS technology.**

***Index Terms*— Analog-to-digital conversion, anti-alias filter, continuous-time, CMOS analog integrated circuits, pipeline.**

I. Introduction

PROCESS SCALING is leading to smaller chips with more dense functionality. Sensitive analog blocks have to coexist close to noisy switching blocks. Traditional spacing isolation techniques require area and are too costly. The need to design blocks that are less susceptible to interference and generate less interference is critical for many applications. Due to shrinking signal voltages most ADCs have large switched sampling capacitors at their input. Large current spikes are required to charge these capacitors. Such (Successive Approximation Register (SAR)/pipeline/time interleaved (TI)) ADCs have a track time that causes large glitch currents to rapidly charge their sampling capacitors. To isolate the sampling capacitors from the package pins, on-chip buffers are required that have high current consumption and compromise linearity and noise performance of the ADC.

Continuous Time (CT) ADCs don't have sampling capacitors at their inputs so they avoid switched capacitor transients and have no kT/C noise at their inputs. They also have built-in input filtering to relax anti-alias requirements. Continuous Time Sigma Delta (CTΣΔ) ADCs are a widely adopted CT ADC architecture. CTΣΔ ADCs scale with process and new architectures are leading to performance

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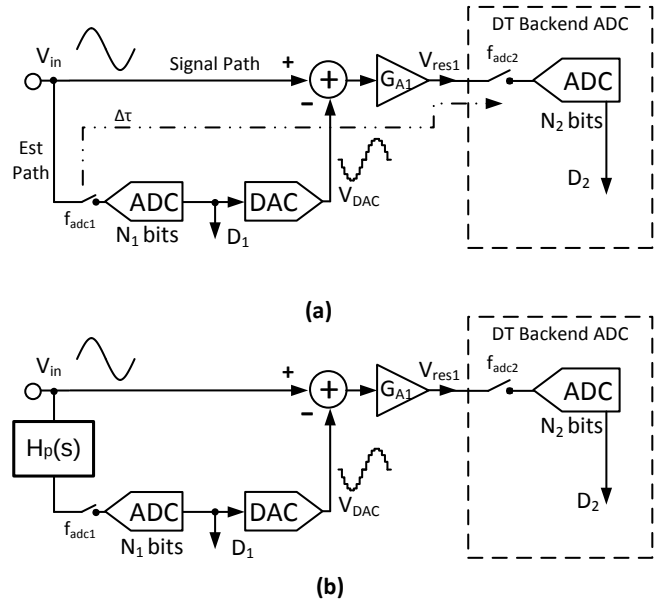


Fig. 1. (a) CTIP ADC (b) CTIP ADC with predictive filter

improvements and much lower power consumption [1]. The major drawback with CTΣΔ is that they require GHz clocks with very low clock jitter [2], and the power requirement of generating these clocks is too expensive in applications where such a clock is not already present. Inter-symbol Interference (ISI) in the feedback DACs limits the performance of CTΣΔ ADCs with larger than single bit feedback DACs. CTΣΔ ADCs also have a feedback loop with memory so they can't be used in applications where different input signals are multiplexed to a common ADC.

Continuous Time Input Pipeline (CTIP) [3] are the Nyquist alternative to CTΣΔ as a continuous time ADC. Fig. 1 (a). shows the architecture of a CTIP ADC. They don't require a GHz clock and use multi-bit DACs without any ISI concerns. CTIP ADCs also reset every sample so they don't have any memory and are suitable for multiplexed applications. These ADCs have a favourable input impedance which doesn't require an input buffer and also provide some anti-alias filtering. Previously published work in this area [3] had very favourable $3k\Omega$ input resistance at the ADC input and built in anti-alias filtering. Despite this, it only achieved 9 ENOB of performance at 10MHz for a 26MHz sampling frequency and the architecture has not been widely adopted.

This work will analyse the bandwidth limitations of CTIP ADCs. It will propose a new CTIP architecture that can achieve signal bandwidths close to the Nyquist frequency. An All Pass Filter (APF) is demonstrated as an analog delay and redundancy in the frontend compensates for any phase non-

linearity. The signal delay benefits of resetting integrator gain stages that allow increased signal bandwidths are demonstrated. Also the noise filtering benefit of resetting integrator gain stages that preserves the medium resistive input benefit of CTIP ADCs is shown. The gain stage topology permits implementation using a feed-forward compensated op-amp which is a low voltage and lower power solution. The complete CTIP ADC design is implemented in TSMC's 65nm LP CMOS technology and simulation results will confirm the bandwidth improvements of the new architecture.

The paper is structured as follows: Section II analyses the bandwidth limitations of CTIP ADCs and presents a new architecture to overcome these limitations. Section III analyses the key building blocks: filter, gain stage and DAC to implement the new ADC architecture. Section IV proposes a design implementation of the CTIP ADC and Section V provides simulation results for the CTIP ADC. Finally the conclusions are then summarized.

II. Signal Bandwidth Analysis of CTIP ADCs

A symbolic diagram of a CTIP ADC is shown in Fig. 1 (a). The input signal is connected to two paths - the signal path and the estimation path. The estimation path uses a coarse quantizer to create an estimate of the input signal and a DAC to convert the digital signal back to the CT analog domain. The estimated signal is subtracted from the input signal and this residue signal is multiplied by the gain stage G_{A1}. The gained residue signal is then sampled and quantised by the backend ADC which can be a SAR, a pipeline or a sigma delta. The sampling thermal noise (kT/C) at the backend ADC input doesn't affect the overall ADC performance as referring the noise power to the ADC input attenuates it by G_{A1}^2. Hence the sampling capacitor size can be decreased, reducing the switch transients and distortion due to non-linear sampling switches. These effects are also attenuated by G_{A1}^2.

This sample and hold free ADC works well for static or slow moving signals. However for faster signals the sample delay time $\Delta\tau$ which is the difference between the delay of the estimation path τ_{EST} and that of the signal path τ_{SIG} limits the maximum signal frequency that can be used. In a simple case where τ_{EST} is zero, $\Delta\tau$ is the delay between the sampling instant of the estimation quantizer and the sampling instant of the backend ADC. As a consequence of this delay, the residue at the backend ADC input is given by

$$V_{res1} = G_{A1}\left[Asin\left(\omega_c\left(t+\frac{\Delta\tau}{2}\right)\right) - Asin\left(\omega_c\left(t-\frac{\Delta\tau}{2}\right)\right) + \frac{\Delta_Q}{2}\right], \quad (1)$$

where $\Delta_Q = V_{ref}/(2^{N_1}-1)$ is the quantisation error of the estimation quantizer, A is the amplitude of the input sinewave signal and ω_c is the angular frequency of the input signal. This ADC operates correctly provided there are no saturation or over-range errors at the backend ADC input. To prevent over-range errors occurring, the maximum residue voltage V_{res1} must be less than half the reference voltage V_{ref} of the backend ADC. By setting $t = 0$ and $A = V_{ref}/2$, solving gives an equation for the maximum signal frequency f_c,

$$f_c \leq \frac{1}{\pi\Delta\tau}\cdot sin^{-1}\left(\frac{\left(1-\frac{G_{A1}}{2^{N_1}}\right)}{2G_{A1}}\right). \quad (2)$$

Evaluating this architecture using $\tau_{EST} = T_S/3, \tau_{SIG} = 0$, $G_{A1} = 8$ and with the number of bits in the first stage $N_1 = 5$, this ADC would be expected to achieve a bandwidth of $\approx 0.045 f_S$ where f_S is the ADC sampling frequency. This is like an oversampled ADC with an Oversampled Ratio (OSR) of 11. To minimise $\Delta\tau$ and increase the maximum f_c it is necessary to understand the block delays. τ_{EST} is the sum of the propagation delays of the estimation path

$$\tau_{EST} = \tau_{EQ} + \tau_{DAC} + \tau_{AMP_DAC}, \quad (3)$$

where the quantizer delay (τ_{EQ}) is the propagation time from the sampling clock edge of the quantizer until the output data is ready, the DAC delay (τ_{DAC}) is the delay from DAC input until the output is ready and the op-amp delay (τ_{AMP_DAC}) is the delay from the DAC transition until the op-amp has settled. Section IV contains further discussion on these delays. For the proposed 100MS/s sampling frequency CTIP ADC, the values of $\tau_{AMP_DAC} = 2.5ns$, $\tau_{EQ} = 0.6ns$ and $\tau_{DAC} = 0.2ns$ are used giving $\tau_{EST} = 3.3ns$. The reasons for these values are given in Sections III and IV. The only delay in the signal path is the op-amp delay, therefore $\tau_{SIG} = \tau_{AMP_SIG}$. There is a different op-amp propagation delay for the estimation and signal paths due to the nature of the two signals. This is discussed further in the Appendix. $\Delta\tau$ can be written as

$$\Delta\tau = \tau_{EST} - \tau_{SIG} = \tau_{EQ} + \tau_{DAC} + \tau_{AMP_DAC} - \tau_{AMP_SIG}. \quad (4)$$

To overcome the bandwidth limitation of the CTIP ADC, a solution is to use predictive filtering [3]-[4] in the estimation path. For periodic signals such as sine waves, future values can be estimated from previous outputs. Predictive filters operate on band-limited signals and look ahead to cancel the sample delay $\Delta\tau$. The CTIP ADC in [3] uses an analog prediction filter in the estimation path. The architecture is shown in Fig. 1(b). The filter has a positive phase which creates a time advance τ_{PF} to reduce the sample delay $\Delta\tau$,

$$\Delta\tau = \tau_{EQ} + \tau_{DAC} + \tau_{AMP_DAC} - \tau_{AMP_{SIG}} - \tau_{PF}. \quad (5)$$

The disadvantage is that prediction filters have 0dB gain at lower signals but high pass gain at higher frequencies signals. This means that this solution can only convert a fraction of the Nyquist signal band. The filter in [3] is a custom filter for the case in that paper, it is not a general filter design so it is difficult to migrate it to compensate for different delay values.

Instead of trying to reduce τ_{EST}, the limited bandwidth of CTIP ADCs can be improved by adding a delay in the signal path. This solution works by adding a delaying filter τ_{Filt} to

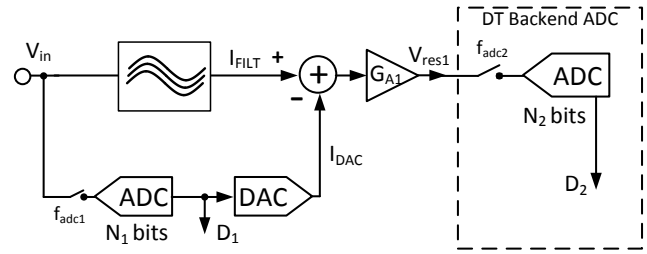


Fig. 2. CTIP ADC with delaying filter in the signal path

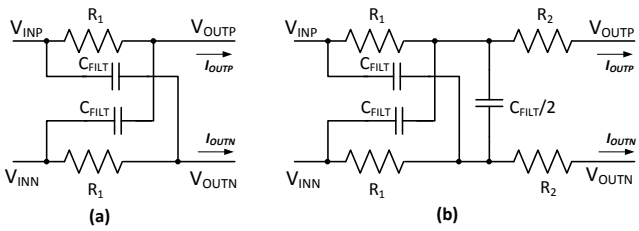


Fig. 3. (a) All-pass filter (b) Modified All-pass filter

equalise the different delays in the signal and estimation paths for the complete frequency range

$$\tau_{SIG} = \tau_{Filt} + \tau_{AMP_SIG} \approx \tau_{EST}. \quad (6)$$

The new proposed CT architecture is shown in Fig. 2.

A simple passive differential Low Pass Filter (LPF) can be used as the delaying filter. The phase of the filter, $\phi = -\tan^{-1}\omega CR$ is non-linear and has maximum phase of 90° so it can only compensate for a limited frequency range or small delay $\Delta\tau$. For larger delays the magnitude response of the LPF will also attenuate the signal path and cause mismatch between it and the estimation path creating out of range errors at the input to the backend ADC.

A better solution is the All Pass Filter (APF) shown in Fig. 3(a), the cross coupled capacitors create a right half plane zero and a left half plane pole. The APF in Fig. 3(a) has the transfer function

$$H(s) = \frac{V_{OUT_{diff}}}{V_{IN_{diff}}} = \frac{(1 - j\omega C_{FILT} R_1)}{(1 + j\omega C_{FILT} R_1)}. \quad (7)$$

It has a flat magnitude response and its phase is given by a non-linear function $\phi = 2\tan^{-1}(\omega C_{FILT} R_1)$ with a maximum value of 180°. The filter is designed by setting $\phi \approx \omega\Delta\tau$ where ω is the maximum angular signal frequency. A similar APF has been employed in a cascaded CTΣΔ ADC [5] to convert the quantization error at the output of the first stage.

A Simulink simulation of the CTIP ADC SNDR with different filters at different tone frequencies is shown in Fig. 4. The estimation quantizer has redundancy as it has 5 bits while the residue gain is only 8, the requirement for this redundancy is discussed in Section III A. The bandwidth for the no filter case agrees with the result of (2). A low pass filter as an analog delay shows increased bandwidth up to $f_S/4$. The CTIP APF ADC achieves full Nyquist signal bandwidths.

This section analyzed the delays that limit the signal bandwidth in a CTIP ADC with no filtering. MATLAB

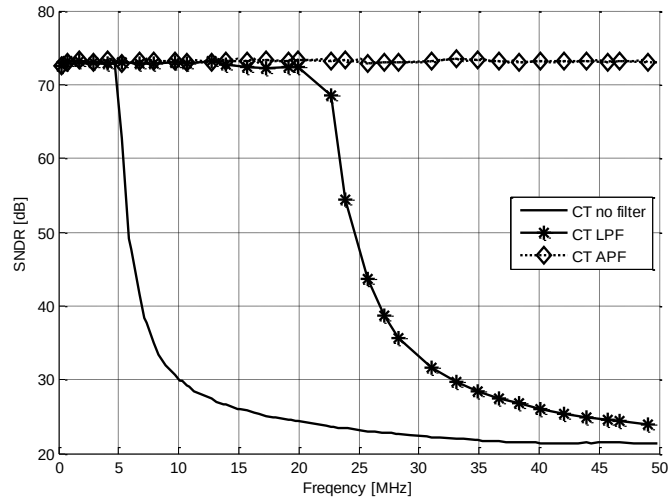


Fig. 4. Signal bandwidth comparison for a CTIP ADC with different filters. The APF filter is designed to have the correct phase at 50MHz, LPF simulation has the correct phase at 25MHz to maximize its bandwidth. Simulation has frontend gain of 8, a backend ADC with 9 bits clocked at 100MS/s and a 5 bit estimation quantizer clocked at 300MS/s which generates a sample time delay of Δτ=3.33ns.

simulations for a new ADC demonstrate that a CTIP ADC with an APF filter delay in its signal path combined with quantizer redundancy to compensate for filter non-linearity can achieve full Nyquist signal bandwidths.

III. KEY BLOCKS IN CTIP ADC

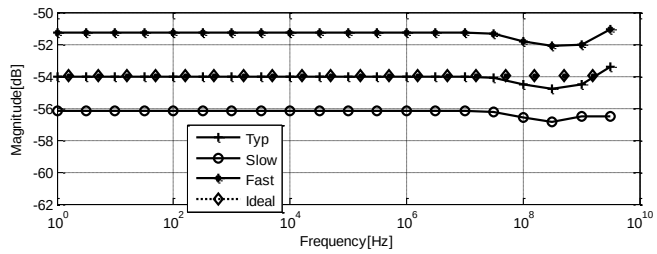
The results shown in Fig.4 demonstrate that a CTIP ADC with a full Nyquist signal bandwidth is achievable. Those simulations contain ideal components and do not take into account linearity, gain stage settling, thermal noise and DAC matching. Overcoming these limitations is essential to build a robust CTIP ADC. In this section the necessary key blocks to implement the CTIP ADC in Fig. 2 will be addressed.

A. All Pass Filter

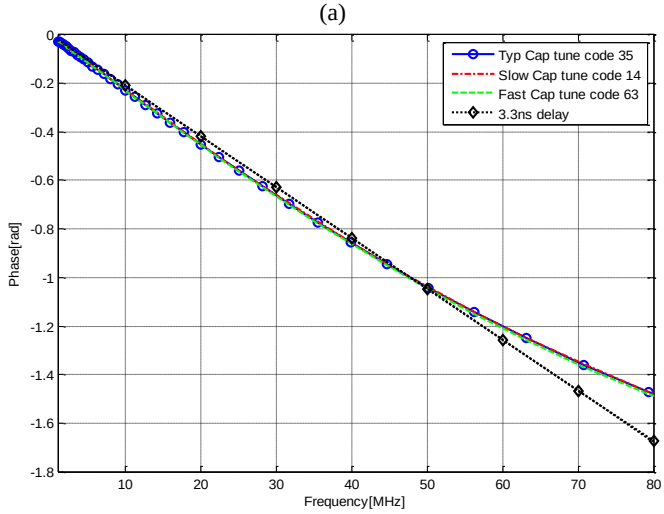
The APF circuit in Fig. 3(a) has a voltage transfer characteristic. It is desired that the filter has a trans-resistance or voltage to current transfer function so that it can be connected to the virtual ground node of the op-amp in the gain stage and convert the input voltage to an output current. A modified APF is shown in Fig. 3(b). APF resistor and capacitor values can be modified to minimise the filter area but for simplicity if $R_1 = R_2$, the transfer function is given by

$$\frac{I_{OUT_{diff}}}{V_{IN_{diff}}} = \frac{(1 - j\omega C_{FILT} R_1)}{2R_1(1 + j\omega C_{FILT} R_1)}. \quad (8)$$

The capacitor values can be trimmed so the filter can be adjusted for process variations. Fig. 5 shows plots of the simulated magnitude and phase response for a circuit implementation of Fig. 3(b). Three process corners typical, fast and slow are plotted. Each corner has a different capacitor value each tuned to ensure the APFs have the same phase as the delay Δτ at 50MHz. The magnitude responses are different due to resistor process variation but their magnitudes versus frequency response shows only a small deviation from DC. Compared to the linear delay ωΔτ, the tuned APF response has



(a)



(b)

Fig. 5. (a) magnitude response of the output current of the APF versus frequency for process corners. (b) is the phase response of the trimmed filter corners versus the phase shift ωΔτ of a 3.3ns delay. Δτ=3.3ns is an estimate of the delay for a 100MS/s CTIP implementation.

a bow shape. At the frequencies where the APF deviates from the linear delay, saturation errors can occur at the backend ADC input. Redundancy is used in the estimation path to avoid the requirement that the APF delay must coincide exactly with $\Delta\tau$ and to make the system robust.

Fig. 6 compares the CTIP ADC results for (a) no redundancy - 3 bits for estimation path quantizer and (b) 2 bits of redundancy - 5 bits for estimation path quantizer. As there is no redundancy, the quantization noise Δ_Q will occupy the full voltage range V_{res1} (1) at the backend ADC input. Without redundancy the CTIP ADC will only work to the full 12 bit resolution when $\Delta\tau = 0$ or $\tau_{EST} = \tau_{SIG}$. Due to the non-linear phase characteristic of the APF, this only occurs at DC and 50MHz the frequency at which the filter delay was designed.The bow SNDR shape in Fig. 6 arises from the deviation from linear phase of the real APF as shown in the phase plot of Fig. 5. With redundancy in the estimation path, the CTIP ADC can tolerate non-linearity in the APF. The 5 bit SNDR plot in Fig. 6 has 2 bits of redundancy in the estimation path allowing the APF delay to enable signal bandwidths up to the Nyquist frequency.

B. Resetting Integrator Gain Stage

Like its discrete time pipeline equivalent, the gain stage is the key building block in CTIP ADCs. The gain stage must provide gain but it has two other important requirements. Firstly a signal path delay is required to assist the APF delay (6) enabling increased signal bandwidth. Secondly the gain stage must also provide noise filtering. Fig. 7 (c) illustrates the noise equivalent circuit for the CTIP ADC. The thermal noise

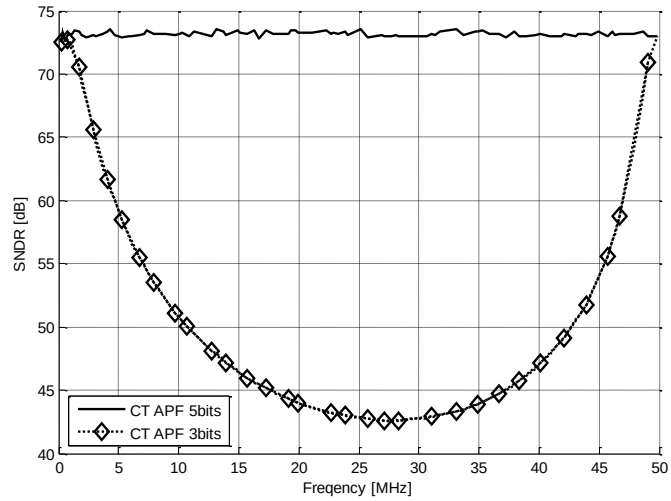


Fig. 6. A plot of the SNDR of the CTIP APF ADC with 5 bit and 3 bit estimation path quantizers. The 3 bit quantizer shows the effect of the non-linear phase of the filter when the estimation path doesn't have redundancy.

of the input resistor, current steering DAC and the input referred noise of the gain stage are filtered by the transfer function of the gain stage and then folded in band by the sampling switch of the backend ADC. A very wideband gain stage will provide very little noise filtering and using a smaller input resistor R_{IN} is the only way to prevent thermal noise from limiting the CTIP ADC resolution. To preserve the medium resistive input benefit of CTIP ADCs, filtering in the gain stage is essential. A resetting integrator gain stage [3] can meet these requirements. The remainder of this section analyzes the resetting integrator gain stage. The Appendix analyzes an alternative resistive gain stage so a comparison can be performed.

The resetting integrator circuit is shown in Fig. 7(a). The input resistor R_{IN} converts the input voltage into a current, it is then summed with the DAC current and integrated in the capacitor C_{INT} for a time T_{INT}. A timing diagram in response to a DAC step input $I_{DAC}(t)$ is shown in Fig. 7(b). On the falling edge of ϕ_{reset} the reset switch opens and charge begins to accumulate on the capacitor C_{INT}. This produces a ramp voltage $V_O(t)$. T_{INT} seconds later, the backend ADC sampling clock ϕ_{adc_samp} samples the integrator voltage and the sampled voltage $V_S(t)$ is quantized by the backend ADC.

A Gm-C version of the resetting integrator was used in an RF receiver application [6] with detailed analysis of the circuit provided. Applying similar analysis gives the following s-domain transfer function for the windowed integrator. The basic transfer function is an ideal integrator $H_{INT}(s) = -1/sR_{IN}C_{INT}$ minus a delayed version of itself

$$H_{RINT}(s) = H_{INT}(s)(1 - e^{-sT_{INT}}). \quad (9)$$

An interesting analogy is made in [6] describing this as operating like a continuous time FIR filter prior to sampling. Re-writing the equation highlights the filtering property

$$H_{RINT}(s) = -\frac{T_{INT}}{R_{IN}C_{INT}}\frac{(e^{sT_{INT}/2} - e^{-sT_{INT}/2})}{sT_{INT}}e^{-sT_{INT}/2}. \quad (10)$$

This has a Sinc filter response with gain $T_{INT}/R_{IN}C_{INT}$, signal delay $\tau_{AMP_SIG} = T_{INT}/2$ and nulls at frequencies which are

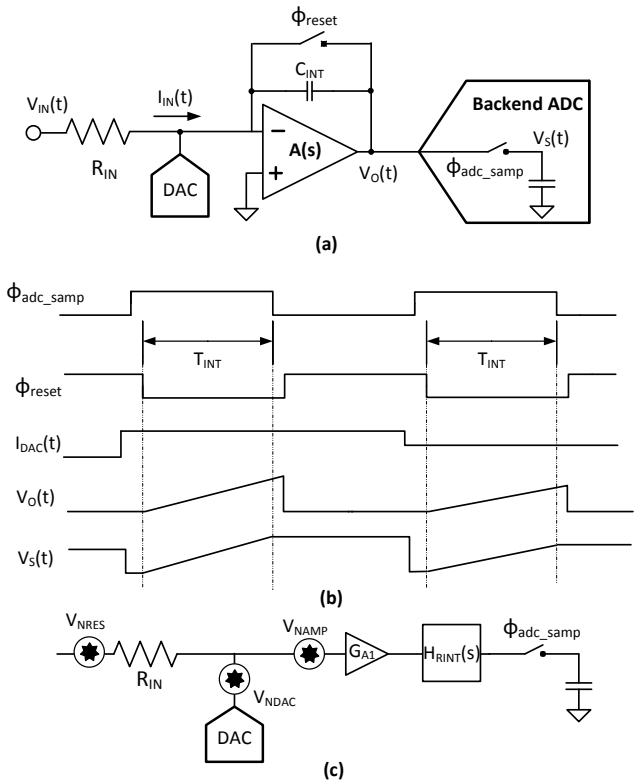


Fig. 7. (a) Resetting integrator stage as part of CTIP ADC. (b) Timing diagram of a response to a DAC step. In this diagram ϕ_{reset} is the signal to short the integrator capacitor and return $V_O(t)$ to 0V, integration occurs when ϕ_{reset} is low. $I_{DAC}(t)$ is the DAC output current, $V_O(t)$ is the gain stage voltage response to the DAC current step and ϕ_{adc_samp} is the backend ADC sampling clock. ϕ_{adc_samp} samples $V_O(t)$ on its falling edge and it is stored as $V_S(t)$. T_{INT} is highlighted, it is the gain stage integration time and starts when the reset switch opens and ends at backend ADC sampling. (c) Noise equivalent circuit for the CTIP ADC.

integer multiples of $1/T_{INT}$. Unlike the resistive gain stage where gain is a ratio of resistors or a switched capacitor gain stage where gain is a ratio of capacitors, this gain depends on a clock time divided by a RC product and will need to be trimmed. The trim is implemented as a coarse capacitor trim and a fine digital gain calibration described in Section IV.

Adding the effects of a real single pole op-amp to the integrator gives the following integrator transfer function

$$H_{INT}(s) = -\frac{A_0}{(1 + sR_{IN}C_{INT}A_0)(1 + s/2\pi f_{GBW})}, \qquad (11)$$

where the amplifier gain bandwidth frequency $f_{GBW} = A_0 \times f_{3dB}$ and f_{3dB} is the op-amp dominant pole frequency. The magnitude and phase frequency response of the resetting integrator using this equation are shown in Fig. 8. The magnitude response shows the improved noise filtering compared to a resistive gain stage. The noise bandwidth for the resetting integrator gain stage has been derived for a similar integrating gain stage [7] and is equal to $1/2T_{INT}$. The input referred voltage noise power from the input resistors is

$$V_{RN}^2 = \frac{2kTR_{IN}}{T_{INT}}. \qquad (12)$$

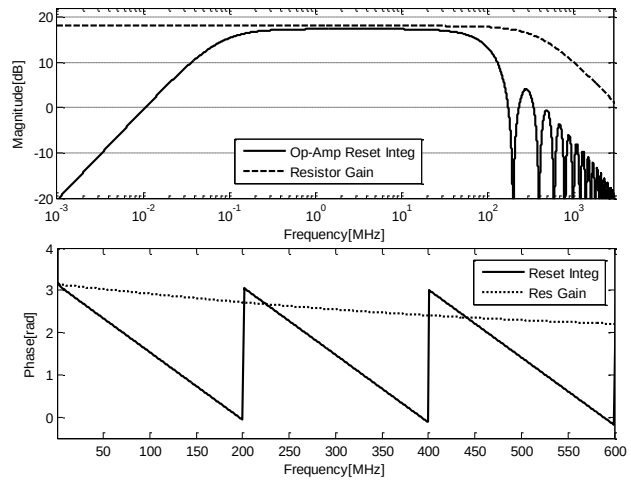


Fig. 8. AC magnitude and phase response of resetting integrator gain stage with A_0 = 70dB and a dominant pole f_{3dB} of 1MHz versus resistive gain stage with $f_{GBW} = A_O \times f_{3dB} = 4GHz$. The magnitude response of the resetting integrator doesn't work at very low signal frequencies due to finite op-amp gain A_0, it has flat response for the rest of the signal band and then has steep roll off. The phase plot shows a linear delay in the signal band with a phase delay of π radians at frequency $1/T_{INT}$, this shows that the gain stage provides a uniform delay of $T_{INT}/2$ seconds.

For a 12 ENOB ADC at 100MS/s with $T_{INT} = 5ns$, the noise bandwidth is 100MHz. This ADC would require a 500Ω input resistance which compares very favourably to the 75Ω required by the settling resistive gain stage in the Appendix. The extra noise filtering allows the input resistance to be kept at a medium value saving power in the DAC and in the input buffer preceding the ADC.

The integrator time response to a DAC step is the inverse Laplace transform of I_{DAC}/s multiplied by (11)

$$v_{OUT}(t = T_{INT}) = -\frac{I_{DAC}R_{IN}T_{INT}}{R_{IN}C_{INT}} \times \left(1 - \frac{1}{T_{INT}2\pi f_{GBW}}\left(1 - e^{-T_{INT}2\pi f_{GBW}}\right)\right). \qquad (13)$$

The decaying exponential gain error needs to be less than half an LSB of the backend ADC, solving this for $T_{INT} = 5ns$ gives value of $f_{GBW} = 1GHz$. With $\tau_{AMP_DAC} = T_{INT}$, Fig. 8 and (10) show that the signal path delay $\tau_{AMP_SIG} = T_{INT}/2$. Using (4) and (6) to solve for the required filter delay gives

$$\tau_{Filt} \approx \tau_{EQ} + \tau_{DAC} + T_{INT}/2. \qquad (14)$$

This feature is significant as only half the time allocated to τ_{AMP_DAC} must be equalized by the filter and larger signal bandwidths can be achieved.

As T_{INT} in Fig. 7 depends on the falling edge of the reset clock and the falling edge of the backend ADC sampling clock, the jitter on both of these clock edges will effect T_{INT} and hence the gain. Analysis of the effect of jitter in an ADC sampling with a resetting integrator gain stage [8] demonstrates a reduced susceptibility to the effects of sampling jitter due to the integrated input signal and the integrated DAC signal having the same errors due to jitter. It is shown that for signals at $f_S/2$, the SNR of an ADC sampling with a resetting integrator gain stage is

TABLE I
SUMMARY OF REQUIREMENTS ON RESISTIVE GAIN STAGE VERSUS RESETTING INTEGRATOR GAIN STAGE

Feature	Resistive Gain Stage	Resetting Integ Gain Stage
Sample time delay $\Delta\tau$ (ns)	3.33	3.33
Settling time τ_{AMP_DAC} (ns)	2.5	5
Op-amp f_{GBW} (GHz)	4	1
Noise BW (MHz)	700	100
R_{IN} (Ω)	75	500
Op-amp rail recovery Required	Yes	No
RMS jitter required for 12 bits @ $f_S/2$ (ps)	<0.7	<1

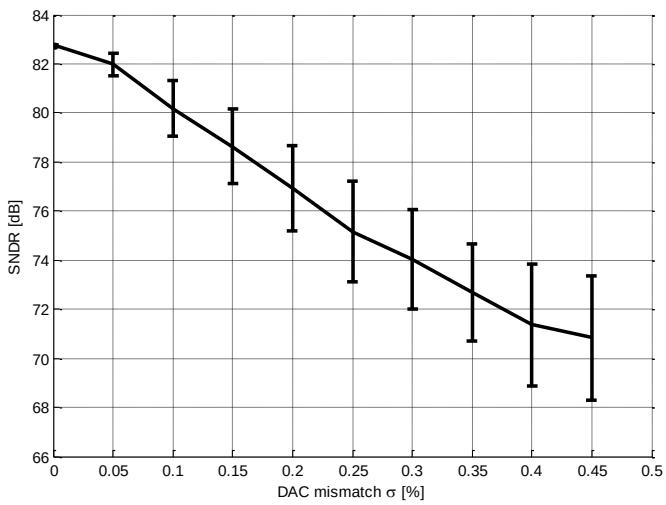


Fig. 9. Plot of mean (line) and standard deviation (error bar) versus complementary DAC mismatch sigma for a MATLAB SINAD simulation of a CTIP ADC. The same sigma value is used for the pMOS and nMOS DACs. A 5bit DAC is used in the simulation with gain=8 and 11bit backend ADC. Each simulation is run 100 times.

approximately 3dB better compared to any conventional impulse sampled ADC for the same sampling jitter.

A summary of the performance of the resetting integrator gain stages compared to the resistive gain stage in the Appendix is shown in Table I.

C. DAC

Jitter and Inter-symbol Interference (ISI) can limit the performance of CTΣΔ ADCs. In such ADCs, the DAC pulse is continuously integrated and so any deviations from an ideal pulse cause errors in the ADC conversion [2]. An advantage of the CTIP ADC with the resetting integrator is that jitter and ISI errors are avoided as the DAC output $I_{DAC}(t)$ changes while the gain stage is being reset. As shown in Fig. 7 (b) $I_{DAC}(t)$ transitions while the reset switch is high, in this case the output current has settled before the reset switch opens and integration starts. Only the static magnitude variation of the current sources limits the overall ADC performance not their dynamic behaviour.

Fig. 2 shows the estimation path signal I_{DAC} that is subtracted from the delayed input I_{FILT}. Despite only reconstructing several bits, the DAC output signal must be accurate to the full resolution of the CTIP ADC. Fig. 9 shows the SNDR of a MATLAB simulation of an ideal 14 bit CTIP ADC with mismatch in the DAC elements. The DAC is a

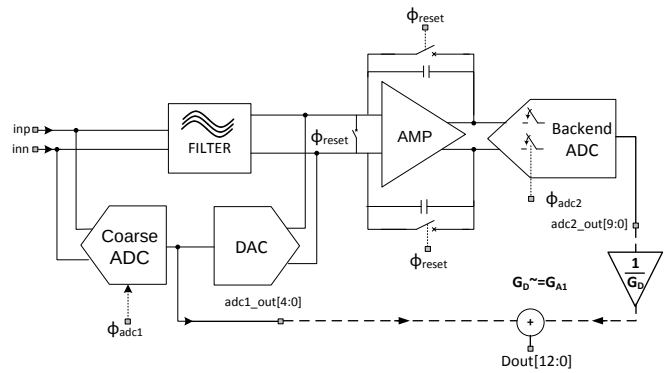


Fig. 10. Complete architecture of CTIP ADC with APF

differential complementary DAC [9] with separate sink and source DACs with different mismatch parameters. The simulation uses a 14 bit model as it is desired that the DAC non-linearity will be the dominant non-linearity for this simulation. This simulation shows that to achieve CTIP ADC SNDR of 12 ENOB (74dB) requires a 5 bit DAC sigma of 0.3% or less. The DAC DNL is the same as the DAC sigma so the 5 bit DAC must have maximum DNL of 0.3% LSB for a 5 bit DAC or 0.39 LSB when referred to 12 bit resolution.

IV. CIRCUIT IMPLEMENTATION

The architecture trade-offs in the CTIP ADC which led to the resolution partition between the estimation quantizer and backend ADC will now be discussed. More than 2 bits of resolution in the first stage of pipelined ADCs is desired because it helps to achieve lower power consumption and better linearity [10]. From (10), the gain of the resetting integrator is $T_{INT}/R_{IN}C_{INT}$. It has also been shown in (12) that the integrated thermal noise of the CTIP ADC is proportional to R_{IN}/T_{INT}. The conversion rate of the ADC also constrains T_{INT}. Therefore C_{INT} is the only free variable to control the gain. Smaller gain would require larger C_{INT} and more power would be consumed by the op-amp to maintain the integrator bandwidth.

As discussed in Section III A, two bits of redundancy in the estimation quantizer are required to allow for comparator offsets and APF group delay non-linearity, hence the number of bits in the first stage is $N_1 \geq 2 + \log_2 G_{A1}$. Therefore setting $G_{A1} = 16$ would require a 6 bit estimation quantizer. For low propagation delay, a flash ADC is used for the estimation quantizer. A flash ADC consists of a reference resistor ladder and $2^{N_1} - 1$ comparators in parallel. Overcoming the input offset of comparators due to mismatch requires large devices; these larger devices have larger parasitic capacitances so the comparators are slower or require more power to achieve fast conversion rates. This means that a 6 bit flash ADC will consume more than twice the power of a 5 bit flash ADC [11]. Taking these trade-offs into account, $G_{A1} = 8$ is chosen for this design as a 5 bit flash is realizable without consuming significant power.

Fig. 10 shows a diagram of the complete CTIP ADC with APF architecture. The filter implementation has already been discussed in Section III A. A differential implementation of the resetting integrator is shown with an extra reset switch

added which shorts the inputs. The purpose of this switch is to be a low resistance path shorting the differential input resistors and DAC outputs together during reset to ensure that the input and DAC currents don't cause shifts in the op-amp input voltages. The frontend quantizer is a flash ADC and the DAC is current steering. The backend ADC has 10 bits to ensure that the quantisation noise of the complete ADC will be below the thermal noise floor.

The resetting integrator gain stage doesn't produce a high precision gain like that produced by a ratio of resistors or capacitors. At ADC turn on, a one-time ramp test should be performed to measure the gain G_{A1}. The backend ADC digital output word is multiplied by the reciprocal of this measured gain $1/G_D$ so that the ADC performs to the desired accuracy. Key design blocks in the ADC architecture will now be discussed.

A. *Resetting integrator*

From the integrator model in (11) f_{3dB} and A_0 are swept to find the required values to achieve the resetting integrator gain of approximately 8. The sweeps show a specification of $A_0 = 70dB$ and f_{3dB}=5MHz are required to get close to the desired gain. A traditional single pole op-amp or dominant pole compensated op-amp with this specification would require the unity gain frequency $f_{GBW} = A_0 \times f_{3dB} \geq 15GHz$ and a non-dominant pole at 2-3 times this frequency. Recent CTΣΔ ADCs have solved this problem by using multi-stage Feed Forward (FF) compensated op-amps [12]-[13] which have more than one pole in their frequency response so their unity gain frequency is no longer the product of A_0 and f_{3dB}.

It is desired that the op-amp has a single ended output voltage swing of $0.8V_{PK-PK}$, with a 1.2V supply voltage this leaves minimal voltage headroom for the output MOS devices. The result of this is an output stage with low gain and thus a two stage op-amp will not achieve $A_0 = 70dB$. A three stage

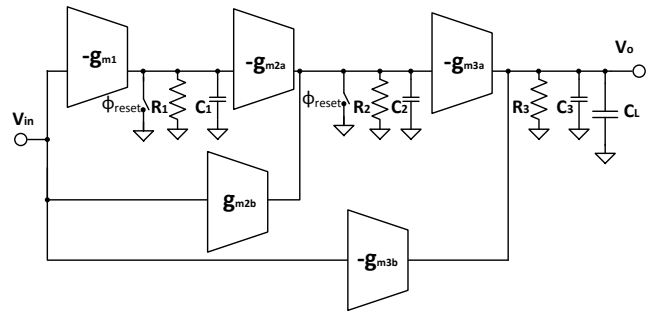


Fig. 11. Symbolic Diagram of FF Op-amp

FF op-amp topology [13] is required. Fig. 11 shows a symbolic diagram of a three stage FF compensated op-amp. Fig. 12 shows the schematic of the three stage FF op-amp [13]. This topology allows the feed forward paths g_{m2b} and g_{m3b} to be implemented without requiring any additional power. Stage 1 dominates the integrated noise performance of the op-amp, it has high gain so the noise contributors of subsequent stages are strongly attenuated.

The noise filtering characteristic of the resetting integrator (Fig. 8) ensures the noise requirements for the op-amp are relaxed, saving power in the first stage. The third stage is designed to be wide bandwidth and have a large output swing so it can drive the integrator and backend ADC capacitors and so it doesn't distort any large signal voltages. The second stage is optimised to achieve a stable integrator and achieve the desired overall op-amp gain. Each stage in the op-amp has its own local Common Mode Feedback (CMFB) with resistor dividers added to each of the op-amp stages to sense the stage output common mode voltages. The separate CMFB stages are easier to stabilise than a multi-stage solution.

A CTΣΔ ADC built in 28nm CMOS with a similar op-amp topology [5] has a signal bandwidth of 465MHz so this op-amp topology's speed will improve with process scaling.

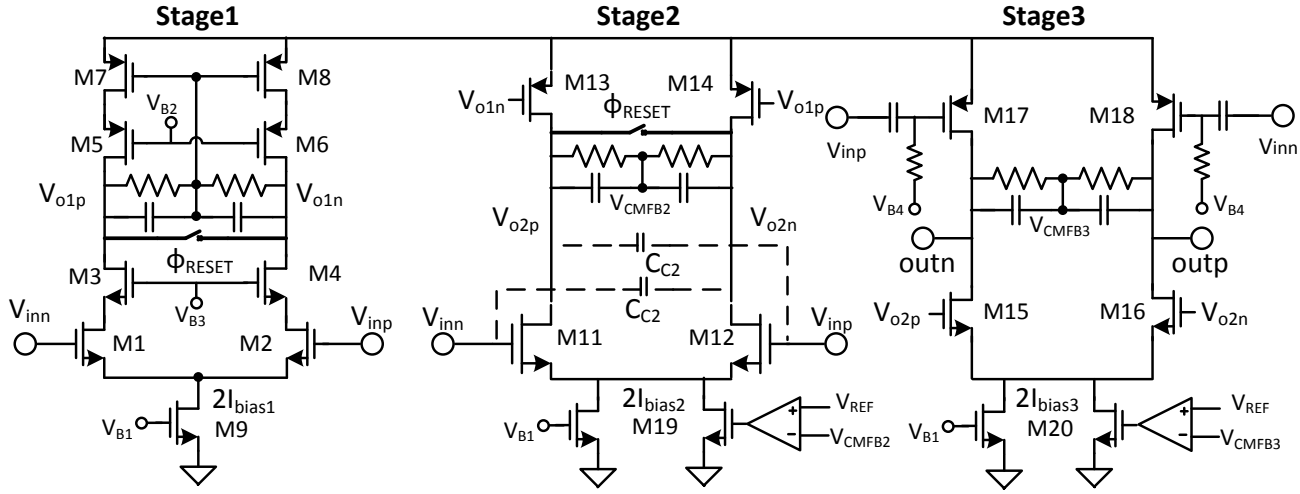


Fig. 12. Three stage FF Op-amp [21]. This topology allows the feed forward paths g_{m2b} and g_{m3b} to be implemented without requiring extra current. The positive feedback capacitors C_{C2} can boost the bandwidth of the second stage feed forward path [22]. AC coupling is required for g_{m3b} as the pMOS output device requires a different bias. Reset switches are shown in stages 1 & 2, these short the differential outputs attenuating the differential signal. The common mode circuits are shorted together and the CMFB circuits keep the stages at the correct bias voltages.

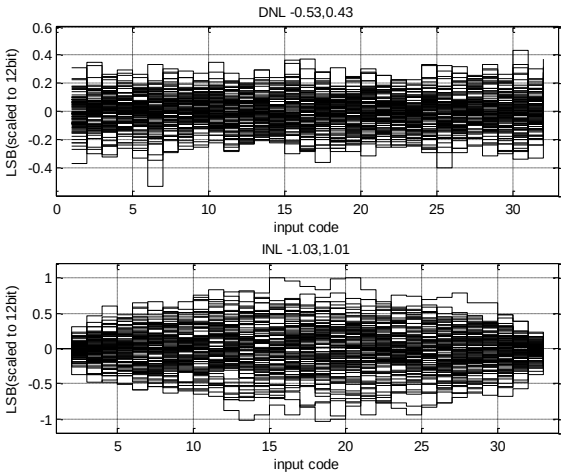


Fig. 13. Monte Carlo simulation of the 5bit current steering DAC. DNL and INL are converted to 12bit resolution. Maximum DNL is 0.53LSBs, max INL is 1.03LSBs.

B. Coarse Quantizer (flash) and DAC

A flash ADC is a good choice for a low latency, low resolution estimation path quantizer as it consists of $2^{N_1} - 1$ comparators in parallel. The quantizer propagation delay τ_{EQ} is due to delay in the flash comparators. The latch in the flash comparator has an exponential gain and needs a certain decision time to avoid metastability and ensure the overall CTIP ADC meets the desired Bit Error Rate (BER). The DAC delay τ_{DAC} is due to the propagation delay on the input logic that drives the DAC switches. CTΣΔ ADCs require their flash ADC to make their decisions and pass the decision to the feedback DAC in one clock cycle [1]. A published CTΣΔ ADC in 65nm CMOS [14] uses a 4GHz clock so its delays for τ_{EQ} plus τ_{DAC} are less than 250ps. The regeneration time constant of the flash comparators gets smaller with advanced technologies as does the delay of the DAC input logic. As a result τ_{EQ} and τ_{DAC} will get smaller with advanced technologies thus enabling CTIP ADCs with faster rates.

A current steering complementary DAC architecture is used [9] as it can be connected directly to the coarse quantizer comparators for low latency. Having this direct connection with the flash ADC comparator output driving the DAC current switches avoids any extra propagation delays due to latency of decoders or encoders. The DAC is not clocked and updates asynchronously as soon as the individual flash comparators make their decisions. Fig. 9 showed that the 5 bit DAC must have linearity greater than the overall resolution of the CTIP ADC. Due to the low supply voltage (1.2V) there is only 0.6V of headroom for each of the nMOS and pMOS DACs, this means the V_{DSAT} of the current sources is smaller than desired. Fig. 13 shows the Monte Carlo circuit simulation results of the DAC output current DNL and INL. The maximum DNL is 0.4% of the 5 bit DAC LSB which is 0.53 LSBs for an equivalent 12 bit DAC.

C. Backend ADC

The backend ADC can be any switched capacitor ADC that can sample the voltage at the resetting integrator output and convert it to a digital word. As discussed in Section III B the backend ADC sampling instant controls the inter-stage gain (10) through determination of T_{INT}. Hence the backend ADC rms sampling jitter must enable the sampling to be accurate to the complete CTIP ADC resolution (12 bits) [8]. An existing 10 bit 150MS/s interleaved SAR ADC with measured SNDR of 55dB was used as the backend ADC. The SAR ADC sampler was modified so that its sampling clock meets the jitter requirements as detailed in Section III B.

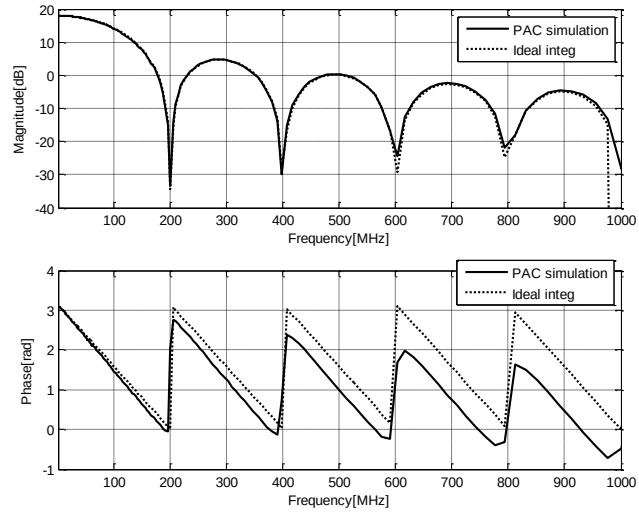


Fig. 14. PAC simulation results of the resetting integrator transfer function versus an ideal resetting integrator

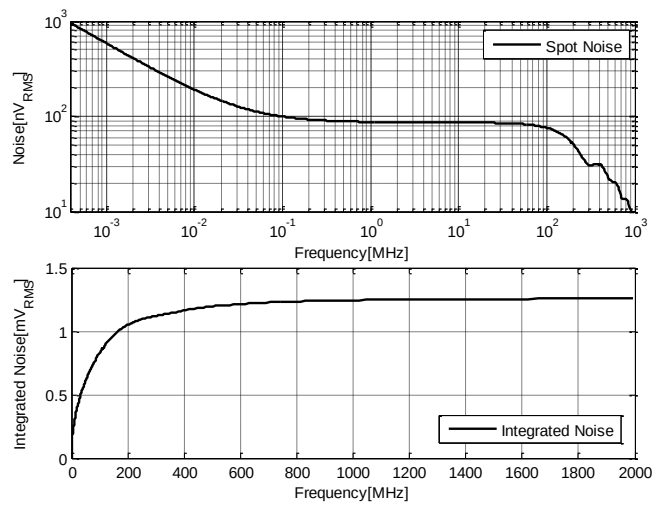


Fig. 15. Periodic noise simulation results of resetting integrator. Spot noise is plotted in top plot and integrated noise versus frequency in the lower plot. Spot noise and rate of increase of integrated noise both reduce at 200MHz showing the effectiveness of Sinc filtering.

V. Simulation Results

The CTIP ADC was designed using TSMC LP 65nm CMOS technology. Simulation results are presented for the resetting integrator to demonstrate its filter characteristic (10). A Periodic AC (PAC) simulation of the resetting integrator produces the plot in Fig. 14. This simulation used an ideal clock generator and ideal switches to reduce simulation runtime. The magnitude results match the plot of an ideal

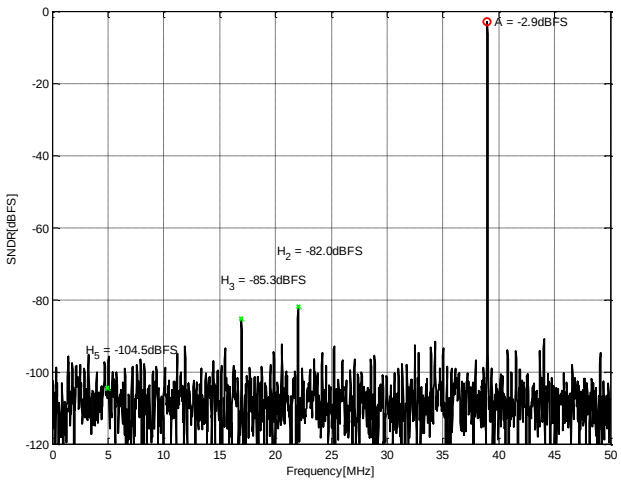


Fig. 16. SNDR for 39MHz tone. $G_D = 8.68$

resetting integrator, albeit with reduced attenuation at the null frequencies. The phase plot agrees with the ideal model at low frequencies but at higher frequencies the finite op-amp bandwidth causes extra phase delay, shifting the periodic phase response.

Periodic noise (PNOISE) simulations were run to prove that the input resistors, DAC and the op-amp MOSFET noise are filtered by the resetting gain stage Sinc characteristic. Fig. 15. shows the spot noise and integrated noise plots for the simulation. The spot noise shows a steep drop in magnitude at the frequency of this first null (at 200MHz) and the rate of increase of the integrated noise slows above this frequency. The dominant noise sources in the simulation are the input resistors, op-amp first stage differential pair, op-amp first stage pMOS bias and the current bias devices of the DAC. Taking the spot noise at 1MHz and applying the noise bandwidth $1/2T_{INT}$ (12) gives an integrated noise of $0.87mV_{RMS}$ compared to a result from the integrated noise plot of $1.3mV_{RMS}$. The difference in values is due not all the op-amp noise being filtered and due to the real resetting integrator not providing ideal Sinc filtering due to finite null depth. However the PNOISE simulation proves the noise filtering of the resetting integrator. Comparing the integrated noise to a $1.6V_{PK-PK}$ differential input signal gives a signal to thermal noise of 71.1dB.

Fig. 16 shows the FFT of the ADC output for a typical corner simulation with mismatch enabled for a 39MHz signal tone. with a $1.6V_{PK-PK}$ input. The second, third and fifth harmonics are highlighted. A SNDR of 70.5dB is shown in this plot. The distortion is due to nonlinearity of the DAC and nonlinearity in the gain stage. Without mismatch the simulation produced SNDR of 73dB with the second harmonic distortion $H_2 = -97.2dB$. The difference between the simulations is due to the input offset of the op-amp created by mismatch in the differential pair.

Fig. 17 shows the performance versus input frequency. Above 42MHz the filter phase delay is less than the estimation path delay and an over-range error occurs in the backend ADC input causing a sharp drop in performance. The black lines show simulation results without mismatch and the colored lines show simulation results with mismatch. The SNDR at

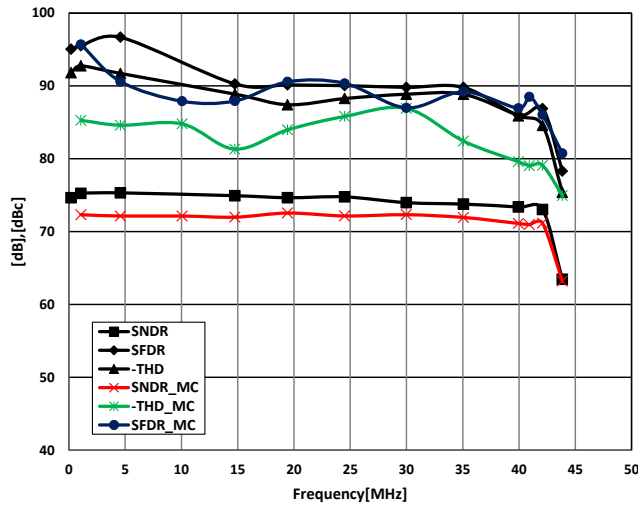


Fig. 17. SNDR, SFDR and THD simulation results versus input frequency for $1.6V_{PK-PK}$differential input voltage. $G_D = 8.68$

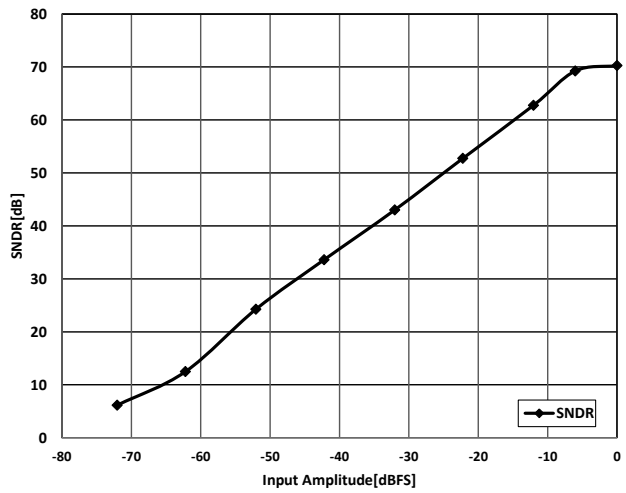


Fig. 18. SNDR versus input amplitude for an input tone at 42MHz. Full scale is $1.6V_{PK-PK}$. $G_D = 8.625$

20MHz drops from 74.7dB to 72.6dB due to mismatch. All simulations use the same calibrated gain value for $1/G_D$ as shown in Fig. 10.

Fig 18 plots the SNDR versus input amplitude. At higher input amplitudes the DAC steps are larger and the mismatch of the output impedances of the nMOS and pMOS DACs and larger residue signals in the gain stage cause increased distortion. Above -6dBFS the distortion limits the SNDR of the ADC. Fig. 19 gives the power breakdown for the CTIP ADC in mW with the integrator op-amp dominating power consumption. The rightmost columns of Table II show a comparison between the simulation results of this work and measurement results of the previously published CT Pipeline ADCs [3] and [15]. This work demonstrates a bandwidth improvement compared to [3]. The recently published CTIP ADC by Shibata et al [15] shows a huge bandwidth improvement but at the cost of this is a high power consuming FIR filter run at the oversampled clock rate 9GHz to compensate for the filtering gain stage. In contrast this work only requires a frequency independent gain calibration.

TABLE II
PERFORMANCE OF THIS WORK AND COMPARISON WITH STATE OF THE ART CT IP AND 1.2V PIPELINE 100MHZ ADCS WITH SNDR >= 70DB.

Reference	Dong [13]	Shettigar [18]	D-Y Yoon [19]	Van der Vel [20]	Panigada [17]	Gubbins [3]	Shibata [15]	This Work
Architecture	CT ΣΔ	CT ΣΔ	CT ΣΔ	Pipeline	Pipeline	CT IP	CT Pipe	CT IP ADC
CMOS Technology[nm]	28	90	28	90	90	180	28	65
VDD[V]	0.9/1.8/-1	1.2	1.2/1.5	1.2	1.2	1.8	1/1.8/-1	1.2
SNDR[dB]	72.6	70.9	74.6	70	69.8	56 @10MHz	66 @ 1GHz	71.2 @42MHz
F_{SIG_MAX}[MHz]	45.7	36	50	50	50	10	1125	42
F_{SAMP} [MHz]	3200	3600	1800	100	100	26	9000	100
OSR	35	50	18	1	1	1.3	4	1.11
RMS Clock Jitter[psec]	0.1					6	?	1
Power[mW]	235	15	78	250	130	21.4	2330	39
Z_{IN}	25Ω				4.5pF	3000Ω	200Ω	500Ω *
Schreier FOM[dB]	155.5	164.7	162.7	153	154.65	142.7	153.3	161.5
Walden FOM[fJ/conv]	721	72.7	177.7	967	577.6	892	520	128
Area [mm^2]	0.9	0.12	0.34	1	4	1.63	5.1	0.45

*CTIP ADC APF impedance behaves like a resistor

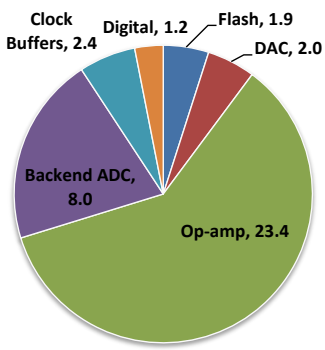


Fig. 19. Power consumption of CTIP ADC in mW.

Table II also shows a comparison between the simulation results of this work and measurement results of recently published ADCs with 70dB of SNDR and signal bandwidth of 50MHz. Comparison with the measured results of CTΣΔ ADCs in Table II [13], [18] and [19] shows that similar performance is achieved without the requirement for a GHz clock. The CTIP ADC power is comparable to the power consumed by state of the art pipelined ADCs [20] and [17]. These DT ADCs require an input buffer to settle a switched capacitor load in a fraction of the sampling period. Compared to these ADCs the CTIP ADC has easy to drive input impedence Z_{IN}. The CTIP ADC input impedance is not switched and can be easily driven by a low power buffer or even a combined active filter and buffer.

CONCLUSION

This paper presented analysis of the bandwidth limitations of CTIP ADCs. Based on this analysis a new CTIP architecture with an all pass delaying filter in the signal path was proposed. This architecture can achieve Nyquist signal bandwidths. The key components to achieve the CTIP ADC are presented. The APF simulated performance is shown versus process corners and its linearity is proven by the complete ADC performance. The resetting integrator signal path delay benefit is highlighted and demonstrated by simulation. The noise filtering benefit of the resetting integrator which is essential to achieve the 500Ω input impedance is also demonstrated by simulation. The resetting integrator gain stage is implemented as a low voltage stage using a feed-forward compensated op-amp. Comparison of the simulation results with the measured results of a previously published work highlights the bandwidth enhancement of this work. Comparison is also made with state of art CTΣΔ ADCs and DT Nyquist ADCs .The bandwidth limitations of this CTIP ADC are technology dependent and will reduce with advanced CMOS processes. Future work will remove the op-amp distortion limitation at the Nyquist frequency and will look to exploit the filtering benefits of this ADC architecture.

APPENDIX

A resistive settling Gain stage is presented so it can be compared to the resetting integrator gain stage in Section III B. An explanation for the difference between τ_{AMP_DAC} and τ_{AMP_SIG} will also be given. The frequency domain transfer function of the resistive gain stage in Fig. 20(a) where the op-amp has a single pole response with finite bandwidth f_{GBW} and finite DC gain A_o is

$$H_{RG}(s) = -\frac{G_{A1}}{1 + (1 + G_{A1})\left({}^{1}/_{A_o} + {}^{s}/_{2\pi f_{GBW}}\right)}. \quad (15)$$

For the gain stage response to a DAC current signal the numerator term is replaced by R_F. The transient DAC step response is calculated by the inverse Laplace transform of the DAC step I_{DAC}/s multiplied by (7)

$$v_O(t) = I_{DAC}R_F(1 - e^{-t2\pi f_{GBW}/(1+G_{A1})}). \quad (16)$$

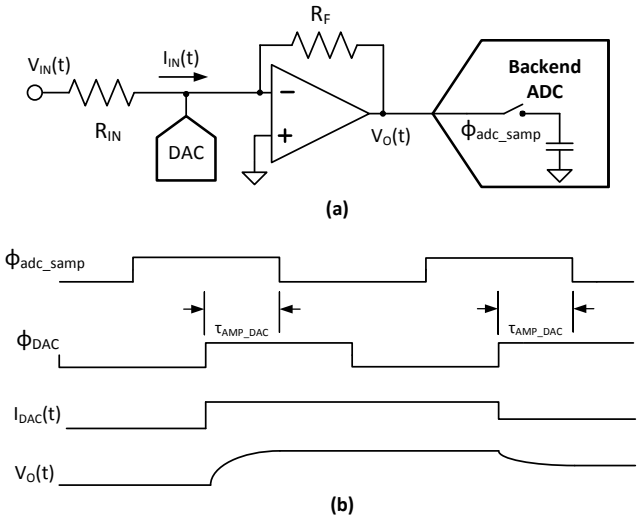


Fig. 20. (a) Resistive gain stage part of CTIP ADC, $G_{A1} = -R_F/R_{IN}$. (b) Timing diagram of a response to a DAC step. In this diagram ϕ_{DAC} is the DAC update signal, $I_{DAC}(t)$ is the DAC output current, $V_O(t)$ is the gain stage response to the DAC current step and ϕ_{adc_samp} is the backend ADC sampling clock. ϕ_{adc_samp} controls the switch that samples $V_O(t)$. τ_{AMP_DAC} is the time available to settle the DAC step.

The decaying exponential term is the settling error and it is required that the normalised error due to this term is less than half an LSB $2^{-(N_2+1)}$ of the backend ADC. The time allocated for this settling is

$$\tau_{AMP_DAC} = \frac{(G_{A1}+1)*ln\,2^{(N_{ADC2}+1)}}{2\pi f_{GBW}}. \quad (17)$$

For a continuous time sinusoid input signal $V_{in}(t) = A\cos(2\pi f_{SIG}t + \phi)$ and the gain stage transfer function of (15) the output transfer function is

$$v_O(t) = \frac{-G_{A1}A\cos(2\pi f_{SIG}t+\phi-\theta)}{\sqrt{1+\omega^2(G_{A1}+1)^2/(2\pi f_{GBW})^2}}, \quad (18)$$

where the phase shift $\theta = \tan^{-1}\left(\omega\,(G_{A1}+1)/2\pi f_{GBW}\right)$. Assuming $\omega\,(G_{A1}+1)/2\pi f_{GBW} < 1$, the group delay $d\theta/d\omega$ of this phase shift is the signal path amplifier delay

$$\tau_{AMP_SIG} \approx \frac{(G_{A1}+1)}{2\pi f_{GBW}}. \quad (19)$$

It can be observed that τ_{AMP_SIG} is a small fraction of the delay in response to a DAC step τ_{AMP_DAC}.

Solving (17) for $\tau_{AMP_DAC} = 2.5ns$, $N_2 = 9$ and $G_{A1} = 8$ requires f_{GBW} to be 4GHz. Designing an op-amp with this unity gain bandwidth is a non-trivial design and consumes a lot of power. A recent pipelined ADC [21] with an op-amp with similar specs requires a 2.5V op-amp supply. This sets an upper bound on f_{GBW} for this technology, hence the choice of the value of τ_{AMP_DAC}.

An additional limitation of the resistive gain stage is due to thermal noise. The input resistor, DAC and op-amp all add thermal noise to the signal, this noise is filtered by the resistive gain transfer function $H_{RG}(s)$ and then all this noise is folded into the signal band by the sampling switch. Due to settling requirements $H_{RG}(s)$ has a wideband response and provides very little filtering. Its equivalent noise bandwidth, Δf is 700MHz.

The voltage noise power from the input resistors is $4kTR_{IN}\Delta f$. The current steering DAC noise referred to the CTIP ADC input is also proportional to R_{IN}. As the op-amp bandwidth is set by settling, reducing R_{IN} is the only way to reduce the input referred thermal noise of the CTIP ADC. The cost of smaller R_{IN} is more power consumed in the input buffer preceding the ADC and in the DAC. Setting $R_{IN} = 75\Omega$ achieves a signal to thermal noise ratio of $75dB$.

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