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Mobility improvement in nanowire junctionless transistors by uniaxial strain

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Improvement of current drive in n- and p-type silicon junctionless metal-oxide-semiconductor-field-effect-transistors (MOSFETs) using strain is demonstrated. Junctionless transistors have heavily doped channels with doping concentrations in excess of 10^{19} cm^{-3} and feature bulk conduction, as opposed to surface channel conduction. The extracted piezoresistance coefficients are in good agreement with the piezoresistive theory and the published coefficients for bulk silicon even for 10 nm thick silicon nanowires as narrow as 20 nm. These experimental results demonstrate the possibility of enhancing mobility in heavily doped silicon junctionless MOSFETs using strain technology. © *2010 American Institute of Physics*. [doi:10.1063/1.3474608]

Mechanical strain is a widely used technique to increase carrier mobility in the channel of silicon metal-oxide-semiconductor-field-effect-transistors (MOSFETs). The technique has been applied to bulk MOSFETs,[1] silicon-on-insulator (SOI) transistors,[2–4] as well as to multigate FETs (MuGFETs).[5] These studies demonstrate the great interest of strain engineering to boost up the performance of those advanced MOS devices with extensive industrial applications. As mentioned by Chu *et al.* in Ref. 6, the viability of novel transistor architectures or channel materials will depend on their ability to provide device enhancement comparable to strained-Si planar MOSFETs. Recently, the fabrication of silicon nanowire transistors with no junctions has been reported.[7] In these devices, the channel doping concentration is high with typical values ranging from 10^{19} to over 5×10^{19} cm^{-3}. n- and p-channel devices are uniformly doped with donor and acceptor impurities, respectively. The doping type and concentration are the same in the source and drain extensions as in the channel. The absence of doping concentration gradients greatly simplifies fabrication and relaxes thermal budget requirement, especially in ultrashort-channel devices. Those original devices have demonstrated near-ideal subthreshold slope, extremely low leakage current, and less degradation of mobility with gate voltage and temperature than classical transistors. Since the channel of junctionless transistors is heavily doped, one might wonder if strain-induced mobility enhancement techniques can be effectively used in these devices. The aim of the present article is to experimentally analyze the impact of mechanical strain on drive current for n- and p-type junctionless Si nanowire MOSFETs.

The piezoresistance coefficients (π) of doped bulk silicon can be found in the literature.[8] The piezoresistance factor in silicon decreases when the doping concentration is increased above 5×10^{17} cm^{-3} in n-type silicon and when it is increased above 2×10^{17} cm^{-3} in p-type silicon. The reduction of piezoresistance coefficients in n- and p-type silicon is shown in Table I for some typical doping concentrations used in the channel of junctionless transistors. To the reduction of piezoresistance coefficients corresponds a reduction in strain-induced mobility enhancement. Indeed, the piezoresistance coefficient is defined as the normalized change in resistivity with stress, $\pi=\Delta\rho/(\rho\cdot\sigma)$, where σ is the applied stress and ρ is the resistivity which is directly related to the carrier mobility by $\rho=1/(q\mu_n n+q\mu_p p)$.

The strain-induced mobility enhancement (π_L) can readily be calculated using the data supplied in Ref. 8 and one finds $\pi_L=35.2$ $cm^2/dyne=352\times10^{-6}$ MPa^{-1} for p-type silicon and $\pi_L=31.2$ $cm^2/dyne=312\times10^{-6}$ MPa^{-1} for n-type silicon at a doping concentration of 2×10^{19} cm^{-3}.

The devices were fabricated on standard (100) Unibond SOI wafers with a 340 nm top silicon layer and a 400 nm buried oxide. The starting SOI film was p-type with a resistivity of 10–20 Ω cm. The SOI layer was thinned down to 10–15 nm and patterned to form silicon nanowires using e-beam lithography. Nanowires with different widths were patterned, in order to obtain devices with a width ranging between 20 and 40 nm. A 10 nm gate oxide was grown and ion implantation was used to dope the devices *uniformly* n^+ and p^+ with a concentration of 2×10^{19} cm^{-3} to realize n-channel and p-channel devices, respectively. A 50 nm thick polysilicon layer was deposited by low-pressure chemical vapor deposition on the gate oxide and doped either p^{++} for

TABLE I. Reduction of piezoresistance coefficient (in percents) in n-type and p-type silicon for some values of doping concentration used in the channel of junctionless transistors.

Doping concentration	n-type	p-type
1×10^{19} cm^{-3}	14%	30%
2×10^{19} cm^{-3}	26%	51%
5×10^{19} cm^{-3}	46%	71%

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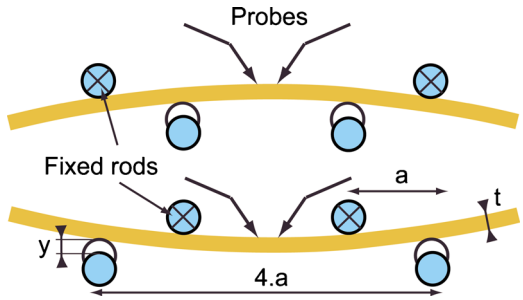


FIG. 1. (Color online) Four-point bending measurement setup and relationship between the induced stress (σ) and vertical displacement (y) of the bottom movable rods. For all measurements, the spacing "a" was equal to 20 mm.

nMOS devices or n^{++} for pMOS devices. The devices studied here have a gate length of 1 μm. No source or drain implant was performed on the junctionless MuGFETs. Oxide was deposited and etched to form contact holes, and TiW +aluminum metallization completed the process. The channel of the devices follows the ⟨110⟩ crystal direction. Mobility measurements made using the maximum of transconductance method yield mobility values in the range 80–100 $cm^2/V\,s$ for both electrons in n-channel devices and holes in p-channel device.[9] Unlike inversion-mode and accumulation-mode MuGFETs, junctionless transistors in the on-state operate by bulk conduction (i.e., not surface channel conduction). Thus, their piezoresistance coefficients and mobility enhancement effects must be compared to bulk silicon values.[8]

The devices were measured using a wafer probe system equipped with a four-point bending setup that allows for bending the wafers in order to generate uniaxial strain in the transistors.[4] Bending the center of the wafer upwards creates a tensile stress on the top fiber of the wafer, and bending it downwards creates a compressive stress (Fig. 1). The transfer and output characteristics were measured for various devices geometries and applied stress values. The maximum stress is limited to 150 MPa to avoid breaking the wafers. This experimental setup provides a simple way to gain confidence in the effect of strain on transistor performance without modifying the process flow. This is quite important since many process flow parameters are changed when fabricating strained MOSFETs, there is thus uncertainly as to whether strain is the unique responsible for performance enhancement.

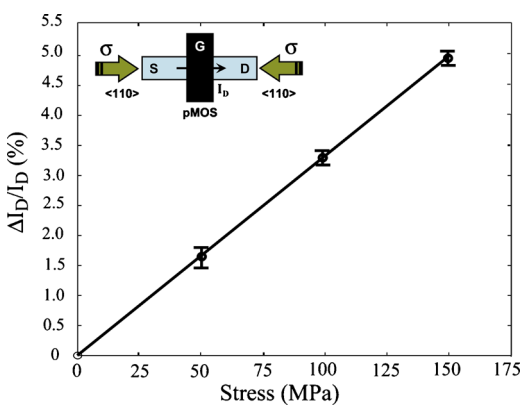


FIG. 2. (Color online) The variation in drain current, $\Delta I_D/I_D$, as a function of applied compression stress in a p-type junctionless MuGFET with a fin width of 30 nm.

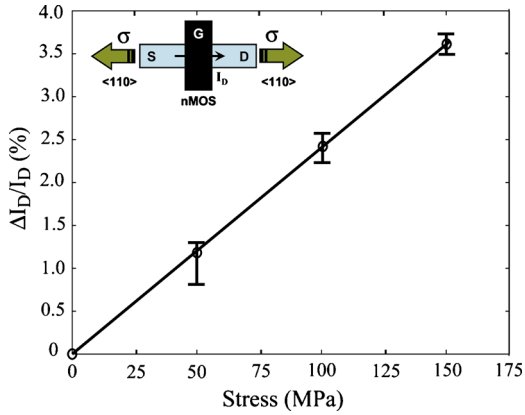


FIG. 3. (Color online) The variation in drain current, $\Delta I_D/I_D$, as a function of applied tensile stress in a n-type junctionless MuGFET with a fin width of 30 nm.

The stress is applied in ⟨110⟩ crystalline direction, i.e., parallel to the current flow in the devices. Compression and traction stresses are, respectively, applied to p- and n-type junctionless MuGFETs. The devices were measured for a gate voltage ranging from 0.4 to 1.1 V (n-channel, V_{TH}= –0.8 V) and –0.6 to –1.8 V (p-channel, V_{TH}=+0.2 V). The variation in drain current, $\Delta I_D/I_D$, as a function of the applied stress is plotted for p-(compression) and n-(traction) type junctionless MuGFETs in Figs. 2 and 3, respectively. The fin width of those devices is 30 nm and the gate voltage overdrive, V_{GS}-V_{TH}, considered for the current extraction is 0.5 V. At least five devices for each stress level were measured. The characteristic fluctuation between devices is represented by a vertical bar in the graphs for each stress level. This fluctuation is pretty low, especially for p-type junctionless MuGFETs. The origin of this scattering might be of course related to the variability between devices but also to the measurement accuracy in terms of actual applied stress. The bars are more important for low level of applied stress. In fact, the main source of inaccuracy comes from the operator ability to define the zero point, σ=0 MPa. For this particular measurement point, the pressure applied between the two bottom metallic rods and the metallic back side of the Si wafer must be sufficient to assure a good ground contact but cannot induce bending of the wafer.

In both cases, we observe a linear increase in the drain current relative change as a function of stress. From the slope of represented straight lines in Figs. 2 and 3, the longitudinal piezoresistance factors, π_L, are extracted for, respectively, p- and n-type junctionless MuGFETs. The results are summarized in Table II and are found to be in excellent agreement with the theoretical values proposed by Kanda.[8]

TABLE II. Piezoresistance coefficients in n-type and p-type devices. The calculated values are taken from Ref. 8 for a doping concentration of 2×10^{19} cm^{-3}.

	π_L measured (MPa^{-1})	π_L calculated (MPa^{-1})
n-type	$233\pm25\times10^{-6}$	230×10^{-6}
p-type	$333\pm10\times10^{-6}$	352×10^{-6}

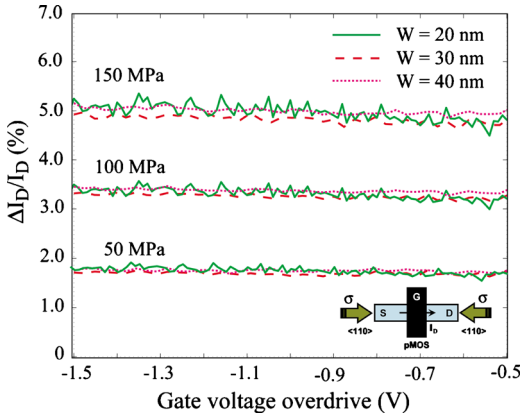


FIG. 4. (Color online) The variation in drain current, $\Delta I_D/I_D$, as a function of gate voltage overdrive, V_{GS}-V_{TH}, in a p-type junctionless MuGFET characterized by fin width of 20, 30, or 40 nm for various applied compressive stresses.

Figure 4 shows the variation in drain current, $\Delta I_D/I_D$, as a function of the gate voltage overdrive for p-type MuGFET characterized by fin width of 20, 30, or 40 nm and for applied compressive stress of 50, 100, or 150 MPa. No variations with the fin width demonstrate that there is no lateral geometry confinement on the piezoresistance effect. Contrary to classical planar or nonplanar MOSFETs working in inversion regime, the current relative change, $\Delta I_D/I_D$, is nearly independent on gate voltage overdrive for each recorded stress value. This beneficial behavior is directly related to the bulk conduction mode of junctionless MOSFETs. It means strain channel engineering improves carrier mobility over the whole gate bias range in on-state whereas for inversion mode strained-transistors the mobility enhancement degrades with gate voltage overdrive.

In conclusion, improvement of current drive using strain in junctionless n- and p-type nanowire MOSFETs is demonstrated. The extracted piezoresistance coefficients are in good agreement with the published piezoresistance coefficients for bulk silicon. A constant mobility enhancement factor is obtained over the whole gate bias range of interest in on-state. The combination of strained SOI and junctionless concept should lead to high-performance nanowire complementary MOS devices.

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