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# Electrical characterization of top-gated molybdenum disulfide field-effect-transistors with high-k dielectrics

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## Abstract

High quality HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> substrates are fabricated in order to study their impact on top-gate MoS<sub>2</sub> transistors. Compared with top-gate MoS<sub>2</sub> FETs on a SiO<sub>2</sub> substrate, the field effect mobility decreased for devices on HfO<sub>2</sub> substrates but substantially increased for devices on Al<sub>2</sub>O<sub>3</sub> substrates, possibly due to substrate surface roughness. A forming gas anneal is found to enhance device performance due to a reduction in charge trap density of the high-k substrates. The major improvements in device performance are ascribed to the forming gas anneal. Top-gate devices built upon Al<sub>2</sub>O<sub>3</sub> substrates exhibit a near-ideal subthreshold swing (SS) of ~69 mV/dec and a ~10× increase in field effect mobility, indicating a positive influence on top-gate device performance even without any backside bias.

**Keywords: MoS<sub>2</sub>; top-gated transistor; HfO<sub>2</sub>; Al<sub>2</sub>O<sub>3</sub>; high-k; substrate;**

## 1. Introduction

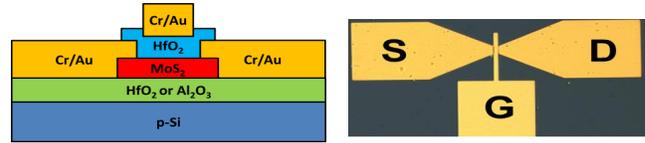
At the moment, transition metal dichalcogenides (TMDs) are one group of 2D materials that is being studied as a possible replacement for the semiconductor channel in future field-effect-transistor (FET) technology that require low power, high mobility devices[1][2][3][4]. Chief among them is molybdenum disulfide ( $\text{MoS}_2$ )[5][6], which has some of the earliest studies that report high mobility values ( $>200 \text{ cm}^2/\text{V}\cdot\text{s}$ ), high  $I_{\text{ON}}/I_{\text{OFF}}$  ratios ( $\sim 10^8$ ), and low subthreshold swing ( $\sim 74 \text{ mV}/\text{dec}$ ) for top-gate, few-layer  $\text{MoS}_2$  devices, usually fabricated on  $\text{SiO}_2/\text{Si}$  substrates[7]. While recent studies have demonstrated back-gate devices with  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  dielectrics[8][9][10] with high mobility values as a result of the high-k screening effect[11], few have studied the effects of these high-k dielectric substrates ("substrate" =  $\text{HfO}_2/\text{Si}$  or  $\text{Al}_2\text{O}_3/\text{Si}$ ) on a top-gate devices structure akin to the silicon-on-insulator (SOI) technology in use today.

With high-k materials such as  $\text{HfO}_2$  being utilized in current CMOS technology, their integration with TMDs can be advantageous for future applications. One recent bottleneck that has been overcome is the functionalization treatment of the inactive  $\text{MoS}_2$  surface using a UV-ozone process that allows a uniform, high-k dielectric to be deposited[12]. With a proven top-gate  $\text{MoS}_2$  FET fabrication process[13], an understanding of the effects of the unbiased back-gate dielectric on top-gate device performance is needed. In this paper, we demonstrate and discuss the use of high-k dielectric substrates in conjunction with a forming gas ("FG": 5%  $\text{H}_2/95\% \text{N}_2$ ) anneal and their effect on top-gate  $\text{MoS}_2$  devices.

## 2. Experimental

$\text{HfO}_2$  ( $\sim 10\text{nm}$ ) and  $\text{Al}_2\text{O}_3$  ( $\sim 15\text{nm}$ ) were deposited onto Si using an atomic layer deposition (ALD) process. Metal-oxide-semiconductor (MOS) capacitors were fabricated and an FG anneal study was performed to achieve an optimal annealing temperature of  $400^\circ\text{C}$  (1 hour) in order to establish the anneal impact on interface traps and achieve high quality dielectric substrates for top-gate devices. For the  $\text{MoS}_2$  devices, high-k substrates used for the MOS capacitors had  $\text{MoS}_2$  exfoliated onto them, with the source and drain patterned using photolithography and Cr/Au (20nm/150nm) deposited in a high-vacuum ( $10^{-6}$  mbar) evaporation and lift-off process. Afterwards, these back-gate devices were FG annealed at  $400^\circ\text{C}$ , with pre- and post-anneal I-V measurements. Both sets of  $\text{MoS}_2$  devices ( $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  substrates) were then functionalized using a 15 minute, in-situ UV-ozone treatment followed by a ALD of 4nm of  $\text{HfO}_2$  at  $200^\circ\text{C}$ . This combination of the FG anneal and UV-ozone treatment is done to reduce any residual, process induced contamination from lithography prior to top-gate dielectric formation[14][15][16]. The last step of the process

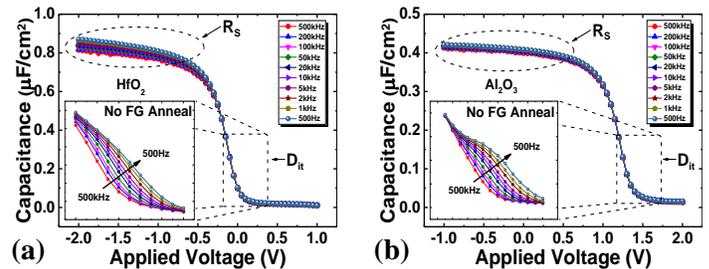
involved the deposition of a Cr/Au top gate using the same process as the source/drain, converting back-gate devices into top-gate, 3-terminal FETs as shown in Fig. 1. C-V and I-V measurements were performed using a Cascade Microtech station in conjunction with a Keithley 4200 SCS and an Agilent E4980A LCR meter.



**Fig. 1.** Cross-section (left) and top-view (right) of the final top-gate device structure.

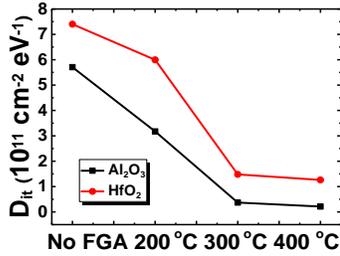
## 3. Results and Discussion

Frequency dependent C-V measurements were performed from 500Hz to 500kHz on  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  capacitors. Fig. 2 shows the low dispersion C-V curves after a  $400^\circ\text{C}$  FG anneal, with the insets showing the high dispersion "hump" before annealing, which is typically attributed to interface traps ( $Q_{it}$ ). While the dispersion in accumulation, typically attributed to series resistance ( $R_s$ ), did reduce slightly after FG annealing, the  $Q_{it}$  was the most impacted by the FG annealing for both  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  as the dispersion is nearly non-existent in the depletion region post anneal.



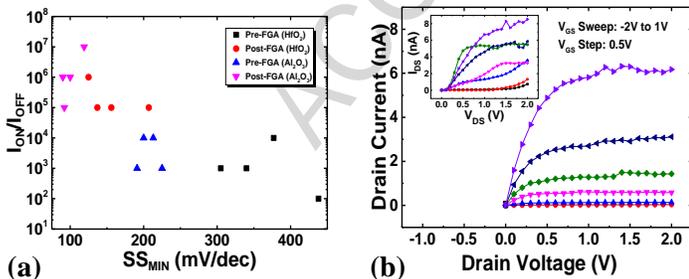
**Fig. 2.** C-V frequency dependence for (a)  $\text{HfO}_2$  and (b)  $\text{Al}_2\text{O}_3$  capacitors post  $400^\circ\text{C}$  FG anneal with the insets showing high dispersion before annealing.

Initially, the FG annealing was performed at  $200^\circ\text{C}$ ,  $300^\circ\text{C}$ , and  $400^\circ\text{C}$ , and the C-V measurements were done pre- and post-anneal. Interface trap density ( $D_{it}$ ) was extracted using Low-High Frequency method[17] with Fig. 3 showing the trend of  $D_{it}$  reduction as a function of FG annealing temperature. While both high-k dielectrics show a major reduction in  $D_{it}$ , the  $\text{Al}_2\text{O}_3$  appears to have the lowest  $D_{it}$  of  $2 \times 10 \text{ cm}^2\text{eV}^{-1}$  post  $400^\circ\text{C}$  anneal, suggesting an  $\text{Al}_2\text{O}_3$  substrate may yield a better interface than a  $\text{HfO}_2$  substrate for the deposition conditions used.



**Fig. 3.** Interface trap density ( $D_{it}$ ) extraction shows  $\text{Al}_2\text{O}_3$  substrates with lower  $D_{it}$  values than  $\text{HfO}_2$  substrates as a function of FG annealing temperature.

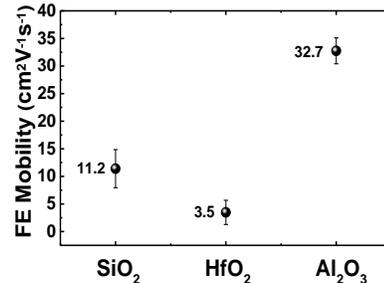
Using  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  substrates, several back-gate  $\text{MoS}_2$  FETs were fabricated in order to study the effect of the FG anneal on device performance and compare the substrates. As the  $\text{MoS}_2$  flakes were untreated[18][19], their thickness was kept relatively the same ( $\sim 4\text{-}5\text{nm}$ ) in order to lower variability amongst devices. The I-V characteristics of the devices were measured pre- and post-anneal at 400 °C, with the statistics of the  $\text{SS}_{\text{MIN}}$  and  $I_{\text{ON}}/I_{\text{OFF}}$  shown in Fig. 4a. With an average  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10^3$  and  $\text{SS}_{\text{MIN}}$  of  $\sim 365$  mV/dec pre-anneal, the performance of the  $\text{HfO}_2$  devices improved in all instances with an average  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10^5$  and  $\text{SS}_{\text{MIN}}$  of  $\sim 156$  mV/dec post-anneal. For the  $\text{Al}_2\text{O}_3$  devices, with an average  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10^3$  and  $\text{SS}_{\text{MIN}}$  of  $\sim 207$  mV/dec pre-anneal and an average  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10^6$  and  $\text{SS}_{\text{MIN}}$  of  $\sim 100$  mV/dec post-anneal, there was also significant device improvement. This increase in performance can be attributed not only to passivation as a result of the FG anneal, but also to a possible reduction in impurities at the backside  $\text{MoS}_2/(\text{HfO}_2$  or  $\text{Al}_2\text{O}_3)$  interface. It is worth noting that even though the net difference in device improvement was approximately the same, the post-anneal performance for devices on  $\text{Al}_2\text{O}_3$  substrates was better than for devices on  $\text{HfO}_2$  substrates. This may partly be as a result of better adhesion during  $\text{MoS}_2$  exfoliation as the  $\text{Al}_2\text{O}_3$  substrate yielded a greater number of few-layer flakes than the  $\text{HfO}_2$  substrate, possibly due to substrate surface roughness as discussed later in this section.



**Fig. 4.** (a) Several back-gate FETs on high-k substrates pre- and post-anneal indicating a beneficial trend in device performance. (b)  $I_D$ - $V_D$  characteristics of a back-gate FET pre-(inset) and post-anneal indicates a beneficial effect on the contacts.

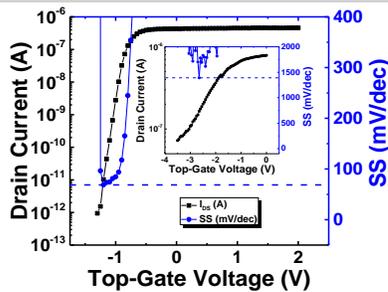
There was also a beneficial effect of the FG anneal on the contacts as (Fig. 4b) the  $I_D$ - $V_D$  shows Schottky behavior (inset) pre-anneal and Ohmic behavior post-anneal, potentially reducing the need for sulfur passivation treatments[20][21][22]. While these back-gate devices can be useful to study the effects of the FG anneal, full device evaluation is limited, especially since current CMOS technology does not use this device structure. To properly compare the effect of the  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  substrates, a top-gate FET structure is needed.

Converting from a back-gate to a top-gate FET allows for continuous study of the same  $\text{MoS}_2$  flake. The back-gate devices on  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  substrates, already FG annealed at 400 °C, all had UV-ozone functionalization treatment followed by in-situ  $\text{HfO}_2$  ALD, converting to a top-gate FET with a Cr/Au (20nm/150nm) gate (Fig. 1). These devices were electrically characterized without any back-gate bias and their field effect mobility ( $\mu_{\text{FE}}$ ) statistics are shown in Fig. 5, along with those of top-gate devices characterized on  $\text{SiO}_2$  substrates. There was  $\sim 10\times$  increase in mobility for devices on  $\text{Al}_2\text{O}_3$  substrates compared to devices on  $\text{HfO}_2$  substrates. The  $\text{HfO}_2$  substrates appear to have yielded devices with mobility values worse than those of devices on  $\text{SiO}_2$  substrates.



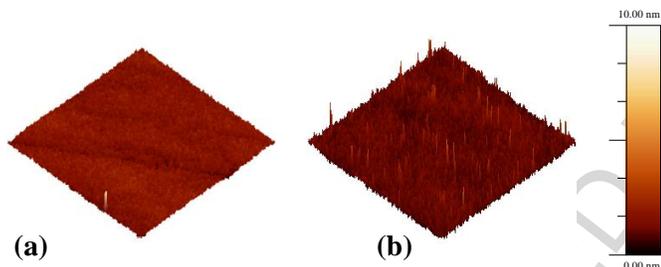
**Fig. 5.** Mobility statistics of multiple top-gate FETs shows a  $\sim 10\times$  improvement in field effect mobility ( $\mu_{\text{FE}}$ ) on  $\text{Al}_2\text{O}_3$  substrates over  $\text{HfO}_2$  substrates.

Comparing the  $I_D$ - $V_G$  of two best top-gate devices in Fig. 6, the device on a  $\text{HfO}_2$  substrate (inset) demonstrates a poor  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10$  and a high  $\text{SS}_{\text{MIN}}$  of  $\sim 1400$  mV/dec, while the device on an  $\text{Al}_2\text{O}_3$  substrate demonstrates a good  $I_{\text{ON}}/I_{\text{OFF}}$  of  $\sim 10^6$  and a near-ideal  $\text{SS}_{\text{MIN}}$  of 69 mV/dec. Even though the devices on both high-k substrates had good performance as FG annealed back-gate devices and went through the same top-gate conversion, those on  $\text{Al}_2\text{O}_3$  substrates showed an improvement while those on  $\text{HfO}_2$  substrates became worse as a top-gate device than as a back-gate device. This suggests that for  $\text{MoS}_2$ , a high-quality  $\text{Al}_2\text{O}_3$  substrate may provide a beneficial effect to top-gate devices under the conditions stated earlier as opposed to  $\text{HfO}_2$  substrates, with further study required for combinations of top-gate dielectrics and TMDs.



**Fig. 6.**  $I_D$ - $V_G$  for top-gate FETs show a subthreshold swing (SS) from  $\sim 1400$  mV/dec for a  $\text{HfO}_2$  substrate (inset) to a near-ideal  $\sim 69$  mV/dec for  $\text{Al}_2\text{O}_3$  substrate.

To determine a possible origin of the better device performance on  $\text{Al}_2\text{O}_3$  substrates than on  $\text{HfO}_2$  substrates, atomic force microscopy (AFM) was used to ascertain surface roughness. AFM images shown in Fig. 7 demonstrate the average RMS roughness of the  $\text{Al}_2\text{O}_3$  substrate to be 0.19 nm, compared to 0.25 nm for the  $\text{HfO}_2$  substrate. There are also indications of contaminants on the  $\text{HfO}_2$  surface, most likely attributed to carbon residue[23]. The surface roughness of the backside dielectric appears to influence the exfoliated  $\text{MoS}_2$  flake size and top-gate device performance.



**Fig. 7.** AFM images of (a)  $\text{Al}_2\text{O}_3$  substrate and (b)  $\text{HfO}_2$  substrate with an RMS roughness value of 0.19 nm and 0.25 nm, respectively.

#### 4. Conclusions

High quality  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  substrates were fabricated for top-gate  $\text{MoS}_2$  field-effect-transistors and their impact on device performance was compared. A forming gas anneal was used to reduce the interface trap density and passivate these high-k substrates. The devices on  $\text{Al}_2\text{O}_3$  substrates demonstrated much better performance compared to those on  $\text{HfO}_2$  substrates, possibly due to substrate surface roughness. This suggests a better interface is formed between the  $\text{Al}_2\text{O}_3$  substrate and the  $\text{MoS}_2$  material, leading to a near-ideal subthreshold swing of 69 mV/dec for a top-gate device. This work provides insight into utilizing high-k substrates for top-gate devices in future applications of TMD materials.

#### Acknowledgement

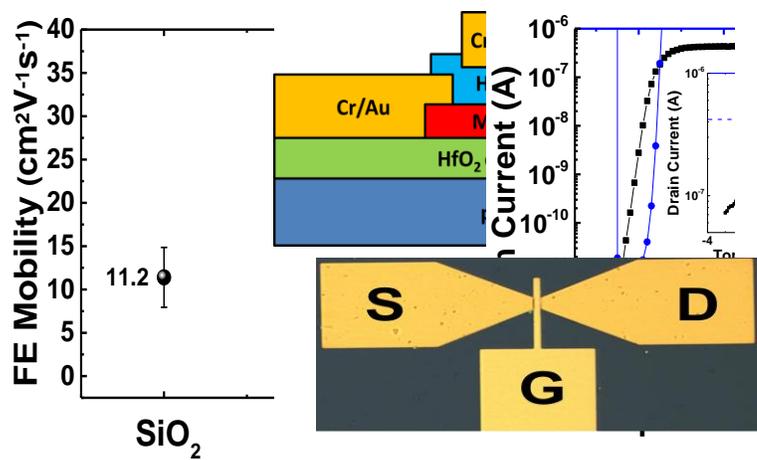
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Graphical abstract



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## Highlights

- Top-gate MoS<sub>2</sub> FETs were fabricated on high-k dielectric substrates
- A forming gas anneal enhances device performance with a reduction in  $D_{it}$
- Top-gate devices on Al<sub>2</sub>O<sub>3</sub>/Si showed better performance than on HfO<sub>2</sub>/Si
- AFM images suggest that substrate surface roughness affects device performance

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