Electrical characterisation of InGaAs on insulator structures

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Abstract

The electrical properties of Au/Ni/$In_{0.53}Ga_{0.47}As$/Al_2O_3/SiO_2/Si structures were investigated using Capacitance Voltage (C-V) analysis. The properties of the InGaAs on insulator structures were analysed by comparing the measured and the theoretical C-Vs obtained using a physics based simulation of this structure. The results show that the measured data obtained on both n-type and p-type silicon match very well the simulated data. This work also shows that this approach allows the characterisation of charges in the buried oxide as well as interface states at the bottom InGaAs/Al_2O_3 interface.

1. Introduction

3D integration consists in stacking layers containing integrated circuits (ICs) in order to achieve higher density per chip while device dimensions remain constant. In the most advanced form of 3D integration individual transistors from different stacked layers are overlaid and connected to form 3D circuits. This is generally referred to as monolithic integration and is represented schematically in figure 1. 3D monolithic integration has the potential to increase the device areal density [1], reduce the wire length of interconnects [2], and improve the transistor performance and power consumption by co-integrating high mobility channel materials [3] (e.g. InGaAs for nFETs and SiGe for pFETs). However, one of the most challenging issues facing this technology is the properties of the interlayer dielectric which bonds the upper level semiconductor to the IC in the 3D integrated structure. Any charges in the interlayer dielectric and interface states present at the interlayer dielectric/upper semiconductor interface may affect device operation. For instance, a high density of positive charge in the interlayer dielectric will result in accumulation of electrons at the interlayer dielectric/nFET channel interface, which will result in a parasitic channel from drain to source at zero gate bias for the upper level nFET. Net negative charge in the interlayer dielectric will modify the nFET threshold voltage. In addition, interface states at the interlayer dielectric/nFET channel interface can also affect the Fermi level position at the interface. The potential at the interlayer dielectric/nFET channel interface clearly has a marked impact of the nFET device behaviour, however, this potential is not directly controlled through the nFET gate voltage. As a consequence, it is important to develop appropriate metrology methods to characterise the properties of the interlayer dielectric used in the bonding process in terms of fixed oxide charges and interface states and also to study how these defect concentrations change as a function of subsequent thermal processing.

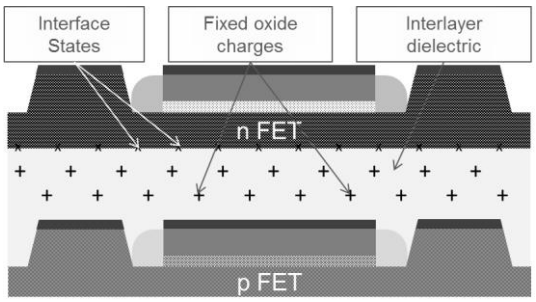

Figure 1: Schematic illustrating the 3D monolithic integration concept where the channel material for the n FET (e.g. InGaAs) is different from the material for the p FET (e.g. SiGe).Fixed oxide charges and interface states are included for illustration. Note that fixed charges in the bonding oxide below the upper level nFET and interface states at the nFET/oxide interface will have a significant impact on the nFET device behaviour.

In this study, we investigate the electrical properties of an $In_{0.53}Ga_{0.47}As$/Al_2O_3/SiO_2/Si structure with an emphasis on the electrical charges present in the interlayer dielectric. This Semiconductor /Insulator/Semiconductor (SIS) stack is obtained using wafer bonding techniques and reproduces process steps similar to those encountered in 3D monolithic circuits when sequential transfer and processing of a III-V layer for nFETs onto fully processed pFETs is required [4]. The electrical properties of the structure are analysed through the experimental multi-frequency capacitance-voltage (C-V) characteristics of the $In_{0.53}Ga_{0.47}As$/Al_2O_3/SiO_2/Si SIS structure and by comparing the experimental C-V

responses to the ideal response predicted by physics based ac simulations on the ideal C-V response.

2. Experimental

Nominally undoped $In_{0.53}Ga_{0.47}As$ layers (50 nm) were grown by Metalorganic Vapour Phase Epitaxy (MOVPE) on 2 inch semi-insulating InP substrates. An intermediate 100 nm thick $In_{0.52}Al_{0.48}As$ buffer was used between the InP substrate and the InGaAs active layer. 30 nm Al_2O_3 was deposited on the InGaAs surface by Atomic Layer Deposition (ALD). The Al_2O_3 deposition was performed at 250°C using Trimethyl-aluminium (TMA) and H_2O. The III-V wafers were bonded to p-type and n-type 4 inch silicon (100) wafers. The doping concentration in the n (phosphorus) type and p (boron) type silicon is ~ $2x10^{15}$ cm^{-3}. Prior to bonding, the silicon wafers were cleaned with a combination of Megasonic, HF and Ozone rich water cleaning. After this chemical treatment, a clean native oxide of approximately 1 nm in thickness is left on the silicon surface. The III-V wafers were cleaned using a combination of Megasonic and Ozone rich water rinsing. The III-V wafers were brought into contact with the Si wafers to initiate the bonding. The bonding interface was reinforced following a 250°C thermal anneal for 1 hour in vacuum. The InP substrate etch is achieved using a combination of a short grinding step and a wet etching step in a diluted HCl solution. Prior to the definition of the capacitor structures, the samples were analysed by X-ray diffraction, which confirmed the thickness of the $In_{0.53}Ga_{0.47}As$ layer as 50 nm, and that the 100nm InAlAs layer was fully removed by the dilute HCl etch process. An image of the 50nm thick InGaAs transferred layer onto a four inch Si wafer is shown in figure 2.

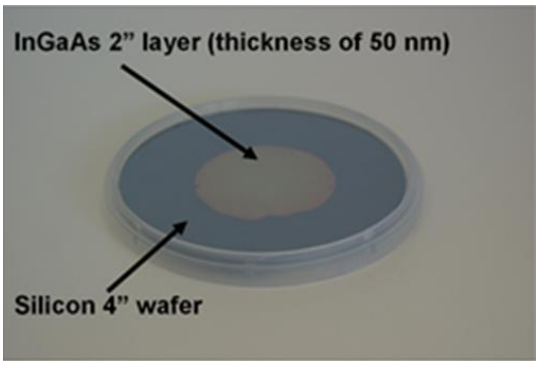

Figure 2: Image of the transferred 50 nm InGaAs layer on a 4 inch Si wafer.

The $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2/Si$ individual test structures were defined by lithography, Au(200nm)/Ti(20nm) ebeam evaporation and metal lift off. Finally, the InGaAs layer is etched to form mesa structures, as shown schematically in figure 3. It is noted that in a real 3D device structure the layer structures below the interlayer dielectric used in the bonding process, will be more complex than in the test structure shown above, and will also vary with lateral position (as can be seen in Figure 1). In this work, the silicon substrate serves as the second contact in the device structure for the C-V analysis. While the structure is not precisely the same as in a real 3D device implementation, the fixed charge densities in the interlayer dielectric will be representative of those encountered in the full 3D structure. Moreover, the charge defect components in the interlayer dielectric used in the bonding process affect the properties in the upper level nFET and are not expected to have any significant impact on the lower level pFET (see Figure 1). As a consequence, it is not necessary to replicate the precise details of the device structure below the interlayer dielectric, and the device structure shown in Figure 3 presents an SIS capacitor which can characterise the fixed charges in the interlayer dielectric used in the bonding process, with relatively few process steps.

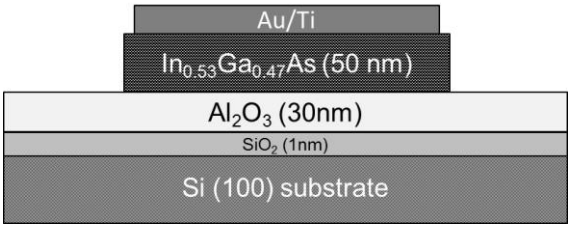

Figure 3: Schematic cross section depicting the $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2/Si$ test structures used in this study.

The experimental results were compared to simulated small ac signal CV characteristics obtained using the ATLAS device simulator. The numerical simulations were performed using transverse field, doping and temperature dependent mobility models in combination with Shockley and Read Hall recombination models and Fermi Dirac carrier statistics.

3. Results and Discussion

Figure 4 shows the multi-frequency C-V characteristics measured on the SIS structure where the Si wafer is n type. It should be noted that the nominally undoped MOVPE InGaAs layers typically result in a residual n-type (~$10^{16}cm^{-3}$) material.
For negative gate voltage (Vg) values (highlighted in grey), the Si/SiO_2 interface is depleted and the $InGaAs/Al_2O_3$ interface is accumulated and for Vg>1.5V, the situation is reversed. It is noted that simultaneous accumulation or depletion of both interfaces is not possible with this doping type combination. A large dispersion of the C-V with measurement frequency is observed for Vg>0.5V (onset of Si accumulation). This dispersion results from charge trapping and de-trapping at/or near the $InGaAs/Al_2O_3$ interface. This result is not surprising since for the current structures there was no attempt to passivate the InGaAs surface prior to the Al_2O_3 ALD deposition step, and high interface state concentration will be present at the $InGaAs/Al_2O_3$ interface [5].

However, it illustrates very well how the bottom interface could affect the final device operation.

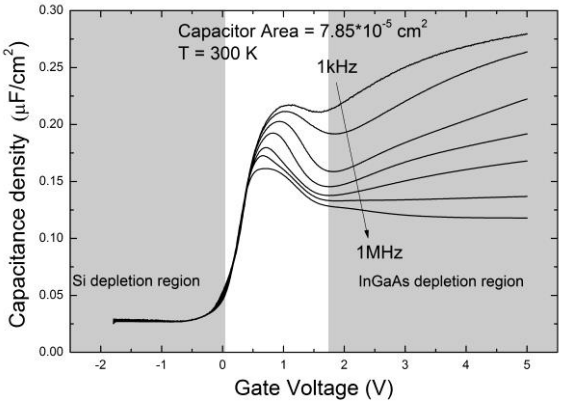

Figure 4: Multi-frequency Capacitance Voltage characteristics for Au/Ti/$In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/n-Si test structures.

For Vg<0.5V, the multi frequency CV characteristics of figure 4 show very little frequency dispersion, this voltage range corresponds to the depletion of the Si interface and the accumulation of the InGaAs interface. This clearly indicates that the Si/oxide interface presents a very low level of Dit.

Figure 5 presents the C-Vs measured on the SIS structure where the Si wafer is p type. In this case, both semiconductors present simultaneous accumulation (negative Vg) or depletion (positive Vg) at their respective interfaces with the interlayer dielectric. As a result the C-V for this sample presents similar characteristic as those of a MOS structure. Since both interfaces accumulate and deplete simultaneously their associated capacitance contributions are comparable and the C-V frequency dispersion originating mainly from the InGaAs/Al_2O_3 interface can be observed in two different regions of the C-V curves. The dispersion observed in accumulation results from the border traps in the Al_2O_3 communicating with the InGaAs layer [6, 7] while the dispersion in depletion is due to interface states at the InGaAs interface.

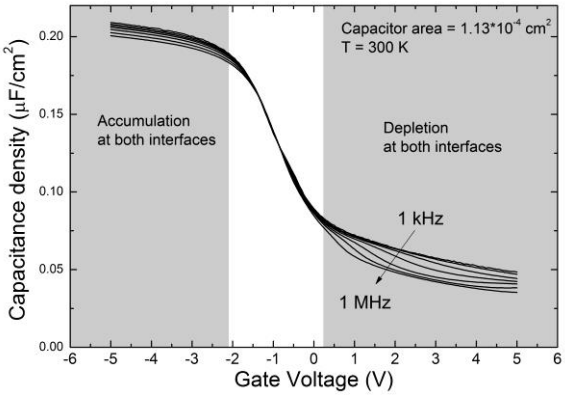

Figure 5: Multi-frequency Capacitance Voltage characteristics for Au/Ti/$In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/p-Si test structures.

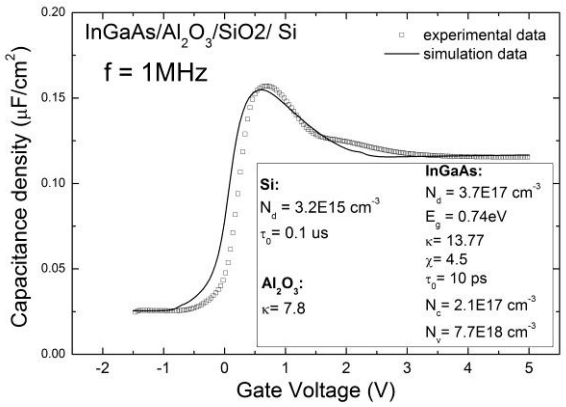

Figure 6: Experimental and simulated 1MHz C-V characteristic for the Au/Ti/$In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/n-Si structure. The inset includes the main material parameters used for the simulation.

The 1MHz simulated C-V obtained using a commercial *ac* physics based device simulator agrees well with the measured C-V (figure 6) considering no fixed charges were assumed in the simulation. The $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/n-Si C-V simulation features the same general response as the experimental results.

The simulated C-V shows a flat band voltage (V_{fb}) shift in the Si region of ~0.1V with respect to the measured C-V, this combined with a theoretical interlayer oxide capacitance value of 0.23µF/cm^2 (k(Al_2O_3)=7.8 and k(SiO_2)=3.9) yields a net apparent fixed negative charge ~ 1.4x10^{11}cm^{-2} at the Si/SiO_2. This assumes a centroid located at the Si/SiO_2 interface. Any other location will yield a higher negative charge density. It is noted that the InGaAs/oxide/silicon structure allows, in principle, for 2 Vfb values to be extracted [8, 9], allowing the independent determination of the centroid and the charge density, and this will be the subject of future work. It must be noted that the InGaAs doping used in the simulation is one order of magnitude higher than expected. This high value could be due to carriers in the InGaAs arising from Fermi level alignment with the Ti contact, which is not taken into account in the simulation.

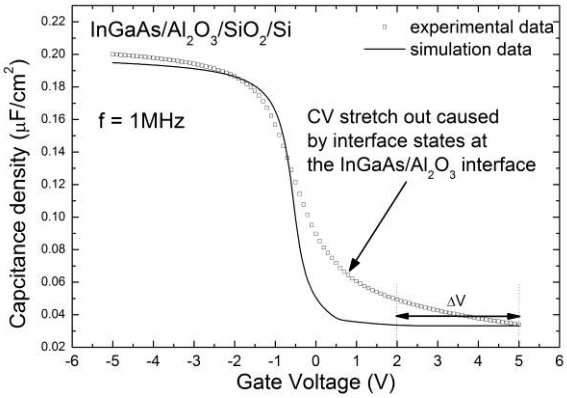

Figure 7: Experimental and simulated 1MHz C-V characteristic for the Au/Ti/$In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/p-Si structure. Except for the Si acceptor concentration

Na=2x10^{16}cm^{-3} all other materials parameters used in this simulation were identical to the structure on n-Si.

Figure 7 compares the $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2$/p-Si simulated 1MHz C-V with the measured response. The simulated and experimental data show some divergence at positive gate voltage. The C_{max} in accumulation is slightly lower than predicted (0.23μF/cm^2). The noticeable C-V stretch out for 0V<Vg<5V is commonly observed in the high frequency C-Vs of MOS structures with high interface state density. It is reasonable to neglect the effect of the interface density at Si/SiO_2 interface considering the level of frequency dispersion observed in Figure 4 around 0V. Therefore most of the stretch out is caused by the interface states at the $In_{0.53}Ga_{0.47}As/Al_2O_3$ interface. The 1MHz simulated C-V characteristic reaches a minimum capacitance at 2V while the experimental structure requires 5V to achieve the minimum capacitance, which corresponds to inversion at both semiconductor/oxide interfaces. This additional ΔV=3V can be attributed to the voltage required to move the Fermi level through a distribution of interface states at the $InGaAs/Al_2O_3$ interface. This yields a total interface state density ~ 4x10^{12} cm^{-2}, which represents the integrated interface state density from the InGaAs valance band edge (E_v) to conduction band edge (E_c). This is comparable to other publications where integrated interface state densities from the E_v to E_c are in the range ~2.5x10^{12}cm^{-2} [10]. The level of Dit present at the bottom interface of the current samples is too high for practical applications, however the focus of this study was not to minimise Dit at the bottom interface but to demonstrate the suitability of this approach to characterise the buried oxide and bottom interface of an InGaAs on insulator film.

4. Conclusion

The results in this work demonstrate that the multi-frequency C-V response of the InGaAs/oxide/silicon structure can be used as a metrology approach to investigate fixed charges in the interlayer dielectric and the properties of the oxide interface with the upper semiconductor channel, which could have as marked impact on the performance of the upper level MOSFET in 3D monolithic integration. For the particular InGaAs/oxide/silicon system examined in this paper, the composite SiO_2(1nm)/Al_2O_3(30nm) oxide yielded a relatively low net negative charge density of 1.4x10^{11}cm^{-2}, assuming the charge is located at the Si/SiO_2 interface, or a value 4.5x10^{16}cm^{-3} if distributed throughout the Al_2O_3 film. Based on the stretch out of the experimental C-V in comparison to the ideal case with no oxide charges or interface states, an integrated interface state density from E_v to E_c of 4x10^{12} cm^{-2} was calculated at the Al_2O_3(30nm)/InGaAs interface. This approach could also be used to monitor the evolution of oxide charges and interface states when the structure is subjected to the thermal budget required for device processing. The method could also assess different passivation strategies for the InGaAs/oxide interface, which could be based on either wet chemical passivation or epitaxially grown capping layers on the InGaAs surface prior to Al_2O_3 deposition.

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References

[1] P. Batude, M. Vinet, C. Xu, B. Previtali, C. Tabone, C. Le Royer, L. Sanchez, L. Baud, L. Brunet, A. Toffoli, F. Allain, D. Lafond, F. Aussenac, O. Thomas, T. Poiroux, O. Faynot, VLSI Symp. Tech. Dig., (2011) p158-159.

[2] O. Turkyilmaz, G. Cibrario, O. Rozeau, P. Batude, F. Clermidy, Proc. Design, Automation and Test in Europe, DATE (2014) 6800552.

[3] L. Czornomaz, N. Daix, K. Cheng, D. Caimi, C. Rossel, K. Lister, M. Sousa, J. Fompeyrine, Tech. Dig.-Int. Electron Devices Meet. (2013) 6724548, 2.8.1-2.8.4

[4] L. Czornomaz, N. Daix, D. Caimi, M. Sousa, R. Erni, M. D. Rossell, M. El-Kazzi, C. Rossel, C. Marchiori, E. Uccelli, M. Richter, H. Siegwart, J. Fompeyrine, Tech. Dig.-Int. Electron Devices Meet. (2012), 6479088, 23.4.1-23.4.4.

[5] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, P.K. Hurley, J. Electrochem. Soc. (2011), 158, G103-G107.

[6] G. Brammertz, A. Alian, H.-C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, IEEE Trans. Electron. Devices, (2011) 58, 3890–3897.

[7] Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, Y. Taur, IEEE Trans. Electron. Devices, (2012) 59, 2100–2106.

[8] P. K. Hurley, S. Hall, W. Eccleston, Electr. Dev. Lett. (1992) 13, 238-240.

[9] I. P. Barchuk, V. I. Kilchitskaya, V. S. Lysenko, A. N. Nazarov, T. E. Rudenko, S. V. Djurenko, A. N. Rudenko, A. P. Yurchenko, D. Ballutaud, J. P. Colinge, Trans. Nucl. Sci. (1997) 44, 2542-2552.

[10] É. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, J. Appl. Phys., (2011) 109, 024101.