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Si/SiGe electron resonant tunneling diodes with graded spacer wells

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Resonant tunneling diodes have been fabricated using graded $Si_{1-x}Ge_x$ ($x=0.3\rightarrow0.0$) spacer wells and strained $Si_{0.4}Ge_{0.6}$ barriers on a relaxed $Si_{0.7}Ge_{0.3}$ n-type substrate which demonstrates negative differential resistance at up to 100 K. This design is aimed at reducing the voltage at which the peak current density is achieved. Peak current densities of 0.08 A/cm^2 with peak-to-valley current ratios of 1.67 have been achieved for a low peak voltage of 40 mV at 77 K. This represents an improvement of over an order of magnitude compared to previous work. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1381042]

Resonant tunneling diodes (RTDs) are now a mature technology in the III–V system with many demonstrations of memory[1] and logic[2] circuits. The vast majority of the microelectronics industry, however, is based on Si and therefore there is great interest in attempting to create RTDs using Si/SiGe heterostructures.[3] The n-type system has the only room temperature demonstration of negative differential resistance (NDR) in Si-based RTDs with peak current densities up to 5 kA/cm^2 (Ref. 4) and peak-to-valley current ratios (PVCR) of up to 2.9 (Ref. 5) for peak voltages above 1 V. The best performance in Si-based tunnel diodes have come from interband diodes[6] with peak current densities of 8 kA/cm^2 with a PVCR of 5.45 (Ref. 7) or 10.8 kA/cm^2 with a PVCR of 1.42.[8] The major problem is that these Esaki diodes have been fabricated by molecular beam epitaxy with δ-doped layers and will be very difficult to place in circuits and processed with metal–oxide field effect transistors or heterostructure FETs. For memory applications, Pascha[9] has modelled a number of circuits in the III–V system and suggested that for optimum performance, the RTDs should have PVCR of 3, peak current densities of 0.1 A/cm^2 and a peak voltage of 0.2 V to allow optimized performance and matching with FETs.

Results are presented on Si/SiGe RTDs aimed at low power memory applications. Structures were designed with strained $Si_{0.4}Ge_{0.6}$ barriers on a relaxed $Si_{0.7}Ge_{0.3}$ to produce an enhanced conduction band barrier above the vitual substrate energy level.[10,4] All previous SiGe RTD designs have spacer quantum wells on either side of the tunnel barriers. Here these spacers have graded Ge concentrations. Modelling using a one-dimensional (1D) self-consistent Poisson–Schrödinger solver of the band structure demonstrates a conduction band which does not have a significant conduction band discontinuity (ΔE_c) at the emitter or the collector (Fig. 1). The lack of a ΔE_c at the emitter prevents a charge layer forming as occurs in the strained-Si wells. This layer of charge, which is formed whether electrons tunnel or do not tunnel through the barriers, requires larger biases to be applied to the system thereby increasing the peak voltage in the system. Therefore, this work demonstrates a technique for reducing the peak voltage in SiGe RTDs.

The wafers for the work were purchased from DERA, Malvern (U.K.). They were grown in an ultrahigh vacuum compatible chemical vapor deposition (CVD) system using

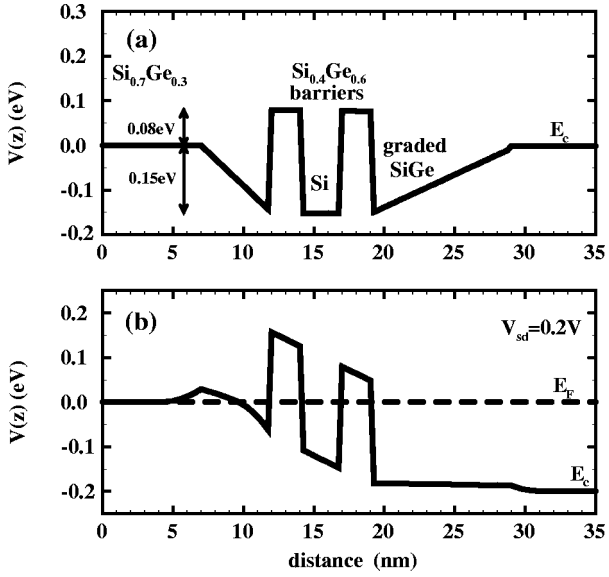

FIG. 1. (a) 1D self-consistent Poisson–Schrödinger solution of a structure with graded spacer wells on either side of the barriers. (b) The conduction band with a source-drain bias of 0.2 V applied. No barrier for electrons to enter the emitter is observed at 29 nm below the surface.

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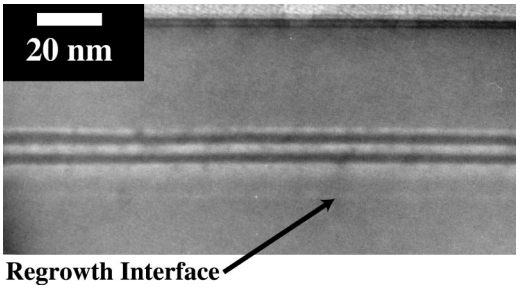

FIG. 2. A cross sectional TEM micrograph from the center of the wafer showing the excellent flatness of the layers. The thicknesses are within experimental tolerances close to the designed values.

SiH_4 and GeH_4 gases in a H_2 carrier. AsH_4 was used to dope the contact regions n-type[11] at $N_D \sim 3\times10^{18}\,\mathrm{cm}^{-3}$. The heterolayers were grown on a n-type (100) Si substrate with approximately a 3 μm thick n-type strain–relaxation buffer graded from Si to $Si_{0.7}Ge_{0.3}$ and a 1 μm thick n-$Si_{0.7}Ge_{0.3}$ buffer. The wafer was then removed from the growth chamber and given a modified Radio Corporation of America clean[11] to remove excess As from the surface in an attempt to circumvent the As dopant segregation problems in CVD material.[12] This technique of regrowth has already demonstrated high mobilities at low temperatures when used in modulation doped samples with the cleaned interface 10 nm below the strained-Si quantum well[11] and SiGe RTDs.[4] The wafers were replaced in the growth chamber and the following layers grown: 10 nm i-$Si_{0.7}Ge_{0.3}$ buffer, 10 nm i-$Si_{1-x}Ge_x$ graded from $x=0.3$ to $x=0.0$, 2 nm i-$Si_{0.4}Ge_{0.6}$ barrier, 3 nm i-Si well, 2 nm i-$Si_{0.4}Ge_{0.6}$ barrier, 5 nm i-$Si_{1-x}Ge_x$ graded from $x=0.0$ to $x=0.3$, 50 nm n-$Si_{0.7}Ge_{0.3}$ doped at $N_D \sim 3\times10^{18}\,\mathrm{cm}^{-3}$, 10 nm n-$Si_{0.7}Ge_{0.3}$ doped at $N_D \sim 1\times10^{19}\,\mathrm{cm}^{-3}$ and a 4 nm n-Si cap. The higher doping of the cap layers is aimed at reducing the contact resistances which also increase the peak voltage.[4] Devices were processed into mesas using reactive ion etching and Au (1% Sb) ohmic contacts were used. Figure 2 shows a transmission electron micrograph of the material. No threading dislocation segments were visible in any of the transmission electron micrographs (TEMs) images of the barrier region.

The current–density versus applied voltage (I–V) measured at 77 K is shown in Fig. 3 for a 30×30 μm device. A positive bias corresponds to the substrate of the wafer being held at 0 V and a positive bias being applied to the surface contact. A number of devices have been measured which all demonstrate nominally identical results. No NDR was observed at room temperature. Three clear NDR regions are observed with the largest PVCR of 1.67 at a peak voltage of 40 mV and current density of $0.08\,\mathrm{A/cm}^2$. Previous results have demonstrated peak voltages of between 1 and 2 V,[4,5] while Fig. 3 clearly demonstrates the large reduction in the peak voltage by using graded spacer wells and higher doping levels in the capping layers. The effect of increasing the graded spacer in the emitter is observed when a negative bias is applied to the surface. Additional asymmetry will result from growth related phenomena such as dopant memory. The NDR shifted to a peak current density of $2.2\,\mathrm{A/cm}^2$, a PVCR of 1.3 and a peak voltage position of -0.29 V.

Previous modelling of strained-$Si_{0.4}Ge_{0.6}$ barriers on relaxed $Si_{0.8}Ge_{0.2}$ has shown that the light (transverse) effective-mass tunneling from the virtual substrate dominates the current–voltage characteristics over the high (longitudinal) effective-mass electrons in the emitter well.[4] The present results suggest that grading the spacers does not change the physics of the tunneling compared to square quantum well spacers. Since the effective-mass in the growth (vertical) direction of a two-dimensional (2D) layer is the longitudinal heavy mass, the wave function of the 2D electron gas will decay very quickly in the vertical direction. Therefore, most of the wave function will be close to the barrier where the Ge concentration is low or zero and the splitting of the valleys is largest. Hence, no electrons populate the valleys with the transverse light effective mass and the tunneling is dominated by the electrons with the light effective mass in the virtual substrate (the transmission coefficient depends exponentially on the inverse of the square root of the effective mass).

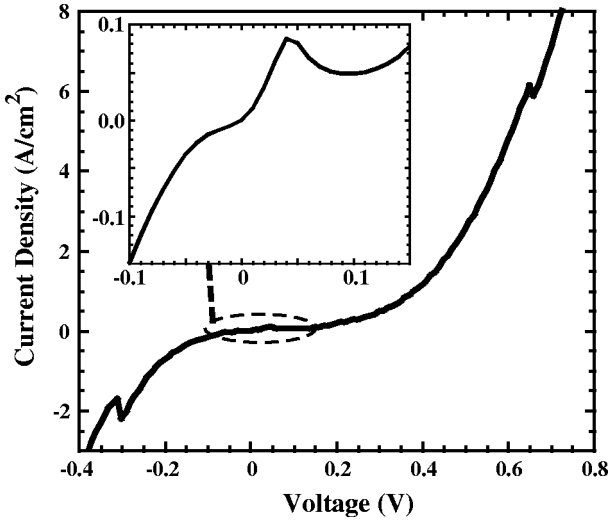

FIG. 3. The I–V plot at 77 K for a 30×30 μm device showing three clear NDR peaks. The insert shows an expanded area in the low bias region with a J_p of $0.08\,\mathrm{A/cm}^2$, a PVCR of 1.67 at a peak voltage of 40 mV.

Figure 4 shows the temperature dependence of the

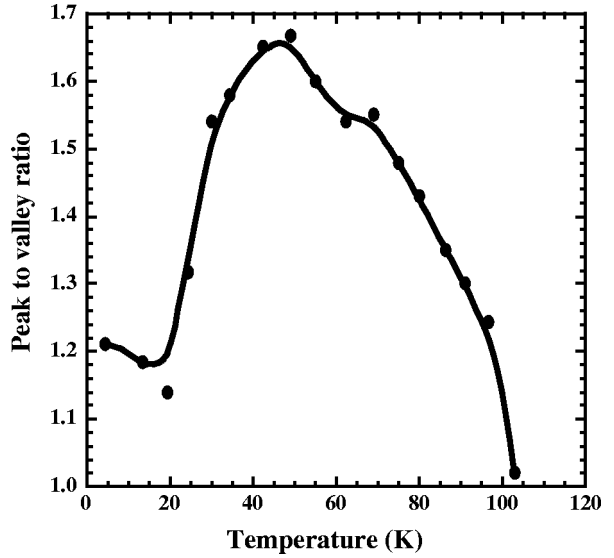

FIG. 4. The PVCR as a function of temperature for the NDR at 40 mV shown in Fig. 3. The curve is a guide to the eye.

PVCR of the 40 mV NDR region in a second device. The differences between the PVCR values in Figs. 3 and 4 is related to the change in layer thicknesses as a function of the radius of the wafer due to heating nonuniformity during growth.[13] The high temperature decrease in PVCR is related to the low barrier height with respect to the virtual substrate which is predicted to be 80 meV from theory.[10] A $Si_{0.7}Ge_{0.3}$ substrate was chosen to allow the band structure to be compared with previous results on $Si_{0.8}Ge_{0.2}$ substrates. Comparison between results of strained-$Si_{0.4}Ge_{0.6}$ grown on relaxed $Si_{0.8}Ge_{0.2}$[4,5] which operate at room temperature and the present $Si_{0.7}Ge_{0.3}$ demonstrate the higher barrier height on the $Si_{0.8}Ge_{0.2}$ virtual substrates as suggested by theory (about 110 meV for $Si_{0.8}Ge_{0.2}$ virtual substrates)[10] through the temperature dependence of the PVCR. The conduction band discontinuities for quantum wells from theory[10] suggests values which are about 50% too large.[3] The present data does not yet allow an accurate estimate of the barrier heights to compare to theory. The decrease in the PVCR at temperatures below 40 K (Fig. 4) is believed to be related to the ohmic contacts, especially in the lower doped substrate, becoming more resistive at lower temperatures. High temperature anneals have not been used for the ohmic contact metallization to prevent spiking of the top metal through the RTD barriers. The present doping and ohmic metallization schemes are adequate for devices to operate at 77 K or above as required for applications but not for measurements at liquid He temperatures.

In conclusion, NDR has been demonstrated in the Si/SiGe system at temperatures up to 100 K. Three clear NDR regions were observed with the largest PVR of 1.67 at a peak voltage of 40 mV and a peak current density of 0.08 A/cm^2. By increasing the graded spacer in the emitter, the NDR shifted to a peak current density of 2.2 A/cm^2, a PVCR of 1.3, and a peak voltage position of -0.29 V. The results also demonstrate that strained-$Si_{0.4}Ge_{0.6}$ barriers grown on relaxed $Si_{0.8}Ge_{0.2}$ have a higher conduction band barrier than those grown on relaxed-$Si_{0.7}Ge_{0.3}$ substrates. Therefore, it may be concluded that using graded spacers on relaxed $Si_{0.8}Ge_{0.2}$ will allow a structure to operate at room temperature. While the present designs do not yet match those required for circuit integration, the results suggest that an appropriately optimized structure could be used in a tunneling static random access memory (TSRAM) at room temperature.

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