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$Si(100)$–SiO_2 interface properties following rapid thermal processing

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Si(100)–SiO_2 interface properties following rapid thermal processing

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An experimental examination of the properties of the Si(100)–SiO_2 interface measured following rapid thermal processing (RTP) is presented. The interface properties have been examined using high frequency and quasi-static capacitance-voltage (CV) analysis of metal-oxide-silicon (MOS) capacitor structures immediately following either rapid thermal oxidation (RTO) or rapid thermal annealing (RTA). The experimental results reveal a characteristic peak in the CV response measured following dry RTO and RTA ($T>800\,^{\circ}\mathrm{C}$), as the Fermi level at the Si(100)–SiO_2 interface approaches the conduction band edge. Analysis of the QSCV responses reveals a high interface state density across the energy gap following dry RTO and RTA processing, with a characteristic peak density in the range 5.5×10^{12} to $1.7\times10^{13}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ located at approximately 0.85–0.88 eV above the valence band edge. When the background density of states for a hydrogen-passivated interface is subtracted, another peak of lower density (3×10^{12} to $7\times10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$) is observed at approximately 0.25–0.33 eV above the valence band edge. The experimental results point to a common interface state defect present after processes involving rapid cooling ($10^1-10^2\,^{\circ}\mathrm{C/s}$) from a temperature of 800 °C or above, in a hydrogen free ambient. This work demonstrates that the interface states measured following RTP ($T>800\,^{\circ}\mathrm{C}$) are the net contribution of the P_{b0}/P_{b1} silicon dangling bond defects for the oxidized Si(100) orientation. An important conclusion arising from this work is that the primary effect of an RTA in nitrogen (600–1050 °C) is to cause hydrogen desorption from pre-existing P_{b0}/P_{b1} silicon dangling bond defects. The implications of this work to the study of the Si–SiO_2 interface, and the technological implications for silicon based MOS processes, are briefly discussed. The significance of these new results to thin oxide growth and optimization by RTO are also considered. © *2001 American Institute of Physics.*
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I. INTRODUCTION

In current silicon based metal-oxide-silicon (MOS) technologies, rapid thermal processing (RTP) is now replacing conventional furnace processing for a range of processing steps. The use of RTP is driven by the necessity to reduce the overall thermal budget associated with device fabrication and in particular to maintain the desired device electrical properties. RTA is now used for process steps such as: dopant activation, dopant redistribution, reflow of dielectric layers, and formation of contacts and metal silicides. There is also a growing interest in RTO to form thin dielectric layers for the gate oxide of MOS field effect transistors (MOSFETs) and for the storage capacitor dielectric in dynamic random access memory (DRAM) applications.

As the properties of the Si–SiO_2 interface and the bulk of the SiO_2 layer are central to the performance and long term stability of MOS based devices, the influence of RTP on the properties of the Si–SiO_2 interface is an area that is clearly important to characterize and understand. In recent years, a range of publications have appeared which indicates the emergence of atypical capacitance–voltage (CV) characteristics obtained on polysilicon/oxide/silicon capacitor structures exposed to RTA, or for mercury or aluminum gate MOS structures measured directly following RTO. These results have been obtained primarily on samples measured directly following exposure to RTA, with no annealing in hydrogen after the RTA process step.[1–7] The atypical CV response has also been obtained from experiments designed to investigate polysilicon depletion effects,[8] on samples intended to characterize boron doping of the polysilicon layer,[9] or on short-loop experiments examining a clustered approach to MOSFET gate stack formation.[2] Peak responses in the CV characteristics have also been observed on aluminum/oxide/silicon structures,[10] and for oxide layers grown by RTO and measured using a mercury probe technique.[11]

The intention of this article is to bring together a range of CV observations that have been reported by the authors, and other groups,[1–8,11,12] to provide detailed information on the properties of the Si(100)–SiO_2 interface measured directly following RTA or RTO. In addition, the work suggests an explanation for the physical origin of the measured interface states, as well as considering the significance of the findings.

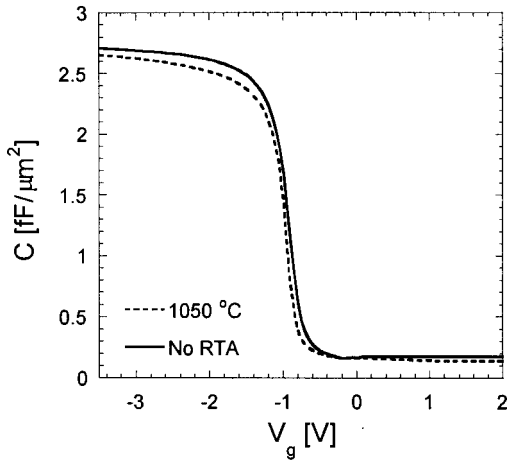

FIG. 1. Measured high frequency (1 MHz) CV characteristics of polysilicon/oxide(120 Å)/*p*-silicon (100) capacitor structures from process 1. The solid line is the control sample which received no RTA. The dotted line is for the capacitor which was exposed to a 1050 °C, 10 s RTA in N_2 as the final processing step. Neither sample received a final forming gas alloy.

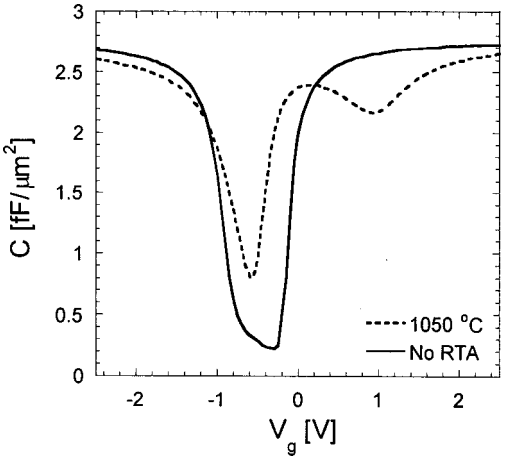

FIG. 2. Measured quasi-static CV characteristics (same capacitor structures as in Fig. 1/process 1). The solid line is the control sample which received no RTA. The dotted line is for the capacitor which was subjected to a 1050 °C, 10 s RTA in N_2 as the final processing step. Neither sample received a final forming gas alloy. The figure illustrates the emergence of a peak in the CV characteristic resulting from the RTA process.

The experimental results are divided broadly into two sections. In the first section, the Si(100)–SiO_2 interface properties of polysilicon/oxide/silicon capacitor structures exposed to an RTA in the temperature range 600–1050 °C (10 s in N_2), as the final processing step, are presented and analyzed. The results in this section also include the effect of annealing the polysilicon/oxide/silicon capacitor samples in forming gas ($T>400$ °C) following the RTA. In the second section, the Si(100)–SiO_2 interface properties measured directly following RTO in the range 1000–1100 °C are analyzed using the mercury probe CV technique. The density of states (DOS) across the energy gap at the Si(100)–SiO_2 interface have been calculated from the QSCV characteristics.

It is important to emphasize that analysis of the QSCV measurements has yielded the same general trend in the DOS profiles for a wide range of samples fabricated in different research centers and semiconductor fabrication facilities. The experimental results have been observed for: *n*- and *p*-type (100) silicon substrates; for furnace and rapid thermal oxidation at various temperatures; and for degenerately doped polysilicon or mercury gate contacts. In the case of polysilicon gate contacts, the results have been obtained for $POCl_3$, *in situ*, and implanted polysilicon layers, wet and dry polysilicon definition, and for LOCOS and non-LOCOS isolated capacitor structures. This eliminates the possibility that the observations are due to process or machine specific contamination effects. In this paper representative experimental results are presented for polysilicon gate capacitor structures fabricated using two thermal processes and for the mercury-gate structures fabricated with three different processes.

II. SAMPLE FABRICATION DETAILS

A. Polysilicon gate MOS capacitors

The experimental and calculated results presented in Figs. 1–5 were obtained for 150 mm boron (B) doped silicon (100) wafers with a dopant concentration of approximately $1\times10^{15}\,cm^{-3}$. Following a pre-oxidation clean, a 120 Å oxide was grown in dry oxygen at 850 °C, followed by a 60 min anneal in N_2 at 850 °C. The ramp down rate following oxidation is 3 °C/min, with a pull from the furnace at 600 °C at 8 cm/min. The gate was formed by chemical vapor deposition of 3000 Å of polysilicon. Following the removal of the polysilicon and oxide layers from the backside of the wafer, the polysilicon was phosphorus doped from a $POCl_3$ source. Dry etching of the polysilicon layer formed capacitors of various areas. Following the resist strip, the samples received a 30 min anneal in nitrogen at 900 °C. As a final process step, capacitors were subjected to 10 s RTAs in nitrogen in the temperature range 600–1050 °C. The RTA treatments were performed in a STEAG Heatpulse 8108 system. Selected samples received no RTA treatment (subsequently referred to as process 1).

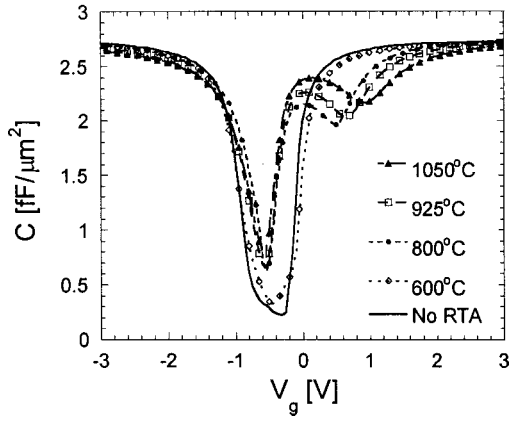

FIG. 3. Measured quasi-static CV characteristics of polysilicon/oxide(120 Å)/*p* silicon(100) capacitor structures (process 1) subjected to RTA at a range of temperatures as the final processing step. All RTA processes were 10 s duration in N_2. The control sample exposed to no RTA is also shown.

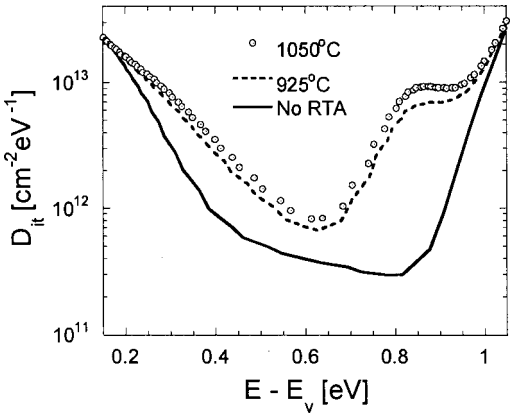

FIG. 4. Densities of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface, extracted from the measured QSCV characteristics in Fig. 3. The interface state densities are plotted with reference to the highest energy in the valence band (E_v). The figure shows the data for the 1050 °C RTA, 925 °C RTA, and for the control sample (no RTA) from process 1.

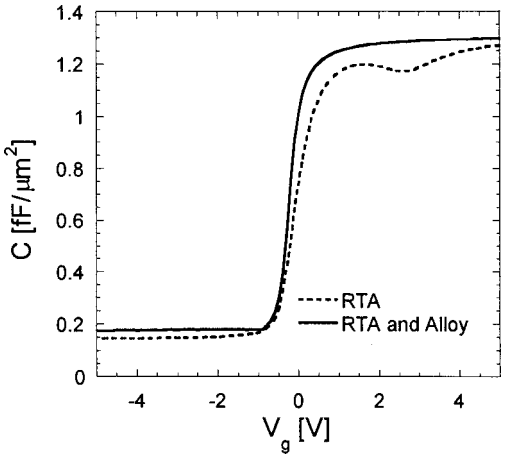

FIG. 6. Measured high frequency (8 kHz) CV characteristics of polysilicon/oxide(263 Å)/*n* silicon (100) capacitor structures from process 2. The figure shows the CV response for the capacitor subjected to a 10 s RTA at 1050 °C in N_2 as the final processing step (dotted line), and for the capacitor processed with RTA at 1050 °C, 10 s, N_2, and final alloy at 440 °C in 5% H_2/95%N_2 for 60 min (solid line).

For the wafers exposed to RTA with a subsequent alloy (Figs. 6–8), the starting material was 100 mm phosphorus (P) doped silicon (100) wafers with a doping concentration of approximately $1\times10^{15}\,\mathrm{cm}^{-3}$. Following a pre-oxidation clean, a 260 Å oxide was grown in dry oxygen at 950 °C, followed by an anneal in nitrogen for 20 min at 950 °C. The gate contact was formed by chemical vapor deposition at 620 °C of 4500 Å of polysilicon. The polysilicon gate layer was doped from a $POCl_3$ source after removal of the oxide and the polysilicon layers from the back of the wafer. Wet etching of the polysilicon layer formed capacitors of various areas. After capacitor definition the wafers were exposed to a 10 s RTA at 1050 °C in a N_2 ambient (AST SHS-100 system). Selected wafers then experienced an additional alloy at 440 °C in 5% H_2/95%N_2 for 60 min after the RTA step. This is subsequently referred to as process 2.

For all polysilicon gate structures the HFCV response was measured on-wafer with a HP4284A multiple frequency CV meter. Prior to all measurements open and short circuit calibrations were performed. The QSCV response was measured using a HP4140B picoammeter/voltage source. In addition, current-voltage characteristics of the MOS structure over the intended CV bias range were recorded on all samples prior to HFCV and QSCV analysis to ensure negligible ($<1\times10^{-12}$ amps) oxide conduction. All measurements were performed at room temperature.

B. Mercury gate MOS capacitors

For the samples measured directly following RTO, three oxidation conditions are considered. The samples were measured directly after RTO, using a mercury probe CV system (Four Dimensions CV map). Measurements were performed at room temperature. For the results presented in Figs. 9 and

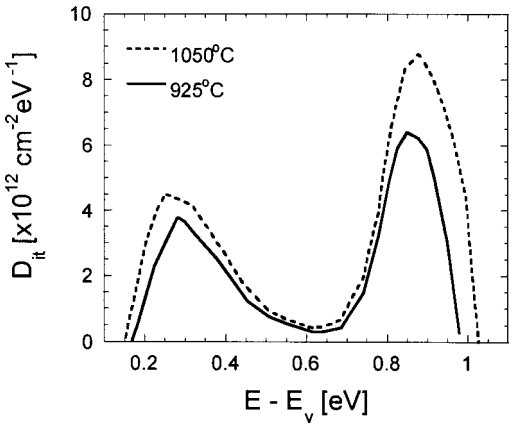

FIG. 5. Densities of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface for the 1050 °C and 925 °C RTA samples from process 1, with the background U-shaped density of states for the control sample (no RTA) subtracted.

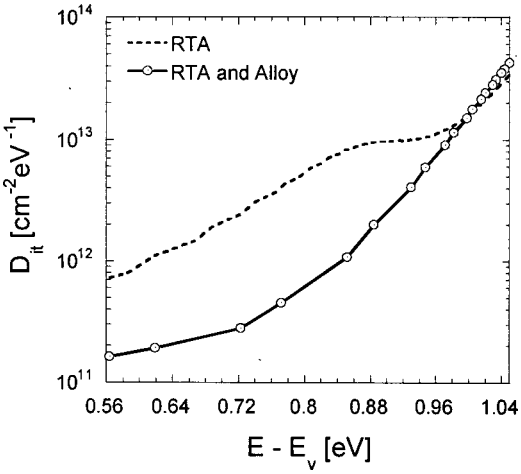

FIG. 7. Density of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface, extracted from the measured HFCV characteristics in Fig. 6 for process 2. The interface state densities are plotted with reference to the highest energy in the valence band (E_v). The figure shows the data for the 1050 °C RTA only sample, and for the sample subjected to RTA and alloy. The D_{it} values from E_v to mid-gap are not plotted as the extraction was performed using HFCV data.

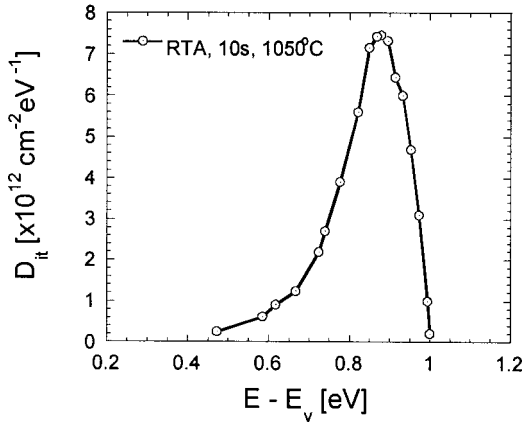

FIG. 8. Density of interface states (D_{it}) from mid-gap to the conduction band edge gap at the Si(100)–SiO_2 interface for the RTA only sample (process 2), with the background U-shaped density of states for the control sample (RTA+alloy) subtracted.

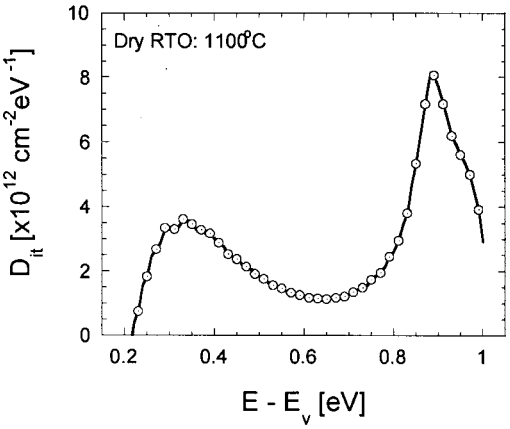

FIG. 10. Densities of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface determined from the QSCV response in Fig. 9 from process 3. The background U-shaped density of states for the control sample (RTO+alloy) has been subtracted. The interface state densities are plotted with reference to the highest energy in the valence band (E_v).

10, the starting substrates were 200 mm *p*-type Si(100), with a substrate doping concentration of $5\times10^{14}\,cm^{-3}$. Following a pre-oxidation HF dip, a 75 Å oxide layer was grown in 100% O_2 by RTO at 1100 °C for 30 s in a STEAG Starfire RTP system (process 3). The CV results in Fig. 11 and D_{it} plot in Fig. 12 are for 200 mm boron doped Si(100) wafers, with a dopant concentration of $8\times10^{14}\,cm^{-3}$. For process 4, a 40 Å oxide film was grown by RTO at 1000 °C (100% O_2) for 8 s in a STEAG RTP Heatpulse 8800. In process 5, a 40 Å film was grown at 1015 °C for 33 s in 2.25 slpm H_2O/2.75 slpm N_2 ambient with a STEAG RTP Steampulse. For all RTO processes the ramp up rate was approximately 60 °C/s, with ramp down rates of approximately 40 °C/s. The ramp down was performed in an N_2 ambient.

III. EXPERIMENTAL RESULTS

A. Polysilicon gate MOS capacitors: RTA

The results in Fig. 1 show the high frequency (1 MHz) CV characteristics obtained for polysilicon/oxide/silicon capacitor structures from process 1. The figure illustrates the CV response obtained following polysilicon gate definition, with no RTA (solid line), and the CV response measured after the 10 s, 1050 °C RTA in N_2 (dotted line). The RTA step has introduced distortion near accumulation, and also induced a flat band voltage shift in the region between accumulation and inversion. These general observations are consistent with the HFCV results presented in Ref. 3. The corresponding QSCV characteristics are shown in Fig. 2. The QSCV of the capacitor exposed to the RTA exhibits the distortion in accumulation, as seen in the high frequency CV characteristic, as well as distortion between accumulation and inversion. However, the most striking feature in the characteristic is the emergence of a peak in the CV response, in the vicinity of strong inversion. Since the effect occurs as the silicon/oxide interface approaches inversion, the peak is not observed by high frequency CV analysis for a *p*-type silicon substrate. The results in Fig. 3 show the QSCV characteristics for a range of RTA temperatures. From the QSCV characteristics, it is evident that the effect of the RTA step on the Si–SiO_2 interface increases as a function of the RTA temperature (for a constant RTA time of 10 s). Also from the

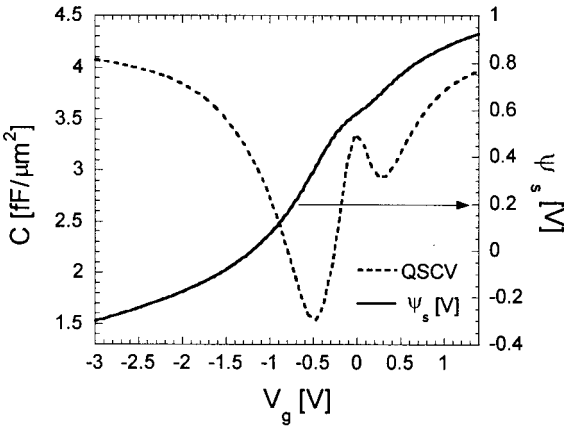

FIG. 9. Quasi-static CV characteristics, and corresponding surface potential (ψ_s) versus gate voltage (V_g) relationship, for a 75 Å oxide grown by RTO at 1100 °C (process 3). The CV response was measured directly following the RTO process using a mercury probe CV technique.

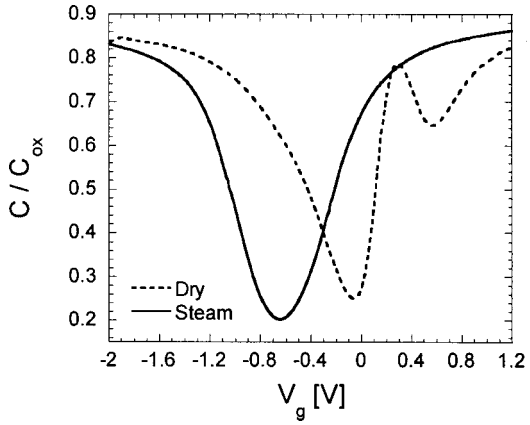

FIG. 11. Normalized quasi-static CV characteristics for ≈40 Å thick oxides layers grown by dry (process 4) and steam diluted (process 5) RTO.

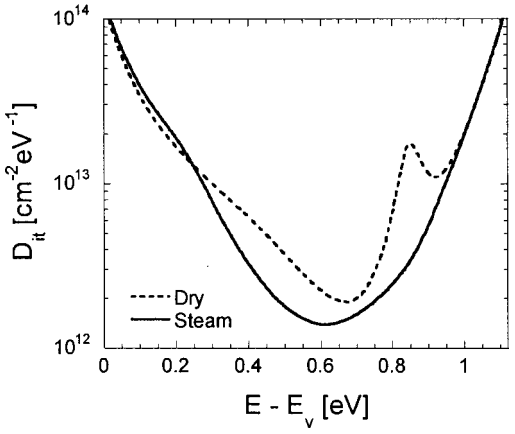

FIG. 12. Densities of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface determined from the dry and steam assisted QSCV responses shown in Fig. 11 (processes 4 and 5).

figure, it is seen that RTA temperatures as low as 600 °C cause a measurable distortion in the QSCV characteristics. (The QSCV characteristics in Fig. 3 demonstrate the same general features as presented in Ref. 1.)

The distortion of the QSCV curves after the RTA indicates the presence of interface states at the Si–SiO_2 surface. Moreover, the presence of the peak near inversion is an indication of an interface state distribution that peaks about a specific energy.[8,12] The interface state density has been determined from analysis of the QSCV characteristics. The surface potential for each corresponding gate voltage has been determined using the Berglund integral.[13] The DOS distribution across the energy gap for the RTA samples (925 °C, 1050 °C), and the control sample are shown in Fig. 4 (for clarity the 600 °C and 800 °C RTA DOS profiles are not shown). The interface state density is plotted with reference to the highest energy in the valence band (E_v). Following the RTA process, the interface state densities are higher than the control sample (no RTA) over the energy range $E_v+0.2$ to $E_v+1.0$ eV. However, the prominent feature is the peak in the DOS value at around 0.85 eV above the valence band edge (E_v). The peak is not observed on the control sample. An increase in the RTA temperature, increases the total density of states (i.e., integral under the peak), but does not change the position of the maximum interface state density.

To examine the contribution of the interface states measured following RTA, the background U-shaped distribution of interface states for the control sample (no RTA and no forming gas anneal) has been subtracted. Interpolation was used, as the data sets do not share common $E-E_v$ values. The result of subtracting the background U-shaped density of states is shown in Fig. 5. The procedure of subtracting the background density of states is considered to be valid over the range $E_v+0.15$ to $E_v+1.05$ eV. When the background is subtracted, a peak in the DOS profile emerges in the lower portion of the energy gap, in the range $E_v+0.25-0.28$ eV, with a peak density of $3.8\times10^{12}\,cm^{-2}\,eV^{-1}$ and $4.6\times10^{12}\,cm^{-2}\,eV^{-1}$ for the 925 °C and 1050 °C RTAs, respectively. The peak interface state density in the lower energy gap has approximately half the density of the upper energy gap maximum. The upper energy gap maximum occurs in the range 0.85–0.87 eV, with peak densities of $6.5\times10^{12}\,cm^{-2}\,eV^{-1}$ and $8.9\times10^{12}\,cm^{-2}\,eV^{-1}$ for the 925 °C and 1050 °C RTAs, respectively. The interface state density has a minimum value at $E_v+0.6$ eV. As a consequence of the lower peak value of the interface state density between E_v and E_i, a clear peak in the DOS profile is not observed prior to subtraction of the background U-shaped density of states. It is worth noting that the interface trap capacitance in the vicinity of the peak in the CV characteristic is significantly greater than the oxide capacitance (C_{ox}). For example, in the case of the 1050 °C RTA, the interface trap capacitance for the upper energy gap DOS peak (at a gate voltage of 0.15 V) is $1.4\,fF\mu m^{-2}$, corresponding to approximately five times the oxide capacitance.

The results in Fig. 6 show the high frequency (8 kHz) CV behavior measured for the case of RTA only (dotted line), and for RTA and subsequent alloy (solid line), for capacitor structures from process 2. Only high frequency CV data were recorded for this process. The MOS capacitor structure measured after RTA exhibits a peak in the CV characteristic as the Fermi level at the Si(100)–SiO_2 interface approaches the conduction band edge. As the silicon doping is *n*-type for this process, the prominent peak occurs as the silicon/oxide surface approaches accumulation, and is therefore observed using both quasistatic and high frequency CV techniques. To allow accurate DOS values to be extracted from the HFCV data, the test signal frequency of the impedance meter was reduced until the peak response in the CV characteristic was frequency independent. Within the limitations imposed by measurement noise, this frequency was determined to be 8 kHz. Hence, for test signal frequencies of $\leqslant$8 kHz, the response of the upper energy gap interface state to the test signal frequency can be considered quasi-static, and DOS values were extracted using this frequency.

The interface state distributions have been extracted from the RTA only sample (8 kHz) and for the RTA+alloy sample. The results are presented in Fig. 7. Interface state density profiles in the lower portion of the energy gap are not available in this case, as the CV data were recorded at a frequency too high for minority carrier response in the substrate. The DOS data are considered to be valid from approximately mid-gap $E_v+0.56$ to $E_v+1.05$ eV. From the figure, it is evident that an alloy in 5% H_2/95% N_2 at 440 °C for 60 min entirely removes the upper energy gap peak in the DOS distribution. The interface state distribution after RTA, re-plotted with the background U-shaped distribution of RTA+alloy subtracted, is shown in Fig. 8. The interface state density exhibits a clear peak of density $7.5\times10^{12}\,cm^{-2}\,eV^{-1}$ at an energy level of 0.88 eV. The upper energy gap DOS profile peaks at the same energy as for process 1, with a similar peak density (see Fig. 5).

Finally, it is noted that the interface states measured following RTA are stable at room temperature. The CV characteristics and associated DOS profiles have been recorded intermittently over a six year period. No changes in the interface state density profile were measured.

B. Mercury gate MOS capacitors: RTO

Figure 9 shows the QSCV response, and corresponding surface potential (ψ_s) versus gate voltage (V_g) relationship, for a 75 Å oxide layer grown by RTO in dry oxygen at 1100 °C (process 3). The measurement was performed using a mercury probe as the gate contact. The samples were measured directly after the RTO growth. Once again, a peak appears in the QSCV response, in the vicinity of strong inversion, as the Fermi level at the Si(100)–SiO_2 interface approaches the conduction band edge. The pinning of the surface potential as the Fermi level at the Si(100)–SiO_2 interface moves through the upper band gap interface defect is also evident. The QSCV characteristics for the dry RTO processes are similar to previous measurements[14] on thin (≈30 Å) SiO_2 layers grown on Si(100) by dry RTO at 900 °C. The interface state density profile extracted from the QSCV (with the background DOS for an RTO+alloy sample subtracted) is shown in Fig. 10. With the background U-shaped DOS removed, the interface state profile exhibits essentially the same features as the polysilicon gate MOS structures measured following RTA, with interface state peaks occurring at $E_v+0.33$ eV and $E_v+0.88$ eV.

Interestingly, the peak in the CV response, and in the corresponding DOS, is not observed for the case of steam assisted RTO. This is illustrated in Fig. 11, where the normalized QSCV data are plotted for the ≈40 Å thick oxides grown by dry (process 4) and steam diluted (process 5) RTO. The extracted interface state density profiles for both QSCV responses are shown in Fig. 12. In the case of the steam diluted RTO growth, no peak is evident in the upper portion of the energy gap.

However, a feature is evident in the lower energy gap at an energy level of approximately $E_v+0.25$ eV [from Fig. 11 a large flat band voltage shift is evident for the steam RTO sample ($V_{fb}\approx -1.2$ V)]. This large V_{fb}, corresponding to fixed positive oxide charge densities in excess of 10^{12} cm^{-2}, is present as the sample received no post-oxidation annealing following the steam assisted RTO.

This positive charge is reduced to negligible values with appropriate inert annealing following the oxidation process. This issue is not considered further here, as it is not relevant to the main focus of the article.

C. Comparison of results

The interface state density profiles across the energy gap measured following RTA or dry RTO demonstrate a striking similarity. This is illustrated in Fig. 13, where the interface state density profiles (with the background U-shaped DOS subtracted) are plotted together for the polysilicon gate capacitors exposed to 925 °C and 1050 °C RTA (process 1), and for the oxide grown by dry RTO at 1100 °C (process 3). The capacitors were fabricated at different facilities using different pre-oxidation cleans, different oxidation processes (RTO/furnace), and different oxide thicknesses. However, within the limitations that are inherent to the extraction procedure,[13] the interface state density profiles exhibit the same characteristic features.

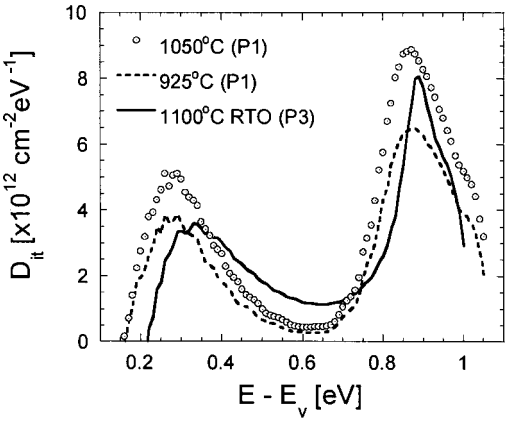

FIG. 13. Densities of interface states (D_{it}) across the energy gap at the Si(100)–SiO_2 interface measured following RTA at 925 °C and 1050 °C for polysilicon gate MOS structures (process 1: P1), and for oxide layer grown by dry RTO at 1100 °C (process 3: P3), measured using a mercury probe CV system.

IV. DISCUSSION: ORIGIN OF INTERFACE STATES

From the results in the previous section, immediately after RTA (for polysilicon gate samples) or directly following a dry RTO process, two interface state peaks at $E_v+0.25-0.33$ eV and $E_v+0.85-0.88$ eV are recorded at the Si(100)–SiO_2 interface. The upper energy gap interface state peak has the higher density (6×10^{12} cm^{-2} eV^{-1} to 1.7×10^{13} cm^{-2} eV^{-1}), and as a consequence, results in a peak response in the CV characteristic. The lower energy gap peak is less distinct, and is only clearly evident when the background U-shaped distribution of states for a hydrogen-passivated sample is subtracted. These results point to a common interface state defect present after processes involving rapid cooling (10^1-10^2 °C/s) from a temperature of ≥800 °C in a hydrogen free ambient. Within experimental accuracy the same DOS profiles are obtained for a broad range of process conditions, oxide thickness values, and processing tools. This eliminates the possibility of the interface states originate from either process or machine specific contamination, and points to interfacial states that are specific to the Si(100)–SiO_2 interface.

The similarity in the interface state distributions for a range of process conditions indicates that the dry RTA/RTO processes either: (1) *generate additional* interface states which are not present for oxides fabricated by conventional furnace processing; or (2) dissociate hydrogen from RTA, or prevent hydrogen passivation of RTO interface states, which are fundamental to the properties of the Si(100)–SiO_2 interface.

Generation of additional defects by RTP has been suggested in other works. It has been proposed that the defect generation occurs as a consequence of the rapid cooling rates experienced during RTP.[3,4,7] The suggestion that the RTA/RTO processes generate additional interface states is problematic for a number of reasons. From the results above, following a 10 s RTA in N_2 at 1050 °C (which would be typical for a polysilicon gate doping activation cycle in a CMOS process), the integrated interface state densities across the energy gap would be in excess of 1×10^{12} cm^{-2}. If

these were additional interface states generated by the RTA/RTO processes, then MOS capacitors or MOSFETs processed using RTA, or RTO for gate oxide formation, would exhibit an additional $1\times10^{12}\,\mathrm{cm}^{-2}$ hydrogen passivated interface states when compared to MOS capacitors or MOSFETs fabricated using no RTP processes. The hydrogen passivation will inevitably occur during full device fabrication, in processes such as polysilicon deposition, oxide deposition, etching, and final alloy.[15] This high density of additional hydrogen passivated interface states would result in reliability degradation of MOS/MOSFET structures fabricated using RTP. However, published results on thin gate oxides grown by RTO exhibit improved oxide reliability during charge to breakdown measurements when compared to oxides grown in a conventional furnace.[16] Also, polysilicon gate capacitors exposed to RTA have been reported to exhibit improved oxide reliability compared to oxides with no RTA processes.[17] The argument that RTA/RTO processes generate additional interface states, not present for conventional furnace oxidation, cannot be reconciled with these published results.

This leaves the second argument as the source of the interface states measured after RTA/RTO. To examine this argument it is instructive to first consider the extensive studies that have been performed on defects that are unique to the $Si-SiO_2$ interface. When experimental procedures are employed to ensure the $Si-SiO_2$ interface states are not passivated by hydrogen, then using techniques such as: electron paramagnetic resonance (EPR),[18,19] CV characterization,[20] and the MOS conductance method,[21] interface states have been detected at specific levels in the energy gap. Using the EPR method it has been shown that for unpassivated $Si-SiO_2$ interfaces the majority of the measured interface states are silicon atoms with dangling bond (P_b) orbitals.[23] The technique most commonly used to dissociate the hydrogen from the $Si-SiO_2$ interfacial defects is vacuum annealing (1×10^{-6} Torr) at temperatures in the vicinity of 700 °C. An alternative technique is to rapidly (<1 s) pull the wafers following a conventional furnace oxidation.[19]

The EPR signal due to the P_b center is characteristic to the $Si-SiO_2$ interface and silicon orientation.[24] In the case of a silicon (111) orientation, it is widely accepted to be a trivalent silicon center ($\cdot Si{\equiv}Si_3$) located at the interface, where the dangling bond is located perpendicular to the silicon/oxide plane.[23] For the $Si(111)-SiO_2$ interface, the DOS distribution across the energy gap demonstrates two clear peaks in the lower and upper portions of the energy gap. The precise energy levels of the peaks in the DOS distribution vary slightly with the characterization method used. Typical values are $E_v+0.27\,\mathrm{eV}(+/0)$ and $E_v+0.84\,\mathrm{eV}(0/-)$.[20] However, at the $Si(100)-SiO_2$ interface, two EPR active defects are detected, termed P_{b0} and P_{b1}. A recent study[25] has established that both P_{b0} and P_{b1} are chemically identical to the P_b center at the $Si(111)-SiO_2$ interface (i.e., $\cdot Si{\equiv}Si_3$).

The interface state distributions resulting from the combined P_{b0}, P_{b1} defects at the $Si(100)-SiO_2$ interface have been examined using EPR, CV, and conductance methods. All of the published works show a clear interface state peak in the upper portion of the energy gap. An interface state peak of lower density is also recorded in the lower portion of the energy gap using EPR. Table I shows the density and energy level of the P_b centers at the $Si(100)-SiO_2$ interface obtained from the works of Gerardi[19] and Uren.[22] The results obtained from this work for polysilicon gate MOS capacitors exposed to RTA, and samples measured following RTO, are presented for comparison.

TABLE I. Density and energy level of P_b centers at the $Si(100)-SiO_2$ interface determined in other works, compared to the values obtained in this study following RTA/RTO. E_t refers to the energy position of the peak in the DOS distribution in the upper and lower portion of the energy gap [eV]. D_{it} is the value of the interface state density [$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$] at the peaks in the DOS profile.

Work	Method	E_t [eV]	Peak D_{it} [$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$]
a	Vacuum anneal +	$E_v+0.33$	3.5×10^{12}
	CV	$\approx E_v+0.90$	6.0×10^{12}
b	Vacuum anneal + conductance	$E_v+0.84$[c]	2.7×10^{12}
This work—RTO	RTO/QSCV	$E_v+0.33$	3.6×10^{12}
	1100 °C, *p*-Si [75 Å]	$E_v+0.88$	8.0×10^{12}
This work—RTO	RTO/QSCV	$E_v+0.29$	6.9×10^{12}
	1000 °C, *p*-Si [37 Å]	$E_v+0.85$	1.7×10^{13}
This work—RTA	RTA/QSCV	$E_v+0.88$[d]	1×10^{13}
	1050 °C, *n*-Si		
This work—RTA	RTA/QSCV	$E_v+0.25$	4.6×10^{12}
	1050 °C, *p*-Si	$E_v+0.87$	8.9×10^{12}
This work—RTA	RTA/QSCV	$E_v+0.28$	3.8×10^{12}
	925 °C, *p*-Si	$E_v+0.85$	6.5×10^{12}

[a]See Ref. 19.
[b]See Ref. 22.
[c]No data available for lower band gap.
[d]Extracted from HFCV. Only upper band gap data available.

The results in Table I show that the interface states measured following RTA/RTO exhibit essentially the same defect density and energy levels as the combined P_{b0}/P_{b1} levels following vacuum annealing, or obtained by a rapid pull following a furnace oxidation. In addition, the results presented in Fig. 13 exhibit very close agreement with the DOS profile across the energy gap determined for the P_{b0}/P_{b1} centers on dry oxidized Si(100) wafers.[19] Based on this observation and the results in Table I, we argue that the measured interface states following RTA/RTO can be reliably identified as the combined effect of the P_{b0}/P_{b1} defects at the $Si(100)-SiO_2$ interface. Moreover, this explanation is also consistent with other published work on P_b defects. For temperatures in excess of 500 °C, hydrogen is dissociated from the dangling bond defect[26] ($Si_3{\equiv}SiH \rightarrow Si_3{\equiv}Si\cdot + H$). Hence, for vacuum annealing, conventional furnace annealing, or RTA above 500 °C, Si–H dissociation will occur. Whether or not the P_b centers are measured following a given thermal process is determined by the cooling rate and the presence/absence of hydrogen/moisture in the ambient. If the cooling from the anneal temperature occurs in a hydrogen/moisture free environment (i.e., vacuum anneal, RTA), or if the cooling rate is sufficiently rapid to prevent the passivation ($Si_3{\equiv}Si\cdot + H_2 \rightarrow Si_3{\equiv}Si{-}H{+}H$) occurring (i.e., rapid pull from a conventional furnace anneal and RTA), then the P_b centers will be measured following the thermal process. Hence, the observation of P_b defects fol-

lowing an RTA in N_2 for a polysilicon gate MOS capacitor is entirely consistent with techniques previously used to examine P_b centers. In the case of a dry RTO, the absence of hydrogen from the processing environment leaves the P_b centers formed during the oxide growth process unpassivated following the RTO cycle. In the case of steam assisted RTO (see Fig. 12), the peak in the DOS distribution is not seen, due to the availability of hydrogen during the cooling process. A further point of relevance for the dry RTO samples is the difference in the peak DOS in the upper and lower energy gap for the 1000 °C and 1100 °C RTO samples. From the work of Stesmans,[27] an increasing oxidation temperature should result in a reduced P_b density over the temperature range 800–1150 °C. This trend is observed in this work, with a lower/upper peak in the D_{it} profiles of $6.9\times10^{12}\,cm^{-2}\,eV^{-1}/1.7\times10^{13}\,cm^{-2}\,eV^{-1}$ for a 1000 °C RTO, reducing to $3.6\times10^{12}\,cm^{-2}\,eV^{-1}/8\times10^{12}\,cm^{-2}\,eV^{-1}$ at 1100 °C.

For oxide layers grown by a conventional furnace oxidation (aluminum gate),[14] or for polysilicon gate MOS capacitors where the dopant activation is achieved by a conventional furnace anneal (see Fig. 1 and Ref. 3), the interface state peaks in the upper/lower regions of the energy gap are not measured. This observation has been used previously to discard the explanation that RTA dissociates hydrogen from pre-existing P_b centers. We suggest here that the P_b centers are not measured in this case, as for a conventional furnace anneal, the cooling rate is typically in the range 3–10 °C/min, with a subsequent slow pull from the furnace (typically 5–20 cm/min), at temperatures in the vicinity of 600 °C. This period, which could be hours in duration, allows hydrogen passivation from moisture in the ambient. Detailed calculations based on previous passivation studies[26,28] cannot be performed, as the wafers are not at a controlled temperature during the pull from the furnace.

V. SIGNIFICANCE

The results and analysis presented in this work are considered to be significant to a number of areas, such as: ''short-loop experiments,'' the study of P_b centers, and for RTO oxide growth optimization. These issues are covered below.

A. Short-loop experiments

The continuing development of silicon based CMOS technologies has resulted in the need for research and process development into a number of aspects relating to the MOS gate stack. Research is on-going into issues such as: polysilicon gate depletion,[29,30] boron penetration of thin gate oxide layers,[31,32] the use of a cluster tool approach for MOS gate stack formation,[2] and gate oxide optimization techniques. In such experiments, or more generally within process development, it is typical to have a reduced number of masking stages, with the processing proceeding to the first metal layer, or with direct contact made to the polysilicon gate layer. Such experiments are typically referred to as short-loop experiments. When this approach is used, the possibility exists that the MOS capacitor will be measured directly following RTA or RTO. In this case a peak response will be measured in the CV characteristic, with curves similar to those presented in Figs. 2, 3, 6, and 10. Furthermore, when low doping is present in the polysilicon layer (e.g., 5×10^{18} to $5\times10^{19}\,cm^{-3}$), or when hydrogen blocking layers such as Si_3N_4 are present,[33] the standard forming gas anneal (400–450 °C for 60 min in H_2+N_2) may not be sufficient to passivate the interface states exposed by the RTA process.[8] (In the case of reduced polysilicon doping levels, this occurs due to an interaction of the hydrogen with exposed defect states in the polysilicon gate layer.) In these cases, peaks occur in the CV characteristics, even after exposure to a forming gas anneal. The measurement of such CV characteristics has caused difficulty with the interpretation of the results. Furthermore, the peak response in the CV characteristic for short-loop wafers, will most probably be absent for fully processed wafers, as the additional processing (e.g., oxide deposition/plasma etching) provides exposure to hydrogen at elevated temperatures, resulting in P_b passivation.

The results in this work indicate that the interface states measured following RTA/RTO processes are the combined effect of the P_{b0}/P_{b1} centers at the Si(100)–SiO_2 interface. The P_b density is set by the precise oxidation conditions,[26] and the results in this article indicate that the RTA/RTO processes do not generate additional Si(100)–SiO_2 interface defects, when compared to conventional furnace oxidation cycles. In the case of metal gate contacts, or heavily doped polysilicon a standard forming gas alloy (i.e., 400 °C, 30 min in 10% H_2/90% N_2) will remove the peak in the CV. In the case of short-loop experiments with reduced doping in the polysilicon gate layer (with RTA dopant activation), the alloy temperature and time must be increased.[8]

B. Alternative method for the study of P_b centers

From a fundamental perspective, this work indicates that RTA in nitrogen or dry RTO provide an alternative and complimentary technique to vacuum annealing, or a rapid pull from a furnace oxidation, for the study of P_b centers at the Si–SiO_2 interface. The method of using RTP is essentially an extension of the procedures reported in Refs. 19, 20, where wafers are rapidly pulled out following a conventional furnace oxidation. The use of RTP has the advantage of a controllable cooling rate and a controlled ambient during the cooling phase. Furthermore, this work demonstrates that RTA can provide a relatively simple technique for examining P_b defects on the technologically relevant polysilicon gate structure. By extension, the RTA technique should also provides a means by which P_b centers could be measured on full MOSFET structures. In the case of oxide layers grown by dry RTO, and measured using a mercury probe technique, the P_b centers can be examined prior to any hydrogen passivation.

C. Optimization of oxide growth by RTO

The ideal approach for optimizing oxide reliability, from an interface state density perspective, is to intrinsically reduce interface defects during the oxide growth process. However, in the case of MOS based processing, the usual

route to interface state reduction is through intentional (forming gas annealing) and unintentional (e.g., polysilicon deposition, plasma oxide deposition, plasma etching) incorporation of hydrogen, at the $Si-SiO_2$ interface, forming P_b-H bonds. However, this approach is not ideal as breaking of P_b-H bond due to high energy electrons/holes results in a gradual degradation of MOS device behavior. Making a quantitative comparison of interface state/P_b densities for varying growth conditions is not usually possible, as following a slow cooling rate from a conventional furnace oxidation, or after forming gas annealing, the majority of interface states/P_b centers are passivated.

The results in this work demonstrate that by using a mercury probe CV system, the properties of the $Si-SiO_2$ interface can be examined directly following dry rapid thermal oxidation, prior to any hydrogen passivation. This opens up a relatively simple route for the intrinsic reduction of interface states (P_b centers) resulting from the oxide growth process. This can be seen in Table I, where the difference in the peak densities in the upper/lower energy gap clearly reduce as the RTO temperature increases. As a consequence, this experimental technique provides a method of optimizing the RTO conditions for the *intrinsic* elimination of oxidation induced interface states, as opposed to hydrogen passivation, which has associated reliability implications. Preliminary results, not shown here, also show that the technique can be used to examine the role of nitrogen at the interface.

D. Device implications

In addition, the results are of relevance to MOS technology. The results show that a high density ($>1\times10^{12}\,cm^{-2}$) of P_b centers are *exposed* at the $Si-SiO_2$ interface following an RTA ($T\geqslant800\,°C$) process. For desired device operation, it is required that the back-end processing, and associated thermal budget, are sufficient to re-passivate the exposed interface states. In the majority of cases, an incorporation of hydrogen does occur in processing stages such as oxide deposition and plasma etching.[15] However, cases can be envisaged where the defects may not be completely passivated after full processing, resulting in shifts in device parameters. The presence of barrier layers to hydrogen diffusion, such as silicon nitride, could block the passivation of the interface states after the RTA step. Variations could also occur in device (e.g., MOS/MOSFET/EEPROM) characteristics as a function of device area. If the passivation occurs by diffusion of hydrogen from the periphery of the structure (e.g., as in the case of Si_3N_4 layers), then small area devices may operate as expected, with anomalies occurring for larger area structures.

VI. CONCLUSIONS

In conclusion, results have been presented which demonstrate the impact of rapid thermal processing (600–1050 °C) on the properties of the $Si(100)-SiO_2$ interface. Analysis of the quasi-static CV measurements, directly following RTA/dry RTO processing, indicates a high density of interface states across the energy gap. When the background U-shaped density of states for a hydrogen passivated interface is subtracted, two distinct peaks in interface state density profile are observed at approximately 0.25–0.33 eV and 0.85–0.88 eV above the valence band edge. The peak densities are in the range $3\times10^{12}\,cm^{-2}\,eV^{-1}-7\times10^{12}\,cm^{-2}\,eV^{-1}$ for the lower energy gap level, with values in the range $6.5\times10^{12}\,cm^{-2}\,eV^{-1}-1.7\times10^{13}\,cm^{-2}\,eV^{-1}$ for the upper energy gap level. The density measured is dependent primarily on the oxidation and RTA temperatures. As a result of the smaller density of states between E_v and E_i, a clear peak is only seen in the DOS profile in the lower energy gap when the background distribution for a hydrogen passivated interface is subtracted. The upper energy gap peak has a sufficiently high density to be detected as a clear peak prior to subtraction of the background DOS and as a consequence results in a peak response in the measured CV characteristic.

Analysis of samples with different processing conditions and different oxide thicknesses exhibit the same general features in the density of states across the energy gap. These results point to a common interface state defect present after processes involving rapid cooling ($10^1-10^2\,°C/s$) from a temperature of $\geqslant800\,°C$ in a hydrogen/moisture free ambient. By consideration of the results in relation to studies on vacuum annealed samples, we argue that the interface states measured following RTA/dry RTO processes can be reliabably identified as the net contribution of the P_{b0}/P_{b1} silicon dangling bond defects for the oxidized Si(100) orientation. It is important to emphasize that the results in this work indicate that the primary effect of RTA is to cause hydrogen desorption from pre-existing P_{b0}/P_{b1} silicon dangling bond defects, and that the RTA process does not create additional interface defects when compared to conventional furnace annealing. The rapid cooling from the anneal temperature, in a hydrogen free environment, preventing passivation of the P_b centers. In the case of dry RTO samples measured directly following the oxidation step, the dangling bond centers formed during the oxidation process are measured prior to any hydrogen passivation. The results presented in this article provide a framework to understand a wide range of apparently contradictory results that have been obtained in experiments where MOS gate stack structures have been measured following RTA or RTO processes. Finally, the relevance of this work to the study of the $Si-SiO_2$ interface, and to silicon based MOS technology development have been briefly discussed.

Note added in Proof. A number of publications have recently appeared relating to the electrical activity of P_{b0} and P_{b1} centers at the $Si(100)-SiO_2$ interface, which are of significance to the results in this article. Stesmans and Afanas'ev recent work indicates that post-oxidation vacuum annealing (600–1100 °C) can generate additional P_{b1} centers, while the P_{b0} density remains essentially constant, or even slightly reduces.[34] This electron spin resonance study primarily concerned oxidized (100) orientation silicon. In addition, it has been proposed that the P_{b1} center does not have energy levels in the silicon band gap,[35] and is therefore electrically inactive, although this is still an area of debate.[36] If P_{b1} is electrically active, it is possible that the RTA (10–20

s in N_2) could generate new electrically active P_{b1} centers, as well as dissociating hydrogen from pre-existing P_{b1} sites. However, it is important to note that these centers would also be created in conventional furnace annealing in an N_2 ambient. If P_{b1} is electrically inactive, then the assertion holds that RTA in N_2 (600–1050 °C) does not generate additional electrically active interface states. Regardless of the electrical activity of the P_{b1} defect, the results in this work indicate that the RTA process does not generate any more additional interface states than a conventional furnace anneal step.

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