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Electrical and physical characterization of the Al_2O_3/p-GaSb interface for 1%, 5%, 10%, and 22% $(NH_4)_2S$ surface treatments

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Electrical and physical characterization of the Al_2O_3/*p*-GaSb interface for 1%, 5%, 10%, and 22% $(NH_4)_2S$ surface treatments

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In this work, the impact of ammonium sulfide ($(NH_4)_2S$) surface treatment on the electrical passivation of the Al_2O_3/*p*-GaSb interface is studied for varying sulfide concentrations. Prior to atomic layer deposition of Al_2O_3, GaSb surfaces were treated in 1%, 5%, 10%, and 22% $(NH_4)_2S$ solutions for 10 min at 295 K. The smallest stretch-out and flatband voltage shifts coupled with the largest capacitance swing, as indicated by capacitance-voltage (*CV*) measurements, were obtained for the 1% treatment. The resulting interface defect trap density (D_{it}) distribution showed a minimum value of $4 \times 10^{12}\,cm^{-2}eV^{-1}$ at $E_v + 0.27$ eV. Transmission electron microscopy and atomic force microscopy examination revealed the formation of interfacial layers and increased roughness at the Al_2O_3/*p*-GaSb interface of samples treated with 10% and 22% $(NH_4)_2S$. In combination, these effects degrade the interface quality as reflected in the *CV* characteristics. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4899123]

While III-Vs are considered strong candidates for the *n*-channel transistor in future complementary-metal-oxide-semiconductor (CMOS) technologies, the *p*-channel device may be Ge-based.[1] However, the challenges facing the cointegration of III-V and IV materials[1] provide a strong argument for an all III-V CMOS technology. Antimonides, with 2–3× higher hole mobility compared to Si,[2] offer a potential *p*-channel solution. GaSb in particular appears suited; in addition to a hole mobility of 1000 cm^2/V.s, highest among III-Vs, it is easy to achieve strong hole inversion in GaSb.[3] Nevertheless, a low-defect, high-quality dielectric/semiconductor interface remains the most notable impediment to a III-V logic solution. This is of even greater concern to GaSb given its higher inherent susceptibility to ambient air exposure.[4] In turn, GaSb surfaces are terminated with thick native oxides that are neither stable, self-limiting nor abrupt.[5,6] The resulting defect-dominated interface impairs Fermi Level movement, thereby limiting the channel charge modulation capability of metal-oxide-semiconductor field-effect-transistors (MOSFETs).[7] Together with atomic layer deposition (ALD), both wet[3,5,8–14] and dry[7] chemical treatments have been explored on GaSb to overcome these detriments. Of these, HCl and hydrogen plasma treatments have been most effective in alleviating surface oxides, thereby improving the electrical properties of the high-*k*/GaSb interface.[5,7,14] However, ammonium sulfide ($(NH_4)_2S$), a wet treatment shown to engineer a high-quality high-*k*/InGaAs interface,[15,16] has received little attention on GaSb. One study[12] reported the elimination of Sb oxides following 2% sulfide treatment. The x-ray photoemission spectroscopy (XPS) analysis further revealed the Ga oxide content to be lower for $(NH_4)_2S$ compared to NH_4OH or HCl treatments. This, together with the absence of Sb oxides, led to a larger capacitance swing in the capacitance-voltage (*CV*) response of the sulfide treated sample. The removal of Sb oxides and the retention of Ga oxides were also noted for 22% $(NH_4)_2S$ treatments.[11] However, the effects of the treatment were not electrically assessed in the study. Other electrical investigations have been limited to combined treatments of $(NH_4)_2S$ and HCl.[8,10] Currently, a systematic examination of the impact of $(NH_4)_2S$ on the high-*k*/GaSb interface for sulfide concentrations in the range 1%–22%, similar to that reported for InGaAs,[15] is lacking. In this letter, we report on the investigation of $(NH_4)_2S$ as a standalone surface treatment for Al_2O_3/*p*-GaSb metal-oxide-semiconductor (MOS) system. The effects of the treatment for varying sulfide concentrations are assessed from frequency dependent *CV* measurements. We also correlate the electrical behavior with surface and structural modifications to GaSb resulting from the treatments.

Epitaxial layers were grown by molecular beam epitaxy (MBE) on a *p*-type (Zn: $0.8 - 1.4 \times 10^{19}\,cm^{-3}$) GaAs(100) substrate. Samples comprised, in the order of the *p*-type layers grown, a 1 μm AlSb (Be: $\sim 5 \times 10^{18}\,cm^{-3}$) buffer, a 150 nm GaSb (Be: $\sim 5 \times 10^{18}\,cm^{-3}$) buffer, and a 500 nm GaSb (Be: $\sim 4 \times 10^{17}\,cm^{-3}$) channel. Following a 1 min degrease in acetone, methanol, and isopropanol, samples were immersed in $(NH_4)_2S$ solutions for 10 min at room temperature (~295 K). $(NH_4)_2S$ concentrations of 1%, 5%, 10%, and 22% in deionized H_2O were used. Samples were introduced into the ALD reactor within ~4 min after removal from the sulfide solution. A 8 nm-thick (nominal) Al_2O_3 film was deposited by ALD using alternating pulses of trimethylaluminum (TMA) and H_2O at 300 °C, in a TMA-first sequence. Gate contacts were defined by e-beam evaporation of Ni (60 nm) and Au (80 nm) through a shadowmask. Electrical measurements were performed on-wafer in a dark, electrically-shielded environment.

Shown in Fig. 1 are the room temperature multi-frequency (1 kHz to 1 MHz) *CV* characteristics of samples without any treatment (control) and with 1%, 5%, 10%, and

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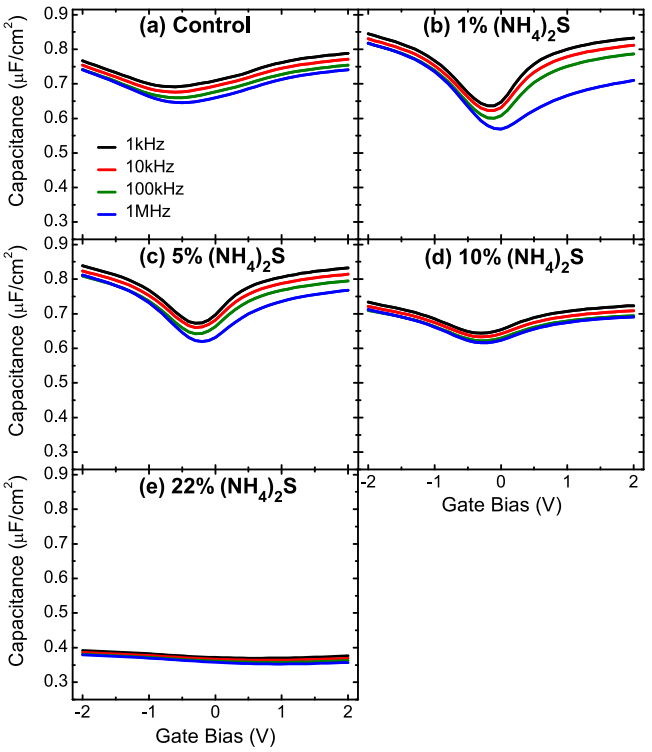

FIG. 1. Multi-frequency (1 kHz to 1 MHz) *CV* characteristics (~295 K) of Au/Ni/Al_2O_3/*p*-GaSb MOS capacitors with (a) no treatment (control) along with (b) 1%, (c) 5%, (d) 10%, and (e) 22% $(NH_4)_2S$ treatments.

22% $(NH_4)_2S$ treatments. All of the samples exhibit modulation of the capacitance with applied gate bias (V_g), with the level of capacitance modulation being dependent on the concentration of the $(NH_4)_2S$ treatment prior to the Al_2O_3 ALD process. The treatment comprising 1% $(NH_4)_2S$ clearly improves the *CV* response, indicative of a reduced interface defect trap density (D_{it}). However, a further increase in the sulfide concentration leads to a degradation of the *CV* response. In the case of the 22% treated sample, the capacitance modulation with gate bias is significantly reduced, which suggests that the Fermi Level is pinned at the Al_2O_3/GaSb interface from a large D_{it} response.

Stretch-out, flatband voltage (V_{fb}) shift, and frequency dispersion in accumulation for all samples are compared in Table I with definitions used in extracting these metrics indicated. With the exception of the 22% treatment, stretch-out and V_{fb} shift of the other treatments are reduced from that of the control sample. The smallest stretch-out and V_{fb} shift are obtained for the 1% treatment, highlighting its effectiveness in reducing the interface trap density from the valence band to midgap. While both metrics degrade with increasing

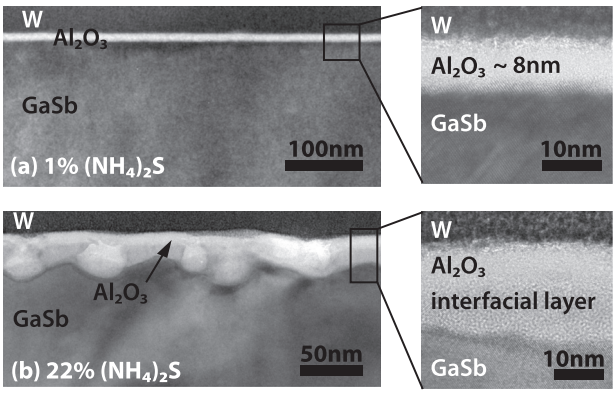

FIG. 2. Cross-sectional TEM micrographs of (a) 1% and (b) 22% $(NH_4)_2S$ treated W/Al_2O_3/*p*-GaSb samples.

$(NH_4)_2S$ concentration, there is no discernible difference for frequency dispersion in accumulation between the samples with the exception of the control and 22% treated samples for which an accumulation response is not visible. The fact that the 1%, 5%, and 10% treated samples show an accumulation response is evidence of the positive impact of the $(NH_4)_2S$ treatment at these concentrations. The small dispersion values of ~1%/dec is one indicator of lower D_{it} towards the valence band.[5]

An obvious inconsistency observed from Fig. 1 is differing maximum accumulation capacitance (C_{max}) between the samples. While C_{max} values are similar for treatments of 1% (0.845 μF/cm^2) and 5% (0.839 μF/cm^2) at $V_g = -2$ V, the 10% treated sample exhibits a capacitance that is ~13% lower in comparison. A drastic reduction in C_{max} by ~50% is observed for the 22% treated sample. To investigate this difference, selected samples were examined by cross-sectional transmission electron microscopy (TEM). Shown in Fig. 2 are the TEM micrographs of W/Al_2O_3/*p*-GaSb structures with 1% and 22% $(NH_4)_2S$ treatments (W is the capping layer used in the TEM sample preparation). A uniform Al_2O_3 film with gate dielectric thickness of 8 ± 0.2 nm, close to the nominal value, is observed for the 1% treatment (Fig. 2(a)). A clear transition from the crystalline GaSb to the amorphous Al_2O_3, with no distinct interfacial layer (IL), is further evident. In marked contrast, the 22% treated sample presents with a very distinct amorphous IL (Fig. 2(b)). This IL, likely composed of Ga and S,[18] results from the enhanced reaction between GaSb and $(NH_4)_2S$ of higher concentration. Antimony-rich voids[18] ranging from 15–25 nm in diameter also appeared to form at non-specific regions along the IL. This IL accounts for the reduction in C_{max} of the 22% treated sample according to

TABLE I. Comparison of stretch-out, flatband voltage shift, and frequency dispersion in accumulation between Au/Ni/Al_2O_3/*p*-GaSb MOS capacitors without any treatment (control) and with 1%, 5%, 10%, and 22% $(NH_4)_2S$ treatments. The method of Hillard *et al.*[17] is used in the extraction of V_{fb}.

	Stretch-out ($\times 10^{-7}$ F/cm^2.V) $\frac{\Delta C_{1\,MHz}}{\Delta V}$ @ (V_{fb} to $V_{fb}+0.3$)	Flatband voltage shift (mV) ($V_{1\,MHz} - V_{1\,kHz}$) @ V_{fb}	Frequency dispersion in accumulation (%/dec) $\left(\frac{C_{1\,kHz}-C_{1\,MHz}}{C_{1\,kHz}} \times \frac{100\%}{N_{dec}}\right)$ @ $V_g = -2$ V
Control	−0.81	402.18	Accumulation response not observed
1% $(NH_4)_2S$	−2.28	171.84	1.12
5% $(NH_4)_2S$	−1.85	230.01	1.10
10% $(NH_4)_2S$	−0.83	314.60	1.01
22% $(NH_4)_2S$	−0.13	1239.38	Accumulation response not observed

TABLE II. Root-mean-square (RMS) roughness from AFM measurements of samples with various $(NH_4)_2S$ treatments.

Sample number	Concentration (% $(NH_4)_2S$ in H_2O)	Immersion time (min)	RMS roughness (nm)
(i)	1	1	1.41
(ii)	1	5	1.39
(iii)	1	10	1.37
(iv)	5	1	1.41
(v)	5	5	1.40
(vi)	5	10	1.45
(vii)	10	1	1.83
(viii)	10	5	2.13
(ix)	10	10	2.58
(x)	22	1	2.62
(xi)	22	5	3.00
(xii)	22	10	3.25

$$C_{tot} = (C_{ox}^{-1} + C_{il}^{-1} + (C_s + C_{it})^{-1})^{-1}, \quad (1)$$

where C_{ox} is the gate dielectric capacitance, C_{il} is the interfacial layer capacitance, C_s is the semiconductor capacitance, and C_{it} is the interface trap capacitance. An IL would also explain the drop in C_{max} of the 10% treated sample, although the capacitance is higher than that of the 22% treated sample. This implies that IL is thinner for the 10% compared to the 22% treatment. Therefore, IL thickness appears to be dependent on the concentration of the treatment, with thicker layers resulting from higher sulfide concentrations. Atomic force microscopy (AFM) was used to analyze the surface roughness of the grown epi following only sulfide treatment. In Table II, root-mean-square (RMS) roughness measurements for a variety of treatments, based on AFM scans taken over $5\,\mu m \times 5\,\mu m$ areas, are illustrated. A wider parameter space comprising variations in sulfide concentration and sample immersion times is investigated. For the 1% and 5% treatments, there is no appreciable difference in roughness for all immersion times. In contrast, roughness of the 10% and 22% treatments monotonically increase with longer immersion times. A surface roughness of 3.25 nm is noted for the 10 min treatment in 22% $(NH_4)_2S$. This reflects the pronounced chemical activity resulting from higher $(NH_4)_2S$ concentrations. Interfacial layers and increased surface roughness at the higher sulfide concentrations would compromise gate control in MOSFETs.

It is notable the 1%, 5%, and 10% treated samples along with the control sample show low-frequency-like *CV* behavior for all measured signal frequencies (Fig. 1). The ability of minority carriers to follow the ac signal (low-frequency behavior) even for a frequency of 1 MHz is observed in narrow bandgap (E_g), high intrinsic carrier density (n_i) semiconductors for which minority carrier response times are very short,[19] e.g., InSb, with a bandgap of 0.17 eV.[2] This is not expected of GaSb, given its E_g of 0.726 eV and n_i of $1.5 \times 10^{12}\,cm^{-3}$,[2] which is four orders of magnitude smaller compared to InSb. Testament to this, high-frequency *CV* behaviors devoid of minority carrier response have been demonstrated at 1 MHz on high-*k*/*p*-GaSb MOS capacitors.[5,7] A high D_{it} in the upper half of E_g is the likely cause of the false inversion response at 1 MHz. To verify this, the 1 MHz response of the 1% treated sample was measured at temperatures between −40 °C and 20 °C, the results of which are plotted in Fig. 3. The capacitance dispersion observed in the gate bias range of +0.5 V to +2 V is characteristic of interface traps.[20] The reduction in capacitance with temperature is related to the exponential dependence of trap emission time constant[21] on the reciprocal of temperature (T). As the sample temperature is lowered, the interface trap response becomes suppressed. As a result of the reduced contribution from C_{it}, the capacitance in inversion drops and the *CV* response approximates towards a high-frequency behavior at lower temperatures. While high-frequency *CV* responses are observed for $T < -10$ °C, the theoretical minimum capacitance (C_{min}) of 0.2 $\mu F/cm^2$ in inversion is still not obtained at −40 °C. This suggests that the trap response is not completely frozen out and manifests as a capacitive contribution, albeit much reduced. These results are evidence of a large D_{it} response in the upper half of E_g. The 1% treated sample though shows a smaller trap response in the bias range of 0 V to +2 V compared to the other samples. This is inferred from the larger capacitance swing of the 1 MHz response at room temperature (Fig. 1), which further underscores the effectiveness of the 1% treatment for surface passivation. In addition, the small capacitance dispersion of ∼3.9% at $V_g = -1.5$ V implies that the observed accumulation behavior is highly likely a result of free carriers as opposed to trap induced response.[20] A V_{fb} shift of 128 mV is also noted. The minimal vertical and horizontal shifts of the *CV* curves with temperature, in accumulation and at flatband, respectively, are indicative of lower D_{it} below midgap.

To quantify the trap distribution of the 1% treated sample, the high-low frequency *CV* method[21] is employed. The trap density is derived from the formula

$$D_{it}(V_g) = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right), \quad (2)$$

where C_{lf} is the low-frequency capacitance, C_{hf} is the high-frequency capacitance and q is the electron charge. The 1 kHz *CV* data at room temperature was taken as C_{lf}. In contrast, C_{hf} was based on the 1 MHz *CV* data obtained at −40 °C to minimize the interface trap response, thereby

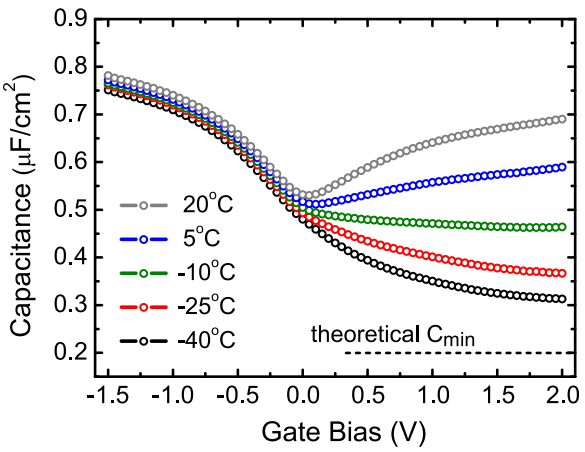

FIG. 3. 1 MHz *CV* response as a function of temperature (−40 °C to 20 °C) for Au/Ni/Al_2O_3/*p*-GaSb MOS capacitor treated with 1% $(NH_4)_2S$.

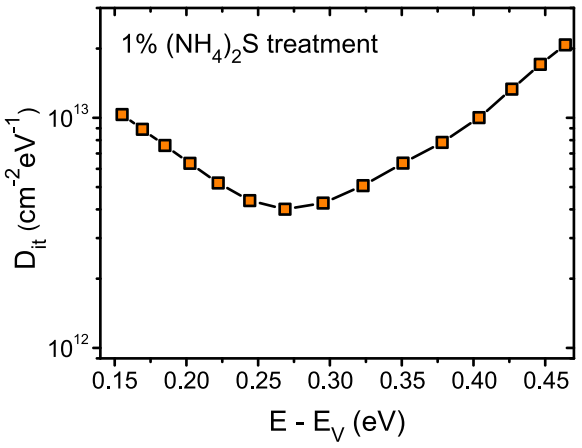

FIG. 4. D_{it} distribution from weak inversion towards the majority carrier band edge of 1% $(NH_4)_2S$ treated sample extracted based on the temperature modified high-low frequency *CV* method.

providing for a more accurate D_{it} determination.[15] Surface potential (ψ_s) as function of gate bias was obtained from the Berglund integral.[22] The $D_{it} - \psi_s$ profile was then extracted over a limited range of the bandgap (from 0.15 eV to 0.46 eV), since the method is only valid from weak inversion towards the majority carrier band edge.[21] The resulting D_{it} distribution is summarized in Fig. 4. A U-shaped distribution is observed with minimum D_{it} of $4 \times 10^{12}\,cm^{-2}eV^{-1}$ at $E_v + 0.27$ eV. Such a D_{it} profile close to midgap offers the possibility of lower subthreshold swings of benefit to off-state MOSFET operation.[3]

In summary, the effectiveness of $(NH_4)_2S$ surface treatments at concentrations of 1%, 5%, 10%, and 22% were assessed for improving the electrical properties of the Al_2O_3/*p*-GaSb interface. Based on *CV* measurements, the 1% treated sample exhibited the largest capacitance swing together with the smallest stretch-out and flatband voltage shift. Alternatively, the 22% treatment resulted in a pinned Fermi level at the interface. Low-frequency *CV* behavior of the samples at all signal frequencies was indicative of a large D_{it} response in the upper half of E_g. Analysis based on TEM and AFM revealed the formation of IL and increased roughness at the high-*k*/*p*-GaSb interface for the 10% and 22% sulfide treatments. The combination of these effects led to the degradation of the electrical properties reflected in the *CV* responses. The extracted D_{it} of the 1% treated sample shows a U-shaped profile with a minimum of $4 \times 10^{12}\,cm^{-2}eV^{-1}$ at $E_v + 0.27$ eV. While the 1% treatment is shown to be most effective in this study, this may not necessarily be the optimum treatment for Al_2O_3/GaSb interface passivation. Sulfide treatments at concentrations between 0% and 5% require further investigation.

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[1]J. del Alamo, Nature **479**, 317 (2011).
[2]Ioffe Institute, Physical Properties of Semiconductors Electronic Archive, http://www.ioffe.ru/SVA/NSM/Semicond/index.html.
[3]M. Xu, R. Wang, and P. D. Ye, IEEE Electron Device Lett. **32**, 883 (2011).
[4]A. Rosenberg, J. Phys. Chem. Solids **14**, 175 (1960).
[5]A. Nainani, Y. Sun, T. Irisawa, Z. Yuan, M. Kobayashi, P. Pianetta, B. R. Bennett, J. B. Boos, and K. C. Saraswat, J. Appl. Phys. **109**, 114908 (2011).
[6]Z. Y. Liu, B. Hawkins, and T. F. Kuech, J. Vac. Sci. Technol. B **21**, 71 (2003).
[7]L. B. Ruppalt, E. R. Cleveland, J. G. Champlain, S. M. Prokes, J. B. Boos, D. Park, and B. R. Bennett, Appl. Phys. Lett. **101**, 231601 (2012).
[8]A. Ali, H. Madan, A. P. Kirk, R. Wallace, D. Zhao, D. Mourey, M. Hudait, T. Jackson, B. Bennett, J. Boos, and S. Datta, in *Device Research Conference (DRC)* (IEEE, 2010), pp. 27–30.
[9]A. Ali, H. S. Madan, A. P. Kirk, D. A. Zhao, D. A. Mourey, M. K. Hudait, R. M. Wallace, T. N. Jackson, B. R. Bennett, J. B. Boos, and S. Datta, Appl. Phys. Lett. **97**, 143502 (2010).
[10]Z. Tan, L. Zhao, J. Wang, and J. Xu, ECS Solid State Lett. **2**, P61 (2013).
[11]S. McDonnell, D. M. Zhernokletov, A. P. Kirk, J. Kim, and R. M. Wallace, Appl. Surf. Sci. **257**, 8747 (2011).
[12]I. Geppert, M. Eizenberg, A. Ali, and S. Datta, Appl. Phys. Lett. **97**, 162109 (2010).
[13]A. Nainani, T. Irisawa, Z. Yuan, Y. Sun, T. Krishnamohan, M. Reason, B. R. Bennett, J. B. Boos, M. G. Ancona, Y. Nishi, and K. C. Saraswat, in *2010 IEEE Int. Electron Devices Meeting* (IEDM) (IEEE, 2010), pp. 6.4.1–6.4.4.
[14]K. Suzuki, Y. Harada, F. Maeda, K. Onomitsu, T. Yamaguchi, and K. Muraki, Appl. Phys. Express **4**, 125702 (2011).
[15]E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, J. Appl. Phys. **109**, 024101 (2011).
[16]B. Brennan, M. Milojevic, C. Hinkle, F. Aguirre-Tostado, G. Hughes, and R. Wallace, Appl. Surf. Sci. **257**, 4082 (2011).
[17]R. Hillard, J. Heddleson, D. Zier, P. Rai-Choudhury, and D. Schroder, *Diagnostic Techniques for Semiconductor Materials and Devices* (Pennington, NJ, 1992), pp. 261–274.
[18]J. A. Robinson and S. E. Mohney, J. Appl. Phys. **96**, 2684 (2004).
[19]H. Trinh, Y. Lin, E. Chang, C.-T. Lee, S.-Y. Wang, H. Nguyen, Y. Chiu, Q. Luc, H.-C. Chang, C.-H. Lin, S. Jang, and C. Diaz, IEEE Trans. Electron Devices **60**, 1555 (2013).
[20]E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanaśev, and P. K. Hurley, Appl. Phys. Lett. **94**, 102902 (2009).
[21]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New Jersey, 2002), pp. 331–332; 351–353.
[22]C. N. Berglund, IEEE Trans. Electron Devices **ED-13**, 701 (1966).