Sodium silicate as an enabler for wafer bonding of glass substrates and lids

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Abstract— The outgassing challenge associated with using polymer-based die-attach adhesives for vacuum seal photonic packages is addressed in this extended abstract. In addition to this, die movement can occur after high temperature anodic bonding of the lid/cap wafer and substrate wafer due to low glass transition temperature of polymer based adhesive systems. This presents a challenge for photonic packages where photonic chip's positional accuracy is critical. Silicate based adhesives are presented as a solution to enable vacuum seal packaging of photonic chips.

Keywords— Sodium silicate; lid wafer; wafer bonding; curing; photonic package

I. Introduction

The packaging of photonic components using glass substrates has gained momentum in recent times [1,2]. Glass substrates offer many advantages for photonic packaging such as optical waveguide routing, low-loss electrical transmission, thermal isolation and mechanical stability [3]. The integration of photonic chips, electronic chips and optical components on glass substrates can be done on a wafer scale. To facilitate the process, encapsulation or capping of these packages becomes a cost-sensitive factor during the assembly [4]. In this paper, the authors are discussing the use of sodium silicate bonding for chip/micro-optical components attachment in glass substrate cavities, which can withstand the wafer-to-wafer bonding mechanisms to support the package capping/integration functions.

The necessity of hermetic sealing/capping for high-performance optical detection systems such as infrared detectors leads us to consider wafer-level vacuum assemblies. These wafer-level assemblies can be carried out through various direct and indirect wafer-bonding approaches [5]. The processing and operating temperatures of these wafer-bonding schemes play an integral role in the selection of adhesive/solder materials required to assemble the chips and micro-optical components in glass-based wafer-scale photonic packages. In this case, we highlight the use of sodium silicate bonding of chips in wafer cavities to assist anodic wafer-to-wafer bonding.

II. Experiment and Results

The authors propose the use of sodium silicate bonding to enable the wafer-level anodic bonding of the cap glass wafer and the substrate glass wafer. In this study, the 100mm diameter borofloat 33 Pyrex wafers of thickness 1mm and 0.5mm are used. The 1mm thick borofloat substrate wafer is coated with 0.2µm polysilicon on both sides. This wafer is then isotropically wet-etched using concentrated HF with an etch rate of 7µm/min to create 5.1mm×5.1mm×0.8mm square cavities in the wafer. This is followed by the removal of the polysilicon mask and embedding of the 5mm×5mm×0.5mm silicon chips in these square substrate cavities with sodium silicate bonding. The 0.5mm thick borofloat cap wafer is covered with 0.2µm polysilicon which is etched at the cavities position corresponding to the substrate wafer. The substrate wafer and the cap wafer are then aligned using the semi-flat and anodically-bonded using the EVG 501 wafer bonder. This anodic bonding is carried out at 600V, 400ºC and an applied pressure of 500N. The main focus of using sodium silicate bonding for the chips inside the substrate cavity is the ability of the oxide bond to withstand the high pressure and temperature during the anodic bonding process. The application of sodium silicate (Merck 105621) in the glass cavity is done by first changing the viscosity of the sodium silicate solution, which is heated to 75ºC for 1 minute to increase its' viscosity. Once the solution becomes more viscous, it is easier to handle and deposit in the substrate cavity. A Finetech flip-chip bonder is used for uniformly placing the chips inside the cavity and the subassembly is then placed on the hot plate at 100ºC for 2 hours with a placement accuracy of ±3µm across the chip. The placement accuracy needed for the pick and place of micro-optical components can be even more constrained depending on the mode size of the coupled elements. This helps with the removal of the remaining moisture out of the bonding zone and the wafer is put upside down to check the bonding of the chips in the substrate cavity. This substrate wafer is then capped with the cap glass wafer using anodic bonding as mentioned before. The process flow and the embedded chips in wafer cavity with and without cap wafer are shown in Fig.1 and Fig.2 respectively.

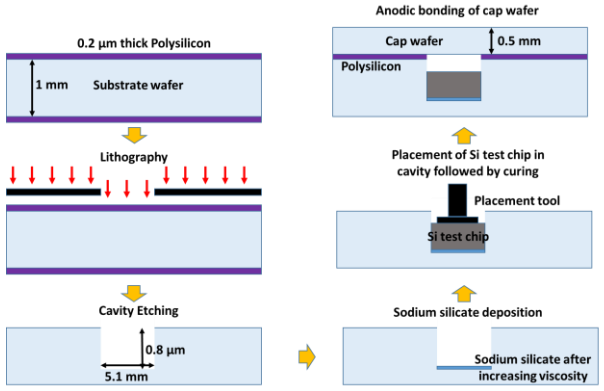

Fig. 1. Fabrication and bonding process flow for embedding chips in glass substrate wafer cavity followed by bonding the cap glass wafer.

The shear strength of a 25mm2 silicon test chip attached to a glass substrate using sodium silicate bonding is measured to be 5 kg thus qualifying the MIL-STD-883E standard. This concept holds importance as it can potentially be used for building out a photonic assembly with micro-optical components, where the micro-optical assembly process need not be dependent on the solder reflow hierarchy. As most epoxies and solders have reliability challenges at higher operating temperatures (>250ºC-300ºC) [6], we need the assembly to be compatible with the thermal variations experienced by the package. This method can be taken further to facilitate optical coupling between photonic chips on glass substrates and waveguides in glass lids as seen in Fig.3.

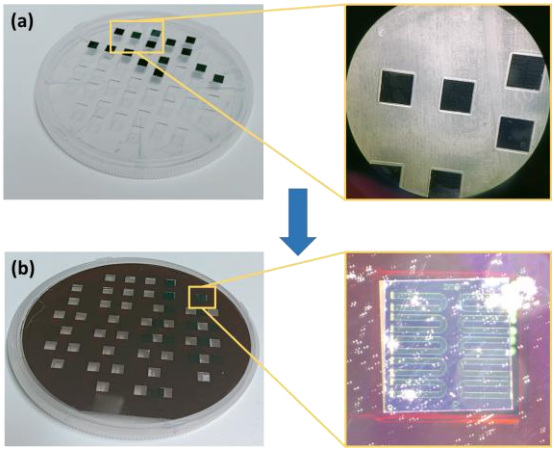

Fig. 2. (a) Embedded test chips in a cavity etched 1mm thick glass substrate wafer, cavities using sodium silicate bonding followed by (b) anodic bonded glass cap wafer on top of the chip embedded substrate wafer with 200 nm polysilicon film in the middle of the wafers.

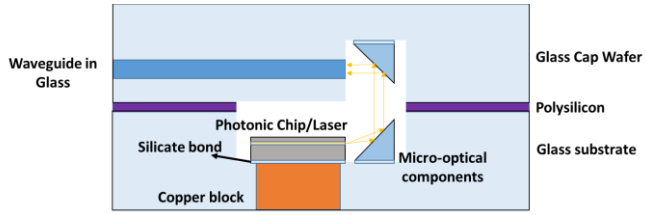

Fig. 3. A glass-based photonic package using sodium silicate enabled wafer-to-wafer bonding mechanism suitable for high operating temperatures.

The epoxy/solder/die attach film attachment of the chips and micro-optical components to the substrate can be substituted with sodium silicate bonding, which has more thermal stability that can withstand temperature variations due to its high glass transition temperature (≈450ºC) [7, 8]. This then enables the hermetic anodic bonding of the substrate wafer and the cap wafer. The focus points to further facilitate the silicate bonding would be to maintain positional accuracy and bondline thickness of the bonded chips/components with viscosity tuning of the silicate solution, silicate solution dispension methods, moisture absorption of the silicate bond and avoiding voids/bubbles in the cured silicate bond.

III. Discussion

As anodic bonding can induce mechanical deformation of the bonded wafer [5], the silicate bonding of components can also be taken further to enable other wafer bonding schemes such as 3D bonding of glass wafers through solder reflow, hybrid plasma bonding etc. This is because the silicate bond can withstand the temperatures required for the reflow of the solder microbumps, Cu-Cu hybrid bonding and annealing. The cap wafer and glass substrate can be aligned through active or passive mechanisms depending on the alignment accuracy required across multiple devices on the wafer while testing. This approach also allows micromachining of the assembly for placing heat spreaders such as copper blocks or micro-thermoelectric coolers underneath ensuring thermal management of the photonic device. However, the precise wafer-to-wafer alignment can be a factor leading to increased process complexity and cost. The pros and cons of using the sodium silicate bonding method are listed in Table I below.

TABLE I. PROS AND CONS OF SODIUM SILICATE ADHESIVE

	PROS	CONS
Thermal Properties	Can withstand processing temperatures up to 400°C [8]	Needs fillers for increasing thermal conductivity [MB600S Master Bond Polymer System]
Electrical properties	High volume resistivity [MB600 Master Bond Polymer System]	Can be used for electromagnetic shielding with the addition of fillers [MB600S Master Bond Polymer System]
Mechanical Properties	Ability to fill high aspect ratio gaps due to low viscosity prior to curing [9]	Good dimensional stability with mechanical pressing [10], need fillers for CTE tuning [9]
Microfabrication Compatibility	Can be spin coated or spray coated [9, 10]	High sodium content [9]
Curing Conditions	Volume can be controlled through syringes	High cure time [MB600 Master Bond Polymer System]

Thus, choosing the appropriate wafer bonding mechanism based on the alignment tolerance required by a particular application will play a huge role in the selection of the silicate bonding process. Also, looking at the pros and cons of the silicate bonding procedure, fillers will be needed to build out a composite to cater to the electrical and thermal demands of advanced photonic packages which requires further investigation. The CMOS incompatibility of sodium silicate also pushes further investigation into other silicate materials suitable for wafer-scale glass based packages [11].

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