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TiN/ZrO_2/Ti/Al Metal–Insulator–Metal Capacitors With Subnanometer CET Using ALD-Deposited ZrO_2 for DRAM Applications

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***Abstract*—We provide the first report of the structural and electrical properties of TiN/ZrO_2/Ti/Al metal–insulator–metal capacitor structures, where the ZrO_2 thin film (7–8 nm) is deposited by ALD using the new zirconium precursor ZrD-04, also known as Bis(methylcyclopentadienyl) methoxymethyl. Measured capacitance–voltage (C–V) and current–voltage (I–V) characteristics are reported for premetallization rapid thermal annealing (RTP) in N_2 for 60 s at 400 °C, 500 °C, or 600 °C. For the RTP at 400 °C, we find very low leakage current densities on the order of nanoamperes per square centimeter at a gate voltage of 1 V and low capacitance equivalent thickness values of ∼0.9 nm at a gate voltage of 0 V. The dielectric constant of ZrO_2 is 31 ± 2 after RTP treatment at 400 °C.**

***Index Terms*—ALD, capacitor, dynamic random access memory (DRAM), effective dielectric constant, gate oxide, high-k, metal–insulator–metal (MIM), ZrD-04, ZrO_2.**

I. Introduction

THE METAL–INSULATOR–METAL (MIM) capacitor for dynamic random access memory (DRAM) and for other analog and radio-frequency applications is attracting great interest in recent times [1]–[3] and must be aggressively scaled to meet the expectations of the semiconductor roadmap [4]. This demands the replacement of SiO_2 with a high dielectric constant (k) oxide that will provide a capacitance equivalent thickness (CET[1]) for the dielectric in the low subnanometer regime and a leakage current density of less than 1 fA/cell, equivalent to approximately 1×10^{-8}–1×10^{-7} A/cm^2.

Replacing SiO_2 $(k = 3.9)$ with $ZrO_2$$(k \sim 20$–$40)$ is considered by the authors as an investigative step toward introducing favored Hf/Zr-based crystalline ternary oxides $(k > 40)$ that will further reduce the CET value in line with current expectations [4]. Although DRAM MIM capacitor dielectrics with a CET of ∼0.9 nm are currently being implemented by the semiconductor industry, the high-k values and the very low leakage current densities reported here presently allow a margin of opportunity for the ALD method to further reduce the physical thickness of the oxide and improve on the ∼0.9-nm CET while still maintaining acceptable leakage current densities [4].

II. Sample Details and Technique

The substrate is n-type silicon with n+ type As surface doping $(\sim 5 \times 10^{19}$ cm$^{-3})$ of Si(100). This surface is exposed pre-MIM processing and forms a heavily As-doped SiO_2 layer, on which a layer of TiN metal (∼10 nm) is formed by metal–organic chemical vapor deposition. An ∼7–8-nm thick ZrO_2 film is deposited by ALD in an ASM Pulsar 2000, hot wall cross-flow reactor, at a reaction temperature of 275 °C, using Bis(methylcyclopentadienyl) methoxymethyl zirconium (SAFC Hitech, ZrD-04, see [5]) and ozone as precursors. Crystallization to the preferred tetragonal ZrO_2 symmetry would maximize the dielectric constant and minimize the CET; hence, premetallization rapid thermal annealing (RTP) treatments are employed to investigate the optimum temperature for increasing the k-value without significantly increasing the leakage current density. RTP is carried out for 60 s in N_2 (1000-mbar pressure) either at 400 °C, 500 °C, or 600 °C, using the Jipelec JetFirst 150 system. As-deposited samples (no RTP processing) are retained for comparative measurements. DRAM test MIM planar capacitors of various areas are formed from the as-deposited and RTP-treated samples using photolithography and a lift-off process for gate metallization. Device areas range from 400 to 160 000 μm^2. The metal gate consists of 10 nm Ti and 200 nm Al, both deposited *ex situ* by e-beam. Ti, Al, and TiN are the preferred metals because they meet the basic industrial standards, such as acceptable work functions, good adhesion, low cost, good step coverage, high temperature stability, and low resistivity.

Capacitance voltage (C–V) and capacitor quality factor voltage $(Q-V)$ measurements were performed at 25 °C using

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[1]The CET rule gives the same capacitance for a physically thicker high-k oxide layer, where CET $= 3.9\varepsilon_0 A/C_{\text{high-}k}$. CET and the equivalent oxide thickness (EOT $= 3.9t_{\text{high-}k}/k_{\text{high-}k}$) are approximately equal for MIM devices; hence, we can use this to get an effective value for $k_{\text{high-}k}(k_{\text{eff}})$. Hence, $k = k_{\text{high-}k} \sim k_{\text{eff}}$.

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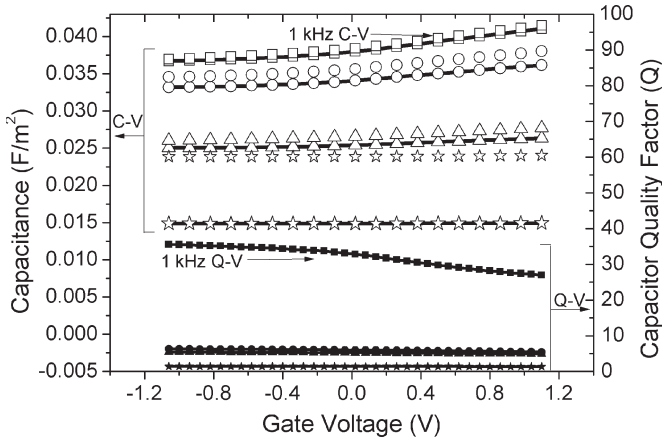

Fig. 1. (Open symbols) C–V and (filled symbols) related Q–V responses for a low leakage current density device of area 40 000 μm^2 with RTP at 400 °C. (Squares) One kilohertz. (Circles) Ten kilohertz. (Triangles) One hundred kilohertz. (Stars) One megahertz. Symbols connected with lines represent the parallel capacitance responses, and symbols with no lines are the series capacitance responses. The 1 kHz responses are almost superimposed, whereas C_p and C_s at other frequencies are dispersed due to the effects of series resistance. The slight bow in the 1 and 10 kHz C–V's is due to nonsymmetric metal work functions and dependences of the quadratic voltage coefficient of the capacitance (α) [1]–[3].

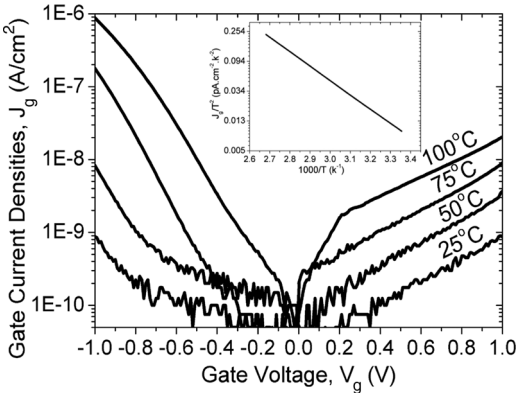

Fig. 2. Gate leakage current $(J-V)$ plots for 40 000 μm^2 area devices with an RTP of 400 °C. Measurement temperatures (T_m) are 25 °C, 50 °C, 75 °C, and 100 °C. At 25 °C, J is approximately 1×10^{-9} A/cm^2 at 1 V. The dominant conduction mechanism for all positive gate voltages up to 1 V is SE, and the dominant conduction mechanisms for negative gate voltages at $T_m = 25$ °C are PF emissions in the range of -0.8 to -1 V, and SE in the range of 0 to -0.8 V. It can be seen that PF becomes increasingly dominant over SE in the range of 0 to -0.8 V as T_m increases, consistent with the lower work function of Ti compared with TiN. (Inset) SE's linear relationship of J/T^2 versus $10^3/T$ ($V_g = 1$ V), with an activation energy of ∼0.4 eV and a TiN/ZrO_2 barrier height of ∼1.4 eV.

an HP4284A Precision LCR Meter. Current–voltage (I–V) measurements were performed with an HP4156A Precision Semiconductor Parameter Analyzer. I–V measurements were recorded at 25 °C, 50 °C, 75 °C, and 100 °C. All measurements were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry-air environment (dew point ∼ −70 °C).

III. Measurements and Results

Before using results from multifrequency C–V responses, it is necessary to establish the effects of series resistance at different frequencies. An established method is to compare the series capacitance–voltage (C_s–V) response with the parallel capacitance–voltage (C_p–V) response. If the C–V responses differ in low leakage current density devices, then this is due to series resistance effects.

Fig. 1 shows the C–V and Q–V responses for a low leakage device of area 160 000 μm^2 having undergone an RTP of 400 °C. The 1 kHz responses are almost identical, whereas the 10, 100, and 1 MHz responses are affected by series resistance. In addition, Q values are good for the 1 kHz responses (∼30) but reduce rapidly as the frequency is increased. Transmission electron microscopy (TEM) energy dispersive X-ray spectroscopy shows a 10–20 nm SiO_2 layer between the Si substrate and the TiN layer, which has a high As doping. The thickness of this interlayer does not increase with RTP treatment; however, its presence gives a substrate resistivity/higher resistivity film underneath the TiN layer and is the likely cause of the series resistance effects for frequencies >1 kHz. Hence, information extracted from C–V responses is confined to the 1 kHz measurements, which are sufficient for electrical characterization. Other higher frequency C–V data are ignored. The observed C–V frequency dispersion for frequencies greater than 1 kHz is more pronounced for devices with larger areas (∼0.005 F/m^2 range →∼0.03 F/m^2 range) and is also more pronounced for devices processed with higher RTP temperatures (∼0.013 F/m^2 range →∼0.025 F/m^2 range). In addition, the Q–V responses show reductions in Q by at least an order of magnitude for devices with larger areas and for devices processed with higher RTP temperatures. It is noted, however, that leakage current densities for all devices remain low on the order of nanoamperes per square centimeter and scale with the device area; hence, the leakage current is not a contributing factor to the observed frequency dispersion.

Leakage current densities (J–V) at 1 V for all devices (except RTP at 600 °C) are low at $\sim 1-2 \times 10^{-9}$ A/cm^2 for a measurement temperature (T_m) of 25 °C. This would indicate that C contamination is low [6]. The $J-V$ of devices with an RTP of 600 °C increases to $\sim 3 \times 10^{-8}$ A/cm^2 ($T_m = 25$ °C) for all device areas. Fig. 2 shows J–V plots for a 40 000 μm^2 area device with an RTP of 400 °C. The conduction mechanisms at $V_g = 1$ V and -1 V are Schottky (SE) and Poole–Frenkel (PF) emissions, respectively (see Fig. 2 inset for SE details).

Fig. 3 shows X-ray diffraction (XRD) data for as-deposited and RTP-treated devices. The inset also shows a TEM micrograph of a post-RTP of 600 °C device. Considering these data with the k values shown in Fig. 4, there seems to be cubic/tetragonal crystallites contained within an amorphous structure. As the RTP temperature increases, the k value increases, possibly due to a cubic-to-tetragonal phase change due to contaminants, such as F becoming less influential on the crystalline phase [6]. The high leakage at the 600 °C RTP is likely due to the higher k polycrystalline structure forming grain boundaries [7] and, possibly, Ti diffusion into the oxide via the TiO interlayer formation at the TiN/ZrO_2 interface [8]. Interlayer roughness can also increase with the RTP temperature, as seen from TEM, where ZrO_2 will follow the crystallization grains of TiN and Ti metals. However, this

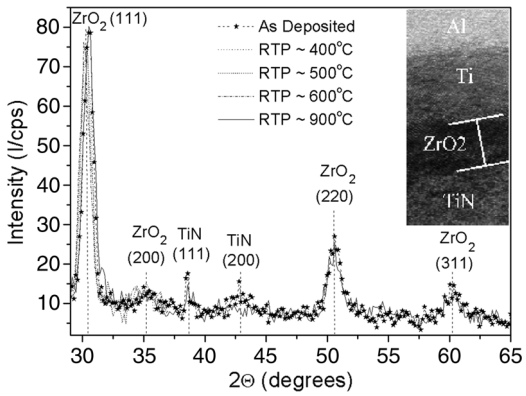

Fig. 3. XRD data conducted at room temperature for the as-deposited and post 900 °C RTP devices ($2\Theta = 29°-65°$) and at ∼400 °C, ∼500 °C, and ∼600 °C *in situ* for the equivalent RTP devices ($2\Theta = 25°-37°$). The dominant response at ∼30° shows a significant cubic and/or tetragonal crystalline contribution which does not change significantly with RTP processing. (Inset) TEM micrograph of a post-RTP of 600 °C device.

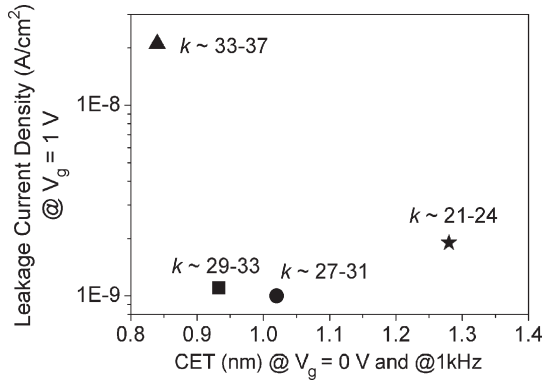

Fig. 4. CET values extracted from 1 kHz C–V responses at $V_g = 0$ V, plotted against leakage current densities at $V_g = 1$ V. The calculated dielectric constants are also shown. (Star) As-deposited devices. (Square) Four-hundred-degree-Celsius RTP devices. (Circle) Five-hundred-degree-Celsius RTP devices. (Triangle) Six-hundred-degree-Celsius RTP devices. The physical thickness of ZrO_2 remains unchanged for all devices at 7–8 nm.

does not affect the device performance at or below an RTP of 500 °C [7].

Fig. 4 shows CET values extracted from 1 kHz C–V responses at $V_g = 0$ V, plotted against leakage current densities at $V_g = 1$ V. The estimated k-value ranges for ZrO_2 are included, indicating an increase in k with RTP processing ($22.5 \pm 1.5 \rightarrow 32 \pm 5$) and an associated reduction in CET with RTP processing (∼0.3 nm). However, the leakage current density increases ($> 1 \times 10^1$) following the 600 °C RTP processing. These results compare well with a recent study [6], apart from the lower leakage observed here for all devices except those with the 600 °C RTP processing.

IV. Conclusion

MIM capacitors (TiN/ZrO_2/Ti/Al), having the oxide formed by ALD with the new ZrD-04 precursor, are investigated for the first time. C–V frequency dispersion (> 1 kHz) is observed, which is more pronounced for devices with larger areas and with higher RTP temperatures. Q–V responses reduce by at least an order of magnitude with increasing frequency. The leakage current densities at 1 V for all devices (except 600 °C RTP) are on the order of nanoamperes per square centimeter. Devices with an RTP of 600 °C show an unacceptable increase in the leakage current density by at least an order of magnitude. CET and k values are extracted using the 1 kHz C–V responses and TEM micrographs. There is an increase in k with RTP processing ($22.5 \pm 1.5 \rightarrow 32 \pm 5$), with an associated reduction in CET with RTP processing (∼0.3 nm) toward the subnanometer regime. The best CET-leakage values for post-RTP (400 °C−500 °C) are ∼0.9 nm and $\sim 1 \times 10^{-9}$ A/cm^2, respectively. As the leakage current density values obtained at 1 V are below the target of $1 \times 10^{-8}-1 \times 10^{-7}$ A/cm^2, there remains scope for further reduction in CET with ZrO_2 MIM structures formed by ALD with the new ZrD-04 precursor.

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