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**NATIONAL UNIVERSITY OF IRELAND, CORK**

# TWO-DIMENSIONAL SEMICONDUCTORS FOR FUTURE ELECTRONICS

THESIS PRESENTED BY

**GIOELE MIRABELLI**

FOR THE DEGREE OF

**DOCTOR OF PHILOSOPHY**

**UNIVERSITY COLLEGE CORK**

**SCHOOL OF ELECTRICAL ENGINEERING**

**TYNDALL NATIONAL INSTITUTE**

HEAD OF SCHOOL: PROF. WILLIAM P. MARNANE

SUPERVISORS: DR. RAY DUFFY, PROF. PAUL HURLEY, DR. SCOTT MONAGHAN

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Gioele Mirabelli

*To my family*

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# ABSTRACT

The aggressive scaling imposed by CMOS technology has put very stringent requirements on the dimensions of Silicon transistors. According to the semiconductor roadmaps (ITRS, IRDS, Nereid), the dimensions of the device might have reached its limits in terms of gate length. Although new device architectures are being studied to keep the pace up with Moore-law, new material systems are still relevant to further improve the performance of integrated circuits. On this regard, 2D-semiconductors, as transition metal dichalcogenides (TMDs), are being considered as potential replacement for Silicon. Because of their intrinsic thin nature, they can guarantee a better channel control at similar channel length, without suffering from high mobility degradation as other 3D-semiconductors.

In this dissertation, the limits and potentials of 2D-semiconductors are investigated by material analysis, electrical characterization and TCAD modeling.

First, the air sensitivity of few TMDs is considered. An initial AFM study show high reactivity in $HfSe_2$, with blisters growing up to 60 nm after one day from ambient exposure. These results are later confirmed by other techniques, showing a high detrimental effect on the semiconductor surface. The surface treatment or protection of these materials needs to be carefully studied for their use in the semiconductor industry.

A second limitation of 2D-electron devices is their low mobility compared with theoretical studies. Material and electrical characterizations of 3-layers $MoS_2$ transistors show a high impurity concentration, which drastically limits the field-effect

mobility and so device performance. Mobility could be improved carefully selecting a proper dielectric environment, which plays an important role in the current transport in thin semiconductors.

However, the major limitation of 2D-based electronics is related to a poor metal-TMD interface, often characterized by high Schottky barriers and Fermi-level pinning. Taking as example modern semiconductor technologies, highly doped $MoS_2$ devices are carefully studied. The contact resistance extracted is lower with respect of undoped or untreated samples, and close to the requirements imposed by the semiconductor roadmaps. Another solution might rely on the annealing of the metal-TMD interface in order to create a 3D-alloy, which might be optimal in terms of contact resistance.

The final part is related to the development of a TCAD model for 2D-semiconductors. At first, the model parameters were carefully tuned against theoretical and experimental results. Then, a TCAD software was used for a deeper understanding of experimental devices, regarding the metal-TMD and oxide-TMD interface. Later, the same model was improved considering a layered-structure, taking into consideration the semiconductive layers as well as the Van-der-Waals gaps in between them.

# Chapter 1: INTRODUCTION

## 1.1 BACKGROUND AND MOTIVATION

The modern electronics technology has its roots in 1947, when the first working transistor was experimentally proven and for which John Bardeen and Walter Brattain together with William Shockley received the Nobel Prize in Physics for their discovery of the transistor effect.[1] Even if revolutionary, another step needed was the integration of more components onto the same chips. The idea of Jack Kilby at Texas Instruments in 1958 was to make all the components and the chip out of the same block of semiconductor material, developing the first integrated circuit. In this way there were no need of discrete components, the process could be automated, and it would allow a much higher performance.

The evolution of electronics technology of those years can be summarized by "Moore's law".[2] Gordon Moore predicted that the numbers of transistors that can be installed on an integrated circuit could be doubled every two years. This can be achieved by shrinking down all the dimensions of the device. In 1974 Dennard et al.[3] showed the benefits of scaling. This is based on the assumption that the electric field inside the transistor is kept constant. Considering a scaling factor $\alpha$, switching speed increases by a factor $\alpha$, power dissipation is reduced by a factor $\alpha^2$ and the power-delay product by a factor $\alpha^3$ . This scaling law implies a reduction in the supply voltage and threshold voltage by a factor $\alpha$.

A clear image of this is reported in Figure 1,[4] where each year the dimension of the single device decreases, allowing a higher density and an always better performance in terms of circuit speed and power dissipation.

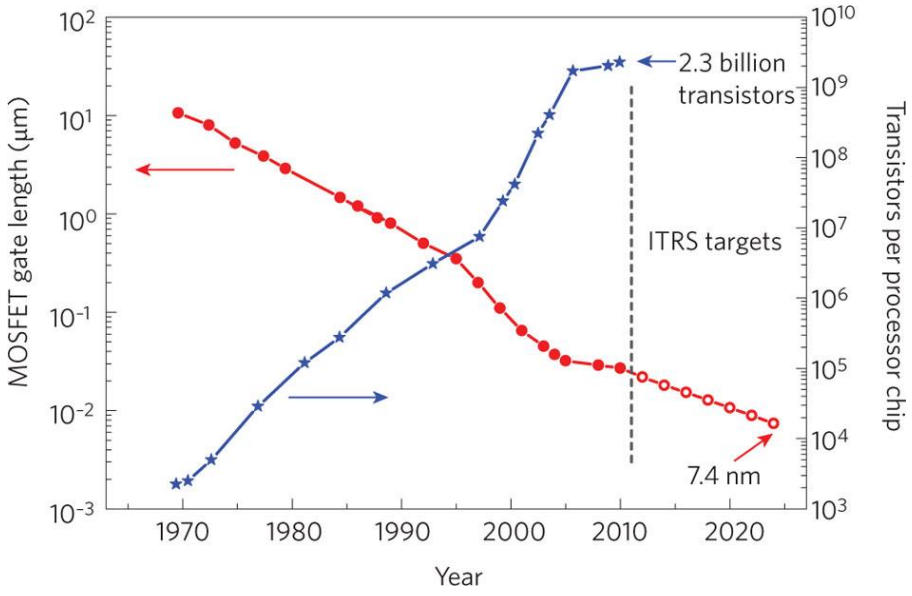


**Figure 1: Trend of gate length and number of transistors per processor chip per year.[4]**

As a consequence of this trend, the miniaturization of circuits by scaling down transistor's dimensions has been a central topic for the last 60 years and Dennard's scaling law was followed by semiconductor industry until 2005 approximately.

The aggressive scaling of devices brought new kind of problems known as "short-channel effects" (SCE), which arise when distance between source and drain regions become very small. Considering a classic MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) architecture, the source and drain junctions create depletion regions which make the actual channel length shorter. The electric fields that penetrate the channel regions make the control of the gate on the channel less effective, because the channel potential doesn't depend on the gate voltage only, but they are also dependent on the voltages applied on source and drain.[5] A visual example is shown in Figure 2, where the drain-junction depletion regions increases for higher drain voltages.

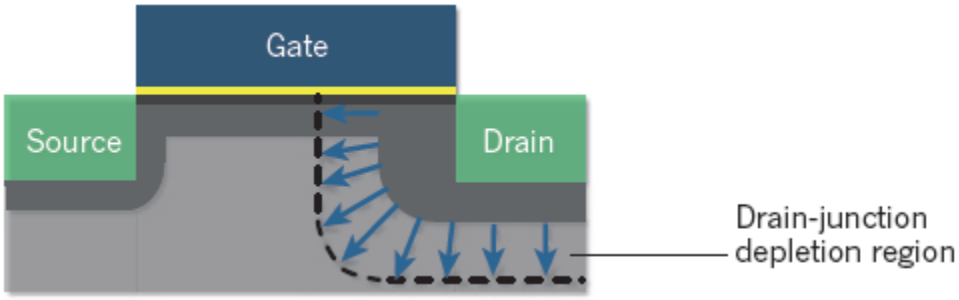


**Figure 2: example of drain-junction depletion region, responsible for short-channel effects.**[5]

In order to mitigate SCE, the research community is actively looking for promising materials to replace Silicon in the future. Among all of them III-V semiconductors, Germanium and 2D materials are the most studied. In particular this last class of semiconductors are gaining much interest in the recent years. Their general characteristics, potential and major limitations will be discussed in the following paragraphs.

A second issue in modern technology is related to power consumption. Figure 3 shows the two components of power consumption in MOSFET technology versus gate length: active and subthreshold power density. The former is related to the operation frequency of the device:

$$P_{Act} = CV_{DD}^2 f \qquad (1)$$

where $P_{Act}$ is the active power consumption, C is the load capacitance, $V_{DD}$ is the supply voltage and f is the operation frequency.

The latter, subthreshold power consumption, depends on the OFF current, $I_{OFF}$:

$$P_{Sub} = V_{DD} I_{OFF} \quad (2)$$

Although the active power consumption can be reduced with a scaling of $V_{DD}$, this will in turn affect $I_{ON}$ and so device performances. That is why beyond the 100 nm technology node the improvement of device performance departed from dimensional scaling alone,[6] and an increase in the drive current was supplemented by boosting mobility with uniaxial strain,[7] high-k oxides[8] and novel architectures.[9] It is also clear from Figure 3 that below 20-nm gate length the subthreshold power density is higher than the active power density.[10] For this reason materials or architectures capable of achieving a lower $I_{OFF}$ are necessary to optimize power consumption.

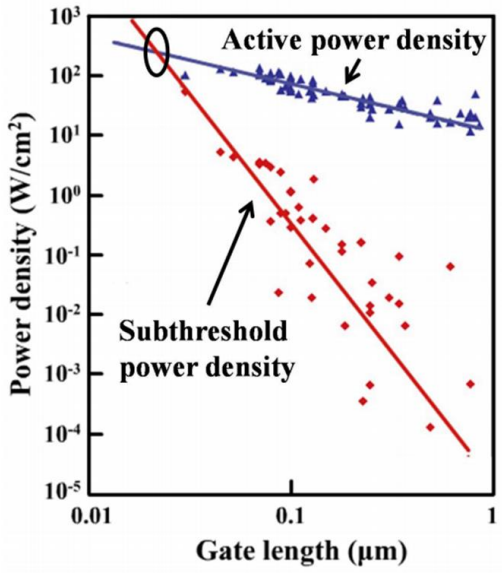


**Figure 3: Active and subthreshold power densities for Si MOSFETs with respect of gate length. The cross-over point at 20-nm gate length indicates where subthreshold power density surpasses active power density.[10]**

## 1.2 2D-MATERIALS PROPERTIES AND APPLICATIONS

### 1.2.1 Crystal structure

The interest in 2-Dimensional materials started after the successful experimental demonstration of graphene in 2004, one atomic layer of carbon atoms.[11]

These carbon layers are held together by weak Van-der Waals forces, which allows the isolation of thin flakes by mechanical exfoliation. Graphene has interesting characteristics, such as high mechanical strength, thermal and electrical conductivity, which makes it an interesting material for next-generation interconnects.[12] Nevertheless, graphene is characterized by a zero bandgap, and a bandgap is essential for logic based electron device applications. Several 2D materials have been studied by the research community since the discovery of graphene, and the class of materials called Transition-Metal Dichalcogenides (TMDs) have been the subject of particular research attention. These are semiconductors in the form of $MX_2$, where M is a transition metal (Mo, W, Hf), and X is a chalcogen (S, Se, Te). Each TMD layer is composed by a layer of metal atoms "sandwiched" between the chalcogen atoms and the interlayer distance is ~0.65 nm, as schematically shown in Figure 4a.[13] The metal and chalcogen atoms are covalently bonded together, while each layer is heal together by weak Van-Der-Waals forces. Figure 4b shows a high-resolution Cross-Section TEM of $MoTe_2$ to highlight the layered structure of the material system. The atom configuration of Figure 4a was overlapped in some regions in order to help the eye distinguishing each semiconductive layer. The weak Van-Der-Waals forces between each monolayer of which they are formed, allow thin multilayers to be easily exfoliated by a scotch tape technique from their bulk form, as was first shown for graphene. Although a large area growth technique will be needed to integrate them with the modern technologies, the mechanical exfoliation offers a fast and reliable route to characterize the material properties.

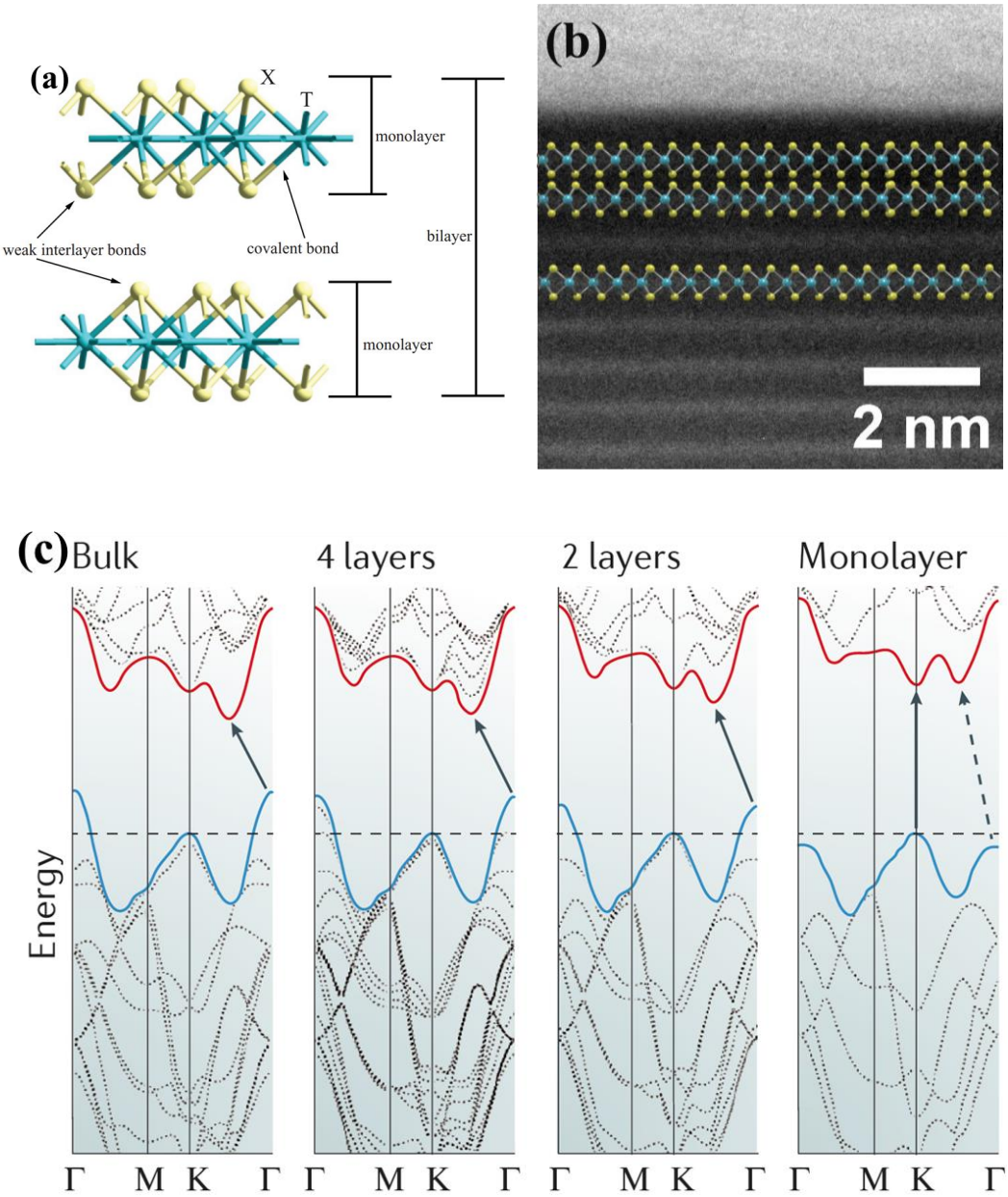


**Figure 4: (a) Typical crystal structure of a TMD. [13] (b) Transmission electron microscopy cross section of a $MoTe_2$ exfoliated flake. Superimposed the crystal structure to emphasize the layered nature of these materials. (c) Bandgap evolution with respect of number of layers of $MoS_2$, from monolayer to bulk.[17]**

As said, TMDs show a finite direct bandgap from few meV to ~2 eV, predicted by density-functional-theory (DFT) calculations,[14] which makes them suitable for logic devices.[15, 16] Figure 4c show the bandgap variation with respect of number of layers for $MoS_2$. The gap of bulk $MoS_2$ is ~1.2 eV and it increases to ~1.9 eV in its

monolayer form. Interestingly, bulk $MoS_2$ is an indirect bandgap semiconductor, while it becomes direct at the monolayer. As shown in Figure 4c, the bandgap properties of $MoS_2$ with respect of number of layers depend on the transition of the top of the valence band from the Γ to the K point, while the minimum of the conduction band shifts from halfway between Γ and K to the K point.[17] It is important to notice that this point is not a high symmetry point of the Brillouin zone, and its exact position depends on thickness and Metal/Chalcogen.[18] These two valley have been shown to be important for to understand the velocity saturation in monolayer $MoS_2$.[19]

**Table 1: comparison of Nb, Ta,[20-22] Mo and W[13, 22-26] TMDs considering their electronic characteristics. Table adapted from [27].**

| | **$-S_2$** | **$-Se_2$** | **$-Te_2$** |
|---|---|---|---|
| | **Electronic characteristics** | **Electronic characteristics** | **Electronic characteristics** |
| **Nb** | Metal; Superconducting; Charge density wave; | Metal; Superconducting; Charge density wave; | Metal |
| **Ta** | Metal; Superconducting; Charge density wave; | Metal; Superconducting; Charge density wave; | Metal |
| **Mo** | Semiconducting 1L:1.8 eV Bulk: 1.2 eV | Semiconducting 1L:1.5 eV Bulk: 1.1 eV | Semiconducting 1L:1.1 eV Bulk: 1.0 eV |
| **W** | Semiconducting 1L: 2.1 eV Bulk: 1.4 eV | Semiconducting 1L: 1.7 eV Bulk: 1.2 eV | Semiconducting 1L: 1.1 eV |

In addition, TMDs exist in other phases as well. The 2H is the most common semiconducting phase, but interesting properties were also found in the metallic 1T-phase.[28] As will be detailed later in chapter 3 and 5, the opportune modulation of the

material below the contact region can open up new ways in order to drastically reduce contact resistance in 2D-Field Effect Transistors (2D-FETs). Due to the high number of possible combinations between transition metal and chalcogenides, TMDs show a wide range of electrical properties as summarized in Table 1, where four different chalcogens, namely Nb, Ta, Mo and W are compared. Considering a variation of the transition metal or the chalcogen the properties of the material can change drastically, from semiconducting to superconducting, which makes TMDs generally suitable for a wide range of applications.

### 1.2.2 **Growth of TMDs**

As briefly said in the last section, most studies on the electrical or optical behaviour and material properties of TMDs have been based on mechanically exfoliated flakes. In these works, TMDs are exfoliated by scotch tape technique from their bulk counterpart, grown by chemical vapour transport at high temperature.[29, 30] It is relatively easy to isolate few or single layers of material, and the flakes so obtained are surely a fast and easy way to study the material. However, the process is not scalable, and therefore not compatible with the modern nano-electronic industry. Therefore, many research groups showed interest in looking for the optimal growth technique and condition of TMDs in the recent years. The most common techniques used to grow TMD films is probably chemical vapour deposition (CVD), although there are also examples of atomic layer deposition (ALD) or molecular beam epitaxy (MBE) grown materials.[31-34]

In CVD, a film of metal oxide (e.g.: $MoO_3$) is in close proximity or deposited directly to the desired substrate. The desired chalcogen is then heated and flows in vapour phase in the same chamber. It then reacts with the pre-deposited (or adjacent)

film at relatively high temperature, usually around 800 $^{o}$C.[35-37] The growth is not homogenous, and it is characterized mainly by "triangular" grains that merge together after sufficient growth time.[38] The thermal budget of these processes is usually high to obtain a reaction of the chalcogen with the metal oxide. However, high performance devices were reported by this method, where $MoS_2$ was deposited on $Al_2O_3$.[39]

Conversely, ALD allow the deposition of TMDs at relatively lower temperatures between 100 and 475 $^{o}$C.[40-45] An example is the work of Tan et al.,[42] where a high control over the $MoS_2$ thickness was achieved. Nonetheless, a high temperature annealing of 800 $^{o}$C was necessary to grow large size crystals of ~2 µm. Similarly, Jurca et al.[46] studied the ALD deposition of $MoS_2$ varying temperature and pulse time. The temperatures used are very low, between 60 and 120 $^{o}$C. Although a uniform deposition was achieved the grain size is extremely small, and it is improved only by annealing for 5h at 1000 $^{o}$C. This is extremely detrimental for TMD-based FET, as mobility is highly dependent on the grain size.

An alternative technique is thermal assisted conversion (TAC), by which a metal initially deposited on the desired substrate is converted into a TMD through high temperature annealing in a chalcogen atmosphere. This method has previously been used for $MoS_2$, and both a high temperature (750 $^{o}$C) and a thin initial film thickness were necessary to obtain a complete conversion and a uniform film coverage.[47, 48] This process can also be used for the growth of $PtSe_2$,[49] a TMD which interest increased in the last few years. In contrast to other TMDs, the synthesis by TAC of $PtSe_2$ does not require a high thermal budget[50] (temperature is ~400 $^{o}$C) which it makes growth compatible with back-end-of-line processing.[51-53]

Molecular beam epitaxy is another technique that has become more common in the last years. With respect of CVD, it requires typically lower temperature, offers a greater control of film thickness,[34] as well as the possibility to incorporate dopants[54] or to grow high quality heterostructures.[55] Recently, Yue et al.[56] studied the deposition of $WSe_2$ by MBE, considering the effect of the metal flux, chalcogen flux and temperature in order to achieve higher grain sizes. Although promising and improved with respect of similar works, the results are far from satisfying the large area growth required by the CMOS industry.

A proper compromise of the temperature growth with the requirements of the preferred application is certainly required for the usage of TMDs in future electronics and optoelectronics applications. In order to respect the stringent temperature requirements of the CMOS industry and still obtaining high crystal quality, Huyghebaert et al.[57] proposed the high temperature growth of $WS_2$ and its transfer to the target substrate, since several methods wafer scale quality growth of TMDs have been reported.[58] With this process a temporary adhesive/laser release layer is spun on the glass wafer and bonded to the $WSe_2$ layer. The $WS_2$ is then peeled off from the initial substrate and transferred to the preferred substrate. The temporary stack is then released by laser. The transfer process can influence the electrical properties of 2D-materials, because of local strain, cracks and wrinkles,[59] but the use of a 300 mm grown material allow the use of wafer handling methods, with higher control and precision.

### 1.2.3 **Optoelectronic applications**

These characteristics open a wide range of possible applications for TMDs in optoelectronics and photonic applications, as photo-detectors, emitters, single-photon

emitters and valleytronics.[60, 61]

Due to the enhanced absorption observed in $MoS_2$ photovoltaic applications are of particular interest. This research area is not recent and started in 1982, when Fortin and Sears reported the photovoltaic effect in bulk $MoS_2$ with efficiency of 1%.[62] More recent results showed an efficiency of 4.5% of 12.5 nm of $MoS_2$ on p-type Silicon.[63] Similar results were obtained considering heterojunction of $MoS_2$ on Si or GaAs, which yielded 5.23% and 4.82% respectively.[64, 65] These results might be further improved considering that the $MoS_2$ was transferred after growth with a sacrificial PMMA layer, where residues might affect the device efficiency. In addition further improvement can be achieved by considering a h-BN interlayer, electrical gating or chemical doping or with graphene quantum dots.[65, 66] The change of bandgap with respect of number of layers, or through heterostructures of different TMDs, might be particularly suitable for photovoltaic applications.[67] In particular, using materials with different bandgaps in a singular multijunction solar cell, would allow photons of different energies to be absorbed, reducing losses due to thermalization.[68]

In addition, several reports have shown photodetection using a wide range of TMDs. Considering $MoS_2$, phototransistors were fabricated with mono- or few-layers of material, exfoliated or grown by chemical vapour deposition, with photoresponses ranging from 7.5 mA/W to 800 A/W.[69-71] However, similar results were also obtained considering $MoSe_2$,[35, 72, 73] $WS_2$[74, 75] and $WSe_2$.[76] The photodetection sensitivity in specific wavelength ranges can also be tuned considering different thicknesses, as mono- and bi-layer $MoS_2$ showed greater green light sensitivity, while tri-layers showed an improved sensitivity to red light.[77] Interestingly, some reports showed photodetectors based on heterostructure using $MoS_2$ and $WS_2$.

### 1.2.4 **Electronic applications**

TMDs have been shown to be possible solution for high performance electronic devices. Due to their properties and 2D-nature TMDs can be very useful for Tunnel-FET (TFET). With respect of classic MOSFET, TFET can show subthreshold swing below the classic 60 mv/dec, which is very important for low-power devices, as portable electronics and sensors in the future. The working principle between the two architecture is different.[78] As depicted schematically in Figure 5a, n-type MOSFET devices can be switched on when the gate voltage applied lowers enough the barrier between the source and drain region for electron transport from source to drain in the semiconductor conduction band. On the contrary, for a n-channel TFET carriers originate from valence band in the source. The gate voltage applied lowers the conduction band of the channel region, so it overlaps with the valence band of the source region, allowing tunneling of carriers.

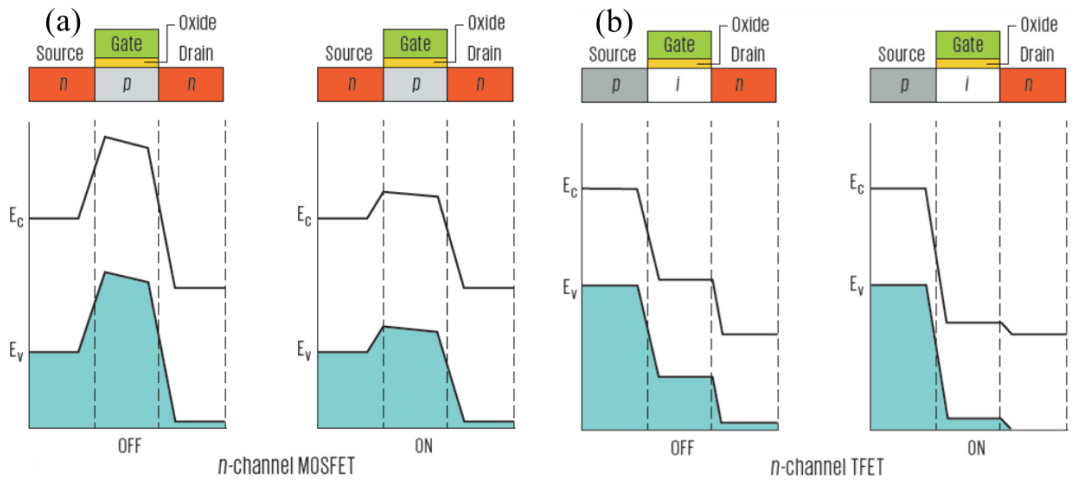


**Figure 5: Comparison of band diagrams of (a) a n-channel MOSFET and (b) a n-channel TFET during off and on operation, showing the main difference between their working principle. The terms $E_C$ and $E_V$ refer to the minimum energy of the conduction band and maximum energy of the valence band, respectively. Adapted from [78]**

The difference in bandgap and electron affinity among different TMDs can be exploited in order to properly align the conduction and valence band of the source and drain regions, which can be made out of two different materials.[79, 80] Since both materials are layered, the interface can in principle be free of defect states or dangling bonds, which can cause inelastic trap-assisted tunneling in the OFF-state and degrade the device behavior.[81-83]

On this topic, Li et al.[84] explored by theoretical simulations the band alignment of vertically stacked $WSe_2$ and $SnSe_2$. It was reported a subthreshold swing of ~14 mV/dec for both p- and n-TFET at a $V_{DS}$ of 0.4V, with higher energy efficiency with respect of other architectures. A similar architecture was fabricated by Sarkar et al.[85] using p-type Germanium and bi-layer $MoS_2$. Although the desired $I_{ON}$ performances were not achieved, a steep subthreshold slope of ~31.1 mV/dec was obtained for almost 4 orders of magnitude.

### 1.2.5 **Comparison and advantages of TMDs for electronics applications**

Although promising, the study and experimental reports of TFET based on 2D-semiconductors is still at an early stage. In order to compare the characteristics of 2D-materials with other semiconductors it is possible to consider a MOSFET architecture, which has been extensively used as a benchmark architecture to analyze and study the properties of these materials. On this regard, it is important to consider that the NanoElectronics Roadmap for Europe (NEREID) states that a fully depleted Silicon On Insulator (SOI) node "can be a long lasting technology with differentiated options (RF, mixed signal, ultra-low power, embedded memories, sensors…)".[86] MOSFET based on TMDs can be considered as a close analogy to fully-depleted SOI due to their intrinsically thin nature. Therefore, the study and optimization of this architecture is

still of interest. To do so, it is possible to study the behavior with respect to SCEs. As will be clarified in this section, the minimization of SCEs depends on several different properties.

To quantify the effectiveness against SCEs it is possible to consider the natural length λ, which represents the electric field lines of source and drain region in the channel. In a single gate MOSFET, as evaluated by Yan et al.[87]:

$$\lambda = \sqrt{\frac{\varepsilon_{Ch}}{\varepsilon_{ox}} t_{Ch} t_{ox}} \tag{3}$$

Where $\varepsilon_{Ch}$ is the electrical permittivity of the channel material, $\varepsilon_{ox}$ is the electrical permittivity of the oxide, $t_{Ch}$ is the channel thickness and $t_{ox}$ is the oxide thickness.

Generally, to produce a good subthreshold behavior the natural length should be 5-10 times lower than the effective channel length. Since a short channel length is desired to keep up with Moore's law, the natural length should decrease too in order to guarantee a good device behavior. From Equation 3, λ is proportional to both the thickness of the oxide and the thickness of the channel. As known a thinner oxide guarantees a better capacitive coupling of the gate, but the channel thickness impacts the natural length just as much. Even if Equation 3 was derived for fully depleted SOI and does not strictly apply to 2D materials,[88] a thinner channel can be more effective against SCE. This is true for every semiconductor device, but the electrical properties of 3D-semiconductors degrade significantly when thinned down do the 5-10 nm scale.

To appreciate the difference between different materials when the thickness is scaled, as initial step it is possible to consider the semiconductor carrier mobility. DFT calculations for monolayer $MoS_2$ showed an upper limit of 400 $cm^2/V.s$.[89]

Experimental results show usually much lower values because of the presence of impurity, defects and contact resistance.[90-92] The mobility of 3D-semiconductors instead scales between $t_{ch}^{6}$ and $t_{ch}^{4}$ due to surface roughness and phonon scattering.[93, 94] High-mobility materials, such as III-V, can easily exceeds $10^4$ $cm^2/V.s$. However these values degrade drastically at low thicknesses.[95-97] As well, Silicon films showed a high resistivity approaching small dimensions (1-5 nm).[98, 99] The situation is depicted schematically in Figure 6a.[100] The mobility of TMDs is lower with respect of graphene or classic 3D-semiconductors, yet they keep a reasonable mobility at low thicknesses.

High mobility values are a consequence of low effective masses. The comparison is depicted in Figure 6b. Since the effective mass is inversely proportional to mobility, the trend is opposite with respect of Figure 6a. For aggressive scaled devices (sub-5 nm scaling), the distance between source and drain region is short enough that quantum-mechanical source-drain tunneling can significantly degrade the subthreshold swing and increase $I_{OFF}$ (indirectly it reduces $I_{ON}$ as well, as gate work-functions are chosen to match a certain $I_{OFF}$). For this reason, the physical gate length predicted by the ITRS roadmap in 2015 reached a plateau value of 10 nm from 2021 onwards. The newer IRDS roadmap in 2017 predicted instead an even larger value, from 16 to 12 nm from 2021 to 2030.[101] Therefore, materials with lower mobility but higher effective mass might become preferable.[89, 102, 103] 2D-semiconductors are in general characterized by a higher effective mass (Figure 6b), making them more immune to SCEs. It is also important to consider that both mobility and effective mass values might still be optimized by strain engineering,[104, 105] which might be another method to tune the properties of 2D-semiconductors.

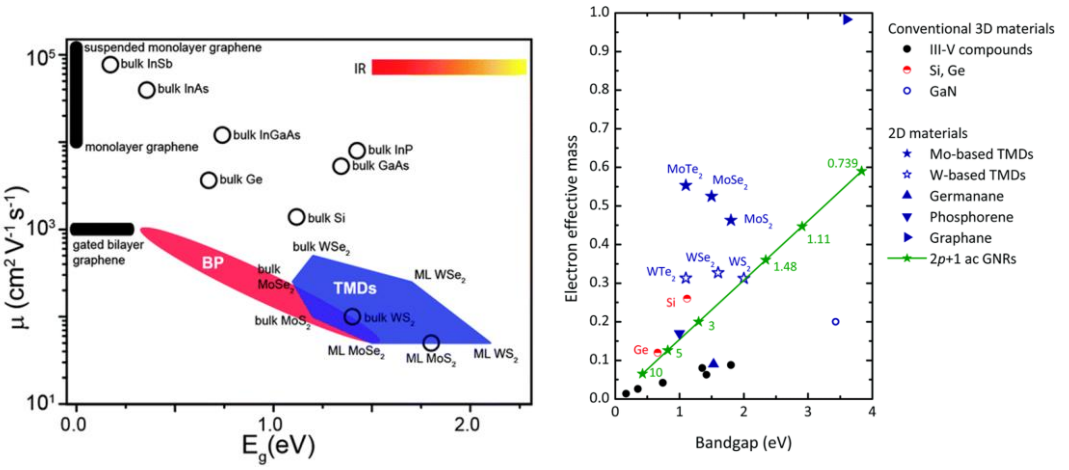


**Figure 6: (a) Plot of mobilities versus band gap for TMDs, Si, Ge and III-Vs. The color scale represents the energy range of visible and infrared light with respect to the band gap energy.[100] (b) Electron effective mass versus bandgap. III–V data are InSb, InAs, $In_{0.53}Ga_{0.47}As$, InP, GaAs, $Al_{0.3}Ga_{0.7}As$ from left to right.[88]**

It is also important to consider that effective mass is directly related to the effective conduction band density of states (DOS). III-V materials for example, are characterized by a low effective mass and so low density of states in the conduction band. This problem is commonly known as "DOS bottleneck", where a large gate voltage is necessary to swing the Fermi enough to strongly invert the III-V surface.[106] For the sake of comparison, the effective DOS for the conduction band of GaAs is $4.7x10^{17}$, while it is $3.2x10^{19}$ for Silicon and in the order of $10^{20}$ for monolayer $MoS_2$.[107, 108]

In addition, following again Equation 3, λ is also directly proportional to the dielectric constant of the semiconductor, $\varepsilon_{ch}$. The dielectric constant of TMDs (~3-6) is generally lower than the one of Silicon (~12), Germanium (~16) or III-V materials (~9-16). Therefore, for the same oxide or channel thickness, the immunity to SCE is higher.

An advantage that holds for both the MOSFET and the TFET architecture is

related to the interface of the material. As briefly introduced in the previous section, the lack of dangling bonds allows a more performant TFET. However, in addition to that, for both architectures, a semiconductor-oxide interface is also necessary. For this same reason the interface between an oxide and a 2D-semiconductor is theoretically perfect, allowing for low density of interface traps and so better performances in terms of subthreshold swing, mobility and reliability.

## 1.3 CHALLENGES OF 2D-MATERIALS

### 1.3.1 Defects and impurities

The performances of any FET device are highly dependent on the quality of the channel material as defects and impurities can drastically change its electrical behaviour. Considering Silicon as example, unintentional impurities are controlled to be less than $5x10^{10}$ $cm^{-2}$, and structural defects below 0.008 $cm^{-2}$.[109] This is necessary in order to maintain a good mobility and avoid variability between different devices. Several reports using different techniques have shown a high concentration of defects and impurities on different TMDs.

Studies on the surface of natural and synthetic exfoliated $MoS_2$ by scanning tunnelling microscopy (STM) showed a high concentration of defects present on the surface, attributed to Sulphur vacancies.[90, 110] Some point defects instead pointed to a high concentration of impurities. An inductively-coupled plasma mass spectroscopy analysis carried out on the same crystals showed that a concentration greater than $10^{13}$ $cm^{-2}$, way higher with respect of what is required in the Si-based integrated circuit industry. The high presence of impurities is extremely detrimental for the carrier mobility of these materials. Several theoretical calculations have shown how the effect of impurity concentration impacts the carrier mobility in 2D semiconductors.[92, 111, 112]

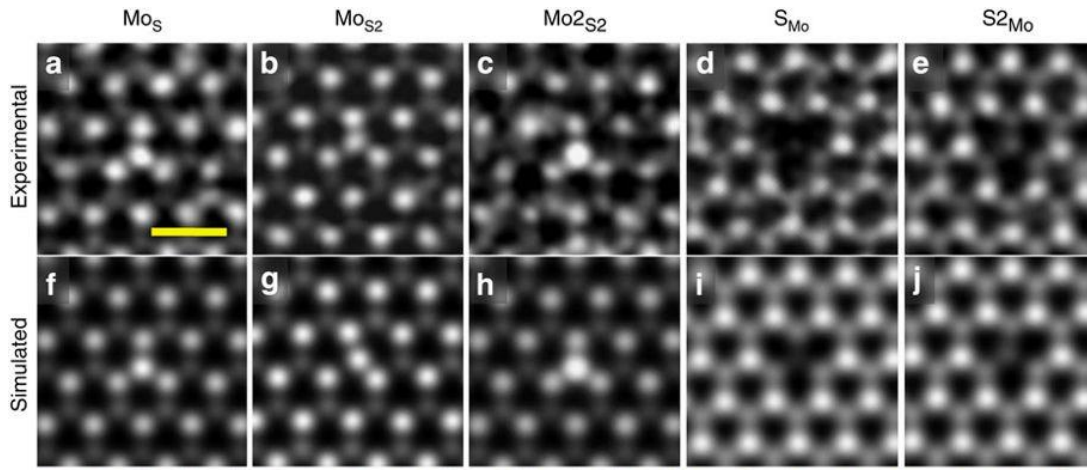


**Figure 7: Atomically resolved annular dark-field scanning transmission electron microscopy of defects in $MoS_2$: (a) Mo replacing (a) one or (b) two S atoms, (c) two Mo atoms replacing two S atoms, (d) one and (e) double S vacancy. Scale bar is 0.5 nm. [113]**

Another systematic studied was performed by Hong et al.[113] by electron microscopy. The monolayer $MoS_2$ mechanically exfoliated showed several different defects: sulphur vacancy, double sulphur vacancy, Mo vacancy, one S atom replacing Mo site, shown in Figure 7. Statistically, the sulphur vacancy (SV) is the most common defect in exfoliated $MoS_2$, with a concentration up to $3.5x10^{13}$ $cm^{-2}$.

In addition, Qiu et al.[114] combined an electron microscopy study of monolayer $MoS_2$, confirming a SV concentration of ~$10^{13}$ $cm^{-2}$, with density functional theory (DFT) calculations and electrical transport. The electrical transport of monolayer $MoS_2$ was explained by hopping transport through defects. In agreement, DFT calculations have shown that sulphur vacancies are characterised by energy levels that lie in the bandgap of $MoS_2$, 0.2-0.3 eV below the conduction band. In particular, theoretical works predicted that a sulphur vacancy is occupied by two electrons in its neutral state, which correspond to the valence of the missing sulphur atom.[115-117]

It is also important to state that few layers of $MoS_2$ are much more affected by defects with respect of thicker samples.[118, 119] Figure 8a and 8b show the transfer

characteristic of multi- and mono-layer $MoS_2$ at different temperatures. For temperatures below 100 K the signature of defects is much clearer and it causes "jumps" of the transfer characteristic in the subhreshold region. Figure 8c shows a schematic of multilayer $MoS_2$ on $SiO_2$ to explain the difference related to the thickness of the two devices. Both devices are characterized by a high presence of defects, but in the multilayer case, adjacent layers can screen the defects. On the contrary this can't happen in monolayer devices. It is not certain if the defects are localised inside the $MoS_2$ or at the $MoS_2/SiO_2$ interface, but the sensitivity of thinner devices to defects is clear.

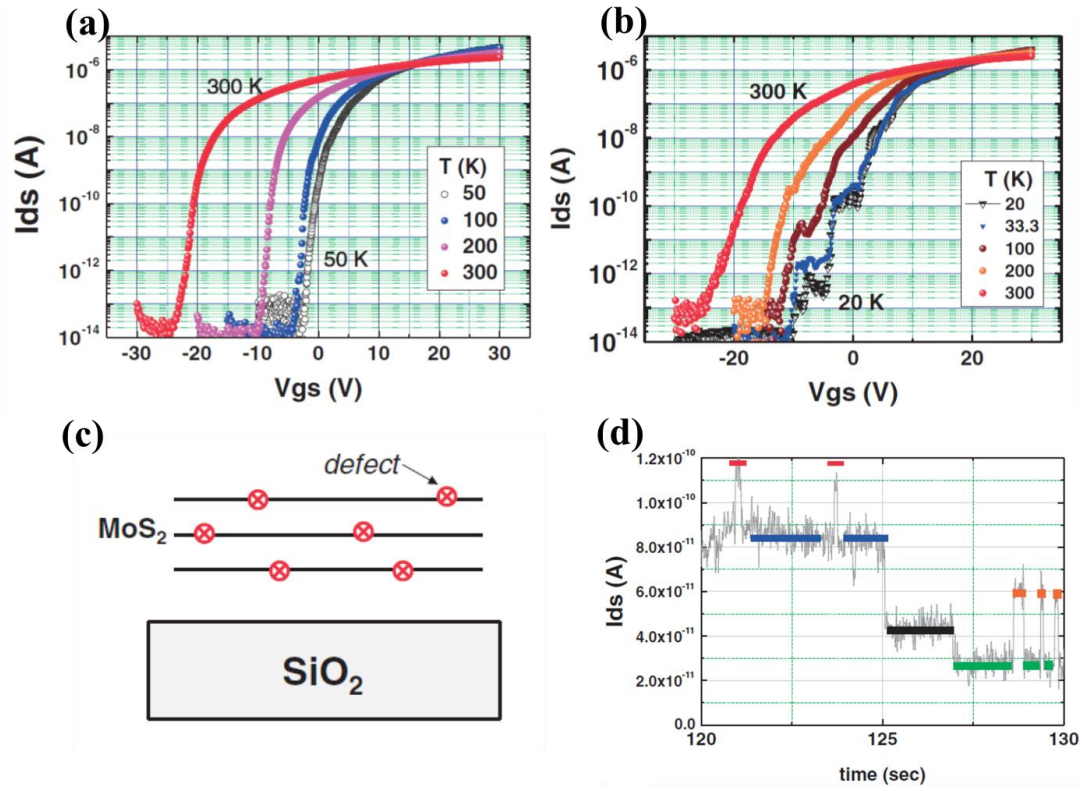


**Figure 8: Subthreshold characteristics of (a) multilayer and (b) monolayer $MoS_2$ at different temperature. The monolayer device clearly shows the presence of active defects, on the contrary of the multilayer device (c) Schematic illustration of the multilayer device to show the difference between the multi- and mono-layer device, as in a multilayer device a defect can be screened by carrier in the adjacent layers. (d) Example of temporal characteristic of monolayer $MoS_2$ at 20K showing several current levels.** [118]

The high presence of these defects can also be responsible for the Fermi-Level Pinning usually present in $MoS_2$, and for the contact behaviour in general, but this will be further discussed in the next section. The presence of impurities and defects as well as their impact on the electrical behaviour of $MoS_2$ are going to be studied in Chapter 4 and 6.

### 1.3.2 Metal-TMD interface: Schottky barrier and Fermi-level Pinning effect

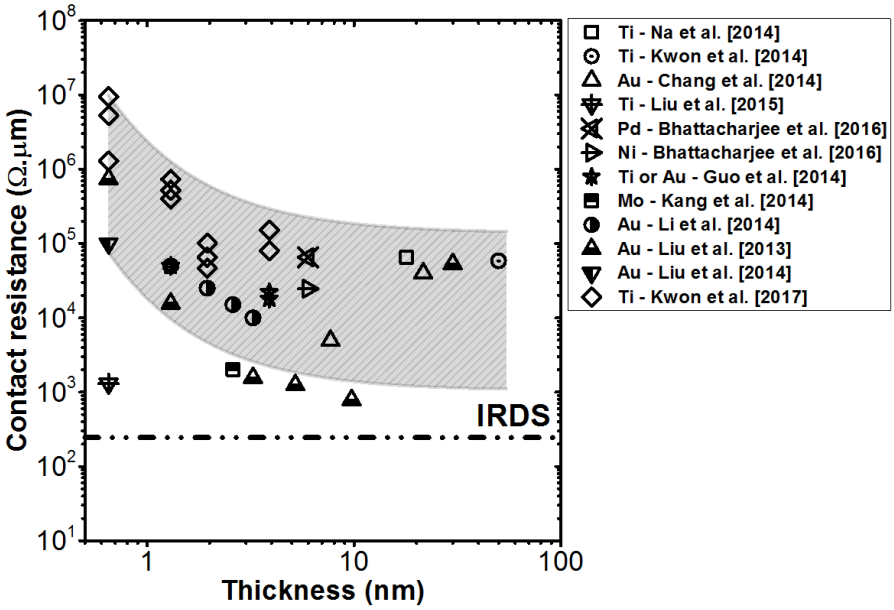


**Figure 9: Summary of contact resistance values found in literature considering as-exfoliated devices. The gray area shows the general trend of contact resistance, characterized by high variability and excessive high values.**

A low contact resistance is of great importance for scaled semiconductor devices and this is of particular interest for 2D semiconductors.[120] It is one of the most studied subject on TMDs and the issues has been treated from a material, electrical and theoretical perspective. Indeed, a reliable process to obtain an ohmic contact with TMDs is still missing and most of the time the contact is characterized by high Schottky barriers. For a clearer idea, Figure 9 shows a trend of contact resistance versus $MoS_2$ thickness considering several reports.[121-131] The dashed line represents

the goal set by the IRDS roadmap for 2027.[101] These data are in fair agreement with each other. The contact resistance decreases from ~$3x10^6$ Ω.μm for monolayer $MoS_2$, to ~$6x10^4$ Ω.μm for thick samples. In addition, these data consider both low and high work-function metals, but there is not any trend considering a variation of the metal contact.

To explain the behavior of the $MoS_2$-metal contact, Figure 10a show the band-diagram of a metal-semiconductor interface before contact. $\phi_M$ and $\phi_S$ are the metal and semiconductor work functions respectively, while $q\chi$ is the semiconductor electron affinity. When the two materials come in contact an electrical current flows across the interface.[132] Due to the migration of electrons from the semiconductor to the metal a depletion region creates at the interface and a potential barrier is formed (Figure 10b).

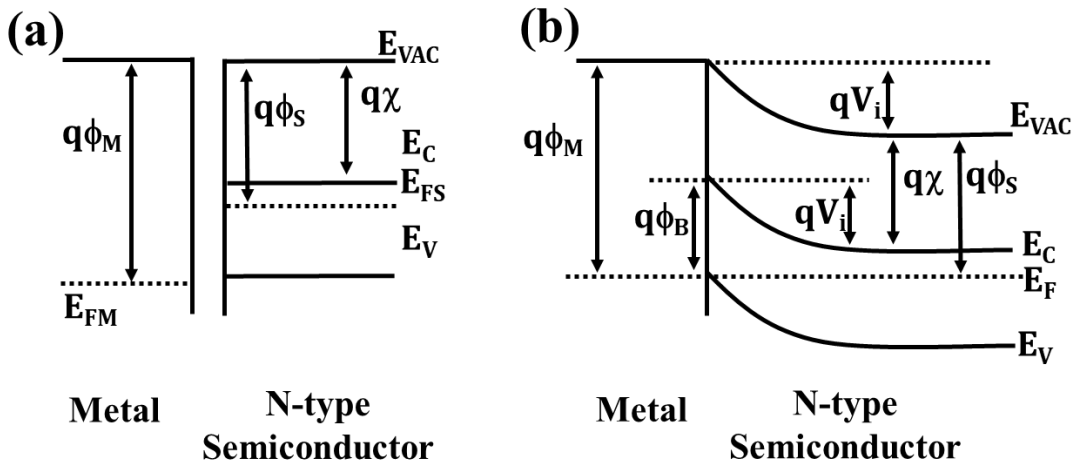


**Figure 10: Schematic of the energy band diagram of metal and n-type semiconductor (a) before and (b) after making contact.**

On the semiconductor side, the potential barrier formed is given by the difference of the metal work function and semiconductor work function:

$$qV_i = q\phi_M - q\phi_S \quad (4)$$

On the metal side, the built-in potential barrier formed is known as Schottky barrier height (SBH) and it is given by:

$$q\phi_B = q\phi_M - q\chi \quad (5)$$

This barrier leads to a rectifying behavior as the current flows only from one side to the other. When a positive voltage bias is applied to the metal the potential barrier is reduced for the electrons in semiconductor but not for the electrons in metal, thus increasing the electron current flow from the semiconductor to the metal. When a negative voltage is applied the potential barrier is reduced, decreasing the current flow from semiconductor to the metal. The SBH does not change in both cases. The electron current flow from the metal to the semiconductor remains unchanged leading to a rectifying non-linear current–voltage behavior.[133] Similar behavior applies to p-type semiconductors, where holes are the majority carriers.[134]

An additional problem is related to the Fermi-level pinning at the metal contact. A study by Das et. al.[135] showed that the Schottky barriers between metals and $MoS_2$ are not consistent with the energy difference between the metal work function and the TMD Fermi level. They showed that even metals which would be expected to act as p-type contacts (i.e. Ni and Pt) instead exhibited electron injection consistent with n-type contacts. Due to this effect the SBH is independent on the metal work function, and it is dependent on the Schottky pinning factor S:

$$q\phi_B = S(q\phi_M - q\phi_{CNL}) + (q\phi_{CNL} - q\chi) \quad (6)$$

Where $\phi_{CNL}$ is the charge neutrality level with respect of the vacuum level and S is equal to:

$$S = d\phi_B / d\phi_M \quad (7)$$

The value S is equal to 1 for an unpinned interface (the SBH value is the same between Equation 5 and 6), and it tends to 0 when the interface is pinned. There are two principle models to explain Fermi-level pinning: Metal Induced Gap States (MIGS) and defect states.[136] In the first case a semiconductor in contact with a metal possess intrinsic states within its bandgap. These states are the MIGS, which are the evanescent states of the metal's travelling wave states that decay in the semiconductor.[137, 138] The charge neutrality level, is the average energy of the dangling bond states. In contrast, it was shown that the Fermi energy on nonpolar (110) surfaces of III-V semiconductors was pinned at the same energy for different metals or oxygen, therefore it was related to intrinsic defect states.[139] In general both effects can cause pinning, and the prevalent one depends on their concentration.[140, 141]

In the case of $MoS_2$ typical S values are between 0.11 and 0.15. The charge neutrality level was evaluated to be 4.57 eV for bulk samples and 4.48 eV for monolayers, so almost thickness independent. In terms of $E_C$-$\phi_{CNL}$ the values are 0.12 and 0.2 eV for bulk and monolayer $MoS_2$ respectively. The Fermi level is therefore pinned close to the conduction band minimum at the metal/$MoS_2$ interface.[142] Due to the high density of defects as introduced before, these effects can be connected with the high density of defects present on the semiconductor surface. A defect density of 0.3%, which is common in TMDs, was shown to be sufficient to dominate the contact behavior.[91, 143] Even if some early studies showed ohmic contacts, these are probably related to the high variation of the material.[30, 144, 145]

Undoubtedly, the contact resistance is a major bottleneck for the implementation of $MoS_2$, or other TMDs, in modern technologies. Although several options to improve the contacts are available there is still a certain variability between similar experiments. Typical routes to reduce the contact resistance or the Fermi Level Pinning relies on interface engineering, doping, annealing or process optimization. In addition, the technique needs to be compatible with semiconductor processing and guarantee a proper device behaviour with minimal SCE. This problem will be further studied in Chapter 3.

### 1.3.3 **Modelling capabilities**

Modelling is one of the few enabling methodologies that can reduce development cycle times and costs. It was estimated in the International Technology Roadmap for Semiconductors (ITRS) Modelling chapter that from 2013 onwards a 40% reduction in development time, and equally a 40 % reduction in development cost can be made from modelling activities.[109, 146] These development time and cost saving figures are based on detailed input on the industrial use of Technology Computer-Aided Design (TCAD) which was compiled by approximately 130 separate entities including semiconductor companies, equipment companies, and some leading research institutes working on process integration.

As will be explained in more detail later in this paragraph, in Chapter 6 and Chapter 8, the aim of this dissertation in this regard is the use of modelling to understand the main limitations of 2D-semiconductors and as well study their transport behavior. Several methods exist to model the behavior of an electronic device and several have been applied for 2D-FETs. These methods can be generally divided into two main approaches: quantum transport and semiclassical transport. The

former is based on the work by Landauer[147] and the Keldysh formalism,[148] while the latter is based on the Boltzmann transport equation (BTE).

The non-equilibrium Green's functions (NEGF) formalism is a quantum transport approach where the open-boundary Schrödinger equation is solved.[149] NEGF can accurately provide the free carrier concentration and the transmission coefficient and has been used on a variety of TMDs and heterostructure devices.[150-153] However, since its formalism is based on the single-particle approach and the mean-field approximation, it is not suitable in case of strongly correlated transport or in the Coulomb blockade regime.[154]

Monte Carlo simulations are instead a semiclassical approach. In this method the transport of free carrier is studied considering their scattering mechanisms when an electric field is applied.[155] This method was applied to 2D-semiconductor devices for the study of transport behavior TMDs, silicene and germanene-based devices[156, 157]. Another semiclassical approach are drift-diffusion simulations, which is the most used approximation to model transport in traditional semiconductors. It is derived for BTE under the relaxation time approximation, resulting in independent expressions for the electron and hole current. The continuity equation needs to be solved as well.[158, 159] Lastly, the hydrodynamic model considers in addition to the drift-diffusion model heating effects.

The main difference of these methods is related to the accuracy and computational effort. Although NEGF and Monte Carlo simulations can guarantee a very high accuracy, their computational demand is high, especially if compared with drift-diffusion or hydrodynamic models. These are in turn characterized by lower accuracy since they cannot completely capture quantum confinement effects and ballistic transport, for example.[154] Nonetheless, drift-diffusion models are still being

used to study the behavior of a variety of FET devices at scaled dimensions for advanced nodes.[160-162] It was shown that the effect from quantum confinement or ballistic transport can be implemented in the drift-diffusion model considering the results from more advanced calculations (Monte Carlo, density functional theory, empirical pseudo potential method). In this way, the computational efficiency of the drift-diffusion as well as the accuracy of more advanced calculation is maintained.[160]

Therefore, although opportune tuning from a variety of sources is necessary, drift-diffusion modelling is still a viable option to have an initial understanding of the main advantages and limitations of 2D-semiconductors.

In this dissertation, the drift-diffusion model is considered using the TCAD software Synopsys Sentaurus Device.[146] This is a continuum physics-based modelling software and it solves systems of equations that describe the physics of the semiconductor. The simulations depend on the solutions of Poisson and drift-diffusion equations. In these simulations, a device is represented by a 2D or 3D meshed finite-element structure. For each node each equation is self-consistently solved. In particular, the solution of the Poisson equation is the electrostatic potential:

$$\nabla^2\phi = -q(p - n + N_D - N_A) - \rho_{trap} \tag{8}$$

Where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the electron and hole densities, $N_D$ is the concentration of ionized donors, $N_A$ is the concentration of ionized acceptors and $\rho_{trap}$ is the charge density contributed by traps and fixed charges. The electron and hole densities can be computed from the electron and quasi-Fermi potentials, and vice-versa. As will be detailed in Chapter 6, Fermi statistics will be used for electron and holes:

$$n = N_C F_{1/2}\left(\frac{E_{F,n} - E_C}{kT}\right) \qquad p = N_V F_{1/2}\left(\frac{E_V - E_{F,p}}{kT}\right) \tag{9}$$

Where $N_C$ and $N_V$ are the effective density of states for the conduction and valence band, $E_{F,n}=-q\Phi_n$ and $E_{F,p}=-q\Phi_p$ are the quasi-Fermi energies for electron and holes respectively, $E_C$ and $E_V$ are the conduction and valence band edges, $F_{1/2}$ is the Fermi integral of order 1/2.[163] Lastly, the carrier transport is evaluated through the drift-diffusion model:

$$\begin{aligned}\vec{J}_n &= \mu_n\left(n\nabla E_C - 1.5nkT\nabla \ln m_n\right) + D_n\left(\nabla n - n\nabla \ln \gamma_n\right)\\ \vec{J}_p &= \mu_p\left(p\nabla E_V + 1.5pkT\nabla \ln m_p\right) - D_p\left(\nabla p - p\nabla \ln \gamma_p\right)\end{aligned} \tag{10}$$

where:

$$\gamma_n = \frac{n}{N_C}\exp\left(\frac{E_{F,n} - E_C}{kT}\right) \gamma_p = \frac{p}{N_V}\exp\left(\frac{E_V - E_{F,p}}{kT}\right) \tag{11}$$

The first term in Equation 10 considers the contribution due to spatial variations of the electrostatic potential, the electron affinity and the bandgap. The remaining terms consider the spatial variation of the effective masses of electrons ($m_n$) and holes ($m_p$) and the contribution due to gradient of the electron and hole concentrations through the diffusion coefficient $D_n$ for electrons and $D_p$ for holes.[163, 164]

In addition, to properly simulate a device any TCAD software require a so-called “parameter file” of the materials under consideration. This file contains the basic material parameters that are necessary for the software to evaluate the behavior of the material (Table 2). In the case of $MoS_2$, or any other new semiconductor, these parameter files are not yet present. Therefore, it was necessary to implement them

considering previous ab-initio calculations and experimental results. Table 1a summarizes the main parameters. This kind of work is similar to what was done before to develop models for Si and Ge, which are now widely used and extremely important in the integrated circuit community to analyze materials and device architecture at advanced technology nodes.[165] For the case of 2D-semiconductors it is necessary to manually add them, as a properly formulated model for $MoS_2$ or any other TMD is not yet available. Because of the high number of parameters and data required, TCAD models for new material systems are usually missing in the first years, and they take some time to be developed and tuned properly. Therefore, most of the initial work relies only on experimental results.

**Table 2: Main parameters modified in Sentaurus device to introduce $MoS_2$.**

| Material parameters | Note | Thickness dependency |
|---|---|---|
| Bandgap | Ab-initio | ✓ |
| Electron Affinity | Experiment | ✓ |
| Effective mass | Ab-initio | ✓ |
| Dielectric | Experiments and ab-initio | ✓ |
| DOS | Ab-initio | ✗ |

Although experimental results are invaluable, the methodology used in this Thesis is slightly different.[154, 166] This is depicted schematically in Figure 11. Instead of using only the experimental data to study the material and electrical properties of 2D-semiconductors, the experimental results are fed-back into the simulator, previously tuned considering first-principle calculations from literature. In this way, not only the TCAD model will be closer to reality as it was tuned against experimental

data, but it is also possible to have insight into physics that would be otherwise inaccessible experimentally.

In order to have a TCAD model closer to experiment not only it is necessary to adjust basic material parameters, but it is also necessary to add the defects that are at the base of the experimental behavior. In particular, Table 3 shows the main defects or imperfections introduced in Sentaurus device in order to study the experimental devices. Through a careful tuning and introduction of several defects, not only is possible to emulate more correctly the experimental results, but it is also possible to understand the main problems of the device itself. This added knowledge can be useful for a more careful planning of future experiments.

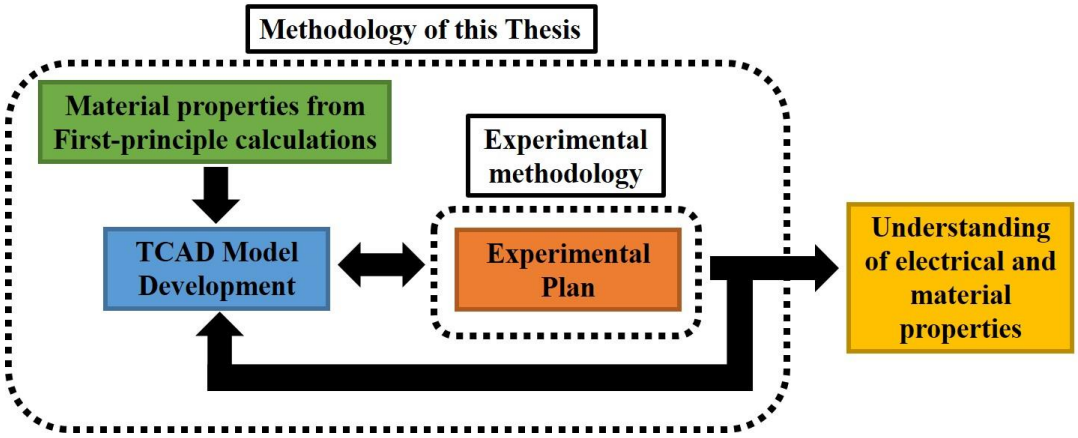


**Figure 11: Schematic of the methodology used in this thesis in order to develop a TCAD model for $MoS_2$ based on both first-principle calculations and experimental data.**

For example, as will be introduced in Chapter 6 in more detail, thanks to the TCAD model it was possible to confirm that it is the high impurity concentration in $MoS_2$ which is the major scattering mechanism, limiting the maximum achievable carrier mobility. As well, considering capacitance-voltage measurements on top-gated $MoS_2$, it was possible to pin-point the energy level responsible for the dispersion in

CV response. This energy level is consistent with the one on Sulphur vacancies, most common defect in exfoliated $MoS_2$ as introduced in the previous paragraph.

A similar methodology was rarely but effectively used in other works related to $MoS_2$. For example, a combination of experimental results and TCAD analysis was used described the charge capture and emission processes in gate oxide trap which were causing hysteresis in monolayer $MoS_2$ back-gated FET.[167] Another study focused on the carrier injection at the metal/$MoS_2$ interface and opportune steps to reduce contact resistance.[168] These works along with a deeper insight on the use of the software will be studied in Chapter 6.

**Table 3: Main models and defect modified in Sentaurus device for a better modelling and understanding of $MoS_2$-based devices.**

| Models considered to study TMD-based devices |
|---|
| Interface traps |
| Impurities |
| Mobility |
| Schottky barrier and FLP |

## 1.4 THESIS STRUCTURE

This dissertation addresses different issue of 2D-semiconductors considering from both a material and an electrical characterization perspective.

Chapter 2 provides a systematic study of the air sensitivity of different TMDs. In particular, $HfSe_2$, the most reactive, is further studied by a combination of several techniques in order to elucidate the degradation mechanism.

Chapter 3 deals with the optimization of contact resistance of $MoS_2$ devices by employing highly doped samples. The data are compared with a short literature review on contact optimization for TMD devices. In addition, the data are used in conjunction with the TCAD model developed for $MoS_2$ in order to study the optimal device structure for ultimate device scaling.

In Chapter 4 a combination of experimental results on thin $MoS_2$ are combined with fitting from DFT calculations to study the impact of impurities on the carrier mobility. The data consider different thickness, doping and substrates of $MoS_2$.

Chapter 5 introduces the electrical and material characterization of a different TMD, $PtSe_2$. Due to the ability of growing this material over a large area, a systematic material and electrical study is carried out in order to elucidate the effect of annealing on the metal-$PtSe_2$ interface.

Chapter 6 summarizes the development of the TCAD model. The first part deals with the setup of all the necessary material parameters and tuning of the basic models. Then, mobility models are opportunely tuned in order to match previous theoretical and experimental results. This model is then used to elucidate experimental results, focusing on contact and interface traps.

In Chapter 7, the software is used to introduce the layered structure concept, in order to further improve the modelling and understanding of 2D-semiconductors. The model is tuned against experimental data and used to study the scaling behaviour of $MoS_2$-based FETs.

Finally, Chapter 8 summarizes the major result of this study and discusses possible future works that can help to expand the understanding of 2D-semiconductors.

# Chapter 2: AIR SENSITIVITY OF TMDS

This chapter is adapted from the following publication:

**Mirabelli, G.**; McGeough, C.; Schmidt, M.; McCarthy, E. K.; Monaghan, S.; Povey, I. M.; McCarthy, M.; Gity, F.; Nagle, R.; Hughes, G.; Cafolla, A.; Hurley, P. K.; Duffy, R., Air sensitivity of $MoS_2$, $MoSe_2$, $MoTe_2$, $HfS_2$, and $HfSe_2$. Journal of Applied Physics 2016, 120 (12), 125102.

## 2.1 INTRODUCTION

In this chapter a systematic study of several TMDs have been carried out to study their reactivity in air. The sensitivity of a material system to ambient degradation can pose significant challenges in their use for electronics applications. First, an AFM study over a period of 27 days was carried out to understand the main differences between each TMD. The study considered the following TMDs: $MoS_2$, $MoSe_2$ and $MoTe_2$ to explore the 3 dichalcogenides of molybdenum. The study also considered $HfS_2$ and $HfSe_2$ which are also of interest as they have energy gaps of 0.9eV and around 2 eV, in the range of interest for logic devices. SEM analysis is used to corroborate the findings of the AFM studies. The most reactive TMD, $HfSe_2$, was studied by XRD to provide a quantitative insight on the reactions of the material. XPS measurements were used to determine the surface chemical composition and to investigate changes in the chemical state of the surface with ambient exposure. By observing the binding energy shifts and broadening of the core level peaks the extent of surface oxidation can be inferred. Finally, TEM cross-sections and EDX analysis give a better understanding of the structure of the surface features.

## 2.2 EXPERIMENTAL

For each of the 5 TMD's studied ($MoS_2$, $MoSe_2$, $MoTe_2$, $HfS_2$, $HfSe_2$) flakes were mechanically exfoliated from their bulk crystal counterpart with Scotch tape[11] and transferred to a substrate composed of 85 nm of $SiO_2$ on a highly-doped Si handle wafer. Immediately after the exfoliation, the samples were examined by AFM for an initial comparison of the materials under study. No methods were applied to clean the TMD surface. The AFM was operated in Tapping-Mode in order to avoid any alteration of the surface due to the contact between the AFM tip and the surface itself.

For each sample, every effort was made to repeatedly measure the same flake at approximately the same location, over an area of 5×5 $\mu m^2$. In the AFM study, the same analysis was systematically carried out periodically on each material over a 27-day period. Root-mean-square (RMS) roughness evolution of the surfaces was used to compare and understand the main differences between the TMDs studied, considering both a change of the metal (Mo or Hf) and/or a change of the chalcogen element (S, Se or Te).

The morphologies of the TMD sample surfaces were investigated using a FEI Quanta 650 SEM in high-vacuum. To improve the imaging gold was sputtered on the samples using an Agar sputter-coater. For structural analysis, cross-section samples were obtained by using the Dual Beam Helios Nanolab 600i system from FEI, using a Ga ion beam. Layers of protective material were used consisting of electron beam deposited C, Pt, and ion beam deposited C. Lamellas were thinned and polished at 30 kV 100 pA and 5 kV 47 pA, respectively. Cross-sectional Transmission Electron Microscopy (XTEM) imaging was carried out using a JEOL 2100 HRTEM operated at 200 kV in bright field mode using a Gatan Double Tilt holder. EDX analysis was performed using STEM-EDX on a FEI Titan 80-300kV S/TEM. Analytical STEM provides a sub-nanometre, high current probe (~0.5 nm, 0.56 nA) allowing for site specific EDX analysis on the nanometre scale.

For the XPS analysis flakes were mounted and held on an XPS sample holder using an adhesive carbon pad. Flakes were then cleaved using the Scotch tape method and placed into a vacuum chamber in less than 30 seconds to minimise atmospheric contamination for the base, freshly cleaved, measurement. Once the freshly cleaved flake was measured the sample was removed and exposed to ambient atmospheric conditions for a period of 1 hour and reloaded for XPS measurement. The process of

exposing the sample was repeated for a 3 hour and a 48-hour exposure. Following the 48-hour measurement the flake was re-cleaved using Scotch tape. For $HfSe_2$ the XPS spectra were taken of the Hf 4f and the Se 3d core level peaks following the different exposure times to observe how the peaks shapes change and more importantly the relationship of the ratio of the area under each peak which directly reflects the relative concentrations of the elements present within the XPS sampling depth which is typically 5-7 nm. The XPS system used an aluminium anode to generate X-ray photons of 1486 eV and had an operating base pressure of approximately $2.0\times10^{-9}$ mbar with the analysis area of the order of 0.5 $cm^2$.

## 2.3 SURFACE AND CROSS-SECTIONAL ANALYSIS

Right after exfoliation none of the materials showed obvious signs of degradation. Figure 1a and 1b are representative AFM images of $MoS_2$ and $HfSe_2$ surfaces 24 hours after exfoliation. These two materials were the most stable and least stable extremes respectively, among the TMDs studied. Twenty-four hours after exfoliation, $HfSe_2$ showed signs of degradation. Its surface, as shown in Figure 1b, is characterised by several protrusions randomly located across the surface, reaching a height of 57.4 nm high after 1 day. This behavior is in clear contrast with the one of $MoS_2$. The 2D AFM image in Figure 1a shows a darker z-shaped region. A cross-sections analysis shows this feature to be ~0.65 nm deep, which suggests a missing single-layer of $MoS_2$, which is known to be ~0.65 nm thick. This slight non-uniformity of the top surface might be related to the mechanical exfoliation method, which does not always guarantee a uniform surface over a large area. The same feature was located in later AFM measurements and there were no signs of any deterioration. Therefore, the material is relatively stable upon air exposure.

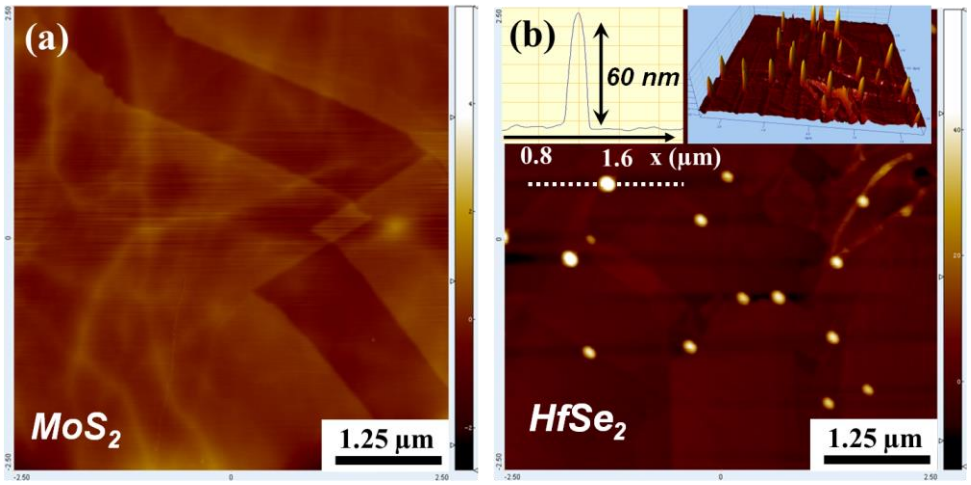


**Figure 1: (a) Representative $MoS_2$ AFM image taken 24 hours after exfoliation. (b) Representative $HfSe_2$ AFM image taken 24 hours after exfoliation. The insets show cross-section of the tallest protrusion found on $HfSe_2$ of approximately 60 nm (white line scan in the main Figure), and a 3D representation of the data.**

The main results of the AFM study can be summarised by the RMS roughness trends of the surfaces shown in Figure 2, for both the Mo-based and Hf-based TMDs. As previously stated, the $MoS_2$ is the most stable and it is the only TMD that did not show any obvious visible features or surface change during the period of study, implying that it is the most suitable TMD for electronic applications from a material point of view. The RMS roughness values for $MoS_2$ are relatively and constant (~0.2-0.4 nm) throughout the 27 days. $MoSe_2$ showed one peak related to air exposure, similar to those found on $HfSe_2$ surface, of ~27 nm height on the 9$^{th}$ day after exfoliation. Subsequently, on the 27$^{th}$ day, the surface was quite degraded, but without any other tall protrusions. $MoTe_2$ surface features were detectable after 3 days and were spread almost uniformly across the surface. These studies indicate a general trend in decreasing ambient stability for a given metal in the TMD as the chalcogen element changes from S to Se and finally Te. For example, from Figure 2(a) it is seen that the RMS roughness of $HfS_2$ is significantly lower than that of $HfSe_2$ during the period

studied. The degradation of $HfSe_2$ is visible 1 day after exfoliation, while signs of degradation are only visible 9 days after exfoliation for $HfS_2$.

Some variation is noted in the RMS data shown in Figure 2 which may be attributed to a number of factors; while it was attempted to return to the exact same 5 µm × 5 µm area on each flake, there may have been some misalignment due to handling or variation caused by changing AFM tip over the period of study. Furthermore, for the $HfSe_2$ it was noted that some of the surface features disappeared from one measurement to the next, which may indicate that these features are not tightly bound to the surface. Despite this "noise" in the data in Figure 2, the overall

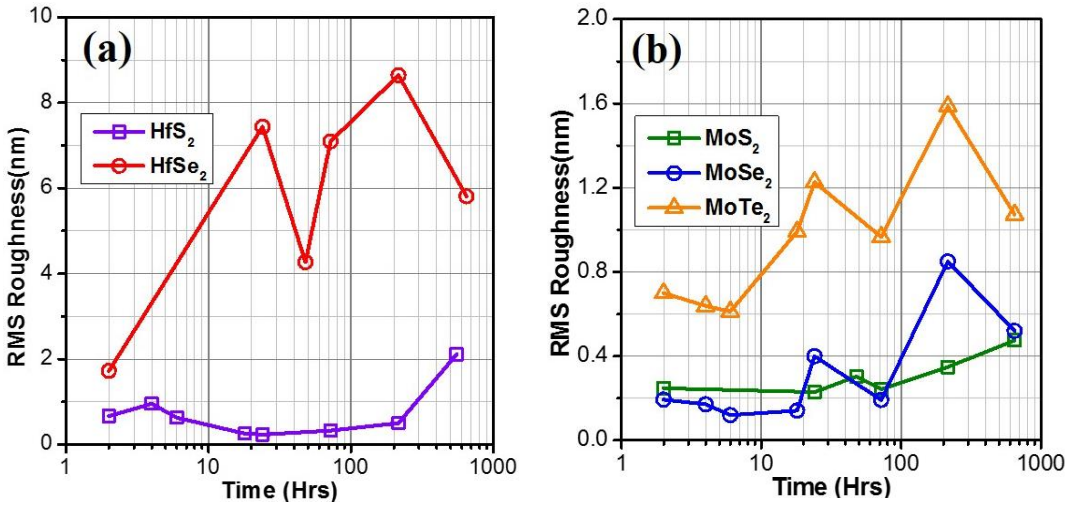


**Figure 2: RMS surface roughness trends for (a) Hf-based and (b) Mo-based TMDs. Note the difference in the y-axis scales.**

trends observed are reliable, namely a general surface roughening with time, with observable differences between the five TMDs under study.

To emphasize the quick degradation of $HfSe_2$, Figure 3a reports the height of the tallest blister found during each AFM measurement, along with the defect density. The blister height is steadily increasing with time, going from ≅60 nm after 1 day to ≅100 nm after 27 days. On the contrary the defect density seems to decrease with time.

Nevertheless, this is likely related to a non-uniform distribution of the blisters and the fact that they coalesce together with time, as it will be clearer later from SEM images. In support of this Figure 3b shows an optical picture of a freshly exfoliated $HfSe_2$. In contrast, Figure 3c shows the same flake after 4 months. Clearly the degradation affects the overall surface of the flake.

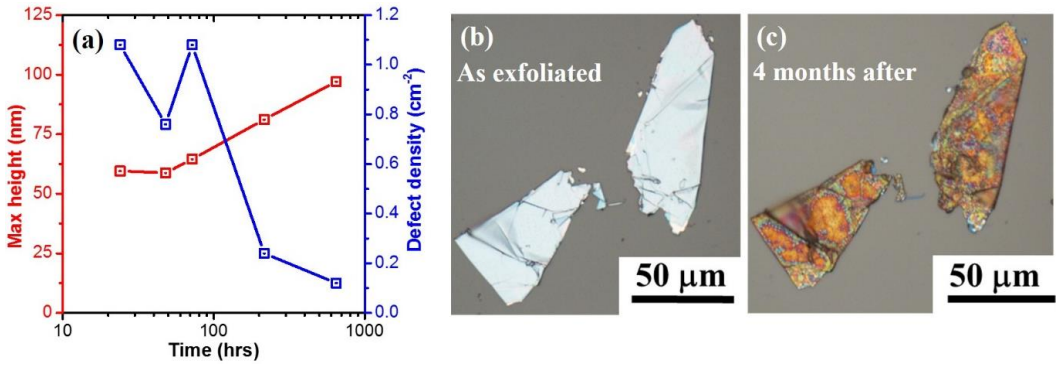


**Figure 3: (a) Maximum height of the blister and defect density found for $HfSe_2$. Optical pictures of $HfSe_2$ (b) as exfoliated and (c) 4 months after.**

In order to analyse the results of the AFM study more thoroughly, all TMDs were examined by SEM, and $HfSe_2$ was further studied by STEM, XTEM, EDX, and XPS, since it showed the highest reactivity on contact with air.

Figure 4a shows an SEM measurement of the $HfSe_2$ surface 1 day from exfoliation. The blisters are found primarily along step edges, even if some are found on the planar surface as well. The inset in Figure 4a show a flake five months after exfoliation. Considering the two images, they show the same kind of blister like protrusions in terms of form and shape, only smaller in fresher samples. Furthermore, it is clear from the images that the blisters have a higher density at the step-edges. The step-edges of the top-surface, related to the mechanical exfoliation method, are characterised by dangling bonds that may be optimal nucleation sites for the growth of the features. Nevertheless, Figure 4b show $HfSe_2$ five months from exfoliation on

a much bigger scale. Even if the protrusions might preferentially growth initial along the step edges, after a certain amount of time the whole surface is degraded, as seen before from optical pictures in Figure 3c.

Also, it is important to compare the density of protrusions found during the AFM study. The blister density in the AFM image in Figure 2, is approximately $8\times10^{7}$ $cm^{-2}$, while the SEM image in the inset of Figure 5a has a blister density of approximately $4.3\times10^{7}$ $cm^{-2}$. The difference in defect density is attributed to the fact that a different area was scanned in AFM and SEM. Note, the same type of terrace edges were found on $MoS_2$ (Figure 1a), but they were not decorated with growths of blister-like features during the period of study. Other TMDs were studied by SEM in a similar way, but no obvious surface features were observed. For example, the inset in Figure 4b shows the $HfS_2$ surface after 5 months of air exposure. The terraced nature of the material is obvious and is related to the layered structure of the material itself, and the mechanical exfoliation process. The surface appears to be uniform with no blisters present, at least under this magnification. A similar lack of obvious surface features was characteristic in the SEM images of $MoS_2$, $MoSe_2$, and $MoTe_2$.

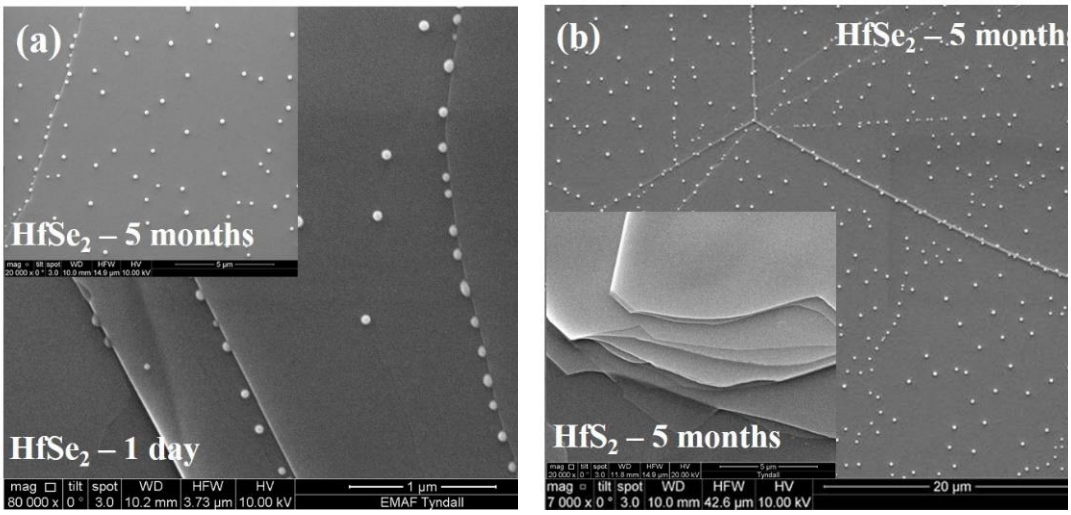


**Figure 4: (a) Representative SEM image of $HfSe_2$ after 1 day from exfoliation; the inset shows the surface 5 months from exfoliation. (b) Representative image of $HfSe_2$, which shows how the whole surface is contaminated with blisters. The inset show $HfS_2$ after 5 months from exfoliation. The terracing is related to the mechanical exfoliation and the layered nature of the material. No blister features appear to be evident.**

A similar comparison was done considering TEM cross-sections of $MoS_2$, $MoTe_2$ and $HfSe_2$ as exfoliated (day 0) and after 30 days from exfoliation. These group of TMDs comprise the best and the worst of the whole group considered before ($MoS_2$ and $HfSe_2$), and the best and worst of the Mo-based TMD group ($MoS_2$ and $MoTe_2$). Figure 5a and 5d show the $HfSe_2$ cross-section at day 0 and 30 respectively. An initial oxidation layer can be clearly seen in Figure 5a, with a complete degradation of the surface after 30 days. In sharp contrast, $MoS_2$ on day 0 (Figure 5c) shows a very sharp interface from the top layer and the C-layer used as protection layer. Similarly, after 30 days (Figure 5d), there are no sign of apparent degradation, and the layered structure is clearly visible throughout the whole lamella (~10 µm). Comparably, $MoTe_2$ did not show any surface imperfections as exfoliated (Figure 5e). After 30 days (Figure 5f), the surface does not show any sign of reaction from this analysis. Interestingly, both the $MoS_2$ and $MoTe_2$ crystals exposed in air for 30 days show sign of what seems to be stress. Nonetheless, it is difficult to conclude that this effect is

strictly related to air exposure. The fabrication process steps used to prepare the lamella might have induced stress in the structure as well.

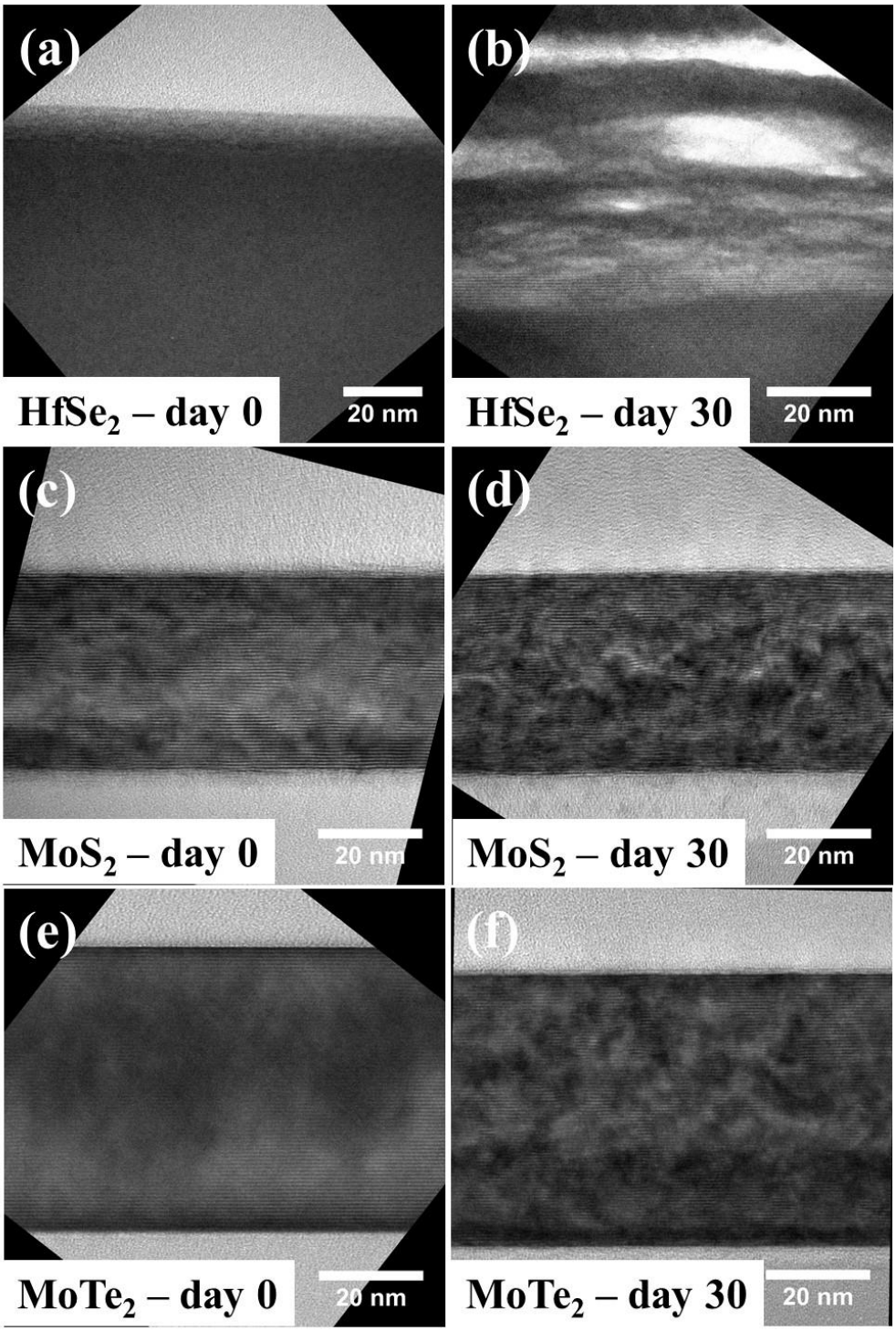


**Figure 5: Cross-section TEM of $HfSe_2$, $MoS_2$ and $MoTe_2$ as exfoliated (a, c, e) and after 30 days (b, d, f) respectively.**

Additionally, EDX analysis was used to study the chemical composition of the blisters found on $HfSe_2$. Figure 6 shows representative TEM images of $HfSe_2$ after 5 months of air exposure. In the following Figures (Figure 6-8) the surface features look like hemispherical shaped blisters which are approximately 180-240 nm tall and 420-540 nm wide. Figure 6a shows a $HfSe_2$ flake approximately 280 nm thick, while Figure 6b shows a thinner flake, approximately 40 nm thick. Blisters appear on both thick and thin flakes with approximately the same dimensional size. The material within the blister appears to be amorphous in nature. Also, they are surface features, as they are not formed throughout the bulk of the material. As it is clear from Figure 6a, the surface region of the $HfSe_2$ beneath the blister is highly disordered. Also the top surface of the $HfSe_2$, between the blisters, appears to be degraded as it is non-uniform and less homogeneous than the bulk portion of the flake. Thus, the surface reactions resulting from ambient exposure of $HfSe_2$ could be considered to consist of two distinct features, namely localised blisters and planar surface modification. A delamination crack is evident in the same figure within the $HfSe_2$, highlighting that these TMDs are layered materials that may have mechanical weaknesses between the layers. It should be noted that the crack is likely to have occurred during TEM sample preparation.

In terms of area coverage, assuming a circular blister with average width of 480 nm, and a density of $4.3\times10^{7}$ $cm^{-2}$, the area covered by these features is approximately 8% of the $HfSe_2$ surface.

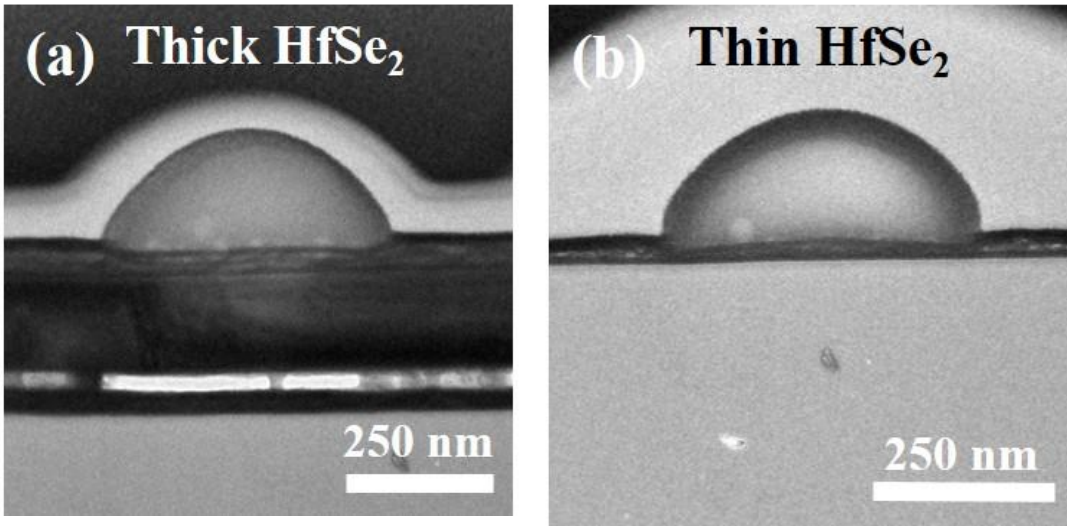


**Figure 6: Representative TEM images of $HfSe_2$ after 5 months from exfoliation. Hemispherical shaped surface features appear amorphous in nature and are of similar dimensional size on both the (a) thick and (b) thin flakes.**

Figure 7 provides extra insight into the structural makeup of the blisters, as the thinner flake, seen in Figure 6b was examined further. A surface blister was magnified, and initially appeared homogeneous. However prolonged electron irradiation over several minutes, a void appeared in the middle of the feature (Figure 7b). The void is likely formed by beam induced knock-on damage causing a small void to appear and proliferate to a large hole. It may be coupled with beam induced heating causing a melting type effect. This may indicate that the middle of these features are structurally less stable, much like a bubble. Also note that the Au, deposited to enable the SEM imaging as indicated earlier, is visible on the outer surfaces of these features.

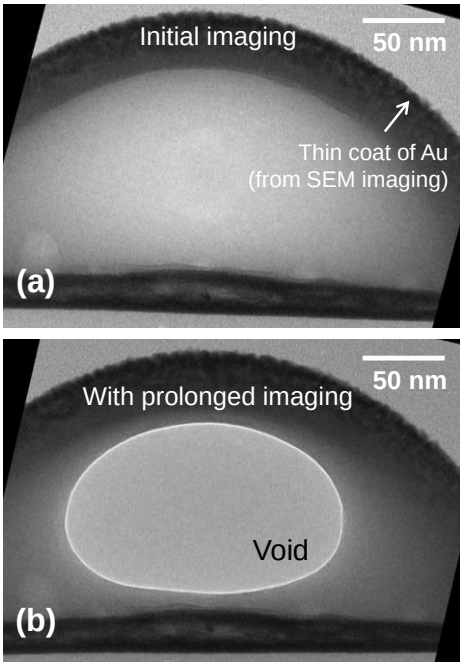


**Figure 7: TEM imaging of the blisters on the thin $HfSe_2$ flake shows that (a) during initial imaging the blister is continuous and that (b) after a few minutes of electron irradiation a void is formed in the middle.**

## 2.4 EDX AND XPS ANALYSIS

Figure 8 shows compositional analysis performed on the surface blisters via STEM based EDX. Figure 8(a) shows a STEM image across which the EDX analysis was performed. In the STEM image the contrast is reversed compared to bright field TEM. The structural non-uniformity is again evident in regions below the blister, and to the left and right of it. Figure 8b and 8c show the EDX maps for Hf and Se respectively recorded across the STEM image in shown in Figure 8a. Notice that the blister is primarily composed of Se, with only trace amounts of Hf. There are patches within the $HfSe_2$ layer that show increased concentrations of Hf accompanied by a Se deficit in the same region. These Hf/Se concentration changes are only present at the top of the layer. The bulk region of the $HfSe_2$ is uniform.

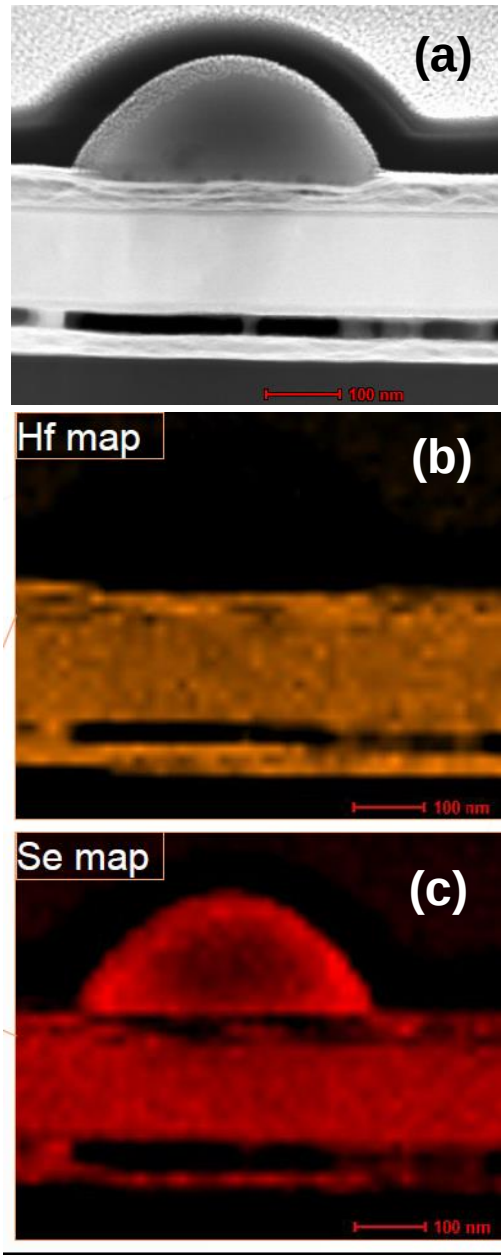


**Figure 8: EDX data showing (a) the region mapped, (b) the Hf map, and (c) the Se map within the $HfSe_2$ flake and surface blister. The blister is Se-rich with little or no Hf present. The regions below the blister are depleted of Se.**

The XPS study data for $HfSe_2$ as a function of ambient exposure are displayed in Figure 9-12. The change in the elemental stoichiometry with ambient exposure time is displayed in Figure 9 and clearly shows the progressive loss of Se from within the XPS sampling depth (5-7 nm) over the 48 hr monitoring period with the Se:Hf ratio reducing from the initial 2:1 to 1.4:1. Note a similar study on $MoS_2$ showed no changes

in the elemental composition under an equivalent ambient exposure again confirming relative surface stability.

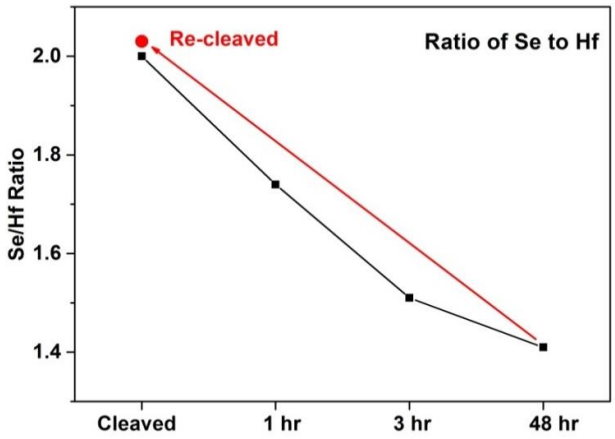


**Figure 9: Plot of the change in Se/Hf elemental ratio following ambient exposure of the freshly cleaved surface. The re-cleaving process restores the surface to the original elemental composition by removal of the oxidised surface.**

Analysis of the changes in the profile of the Hf 4f peak over the time span of this ambient exposure study shown in Figure 10 indicates increasing evidence for Hf oxidation. The Hf 4f peaks from a freshly cleaved sample in Figure10(a) have a binding energy of 14.3 eV and 16 eV for the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ component peaks respectively,[169] which are indicative of a Hf signal in the $HfSe_2$ crystal. The appearance and subsequent increase in intensity of component peaks, at binding energies of 15.4 eV and 17.1 eV in Figure 10 (b, c, and d), are indicative of the progressive oxidation of the Hf as the higher electronegativity of oxygen compared to selenium results in this core level shift.[170] The corresponding curve fitted Se 3d spectra,[171] displayed in Figure 11 show a broadening of the peak profile without any evidence of higher Se oxidation states.

This can be interpreted in terms of the preferential formation of Hf oxides following ambient exposure with the consequential release of Se, some of which

desorbs from the surface and some of which gets trapped in the blister structures. The fact that these blisters are predominantly found along step edges is consistent with the Hf oxidation process initiating along the step edges where ideal surface termination is absent.

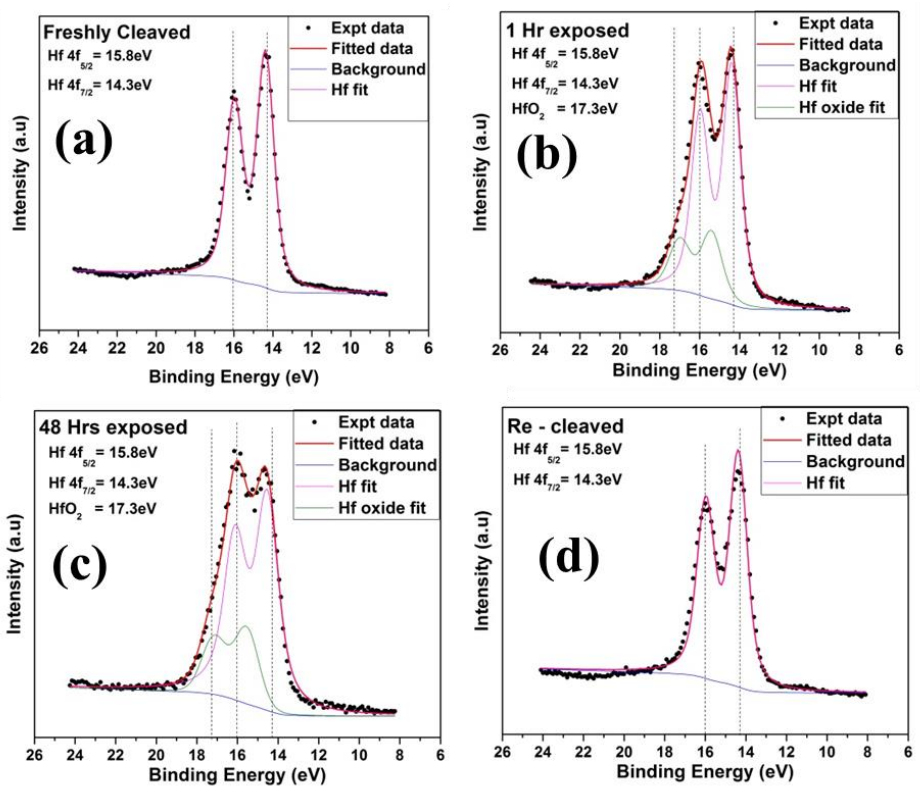


**Figure 10: Hf 4f peaks; (a) Freshly cleaved $HfSe_2$ surface shows the Hf $4f_{5/2}$ and Hf $4f_{7/2}$ component peaks at binding energies of 14.3 eV and 16 eV, respectively. The peak profiles following ambient exposure of 1 hr (b) and 48 hrs (c) clearly display the growth of higher binding energy oxide component peaks at 15.4 eV and 17.1 eV. The unoxidised Hf signal is regained after re-cleaving of the top surface (d), removing the surface oxide.**

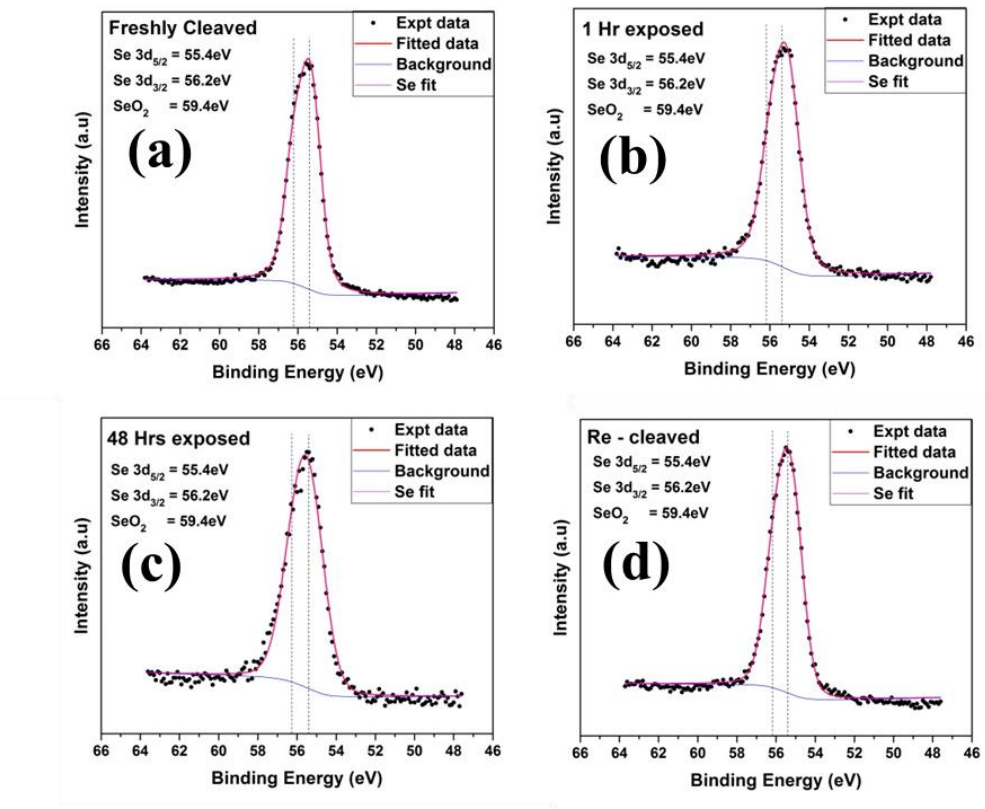


**Figure 11: Se 3d peaks; (a) Freshly cleaved Se3d peak is curve fitted with an unresolved doublet with binding energy of Se 3d5/2=55.4 eV and Se 3d3/ = 56.4eV. Curve fits of the 1 hr (b) and 48 Hrs (c) air exposed samples show no significant change to the peak profile with no evidence of higher oxidation states of selenium (e.g. $SeO_2$ which has a binding energy of 59.4eV). Recleaving the sample as shown in (d) leaves the peak profile unchanged.**

Further evidence for the preferential oxidation of Hf over Se comes from the binding energy and FWHM of the O1s peaks. In Figure 12, the FWHM of the 48 hrs exposed sample is 2.9 eV at 530.9 eV binding energy in agreement with Zhu et al.[172] who reports a $HfO_2$ peak on a Si substrate to have a FWHM of 2.6 eV at a binding energy of 530.8 eV. Combined with the lack of evidence for $SeO_2$ in the Se3d spectra it can be concluded that the oxide is due to $HfO_2$.

Considering the surface area contributing to the XPS spectra is of the order of 0.5 $cm^2$, it is reasonable to conclude that the photoemission spectra are dominated by the areas between the blisters, which remain largely unchanged, as the surface coverage of these feature was estimated to be approximately 8%.

A remaining question is why the Se atoms produced by the preferential Hf oxidation coalesce into hemispherical features, as opposed to aligning parallel to the surface. The presence of a hemispherical shape suggests a construction to minimise surface tension. One possible explanation is that, as a result of the high temperature vapour phase growth process for the $HfSe_2$, gases are trapped between the 2D layers of the crystal, and the surface features contain a gas.

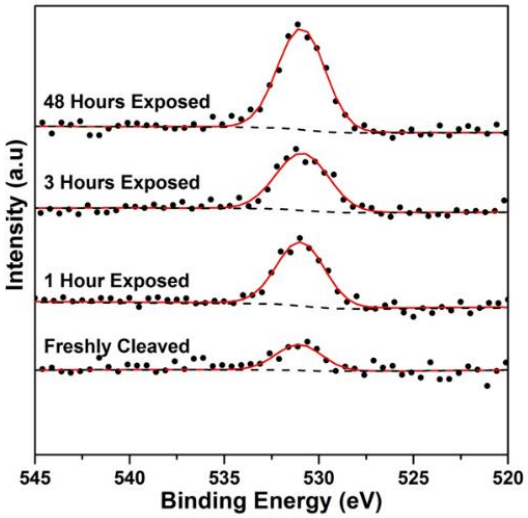


**Figure 12: The O1s core level spectra as a function of exposure time.**

## 2.5 DISCUSSION

Even though $HfSe_2$ was the most reactive among the TMDs studied here, $HfSe_2$-based FETs are currently found and studied in literature, with $I_{on}$-$I_{off}$ ratio exceeding $7.5\times10^6$ reported by Kang et al.[173] These devices were quickly passivated with resist, which can limit the effects of surface deterioration due to air exposure. The AFM images reported in that work of un-passivated $HfSe_2$ surface 1 and 8 days after exfoliation, show similar features to those presented in Figure 1b.

Also, a study of air exposure stability of $HfSe_2$ films grown by MBE is reported by Yue et al.[55]. The oxidation reactions are reported to be related to the top surface of the film, which is less prone to oxidation when the crystalline quality of the film is improved. A higher quality might also mean fewer discontinuities on the surface, like step-edges, which this study would suggest are the optimal (but not essential) sites for $HfSe_2$ surface degradation. Gao et al.[174] showed that CVD grown monolayers of $MoS_2$ and $WS_2$ were very air sensitive. X-ray photoelectron and Auger electron spectroscopy performed in that work showed that gradual oxidation proceeded along grain boundaries along with the adsorption of organic contaminants. Degradation of CVD $WS_2$ was also reported by He et al.[175]. Similar effects were also seen after a longer period on exfoliated thin flakes of $MoS_2$.[176]

Another promising 2D-material is Black Phosphorus, whose surface shows similar features to that found for $HfSe_2$ here.[177-179] The so-called bubbles grow in density and height after air exposure, regardless of the actual thickness of the Black Phosphorus flake, meaning that these effects are top-surface related. The density of these features on Black Phosphorus eventually decreases with air exposure since they become wider, merging together. In a subsequent study, Kim et al. reported the successful preparation of air stable multilayer phosphorene thin-films and transistors.[180] In that work a double layer capping of $Al_2O_3$ and hydrophobic fluoropolymer was used to produce air stability of the material.

The surface roughness trends observed in our AFM data are in accordance with the DFT calculations carried out by Liu et al.[181]. In that work it was stated that a TMD is more prone to oxidation as the chalcogen is varied from S, to Se, to Te, i.e. descending the periodic table. This can be due to the decrease in the electronegativity of the chalcogen from S to Te, which in turn makes the metal-chalcogen bond being

more susceptible to oxidation. Moreover, that work restricts the interaction between oxygen and TMDs to single chalcogen vacancies. These defects are more likely to occur in more reactive TMDs, so, considering that the S vacancy density for $MoS_2$ is reported to be in the order of $10^{13}$ $cm^{-2}$,[113, 114] the Se vacancy density would be expected to be higher in $HfSe_2$. Considering that defect density related to air exposure in this work is found to be in the order of $10^7$ $cm^{-2}$ from both the AFM and the SEM analysis, it is possible that these kinds of features are not related to chalcogen vacancies alone. These defects could play a role in the overall process,[110, 182] but not all of them appear to be optimal sites for the growth of the blister shaped protrusions.[183] Indeed, for the case of $MoS_2$, DFT calculations have shown that a large kinetic barrier of 1.6 eV is present on a pristine $MoS_2$ surface for $O_2$ dissociation, which result in good stability. The calculated dissociation barrier at the edge sites is only 0.31 eV, making the edges and grain boundaries of $MoS_2$ susceptible to oxidation.[182, 184] In addition, sulphur vacancies at the surface of $MoS_2$ are expected to reduce the oxidation barrier to 0.8eV, which would make them reactive defect sites.[185]

It is clear that some of the TMD materials of interest from a device perspective are remarkably air sensitive.[186, 187] Many other groups have reported material or electrical data indicating this, while the systematic study in this work gives more insight into the relative reactivity of the TMDs and the formation of the surface features. To think that these materials are purely 2D in nature is probably misleading, as this implies that top surface is totally unreactive in the perpendicular plane as there are no available covalent bonds in that plane. Unfortunately, it is not that simple, as it is clear that molecules present in air react with the TMD surfaces. As stated above a surface encapsulation using resists, insulators, or dielectrics have been demonstrated elsewhere as being effective protection layers.

Other solutions may lie in the area of chemical functionalisation or passivation of surfaces. For example one might think of graphene as a perfectly 2D material with no free bonds available for surface reactions or functionalisation, however Long et al. [188] found that graphene bonds non-covalently with alkane-amine groups, providing a pathway for solution-phase self-assembly. Furthermore O'Connell et al. discovered recently that molecular monolayer doping via chemisorption of organic molecules on Si surfaces actually supressed oxidation of the Si surface.[189] In terms of surface protection of TMDs, non-covalent surface reactions or functionalisation may prove important to improving their air stability. Additionally, surface functionalization could potential control the oxidation process of TMDs, which native oxide could be used as top-oxide for FET applications or for the growth of other oxides. On this, Mleczko et al.,[190] evaluated the performance of $HfSe_2$ and $ZrSe_2$ with native high-k dielectrics. Nonetheless, the devices were fabricated in an air-free environment, using nitrogen gloveboxes and vacuum chambers. In addition, 2.5 nm of $AlO_x$ were deposited by low-temperature ALD to act as protective encapsulation layer and as a thin tunnelling barrier for the contact. Therefore, the material itself, even if sensitive, present interesting characteristics and opportunities if the fabrication process is designed correctly. Similarly, FETs were fabricated using $HfS_2$ in a vacuum cluster system combined with a number of gloveboxes to maintain an air-free environment.[191] In this work, even if $HfS_2$ was passivated with BN for passivation, it was not enough to completely suppress ambient degradation effectively. Therefore, it is evident that air contact affects the structural and electrical properties of these TMD materials by various degrees. Tackling this issue can be one of the biggest challenges for future TMD-based devices and technologies.

## 2.6 CONCLUSIONS

In this work we compared and contrasted the reactivity of $MoS_2$, $MoSe_2$, $MoTe_2$, $HfS_2$ and $HfSe_2$ in air. AFM, SEM, EDX, S-TEM, and XPS data were collected. Overall, surface roughening occurs for all TMDs over a period of time which indicates a formation of oxides or molecular adsorption on the surfaces. $HfSe_2$ and $MoTe_2$ were the most reactive of the TMDs studied. $HfSe_2$ in particular was characterised by the growth of Se-rich surface blisters, which form within one day of air exposure. It is theorised that the Hf is oxidising into $HfO_2$, which breaks down the $HfSe_2$ and excludes the Se at the surface. The Se atoms coalesce into blisters which continue to grow as more $HfSe_2$ is consumed and more $HfO_2$ is formed.

# Chapter 3: THE EFFECT OF IMPURITIES AND DIELECTRIC ENVIRONMENT ON 2D-SEMICONDUCTORS

This chapter is adapted from the following publication and conferences:

**Mirabelli, G.**; Gity, F.; Monaghan, S.; Hurley, P. K.; Duffy, R. In Impact of impurities, interface traps and contacts on $MoS_2$ MOSFETs: Modelling and experiments, 2017 47th European Solid-State Device Research Conference (ESSDERC), 11-14 Sept. 2017; 2017; pp 288-291.

**Mirabelli, G.**; Duffy, R.; Hurley, P. K.; Monaghan, S.; Cherkaoui, K.; Schmidt, M.; Sheehan, B.; Povey, I. M.; McCarthy, M.; Nagle, R.; Bell, A., Mo-Based Transition-Metal-Dichalcogenide Junctionless Field-Effect-Transistors. Meeting Abstracts 2016, MA2016-01 (26), 1289-1289.

## 3.1 INTRODUCTION

One of the main problems of 2D-materials is the lack of a proper large-area growth technique. Often, grown TMD films are characterised by defects or grain boundaries, which limit their performances. Therefore, most of the MOSFET results to date showing high on/off ratios, low SS and mobilities in the range of tens of $cm^2V^{-1}s^{-1}$, have come from flakes mechanically exfoliated from bulk crystals. Nevertheless, a large concentration of unintentional impurities was reported in TMD crystals,[90, 192] which is known to affect the behaviour of the material. In this study, we report on the electrical characterisation of back-gated $MoS_2$ flakes in order to study the impact of unintentional impurity concentration and dielectric environment. Overall, the performance of the devices are comparable with literature, with good $I_{on}/I_{off}$ ratio, but still, the unintentional impurities present in the material affect its transport properties masking the maximum potential of $MoS_2$ channel MOSFETs.

## 3.2 EXPERIMENTAL

Mechanical exfoliation with scotch tape was used to obtain thin flakes from a $MoS_2$ bulk crystal. The flakes were transferred on a substrate of 85 nm of $SiO_2$ and a highly-doped Si handle wafer. The height of the flakes was established by optical color-contrast.[193] Ti/Au metal contact pads and electrodes were defined by electron-beam lithography, followed by metal evaporation and a lift off process. The definition of the contact pads and electrodes was achieved using 15 kV beam exposures with a Zeiss SUPRA SEM with a Raith Elephy Plus blanker. The metal consisted of a 5 nm Ti adhesion layer and 45 nm of Au using e-beam evaporation.

For structural analysis, cross-section samples were obtained by using FEI's Dual Beam Helios Nanolab 600i system using Ga ion beam. Three layers of protective

material were used, namely electron beam C, electron beam Pt, and ion beam C. Lamellas were thinned and polished at 30 kV 100 pA and 5 kV 47 pA, respectively. Cross-sectional Transmission Electron Microscopy (XTEM) imaging was carried out using a JEOL 2100 HRTEM operated at 200 kV in Bright Field mode using a Gatan Double Tilt holder. For electrical characterization, the HP4156C parameter analyser was used.

## 3.3 MATERIAL ANALYSIS

In Figure 1 the SEM and TEM images of a typical device are reported. The device is referred to as the Trapezium based on its shape. Figure 1a shows the SEM of the flake. It was contacted by two metal tracks of Ti/Au (5/45 nm), separated by 1 μm. The width is approximately 3.5 μm along the length of the sample. Figure 1b shows the TEM cross section of the same device around the metal contact. There seems to be another 3 layers of $MoS_2$ above the actual flake, but in reality this is probably an artefact from TEM and there can be three explanations. Due to its low thickness, the material is bending in a direction perpendicular to the lamella. The second "top" $MoS_2$ is actually the same flake the bulged up inside the metal contact, so bending effects that happen in deeper regions. Probably thicker devices are less prone to bend under the same effect. Another hypothesis is that this kind of bending might be related to stress induced on the flake after the metal deposition or the lift-off process, as this effect seems to be related to regions around the metal contact (Figure 1d). Lastly, it can be related to the exposure of the $SiO_2$ substrate to the TEM electron-beam. The electron bean causes heating, and an associated expansion of the $SiO_2$ layer. The heat is removed more effectively under the metal contact area, resulting in a differential expansion of the $SiO_2$ inside and outside the metallised area. Considering a region

away from the metal contact in Figure 1c the three layers and thickness of 2 nm, assumed before only by optical inspection, are confirmed.

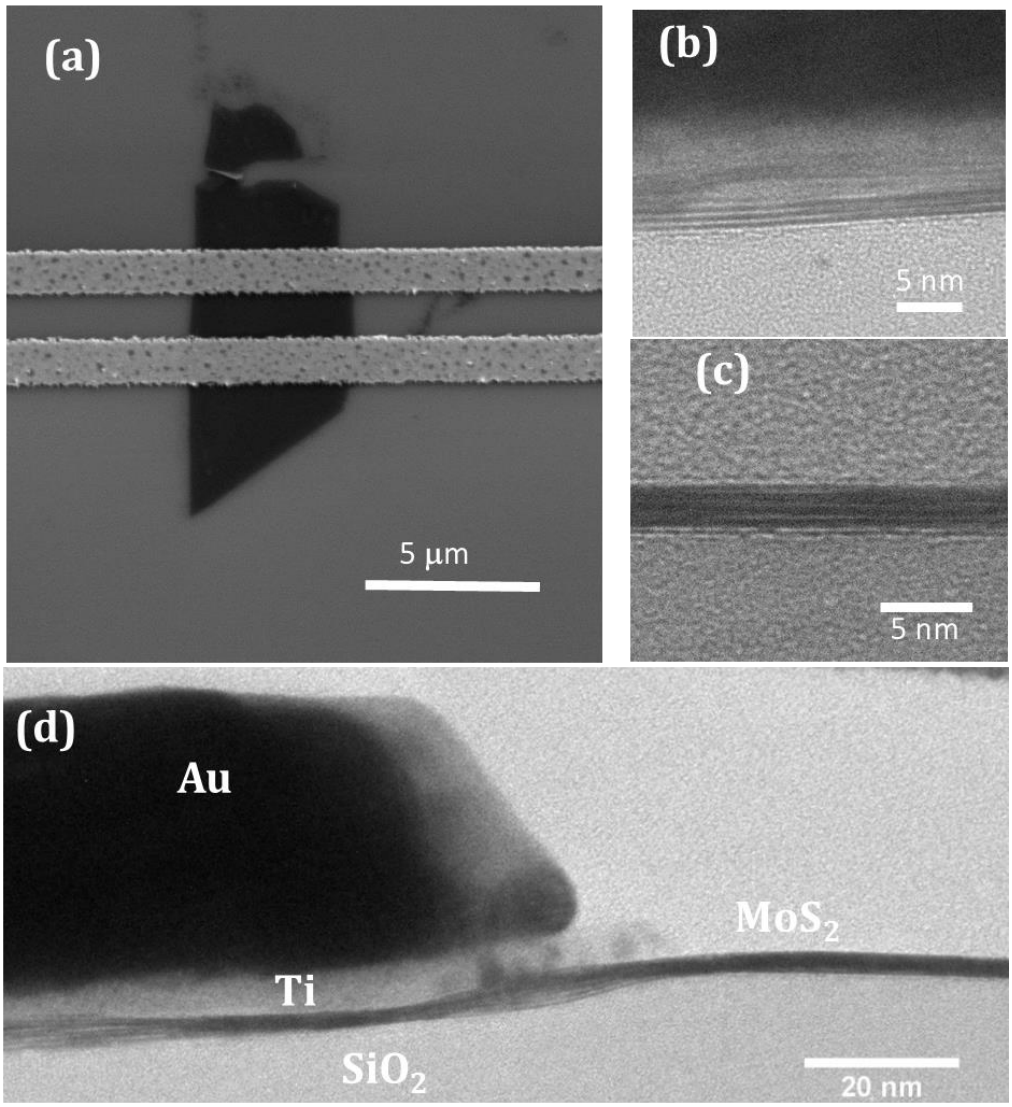


**Figure 1: Representative SEM image of the Trapezium device showing the two metal tracks used to contact it. Representative higher-resolution TEM images showing (b) the $MoS_2$-Metal interface, and the layered structure of the flake (c) beneath and (d) outside the metal contact.**

## 3.4 ELECTRICAL ANALYSIS

### 3.4.1 Extraction of impurity concentration

Figure 2 shows the transfer characteristics of the devices. The length of the devices is determined by the metal track distance, which is equal to 1 μm for all of them. The drain current is normalized by width in order to have a clear comparison between the samples. Along the Trapezium other two devices are present: the Kite and the Triangle, similarly named after their shape. All of them have a comparable thickness of 3-4 layers.

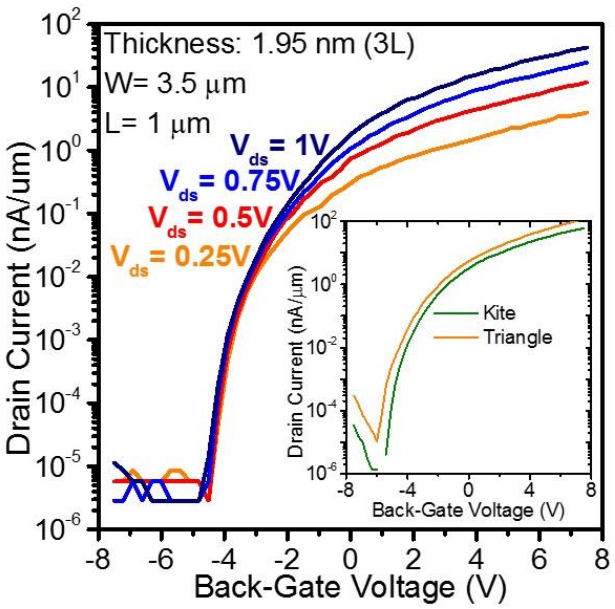


**Figure 2: Transfer characteristics of the Trapezium at different drain-source voltages. Inset: transfer characteristics of the Kite and the Triangle at $V_{ds}$=1V.**

It is possible to notice that there are few variations between the electrical characteristics. The drive current is almost the same, around 50 nA/μm, while the off current is limited by the analyser used, so it can actually be lower. The main differences can be related both to the slightly higher thickness or the high defect

variability of the material. As it was shown by McDonnel et al.[143], a defect density of 0.3%, which is common in TMDs can be sufficient to dominate the contact resistance.

Nevertheless, because of the inability to grow TMDs uniformly, systematic studies on a large number of samples are rare. The flakes here reported were exfoliated from the same bulk material onto the same substrate, facing all the same processes and environment-related exposure effects. Considering this, the variability among these devices is mostly related to intrinsic factors only (defects,[110] grain boundaries,[115] unintentional impurities[194]) and process-related factors (metal contact[120] or air exposure[195]) should affect them all in the same manner. Even if some variations are possible, this is still important for the sake of a first general understanding of the properties and problems of TMDs.

In order to further compare the limits and characteristics of the device field-effect mobility was systematically extracted. The mobility was determined from the derivative of the transfer characteristics, as usually done for TMD-based FET:

$$\mu = \frac{Lg_m}{WC_{OX}V_{DS}} \qquad (1)$$

Where L is the length of the device, W is the width, gm is the transconductance, $C_{OX}$ is the oxide capacitance and $V_{DS}$ is the drain-source voltage.

Figure 3a shows the extracted mobility values (symbols) plotted against the carrier concentration, which can be simply estimated by:

$$n_e = C_{OX}\ \frac{(V_{BG} - V_T)}{q} \qquad (2)$$

Where $n_e$ is the carrier concentration, $C_{ox}$ is the oxide capacitance, q is the electrical charge, $V_{BG}$ is the back-gate voltage and $V_T$ is the threshold voltage, which is extracted by the linear interpolation method.

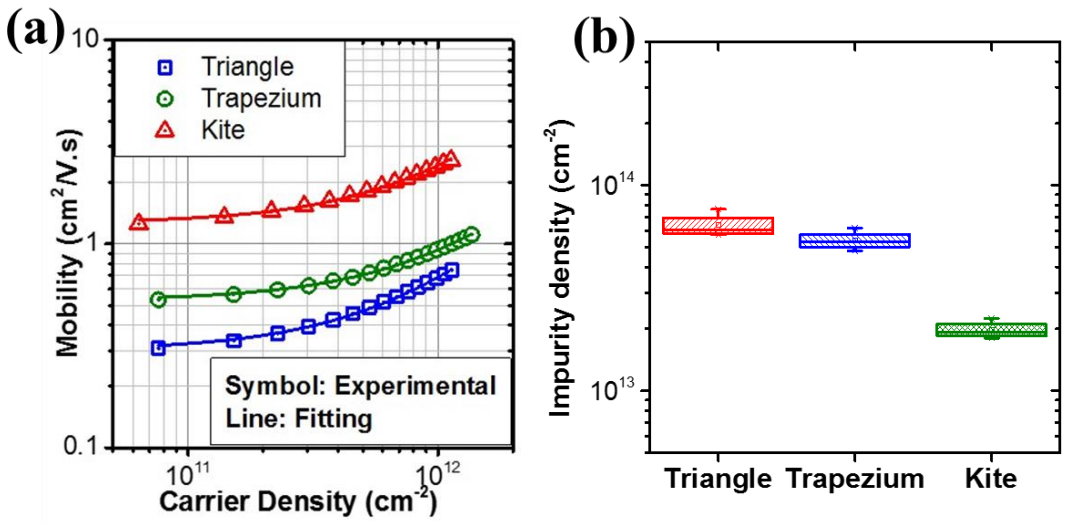


**Figure 3: Mobility versus carrier density extracted from the Triangle, Trapezium and Kite. On the right the unintentional impurity concentration for the three devices.**

From Figure 3a there is no degradation at high carrier concentration. Due the low back-gate voltage applied (maximum value is 7.5 V) and the thick oxide (85 nm of $SiO_2$) the low vertical field might be too low to cause a degradation. Also, typical Mobility versus carrier density/gate voltages, are usually characterised by a peak and then a decrease in mobility. This is not seen here because of the low voltage applied, therefore the actual mobility is likely higher. In addition, there is another factor which effect the calculation of the field effect mobility. The calculation in Equation (1) assumes no source and drain contact resistance, so that the applied voltage $V_{DS}$ drops entirely across the conducting $MoS_2$ channel from source to drain. The presence of source and drain series resistance results in a channel voltage drop $V_{CH} < V_{DS}$. As a result, the electron field effect mobility values in Figure 3 (a) represent the lower limit of the actual electron mobility in the $MoS_2$.

Ma and Jena[92] reported a systematic study on carrier transport of 2D crystals, which are found to be highly dependent on the unintentional impurity density and the dielectric environment, which will be discussed in the next section. In particular, the mobility versus electron density, for low carrier density, follows the relationship:

$$\mu_{CI} \cong \frac{3500}{N_{CI}/10^{11}\,cm^{-2}}\left[A_{CI} + \left(\frac{n_e}{10^{13}\,cm^{-2}}\right)^{1.2}\right]\ cm^2/V.s \qquad (3)$$

Where $\mu_{CI}$ is the mobility, $N_{CI}$ is the unintentional impurity concentration, $A_{CI}$ is a fitting parameter that depends on the dielectric environment and will be discussed in the next section. Considering that $n_e$ can be evaluated experimentally, the unintentional impurity concentration can be extracted by fitting the equation with the electron mobility of the devices introduced before. From Ma and Jena[92] fitted data show an unintentional impurity concentration of $10^{13}$ $cm^{-2}$, while Mori et al.[196], which implemented this same method, found different levels of unintentional impurity concentration ($10^{11}$ and $10^{13}$ $cm^{-2}$), due to the high variability of TMDs.

Figure 3a shows the excellent fitting of the experimental mobility with Equation 1. The results of the fitting are shown in Figure 3b, which shows the unintentional impurity concentration level for each device. Even if a lot of factors can affect the parameter extractions, as widely said before, the unintentional impurity concentration level for all the device is on average $4\times10^{13}$ $cm^{-2}$ for nominally un-doped samples, which carrier concentration is expected to be in the $10^{17}$ $cm^{-3}$ range or lower.[197]

In order to confirm the extraction carried out for the Kite, the Triangle and the Trapezium, another exfoliation was done of Nb-doped $MoS_2$, following the same process steps as the previous devices. The doping level for Nb-doped the crystal was

found to be in the range $4.2\times10^{19}$-$7.4\times10^{19}$ $cm^{-3}$ from Hall measurements.[197, 198] In this case the mobility should as well be limited by charge scattering, therefore the unintentional impurity extraction should give a doping level (intentional impurity) in the high $10^{19}$ $cm^{-3}$ range.

Figure 4a shows an optical picture of the experimental device. Labelled as C1, C2, C3, C4 and C5 the tracks that were contacted for the electrical measurements. Unfortunately some contacts were shorted during the electron beam lithography and were not used for the electrical characterisation.

Figure 4b shows the output characteristic for the contact C3 and C4 (C34) for a drain voltage of 0.5 V. From this curves it is possible to notice the advantages of using highly doped 2D-semiconductor with a Junctionless transistor configuration. Indeed, usually this device are limited by contact resistance, which even if still present in part, it is lowered by the high doping. On top of that, the current is usually higher with respect of nominally undoped flakes. As known, when a highly doped semiconductor is used in this Junctionless transistor configuration the thickness needs to be lower than the maximum depletion width in order to guarantee the full turn-off of the device.[199] Previous calculations have shown this value to be around 4.7 nm for this doping level.[198] From optical inspection the thickness of the flake is slightly higher, around 6 nm. This explains why the $I_{ON}/I_{OFF}$ ratio of the device is around $10^4$, but with a thinner device it can be in principle much higher.

Figure 4c shows the mobility extracted from each contact configuration. The extraction followed the same steps as before. The mobility increases for low carrier density as for nominally undoped samples. For carrier concentrations higher than $2\times10^{12}$ $cm^{-2}$ the mobility starts decreasing, probably related to the high vertical electric

field. As will be discussed in later sections, mobility degradation might be possible for electrical fields higher than $10^8$ V/m, which is the vertical field value at a concentration of $2\times10^{12}$ $cm^{-2}$.

Considering the mobility at low carrier density ($<2\times10^{12}$ $cm^{-2}$) it is possible to extract the impurity concentration, which should be the doping level in this case, for the four contact configurations. Figure 4d shows the extracted intentional impurity concentration level. The contact C12 and C45 shows the same results, as for the contact C23 and C34. The difference between these devices is their length. C23 and C34 are longer (3.5 μm) with respect of C12 and C45 (0.5 μm). In this case the results for longer devices can be more reliable than the results for shorter devices. The fact that there is a high doping concentration means that the contact resistance of the device is lower than usual, as well as the resistance of the semiconductor. However, shorter devices might be dominated by contact resistance. Therefore, the results for longer devices (C23 and C34) might be more reliable than the results for shorter devices (C12 and C45).

Considering the intentional impurity concentration extracted for C23 and C34 at 25 $^oC$, the average value is $8.75\times10^{13}$ $cm^{-2}$. Considering a thickness of 6 nm, the intentional impurity concentration is $1.45\times10^{20}$ $cm^{-3}$. This value is slightly higher than the actual doping concentration measured by Hall effect $2\times10^{19}$-$7.4\times10^{19}$ $cm^{-3}$, but supports the approach used to extract the impurity concentration in non-intentionally doped $MoS_2$ samples.

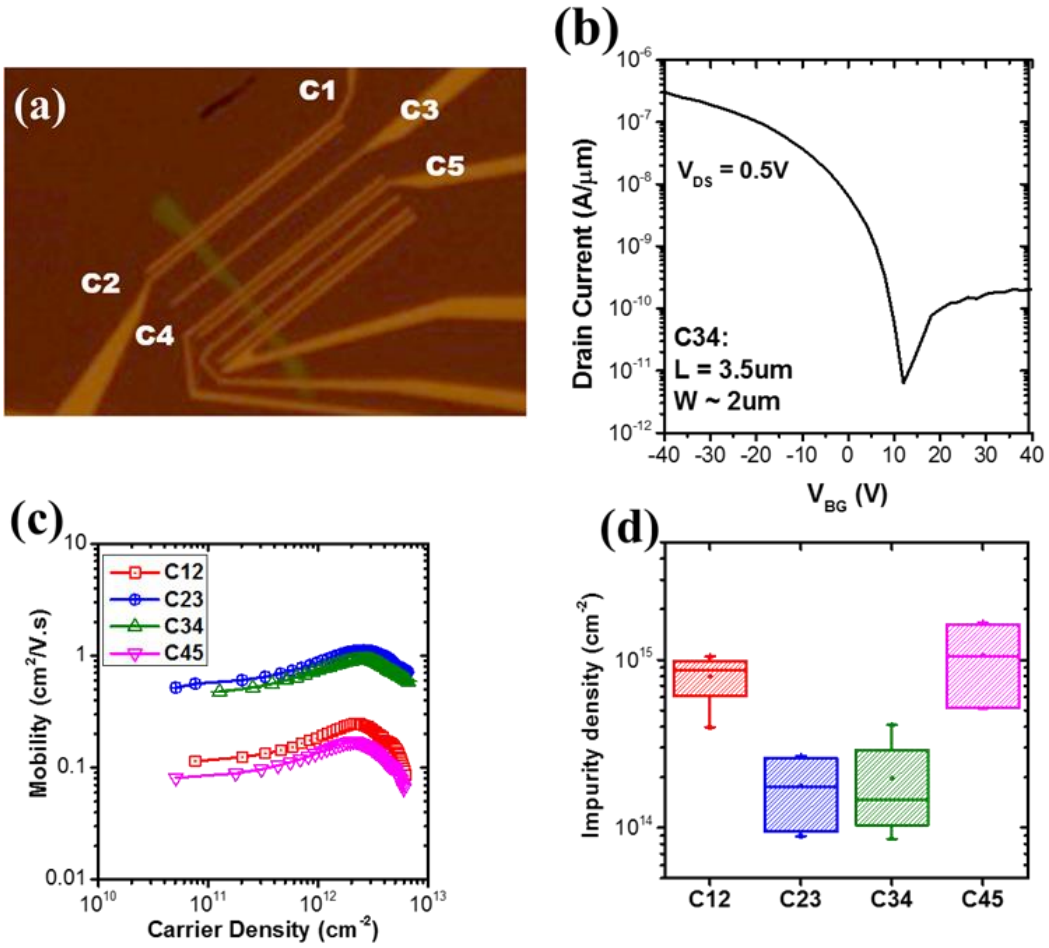


**Figure 4: (a) Optical picture of a thin Nb-doped $MoS_2$ flake. The contacts used for electrical characterization are labelled. (b) Transfer characteristics between the contacts C3 and C4 at $V_{DS}$=0.5V. (c) Mobility versus carrier concentration extracted for each contact. (d) Extracted unintentional impurity concentration from each contact, as labelled.**

The level of unintentional impurity found for the nominally undoped devices ($4\times10^{13}$ $cm^{-2}$) are significantly higher with respect of what is required by Si-based integrated circuit industry. In particular structural defects are requested to be below 0.008 $cm^{-2}$ and impurities less than $5\times10^{10}$ $cm^{-2}$ .[109] Structural defects of $MoS_2$ are outside the aim of this study, but were widely discussed in literature.

In order to confirm the high intentional impurity in the Nb-doped samples and the unintentional impurity concentration in the nominally undoped $MoS_2$, SIMS analysis was carried out on a series of different crystals and the results are reported in

Figure 5. The analysis was based on $MoS_2$, natural and synthetic, nominally doped and undoped. $MoSe_2$, $MoTe_2$ $WSe_2$ and $HfSe_2$. H, C, O F and Sb were collected as negative ions while sputtering with a Cs+ beam. Na, Cr, Zr and Nb were collected as positive ions while sputtering with a $O_2$+ beam. Unfortunately, no direct comparison on the yields can be made in the figure between the different elements, but qualitatively comparisons can be made. In order to make a quantitative comparison a yield normalization of all the species to the yields of common matrix elements is needed. In our case, the yields in $MoS_2$, $MoSe_2$ and $MoTe_2$ have been normalized to the Mo yield, while yields in $WSe_2$ and $HfSe_2$ have been normalised to the Se yield collected in the $MoSe_2$ sample. This provides a way to qualitatively compare the two subsets of samples. The yields of the common matrix elements do not vary much between the different samples, supporting the reliability of the method. The exception is the $WSe_2$ sample analysed with Cs (H, C, O F and Sb elements), where the normalisation has been as large as a factor of x17, thus in this sample errors on H, C, O F and Sb might be larger. In general, the natural sample contains the highest levels of H, C and O contaminations, in particular for H and C. C contamination seems to differ significantly between the different synthetically grown samples. The Nb doping can be clearly seen in the intentionally doped synthetically-grown $MoS_2$ samples. Nonetheless, some Nb seems to be present in both $WSe_2$ and $HfSe_2$ samples. Na and Cr seem to be present only in synthetically grown sample and, particularly for Cr, there seems to be some correlation with doping. A clear isotope fingerprint of Zr contamination is found in the $HfSe_2$ sample.

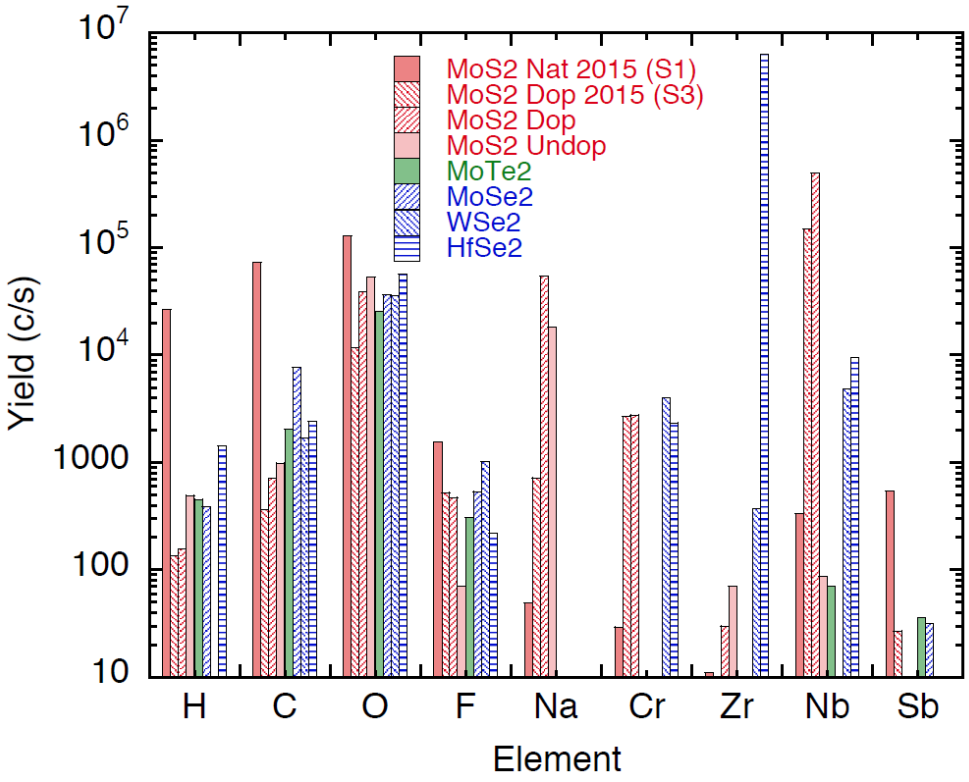


**Figure 5: SIMS analysis carried out on a range of different TMD crystals.**

### 3.4.2 **Effect of the dielectric environment**

The dielectric environment also plays an important role in the electron transport of thin semiconductors. The Coulomb potentials inside a thin semiconductor can be modified by the dielectric environment. As well, electrons in the semiconductors can excite polar-optical-phonon modes in the dielectrics, which become stronger for thinner materials. It is well known that high-*k* are beneficial for FET applications (i.e.: better electrostatic). Nonetheless, carrier transport can be severally degraded. Ab-initio calculations for monolayer $MoS_2$ have shown that high-k dielectric degrades mobility because of smaller surface-optical phonon energies, which can be easily excited and cause scattering in the thin material.[92] In order to extract the best performance from 2D-semiconductor is necessary to find a balance

between high k-values, low surface optical phonon energies (and so lower surface optical phonon scattering) and as well screening of charged impurities.

In order to study the effect of the substrate through the same fitting process used before, other $MoS_2$ flakes were exfoliated on different oxides: 270 nm wet grown $SiO_2$ and 27 nm of ALD $Al_2O_3$. The fabrication steps are similar than the previous, with the only exception of the lithography, UV-lithography instead of e-beam lithography. The other main difference is that the contact length is not specified as it was for the metal tracks with the other devices. However, the contact area is large enough to guarantee an adequate carrier injection from the semiconductor to the metal. The channel length was defined by mask used for the lithography process and it was ~5 μm, as shown in Figure 6a. Figure 6b,c and d show typical IV curves for devices exfoliated on 27 nm of $Al_2O_3$, 85 nm of dry thermal $SiO_2$ and 270 nm of wet thermal $SiO_2$ respectively. The transfer characteristics are fairly similar between each other. The major differences are related to the wider hysteresis in the dry thermal $SiO_2$.

Mobility values were extracted and fitted by Equation 3 as before:

$$\mu_{CI} \cong \frac{3500}{N_{CI}/10^{11}\,cm^{-2}}\left[A_{CI} + \left(\frac{n_e}{10^{13}\,cm^{-2}}\right)^{1.2}\right]\ cm^2/V.s \qquad (3)$$

In this section we will focus on the fitting parameter $A_{CI}$ instead of the impurity concentration, which is related to the dielectric environment.

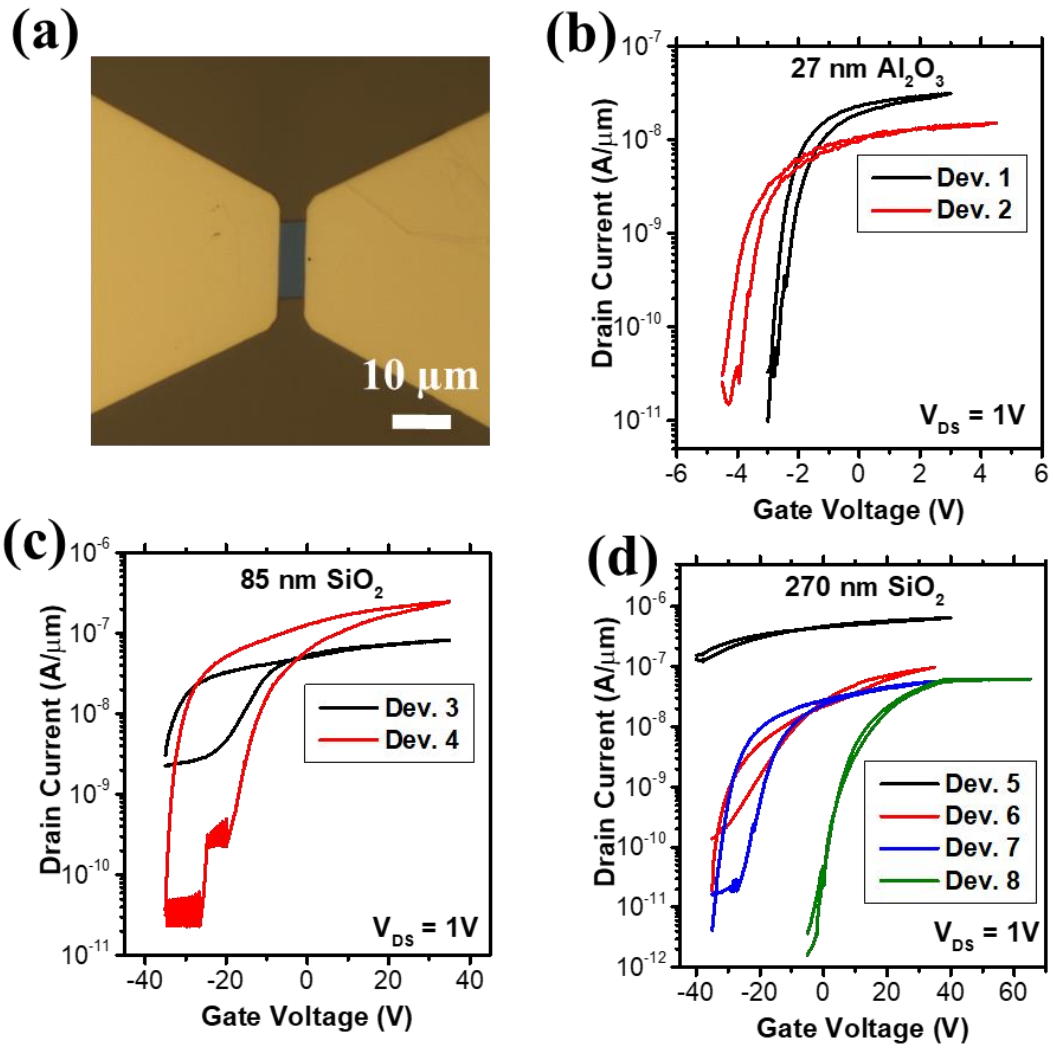


**Figure 6: (a) Optical picture of a typical back-gated device structure. Transfer characteristics for the devices (dev.) exfoliated on (b) 27 nm of $Al_2O_3$, (c) 85 nm of dry thermal $SiO_2$ and (d) on 270 nm wet thermal $SiO_2$ at a drain voltage of 1V. The devices were numbered to distinguish them.**

. Figure 7a shows the value of $A_{CI}$ for devices fabricated in parallel but exfoliated on different substrates. Even if there is an error bar associated with the two sets of extractions, there is a clear difference between the two substrates. The average value is 0.079 for $Al_2O_3$-air and 0.04 for $SiO_2$-air. The fact that the parameter is different is a reflection of the effect of the substrate on the material itself. Even if the original fitting was made for monolayer $MoS_2$, while these flakes are in the 6-8 layers

range, the results are still close. The value from the reference is almost 0.075 and 0.036 for $Al_2O_3$-air and $SiO_2$-air respectively.

Even if this is seen with $A_{CI}$ the results are different for $N_{CI}$. The unintentional impurity concentration extracted for the $SiO_2$-air devices is $\cong 4.3\times10^{12}$ $cm^{-2}$, while the one extracted for the $Al_2O_3$-air devices is $\cong 5.5\times10^{13}$ $cm^{-2}$. Considering that the flakes were exfoliated from the same bulk materials the difference is related to the different substrates. This effect might be related to the different growth techniques used for the two substrates. The $Al_2O_3$ substrates might be affected by fixed charges, which can act similarly to charged impurity centres for thin 2D-semiconductors. For this reason the mobility of the devices fabricated on $Al_2O_3$ are slightly lower than the mobility values extracted from devices fabricated on $SiO_2$ (not shown).

The same extraction was repeated for the Kite, The Triangle and the Trapezium. With respect of the previous set of samples the dielectric is the same ($SiO_2$-air), while the difference is only related to the thickness (from 7 to 3 layers). The values for $A_{CI}$ are reported in Figure 7. The average value at room temperature is 0.065. Even if this is slightly higher than the value reported it is important to consider that the top surface of the devices is exposed to air, which effectively change the top environment of the device.

Lastly, Figure 7a shows also the parameter extracted from the 9-layers Nb-doped sample. The average value at room temperature is 0.15. With respect of the last samples considered not only this sample is slightly thicker, but also highly doped. The high doping might be the main reason of this behaviour, due to different charge screening from the surrounding dielectric environment. In order to understand if this

value is related to thickness, substrate or doping concentration more experiments might be needed. Finally, Figure 7b shows the relationship between $A_{CI}$ and the dielectric constant as reported in literature and as extracted here experimentally. Overall, there is a good agreement considering that the model was developed for monolayer $MoS_2$, which due to the high contact resistance are difficult to realize experimentally. Nevertheless, the effect from different substrates is clear even if thin $MoS_2$ is considered instead of the monolayer.

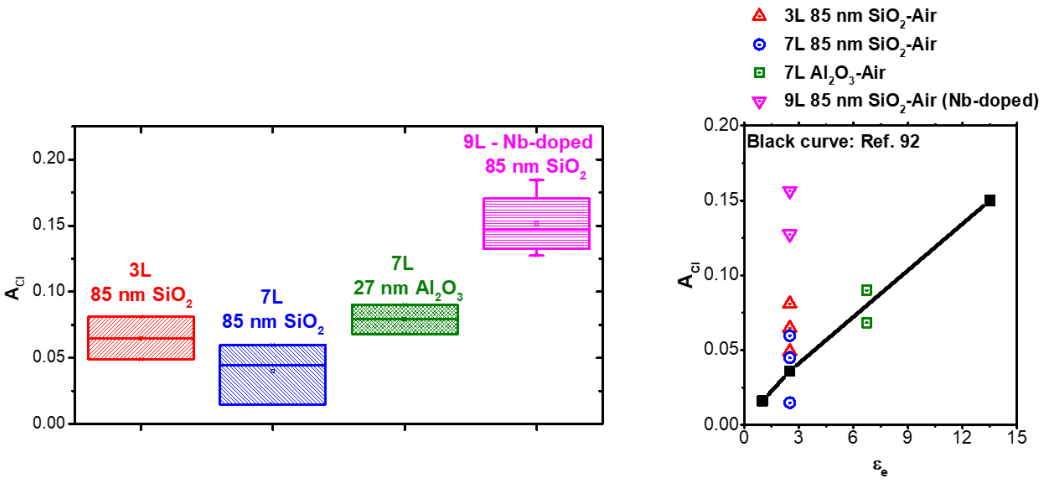


**Figure 7: (a) Value of the parameter $A_{CI}$ with respect of different dielectric environment, $MoS_2$ thickness and doping. (b) Comparison of the parameter $A_{CI}$ varying the dielectric with respect of the theoretical reference.**

These data consider the mobility in the low-field regime, when the mobility is highly dependent on the screening of impurity concentration by the dielectric environment. Another effect that can help in the choice of the optimal dielectric environment is the degradation of mobility at high field. The mobility degradation model reported for $MoS_2$ due to high vertical electric field depends on an empirical mobility model developed for Si MOSFETs.[200, 201] It considers the mobility

degradation observed at the $HfO_2$-semiconductor interface,[202] which was attributed to remote phonon scattering:

$$\mu_{rps} = \frac{\mu_{rps0}}{\left(\frac{F_{\perp}}{10^6\, V/cm}\right)^{\gamma_1}\left(\frac{T}{300K}\right)^{\gamma_2}} \qquad (4)$$

where $\mu_{rps0}$, $\gamma_1$ and $\gamma_2$ are fitting parameters and $F_\perp$ is the actual vertical field. T is the temperature. Considering a fixed temperature of 300 K and different substrates it is possible to extract the dependency of $\gamma_1$ with respect of the dielectric environment.

Figure 8a shows the mobility extracted experimentally from the devices introduced before. The degradation starts in the range 2-4×$10^7$ V/m, consistent with previous experiments.[203] The degradation part of the curve is fitted by Equation 4 and it clearly matches with the experiments. The resulting fitting parameters are $u_{rps0}$ and $\gamma_1$. The former is a fitting parameter that depends on the mobility value at the beginning of the high-field degradation, then it can depend on other factors, as unintentional impurity concentration. The latter depends instead on the rate at which the mobility decreases at high field. Even if the mobility is limited by other factors (so $u_{rps0}$ is different), the mobility degradation rate is a function of the dielectric, because of surface roughness and optical phonon scattering. Figure 8b shows the dependency of $\gamma_1$ with respect of the gate dielectric (the data at for $HfO_2$ ($\varepsilon$~19) refer to ref. [30, 200, 204], while the red data are from ref. [203]). The dashed line was added to help the eye. Considering the data extracted from this work and published results from literature, the relation $\gamma_1$-$\varepsilon$ looks clearer and shows a minimum value between 6 and 11. A lower value of $\gamma_1$ means a lower degradation effect at high electric field. This optimal range

was also found by experimental and theoretical calculations. Back-gated $MoS_2$ FET showed higher mobility using AlN as a dielectric (ε~8) and all-nitride environment FETs, using h-BN and AlN showed the best performance.[203] DFT calculations showed a similar trend.[111] In particular, mobility tends to increase from low *k* material to the optimal range 8-11 because of screening of charged impurities. At higher *k* values mobility decreases because of the smaller surface optical phonon energies, and so increase scattering.

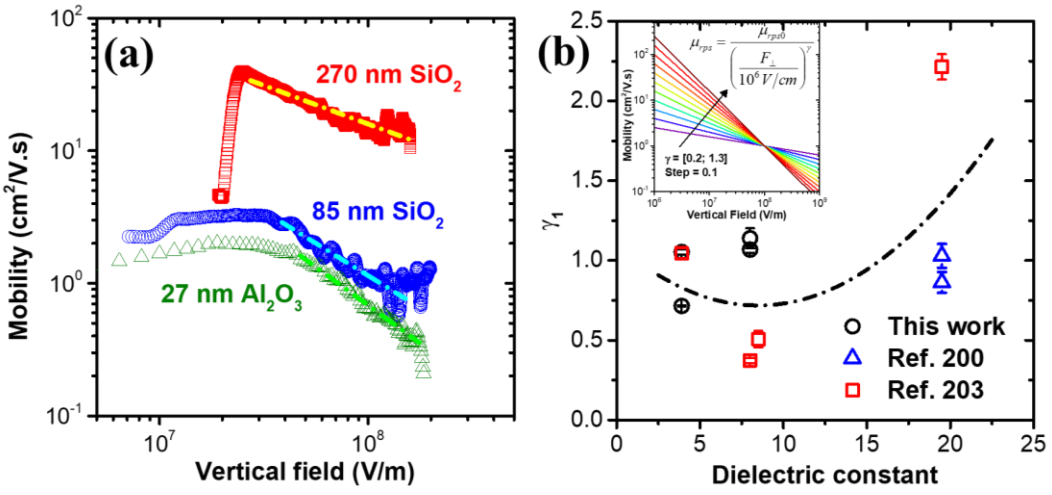


**Figure 8: (a) Mobility extracted from experimental devices considering different substrates. The dotted line refers to the fitting with Equation 4. (b) Trend of $\gamma_1$ with respect of the dielectric constant of the gate dielectric. Inset: mobility degradation at high vertical field for increasing value of $\gamma_1$.**

## 3.5 DISCUSSION

Overall, there is an enormous difference between industry constraints and TMDs. As known, in order to properly extract the characteristics of semiconductors in general it is important to keep low the levels of impurities. Specifically because of their low thickness, the effects of contaminants can be particularly critical for thin 2D-Semiconductors.[205] Indeed, it was shown how different dielectric environment can

affect the mobility of the material, due to the lower effects of long-range Coulomb interaction. The results showed here for $MoS_2$ are most likely valid for other type of TMDs or maybe similar 2D materials. In the case of this study the electron mobility at low carrier concentration was limited by the high impurity concentration, which masks the potential phonon limited mobility of $MoS_2$. At higher carrier concentration the effects of impurity might be less effective, and mobility degradation can come from surface roughness[206] or remote phonon scattering.[207]

Often are also reported field-effect devices with "unknown doping concentration",[208] which can be probably related to impurities acting as dopants. A more detailed quantitatively analysis by ICMPS showed that the concentration of several elements were above $10^{13}$ $cm^{-2}$, for both geological and synthetic $MoS_2$.[90] A similar study conducted on $WSe_2$ showed lower impurity concentration,[192] closer to the upper limit required by Si-based IC technology. Still, the intrinsic electronic properties of the material were strongly influenced by unintentional impurities.

One solution might be the introduction of a suitable dielectric environment capable of screening such impurities. As seen, the variation of the dielectric environment has a certain impact on the parameters extracted, confirming the theoretical model developed for monolayer $MoS_2$. Nevertheless, is still unclear how much this will affect the mobility due to the inability to test pure materials at present.

Also, even if it is important to compare TMDs with Silicon-based devices to benchmark their behaviour and potential, the comparison is not truly fair. Silicon is a mature semiconductor material, where unintentional impurities have been controlled to levels $< 5\times10^{10}$ $cm^{-3}$, and the effect of substitutional doping and strain are well understood both theoretically and experimentally. Several groups are working on

doping techniques and simulation studies on how strain effects TMDs. These two techniques are normally used in industry for Silicon in order to obtain a low contact resistance and higher mobility, and stable doping and controlled strain are yet to be achieved for TMD based semiconductors. Generally, the immaturity of 2D-Semiconductor is due to the early stage of their research. Air stability, contact resistance and impurities, are some of the key challenges for the real application of these material, but with a large-area growth of higher quality material, most of these challenges can be opportunely studied and overcome as it happened at the early years of Silicon.

## 3.6 CONCLUSIONS

In this work, back-gated flakes of $MoS_2$ were electrically characterised for the main purpose of understanding the effect of impurity concentration and dielectric environment on the extracted field-effect mobility. The performance of the devices in terms of on/off ratio, drive current and mobility values extracted are comparable to other publications for back-gated $MoS_2$ MOSFETs. Through a fitting process of the field-effect mobility, impurity concentration was extracted for different devices, considering variation of dielectric environment, thickness and doping concentration. It was found that the unintentional impurity concentration is so high that it can be the limiting factor of electron mobility of the flakes studied to date. The impurity concentration was later confirmed with SIMS analysis in several TMD crystals. One solution might rely on the use of low-k dielectric, but the material system might be right now too immature to show this behaviour experimentally.

# Chapter 4: CONTACT RESISTANCE STUDY OF HIGHLY DOPED P-TYPE $MoS_2$

This chapter is adapted from the following conference:

**Mirabelli, G.**; Duffy, R.; Hurley, P. K.; Monaghan, S.; Cherkaoui, K.; Schmidt, M.; Sheehan, B.; Povey, I. M.; McCarthy, M.; Nagle, R.; Bell, A., Mo-Based Transition-Metal-Dichalcogenide Junctionless Field-Effect-Transistors. Meeting Abstracts 2016, MA2016-01 (26), 1289-1289.

## 4.1 INTRODUCTION

Contact resistance is one of the major bottlenecks of TMD-based devices and for this material to be competitive with other semiconductors an analysis as well as possible solutions are necessary. The first part of the chapter deals with the electrical characterization of $MoS_2$ samples with high p-type levels of intentional impurities, ~$3x10^{19}$ $cm^{-3}$ measured by Hall effect.[209] These results will be compared with a wide range of doping and process optimization techniques used to improve the metal-TMD interface to achieve a low contact resistance. The second section of the chapter describes the use of TCAD modelling to extract basic electrical properties to understand which device architecture can be more useful for ultra-scaled devices.

## 4.2 EXPERIMENTAL

Mechanical exfoliation with scotch tape was used to obtain thin flakes from an intentionally p-type doped $MoS_2$ crystal. The flakes were transferred onto a substrate of 85 nm of $SiO_2$ and a highly p-type doped Si handle wafer. Ti/Au or Ni/Au (5/45 nm) metal contact pads and electrodes were defined by electron-beam lithography, followed by metal evaporation and a lift off process. 20 kV beam exposures were performed with a Raith e-beam lithography tool. For electrical characterization, the B1500 Keysight device parameter analyser was used. The morphologies of the TMD sample surfaces were investigated using a FEI Quanta 650 SEM in high-vacuum.

## 4.3 DEVICE FABRICATION

Figure 1a shows a SEM image of one of the devices studied in this work. Figure 1b shows the Atomic Force microscopy image of the device in Figure 1a. The

white line defines the region from where the thickness is extracted. The inset of Figure 1b shows the thickness extracted (~17 nm).

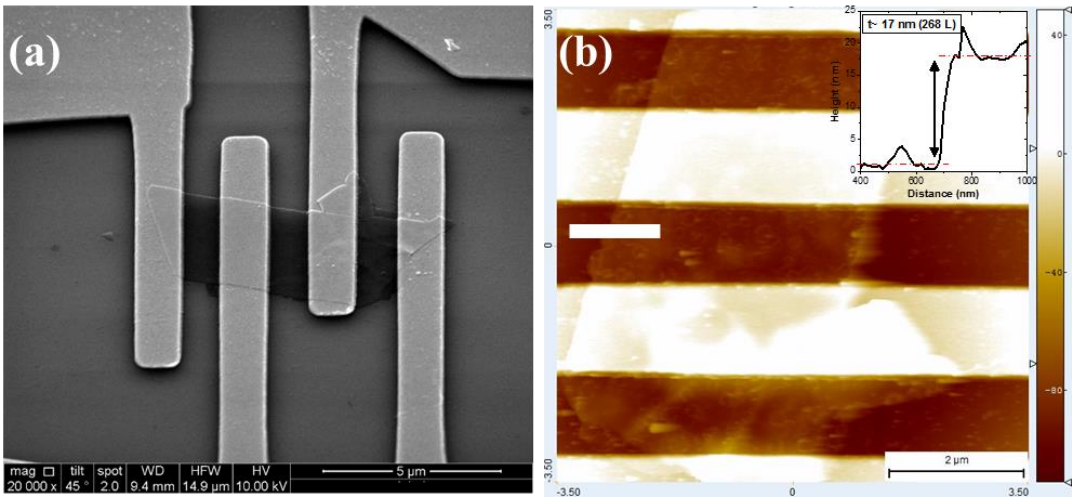


**Figure 1: (a) SEM image of a typical contacted flake. (b) Representative AFM image of the same flake in (a). The white bar denotes where the cross-section was taken from. Inset: cross-section of the flake with its thickness (~17 nm).**

## 4.4 ELECTRICAL CHARACTERISATION

Figure 2a shows a schematic of the four-point probe setup used in this work. A constant current is forced through the two most outer electrodes and the voltage drop across the inner electrodes is measured. Considering this voltage drop, it is possible to measure the real resistance of the semiconductor, without the effect on the contact resistance. Measuring the inner electrodes in a two-point probe setup, it is possible to extract the contact resistance as well. Figure 2b shows an example of this kind of measurements. A constant current of 1 nA is set between the outer electrodes and the voltage drop between the two inner electrodes is measured. This is then divided by the constant current to obtain the resistance of the semiconductor ("4-point-probes" in the plot). A two-probe measurement is repeated to obtain the total resistance of both the semiconductor and the contacts ("2-probes" in the plot). The difference between the total resistance and the semiconductor resistance will give the contact

resistance ("$R_C$"). Figure 2c shows the transfer characteristic of the device measured in Figure 2b with and without the effect of contact resistance.

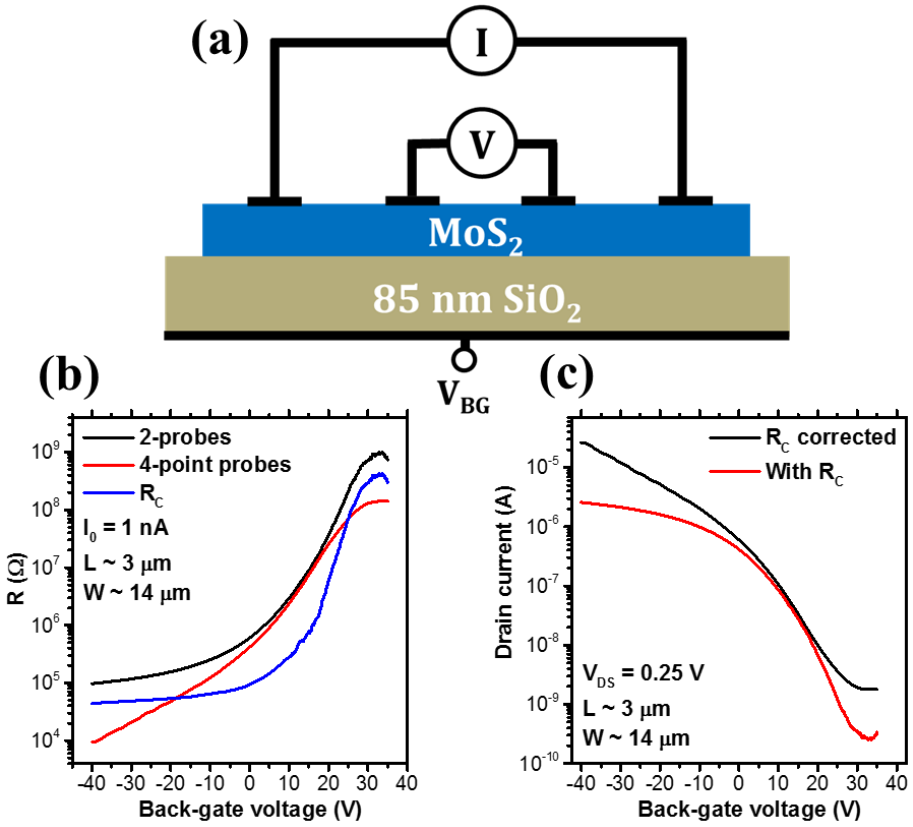


**Figure 2: (a) Schematic of the device architecture used in this work. The external metal contacts are used to force a current in the device. Considering then the voltage drop across the two inner contacts, the resistance of the contact is extracted. (b) Example of 2-probe measurements (across the two inner pads), 4-point probe measurements and the extracted contact resistance. (c) Transfer characteristic of the same device from 2-point probe measurement (with $R_C$) and without the effect of $R_C$.**

## 4.5 DOPING EXTRACTION

An important characteristic of the devices measured so far is their high doping concentration, as widely said, but it is necessary to have an idea of the actual doping concentration. Because of this, most of the transfer characteristic do not have a clear OFF region. In order to have a completely turn off the transistor it is necessary that the thickness of the channel it is less that its maximum depletion width:

$$W_{DM} = 2\sqrt{\frac{\varepsilon k_B T \ln\left(N_A/n_i\right)}{q^2 N_A}} \quad (1)$$

if the flake is thicker than $W_{DM}$ there will be a shunt current ($I_{SHUNT}$), which is equal to:

$$I_{SHUNT} = \mu_p \frac{W}{L} V_{DS}\, q\, N_A (t - W_{DM}) \quad (2)$$

considering these two equations a doping concentration of ~$3.4\times10^{19}$ $cm^{-3}$ was extracted from each transfer characteristic. This same doping level was similarly extracted in previous work[210] and from Hall measurements (Figure 3b).[197] The mobility extracted from the transfer characteristic is ~7 $cm^2/V.s$ after $R_C$ correction from both Ti/Au and Ni/Au devices, which is again consistent with Hall measurements. This is another validation of the reliability of the contact resistance data extracted.

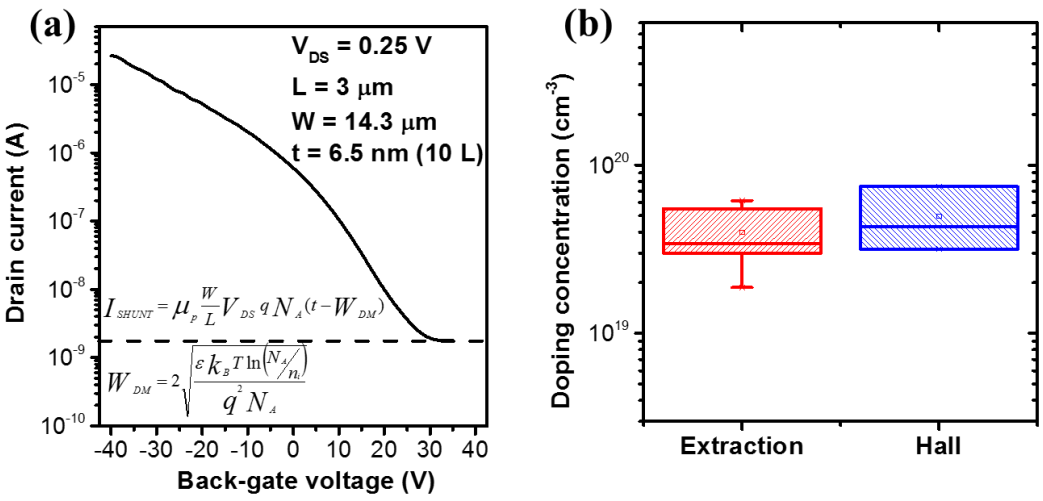


**Figure 3: (a) Transfer characteristics of the 6.5 nm thick device showing the shunt current level, the equation for the shunt current and the equation for the maximum depletion width. (b) Average doping concentration from the extraction process using the transfer characteristics and the Hall measurements.**

## 4.6 DISCUSSION

Figure 4 show the contact resistance versus $MoS_2$ thickness extracted from each device (Blue scatter data) compared with literature. Most of the data refer to Ni/Au metal contacts, while one of them was fabricated with Ti/Au contact. Although there is a slight difference in thickness it is clear that Ni is a far better contact that Ti. This can be related to a higher work-function of Ni. Nonetheless, it is clear that a doped contact reduces drastically the contact resistance with respect of the "as exfoliated" results introduced in chapter 1, where the contact was not optimised.[121-131] These data clearly show the problem related to the metal-$MoS_2$ interface. Not only the contact resistance values are usually higher than what required by the IRDS, but also the data are characterized by a wide spread. All the other data present in the plot refer to works where the contacts was improved in a certain of ways. It is clear that all the treated contacts are well below the un-treated ones. These works were divided for clarity in three sections: contact optimization, process optimization and annealing step.

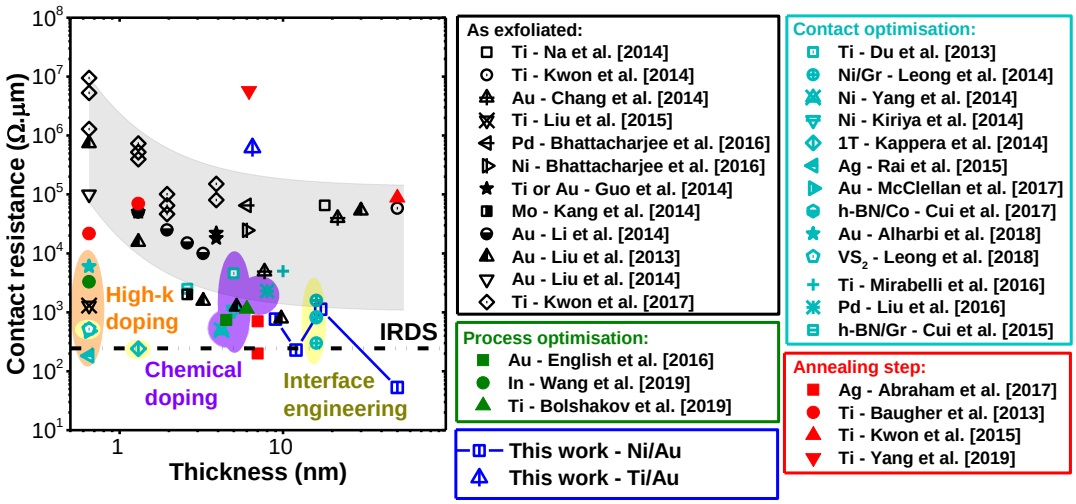


**Figure 4: Contact resistance versus thickness of $MoS_2$ considering Ti/Au and Ni/Au contacts (Blue). The data are compared with other techniques to reduce contact resistance: high-*k* doping, chemical doping and interface engineering.**

Contact optimization refers to those work where the interface metal-TMD is changed considering a buffer layer (interface engineering) or a certain doping technique (substitutional, chemical or high-*k* doping). Leong et al.[211] and Cui et al.[212], improved the contact resistance of $MoS_2$ by adding a layer of Ni/Graphene or h-BN. The additional spacer improves the effective contact resistance as it interacts with $MoS_2$, reducing its work function, and it disrupts the metal−TMD interaction that causes Fermi level pinning. Kappera et al.[213], instead changed the $MoS_2$ 2H-phase (semiconductive) to a 1T-phase (metallic) below the contact regions. Similarly, Leong et al.[214] used $VS_2$ (TMD with metallic phase) between $MoS_2$ and the metal contact to effectively improve the contact behavior. Another way to optimize the contact is by doping, as widely known already for 3D-semiconductors. A common technique is high-*k* doping. Theoretical and experimental works have shown that a doping can be mediated in $MoS_2$ by interfacial-oxygen-vacancies at the high-k/$MoS_2$ interface,[215] considering $HfO_2$ and $Al_2O_3$ on both exfoliated flakes[216] and CVD-grown monolayer $MoS_2$.[217, 218] Another solution relies on the chemical doping, by which the TMD is generally immersed in a chemical solution that acts as a charge transfer donor/acceptor. Both p-[219] and n-type[220-222] doping were demonstrated. Similar results were obtained by substitutional doping,[198] in which the dopant is introduced during growth.

Process optimization refers to published works which aimed to improve or modify the fabrication process to reduce the contact resistance of the device. English et al.[223] demonstrated the beneficial effects of Ultra-High Vacuum (UHV) instead of High-Vacuum (HV) during metal deposition because of a cleaner metal-$MoS_2$ interface. A similar result was confirmed by atomic resolution imaging using In as metal contact, which didn't have any reaction with $MoS_2$ and resulted in a sharp interface.[224] A cleaner contact and a lower contact resistance was also achieved by $O_2$

plasma exposure at the contact, which can remove photoresist residues from the TMD surface, responsible for the Fermi level pinning at the contact.[225]

As a final point, "annealing step" in Figure 3 refers to work that incorporated an annealing step in order to reduce the impact of contact resistance. The annealing techniques used are different: vacuum,[226] microwave,[227] laser[228] and forming gas anneal.[229] Particularly low are the results from Abraham et al.,[229] where the metal contact used for $MoS_2$ is silver. Previous works have shown that silver is a dopant for $MoS_2$ and can be diffused by an annealing step.[230, 231] Therefore, the low contact resistance can be related to a dopant diffusion and activation below the contact region, forming a device similar to a classic MOSFET, with doped source and drain region. In addition, annealing step were also shown to be beneficial to reduce hysteresis[232] or density of interface traps.[233] Nonetheless, although promising, the results are highly variable so a more systematic study considering different metals and thickness is necessary.

It is clear from Figure 4 that the contact resistance of the highly p-type doped $MoS_2$ samples analysed in this chapter are among the lowest values reported and very close to the IRDS requirements. In particular the data are similar to other doping techniques, confirming the utility and the necessity of a reliable doping method for 2D-semiconductors.

Figure 5a shows the transfer characteristic of each device studied in this work. The effect of contact resistance was eliminated considering the 4-point probe method as explained before. It is possible to notice a clear increment in the $I_{ON}/I_{OFF}$ ratio considering thinner flakes. Figure 5b shows instead the transfer characteristic for different $V_{DS}$ of a thinner $MoS_2$ Nb-doped flake (two probes, without using the 4-

probe method). Although it was not possible to remove the contribution of the contact it is clear that the $I_{ON}/I_{OFF}$ ratio increments with decreasing thickness as expected, therefore behaving as a junctionless transistor.

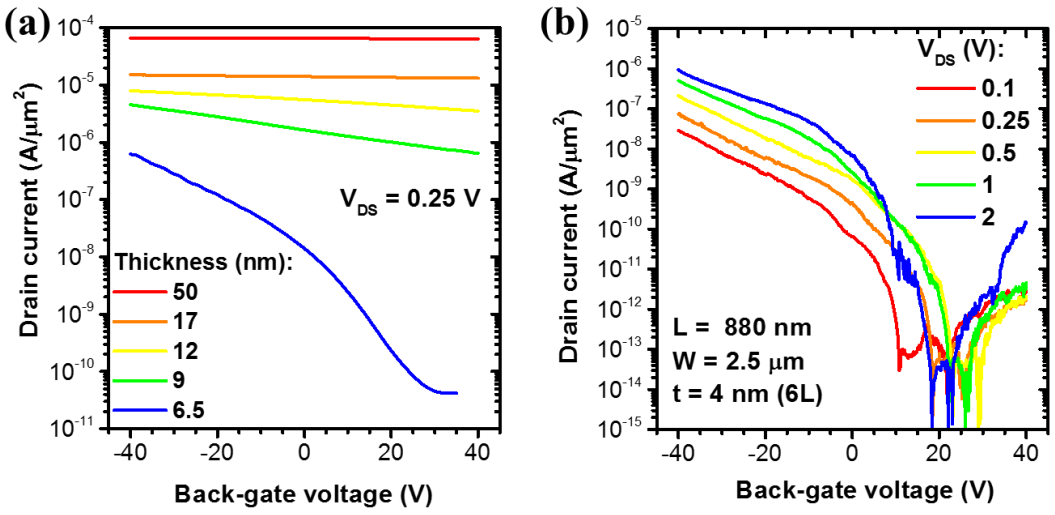


**Figure 5: (a) Transfer characteristics of each device studied in this work. There is a clear dependence of the $I_{ON}/I_{OFF}$ ratio with thickness because of the high doping concentration and the inability to completely deplete the channel. (b) Transfer characteristic of a thinner Nb-doped $MoS_2$, showing much higher defective behaviour.**

To further compare the behaviour of $MoS_2$ p-type doped FETs it is necessary to consider the output characteristics of thinner flakes as well. Figure 6a and 6b compares the $I_{DS}$-$V_{DS}$ curves for different back-gate voltages of the 12 nm and 5 nm thick $MoS_2$ devices respectively. While the curves in Figure 6a are linear, the curves in Figure 6b have more of an exponential behaviour, which means that the carrier transport mechanism is different. There are three main mechanisms that dominate carrier transports at the contacts. If a small Schottky barrier is present, then thermionic emission dominates the transport, and the $I_{DS}$-$V_{DS}$ curve can be modelled with the Richardson-Schottky equation:

$$I_D \propto A \times T^2 \exp\left[\frac{-\phi_B + \sqrt{q^3 V_D / 4\pi\varepsilon_0\varepsilon_r d}}{k_b T}\right] \quad (3)$$

where $V_D$ is the drain voltage, T is the temperature, $\phi_B$ is the Schottky barrier, q is the elementary charge, $k_B$ is the Boltzmann constant, d is the width of the barrier, $\varepsilon_0$ and $\varepsilon_r$ are the absolute dielectric constant and the dielectric constant of the semiconductor, respectively. Therefore, the plot of $\ln(I_D)$ against $V_D^{1/2}$ is expected to have a linear dependency. Instead, in case of a high and wide barrier the transport is described by the Fowler-Nordheim tunnelling:

$$I_D \propto V_D^2 \exp\left[\frac{-4d\sqrt{2m\phi_B^3}}{3\hbar q V_D}\right] \quad (4)$$

where m is the carrier effective mass and $\hbar$ is the Plank constant. In this case $\ln(I_D/V_D^2)$ versus $1/V_D$ is expected to have a linear behaviour with a negative slope. If the barrier is instead thin enough for direct tunnelling, the curve is expected to have a logarithmic growth considering $\ln(I_D/V_D^2)$ versus $1/V_D$. Therefore a linear positive trend considering $\ln(I_D/V_D^2)$ versus $\ln(1/V_D)$.

Figure 6c shows the output characteristic of the 12 nm thick $MoS_2$ plotted as $\ln(I_D/V_D^2)$ versus $1/V_D$. Since they clearly show linear behaviour we can conclude that, as expected, this device is dominated by the resistance of the semiconductor and direct tunnelling model dominates at the contact. Instead Figure 6d shows the output characteristic of the 4 nm thick $MoS_2$ plotted as $\ln(I_D)$ versus $V_D^{1/2}$. Due to its linear behaviour, it is clear that a Schottky barrier is present and thermionic emission dominates the transport.

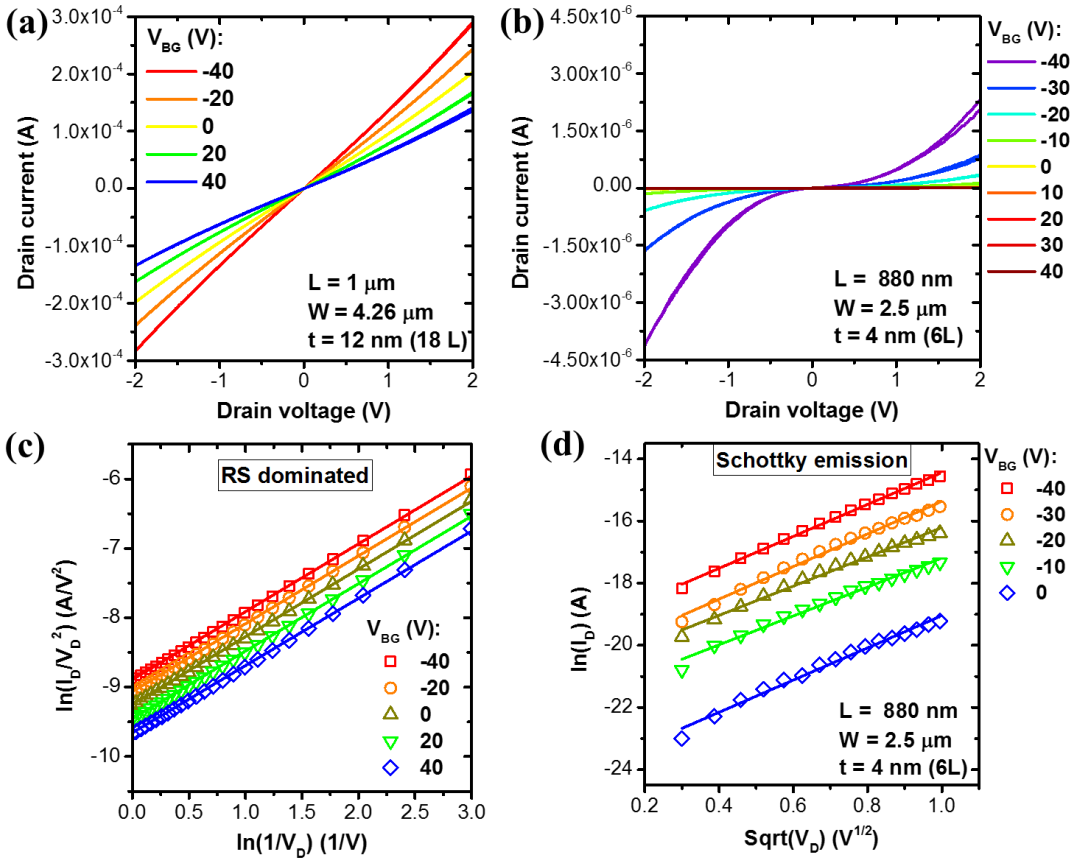


**Figure 6: Output characteristics of the (a) 12 nm thick device and (b) 4 nm thick device. The output characteristic of the 12 nm thick device can be modelled considering direct tunnelling, which means that the behaviour is dominated by the resistance of the semiconductor (RS). Instead, the 4 nm thick sample can be modelled considering the Richardson-Schottky equation, pointing to a Schottky emission behaviour.**

This same analysis was applied by Liu et al.[219] studying the contact behaviour of chemically doped $MoS_2$ transistors. In that case, a doped multilayer $MoS_2$ was dominated by Fowler-Nordheim tunnelling at small gate bias and direct tunnelling at higher gate bias. For the case of the 12 nm thick device we only see direct tunnelling, as there is almost no gate action, due to the high doping and thickness of the device. Instead, considering the 4 nm thick device, the behaviour is always fitted with a Schottky emission model because of the barrier present at the contacts.

Therefore, although there is a noticeable improvement of the contact behaviour for highly doped $MoS_2$, still there are some difficulties to appreciate this for thinner

devices. This can be related to the cleanliness of the contact. As said before, contact studies on $MoS_2$ devices have shown an $O_2$ plasma exposure of the contact area can remove unwanted PMMA residues. The AFM image in Figure 1b shows what are potentially photoresist residues on the $MoS_2$ surface and at the $MoS_2$-metal interface. In our work, thick devices don't seem to be affected by these residues, but thinner devices might be more sensitive. The higher sensitivity can be related to the effective contact area of the device, since the barrier height and width is set by the band alignment and doping level. When the $MoS_2$ thickness is higher than the maximum depletion width the effective contact area is the full metal area, as it can be accessed from below the contact in the quasi neutral region of the $MoS_2$. In the case of the fully depleted sample the contact area approximates to the product between the width of the device and the thickness of the $MoS_2$.

## 4.7 CONCLUSIONS

In conclusions, without any treatment of the metal-$MoS_2$ interface, device performances are usually poor and characterised by high variability. Among other techniques, high doping can be a solution in order to drastically reduce the contact resistance at the source/drain region. However, other process techniques, such as annealing treatment, surface cleaning, or chemical doping, are necessary in order to maintain a good contact behaviour at low thickness.

# Chapter 5: EFFECTS OF ANNEALING TEMPERATURE AND AMBIENT ON METAL-$PtSe_2$ INTERFACE

This chapter is adapted from the following publications and conferences:

**Mirabelli, G.**; Walsh, L. A.; Gity, F.; Bhattacharjee, S.; Cullen, C. P.; Ó Coileáin, C.; Monaghan, S.; McEvoy, N.; Nagle, R.; Hurley, P. K.; Duffy, R., Effects of Annealing Temperature and Ambient on Metal/$PtSe_2$ Contact Alloy Formation. ACS Omega 2019, 4 (17), 17487-17493

Walsh, L. A.; **Mirabelli, G.**; Cullen, C. P.; Gity, F.; O'Coileain, C.; Monaghan, S.; Schmidt, M.; Nagle, R.; McEvoy, N.; Duffy, R.; Duesberg, G.; Hurley, P. K., Investigating contact resistance to $PtSe_2$ using forming gas annealin, WODIM, Berlin, 2018;

**Mirabelli, G.**; Walsh, L. A.; Gity, F.; Bhattacharjee, S.; Cullen, C. P.; Ó Coileáin, C.; Monaghan, S.; McEvoy, N.; Nagle, R.; Hurley, P. K.; Duffy, R., Effects of annealing temperature and ambient on metal-$PtSe_2$ contact alloy formation", European Material Research Society, Nice, France, 2019;

## 5.1 INTRODUCTION

Although promising, the integration of TMDs with other semiconductors is still limited due to (1) the lack of low temperature and wafer-scale uniform growth processes and (2) due to the rather large Schottky barrier that usually characterizes the metal/TMD interface, which limits the device behaviour and masking their full potential.

The lowest values of contact resistance are usually related to high-*k* induced doping, or interface engineering.[211-214] Another possible solution still mostly unexplored is the use of an opportune annealing step to modify the metal/TMD interface. Annealing is a common process step in the modern semiconductor industry. Laser annealing is used for Si and Ge to achieve highly doped and abrupt junctions.[234] Additionally, annealing in forming gas has been used to reduce the density of fixed oxide charges and interface states at the $Al_2O_3$/InGaAs interface.[235] Similarly, for 2D-semiconductors several publications have shown how different annealing steps can improve the performances of TMD-based devices. Vacuum annealing has been shown to reduce the concentration of surface contaminants.[236, 237] Furthermore, annealing in an inert environment or forming gas can be beneficial in terms of reducing the density of interface states at the $MoS_2$-oxide interface.[233] Annealing steps have also been shown to be valuable for the TMD/metal interface. Forming gas annealing (FGA) on graphene/$MoS_2$ contacts was shown to improve the contact resistance of the material system.[238] Other annealing techniques, such as vacuum annealing,[226] microwave annealing[227] or short-term pulsed annealing,[228] were also reported to be advantageous for the metal/$MoS_2$ interface. Nonetheless, the values are still far from the requirement of the IRDS roadmap, and the reaction metal-TMD upon annealing as well as the optimal annealing temperature range and ambient is still unclear.

In this chapter large area grown thin films of $PtSe_2$ are characterised considering different post-growth thermal treatments and their effects on the metal/TMD interface. $PtSe_2$ has attracted increasing interest over the last few years. Interestingly, it shows semi-metallic characteristics in its bulk form, while experiments have shown the opening of a bandgap for thicknesses lower than 3 nm.[239, 240] Therefore, $PtSe_2$ has gained attention due to its potential application in electronics,[241] optoelectronics[242] and sensors.[243] $PtSe_2$ is grown by thermally assisted conversion (TAC) which does not require a high thermal budget (max temperature of 400 $^oC$). This makes the growth compatible with back-end-of-line processing and integration in modern technologies, as it respects the typical thermal budgets of the CMOS Industry (~450 $^oC$).[51-53] This is in sharp contrast with TMD films grown by chemical vapour deposition, chemical vapor transport or molecular beam epitaxy.[31, 32, 34, 244] The growth is not homogenous, and it is characterized mainly by triangular crystals that merge together after a sufficient growth time.[35, 36, 38] Above this, the thermal budget of these processes is usually high to obtain a reaction of the pre-deposited film with the chalcogen, limiting their integration in modern CMOS technology.

The $PtSe_2$ was grown at 400 $^oC$ over a large area. Ti/Au and Ni/Au were used as metal contacts and circular transfer length method (c-TLM) structures were used to electrically characterize the metal/$PtSe_2$ interface and the $PtSe_2$ material itself. The samples were then annealed for 1 hour in a forming gas ambient (5/95% $H_2/N_2$) at different annealing temperatures: 150 $^oC$, 250 $^oC$ and 350 $^oC$. The same experiment was repeated in an inert environment (0/100% $H_2/N_2$). The electrical properties of the material were studied after each annealing step. The TMD-metal interface and alloy formation were studied and characterized by a combination of X-ray photoelectron

spectroscopy (XPS), Raman spectroscopy, energy-dispersive X-ray spectroscopy (EDX) and cross-sectional transmission electron microscopy (XTEM).

## 5.2 EXPERIMENTAL

All $PtSe_2$ samples were grown over large area using a TAC process.[49, 50] Pt metal is evaporated onto a $SiO_2$/Si substrate. This was then converted in a furnace with a Se pressure of ~1 mbar at 400ºC. The specifics of the growth are discussed in detail elsewhere.[50]

Since the $PtSe_2$ sample come from the same growth run and are highly consistent, applying a similar FGA step allows the effect of the process on the material itself and the metal-TMD interface to be decoupled. c-TLM metal contacts were patterned using standard photolithography followed by e-beam evaporation of the metal and a lift-off process. For these devices the targeted thicknesses were 10/90 nm for both Ti/Au and Ni/Au at a background pressure of ~$10^{-5}$ mbar. For the XPS samples the targeted thicknesses were 3 nm for both Ti and Ni. No Au was used in the XPS samples as it does not interface with the $PtSe_2$ film and the added metal thickness would exceed the photoelectron escape depth (of ~ 5nm). After an initial characterization each sample was cleaved into 3 pieces to maintain consistency. Forming gas anneals were performed at 150 ºC, 250 ºC and 350 ºC for 1 hr using 5% $H_2$/ 95% $N_2$. The same annealing conditions were applied again in an inert environment (0% $H_2$/ 100% $N_2$).

XPS characterization was performed using monochromated Al Kα X-rays from an Omicron XM1000 MkII X-ray source and Omicron EA125 hemispherical analyzer with ±0.05 eV resolution. A take-off angle of 45°, acceptance angle of 8°, and pass energy of 15 eV were employed during spectral acquisition. The binding

energy scale was referenced to the adventitious carbon species in the C 1s core level (285.8 eV). Spectra were deconvolved using AAnalyzer,[245] a curve fitting software.

For structural analysis, cross-section samples were obtained by using the Dual Beam Helios Nanolab 600i system from FEI, using a Ga ion beam. Layers of the protective material were used consisting of electron beam deposited C, Pt, and ion beam deposited C. Lamellas were thinned and polished at 30 kV 100 pA and 5 kV 47 pA, respectively. XTEM imaging was carried out using a JEOL 2100 HRTEM, operated at 200 kV in the bright field mode using a Gatan Double Tilt holder. EDX mapping was carried out using a Thermo Fisher scientific Titan Themis operated of 300kV in STEM mode using the Bruker superX Silicon Drift detector.

## 5.3 EXPERIMENTAL RESULTS

Figure 1 shows the process flow adopted to study the reaction of $PtSe_2$ after each annealing step. First, $PtSe_2$ (with an initial thickness of 1 nm) was grown on 4 different samples in a single growth run for high consistency. c-TLM structures were defined and the samples were then measured electrically. The presence of $PtSe_2$ was confirmed by Raman analysis.[246]

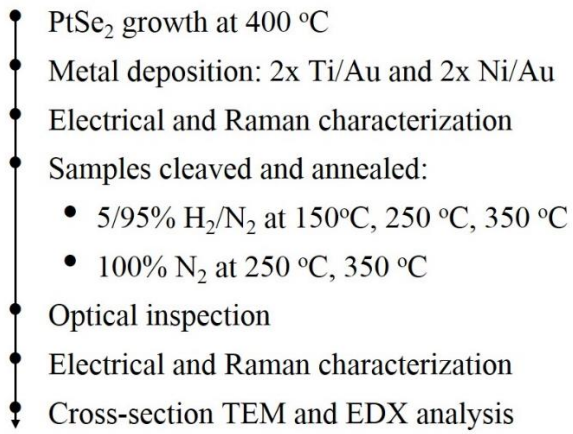


**Figure 1: Experimental steps taken during this work.**

Figures 2a and 2d show the optical microscope images of the contacted $PtSe_2$ with Ti and Ni contacts respectively before any annealing and no visible differences are present between the two samples. The samples then underwent different annealing steps. No obvious differences were found for the samples annealed in forming gas at 150 °C, as the temperature might have been too low to start any reactions. After annealing at 250 °C in forming or inert environment the Ti/Au sample did not show any appreciable differences from optical inspection (Figure 2b and c). On the contrary, the Ni/Au sample annealed at 250 °C in forming gas displayed what looks like an "alloy region" around the metal contacts (Figure 2e). This alloy region is less pronounced for the annealing at the same temperature in the inert environment (Figure 2f). It is noted that the reaction taking place between Ni and $PtSe_2$ is accelerated by the presence of hydrogen during the annealing. The 350 °C anneal in forming gas (pictures not shown), as later confirmed by electrical and Raman characterizations, resulted in a degradation of the $PtSe_2$. Considering that $PtSe_2$ is grown at a temperature of 400 °C, a forming gas anneal at 350° C may be too harsh an environment for this

material, which highlights the importance of understanding the process window for optimal annealing temperature and its effects on the material properties.

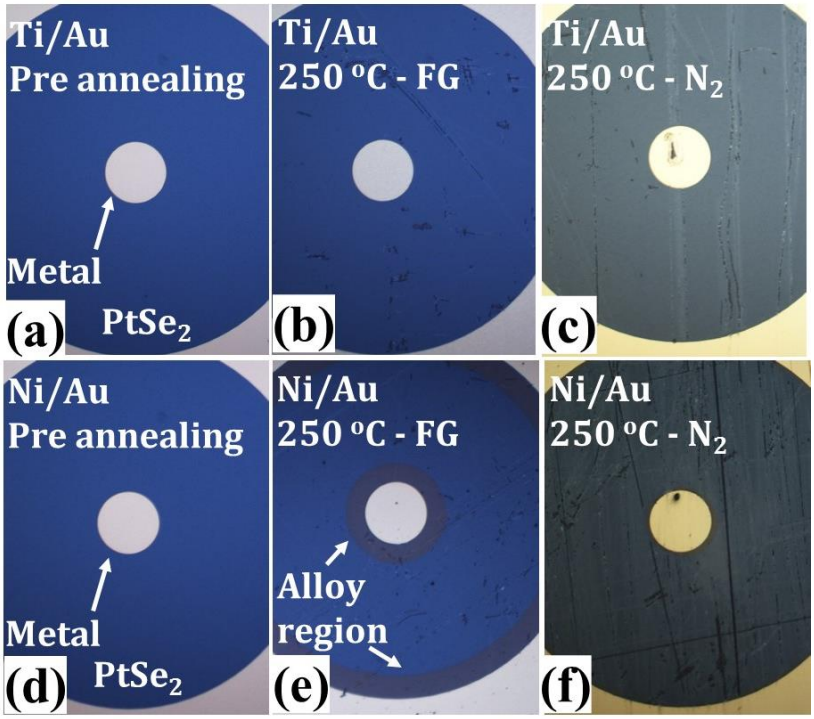


**Figure 2: Optical microscope pictures of the larger c-TLM of $PtSe_2$ before annealing contacted with (a) Ti/Au and (b) Ni/Au. Same optical pictures repeated after annealing in forming gas (FG) and inert ambient at 250 °C for (b, c) Ti/Au and (e, f) Ni/Au respectively. The darker gold ring in (e) clearly shows the alloy region.**

Figure 3 shows the electrical characterization carried out on each sample. Figure 3a shows representative current-voltage measurements on the Ni/Au samples considering a spacing of 43.5 µm. Although no appreciable differences are visible from optical inspection after a forming gas anneal at 150°C, the current decreases with respect to the pre-annealed case. On the contrary, considering the same forming gas environment but a temperature of 250 °C the current increases, indicating that a reaction or process occurred which reduced the $PtSe_2$ resistivity and/or metal-$PtSe_2$ contact resistance. Considering the results in Figure 3c, the $PtSe_2$ for the Ti/Au contacts, the forming gas anneal does not influence the $PtSe_2$ sheet resistance. These

combined results indicate that in the case of the Ni/$PtSe_2$ sample the forming gas anneal is reducing the resistance of the metal-$PtSe_2$ contact. Because the Ni diffusion/reaction with PtSe2 changed the spacing of the structure, the results at 250 $^oC$ in forming gas were corrected, changing the value of the spacing of each structure with the actual channel length. The anneal at 250 $^oC$ in an inert environment and the anneal at 150 $^oC$ in forming gas resulted in a lower current. These two anneal conditions seem to provide similar results. Although one was done at a lower temperature, the presence of forming gas seems to have accelerated the reactions that took place. It is also important to consider that the 250 $^oC$ in the inert environment also resulted in an alloy region, although not as pronounced as the case in forming gas. On the contrary no alloy regions were found for the sample annealed at 150 $^oC$ in forming gas.

Figure 3b shows the total resistance versus spacing for the Ni-Au contacted $PtSe_2$ at each annealing step. It is clear that each annealing is affecting the electrical behavior of the device. Nonetheless, this analysis is problematic for the Ni/Au samples. Due to the presence of the alloy region, the fitting process is less reliable since the spacing of the structures change with the annealing condition. Future work may include linear TLMs with smaller dimensions for a more accurate parameter extraction. Figure 3c shows the same analysis for the Ti/Au sample for each annealing condition. No appreciable differences are present, and the trend remains quite similar, meaning that the film itself, as well as the $PtSe_2$-Ti interface, are not affected by any annealing steps.

Figure 3d shows the sheet resistance extracted from each measurement. The sheet resistance can be extracted from the Ti/Au measurements considering the c-TLM

theory.[247] However, for the Ni/Au samples the total resistance was considered as the resistance of the $PtSe_2$ owing to the low contact resistance. The results for the Ti/Au contacts confirm what is seen in Figure 3b: the annealing temperature and conditions are not changing the metal-$PtSe_2$ interface or the $PtSe_2$ material itself. On the contrary, a much higher variation is seen for the Ni/Au samples, which can be related to the reaction between Ni and $PtSe_2$. Consider that, although obvious "alloy regions" are present from optical inspection it is possible that the Ni diffuses much further into the $PtSe_2$, than what is possible to see with an optical microscope.

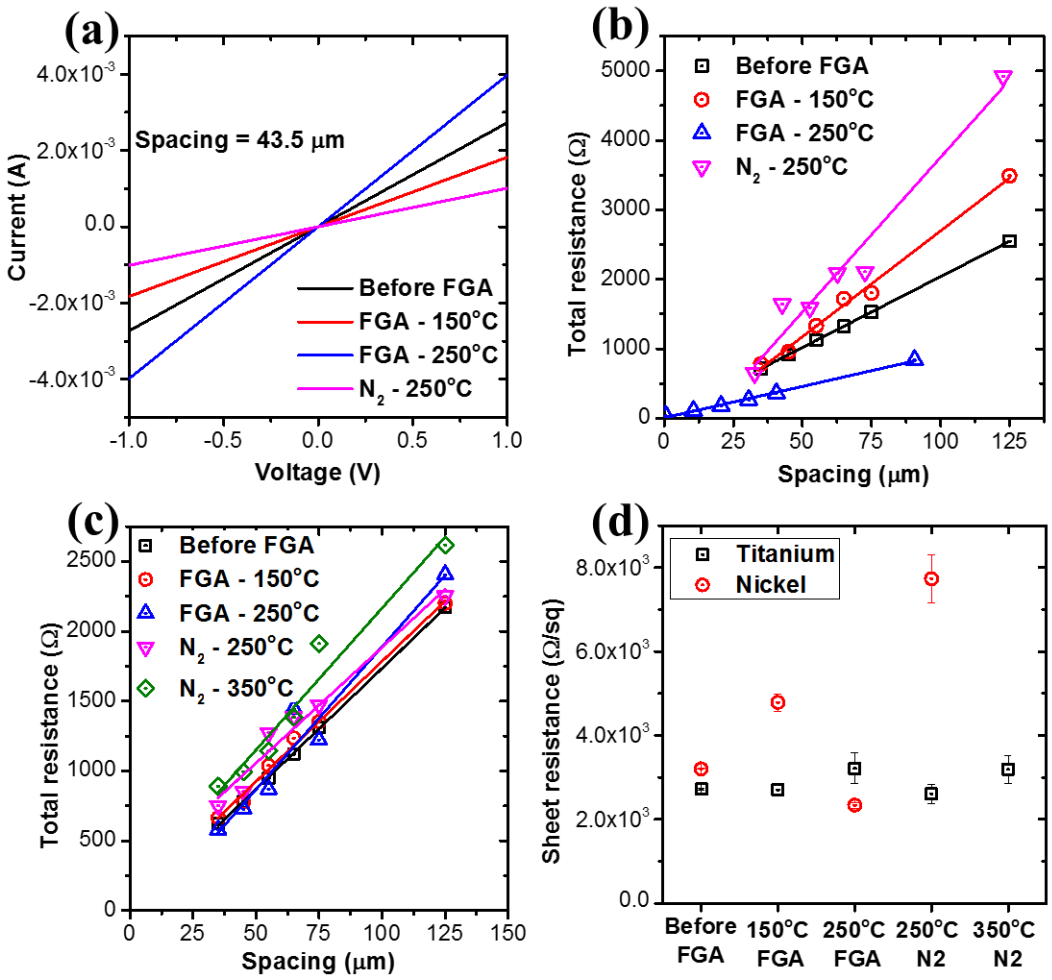


**Figure 3: (a) Current-voltage measurements on the Ni/Au samples after each annealing step. (b) Total resistance versus spacing for the (b) Ni/Au and (c) Ti/Au contacted $PtSe_2$. (d) Extracted sheet resistance after each annealing step.**

A Raman spectroscopy was then performed to confirm the integrity of the $PtSe_2$ and to probe the "alloy region" seen in the Ni/Au samples. The results are summarised in Table 1. In particular, the Raman signal was collected on the bare $PtSe_2$ and near the metal contact. For the Ti/Au sample the signal of $PtSe_2$ is always present, except for the 350 $^oC$ annealing in forming gas, which resulted in degradation of the $PtSe_2$ film. Similarly, for the Ni/Au sample a clear $PtSe_2$ signal is present up to 250 $^oC$, in both forming and inert gas environment in the bare $PtSe_2$ regions (far from the metal contact). For the samples that showed an "alloy region" no $PtSe_2$ signal is present close to the metal contact, suggesting metal interdiffusion and alloying.

**Table 1: Summary of the Raman analysis on the $PtSe_2$ samples after each annealing condition.**

| Annealing condition | Raman peaks of $PtSe_2$ | |
|---|---|---|
| | Ti/Au | Ni/Au |
| 150 $^oC$ 5/95% $H_2/N_2$ | Present | Present |
| 250 $^oC$ 5/95% $H_2/N_2$ | Present | Present, except in diffusion ring |
| 350 $^oC$ 5/95% $H_2/N_2$ | Absent | Absent |
| 250 $^oC$ 100% $N_2$ | Present | Present |
| 350 $^oC$ 100% $N_2$ | Present | Absent |

Figure 4 shows representative TEM images of the Ni/Au contacted $PtSe_2$ samples annealed at 250 $^oC$ in forming gas and in an inert environment. Figure 4a and 4b compare the $PtSe_2$ structure inside and outside of the alloy region, respectively. It is noted that the layered structure is present outside the alloy region, while it is not inside it. Similarly, Figure 4c and d show the $PtSe_2$ below the metal contact and outside of it, respectively. Again, the layered structure is not present below the metal contact

but is preserved outside of it. These representative images confirm the hypothesis. The diffusion ring seen from optical images is a result of Ni interdiffusing and alloying with the $PtSe_2$. This compound is not characterized by the same layered structure of $PtSe_2$, but it has the form of a 3D alloy. Also, although the alloy region around the contact is not present in the sample annealed at 250 $^oC$ in an inert environment, a similar reaction has taken place below the metal contact. Therefore, it can be concluded that the presence of hydrogen accelerates the reaction, and the Ni can react more readily with $PtSe_2$ away from the metal itself.

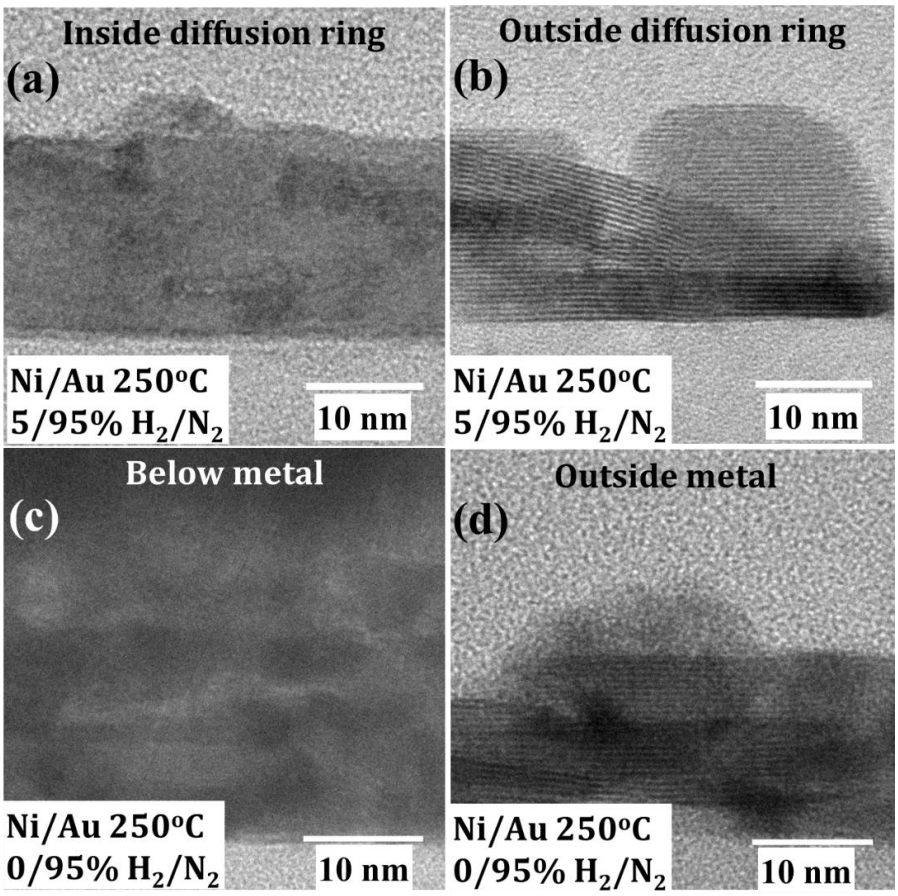


**Figure 4: Representative cross-section TEM images of the $PtSe_2$ contacted with Ni/Au. (a) and (b) show the $PtSe_2$ after annealing in forming gas at 250 $^oC$ inside and outside the diffusion ring respectively. (c) and (d) show the $PtSe_2$ after annealing in inert environment at 250 $^oC$ below the metal contact and outside the metal contact respectively.**

In order to explore the nature of the interdifussional alloying observed an XPS was performed using near-identical samples. Figure 5 shows XPS spectra of the Pt 4*f* and Se 3*d* core levels of $PtSe_2$ before and after metal deposition, with no further annealing. No Au was used here as Au does not interface with the $PtSe_2$. The Pt 4*f* spectra for bare $PtSe_2$ (Figure 5a) shows the presence of two chemical states, both represented by a doublet, one related to $PtSe_2$ (72.15 eV) and another due to surface oxidation ($PtO_x$ at 71.1 eV). The Se 3*d* spectra of the same sample (Figure 5c) show $PtSe_2$ and $SeO_x$ features (53.55 eV and 54.25 eV, respectively), with the additional contribution of the Pt $5p_{3/2}$ (52.6 eV), which overlaps with the Se 3*d*.

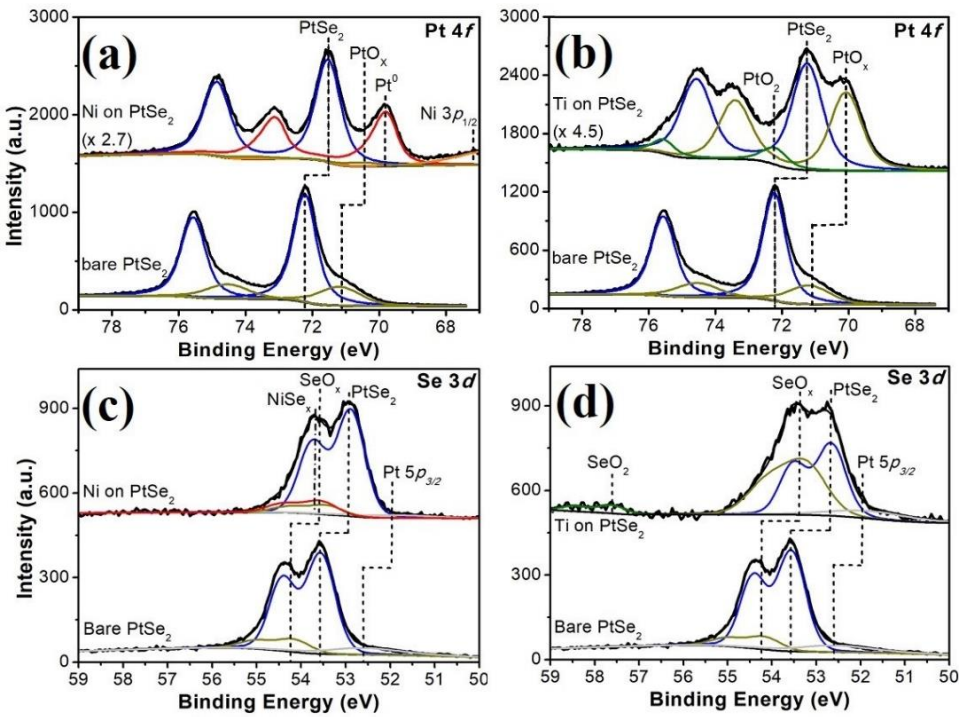


**Figure 5: XPS spectra of (a), (b) Pt 4f and (c), (d) Se 3d core levels for $PtSe_2$ before and after Ni or Ti deposition.**

Upon Ni deposition a significant change in the peak shape of the Pt 4*f* is observed, with the emergence of a feature at low binding energy (BE). This peak is at lower BE than $PtO_x$, consistent with metallic Pt ($Pt_0$). The Se 3*d* spectrum shows a

subtler change with broadening to higher BE, attributed to the possible formation of a Ni-Se compound ($NiSe_x$). The Ni 2*p* spectra are difficult to interpret due to the presence of several satellite features. Although a shift to higher BE is observed compared to a reference Ni film, which could be due to Ni oxidation or the reaction between Ni and another high electronegativity element such as Se. Taken together this suggests the reduction of $PtSe_2$ by Ni, resulting in $NiSe_x$ formation, and Pt metal.

In the case of Ti, a much more subtle change in chemical state is observed. After Ti deposition, the $PtO_x$ peak increases significantly and is accompanied by a higher BE feature consistent with $PtO_2$. The Se 3*d* also shows a significant increase in oxidation with an increase in $SeO_x$ and the appearance of a higher BE $SeO_2$ peak. The Ti 2*p* spectra (not shown) show the complete conversion of Ti to $TiO_2$, which is expected due to the oxygen-gettering nature of Ti. The presence of excess oxygen in the $TiO_2$ film in turn oxidizes the underlying $PtSe_2$.

Lastly, to confirm the presence of Ni in the reacted region, EDX was conducted on the TEM cross-section lamellas prepared with the Ni/Au contacted devices before and after annealing at 250 $^oC$ in both forming gas and inert environment at 250 $^oC$. Figure 6 shows the compositional analysis performed via scanning transmission electron microscopy (STEM) based energy dispersive x-ray spectroscopy (EDX). Figure 6a and 6f shows the high-angle annular dark-field images (HAADF) of the region under study, which is at the edge of the metal contact. Figure 6 b-d and g-j show the spectra for Au, Pt and Se. No significant interdiffusion is observed for these elements after annealing, and the mapping results are fairly similar. Considering that Au and Pt have a similar atomic weight, what would seem to be diffusion of Pt in Au is actually just an artefact from the EDX. This is not an issue as the focus is on the

behaviour of Ni with $PtSe_2$. Figures 6e and 6j show clear Ni diffusion upon annealing. Before annealing the Ni spectra is clearly confined between the $PtSe_2$ and the Au region. While after $N_2$ annealing, significant diffusion of Ni into the Au and $PtSe_2$ regions is observed. This is consistent with the diffusion seen in the optical images of c-TLM structures (Figure 2).

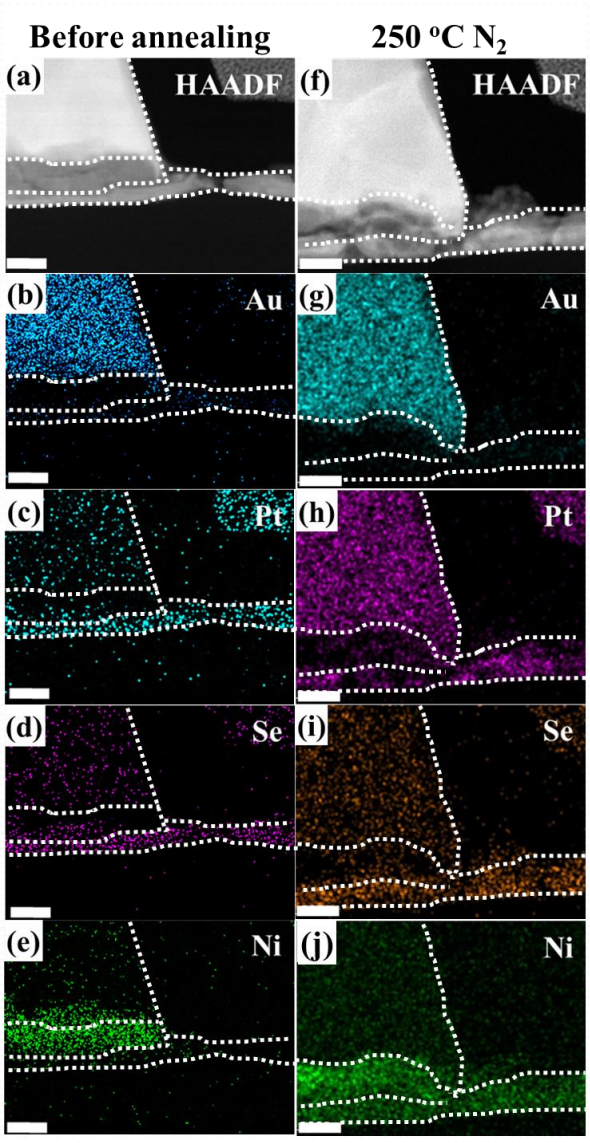


**Figure 6: Compositional analysis performed via STEM based EDX on Ni-Au contacted $PtSe_2$ lamellas before and after annealing at 250 °C in $N_2$. (a) and (f) shows the HAADF image of the region under study before and after annealing respectively. b-e and g-l refer to the Au, Pt, Se and Ni signal, before and annealing respectively. Scale bar is 25 nm. The dotted lines are added around the Au, Ni and $PtSe_2$ regions to guide the eye.**

## 5.4 DISCUSSION

The interaction between top contacts and TMDs is significantly different to contacts on conventional semiconductors due to the Van der Waals nature of the TMD surface. DFT simulations predict that due to the lack of surface covalent bonds for most deposited metals a van der Waals gap exists between the TMD surface and the metal contact.[248] This van der Waals gap acts as a tunnel barrier for carrier injection into the TMD channel, in addition to the Schottky barrier between the metal and TMD,[126] increasing total contact resistance.[50]

A study by Das et al.[135] showed that the Schottky barriers between metals and $MoS_2$ are not consistent with the energy difference between the metal work function and the TMD Fermi level. They showed that even metals which would be expected to act as *p*-type contacts (i.e. Ni and Pt) instead exhibited electron injection consistent with *n*-type contacts. This was ascribed to Fermi level pinning in the $MoS_2$ close to the conduction band minimum at the metal/$MoS_2$ interface.[142]

Previous XPS studies on $MoS_2$ and $WSe_2$ considering a range of various metals[249-252] have shown that similar reactions between the as-deposited metal and a TMD are possible. Nonetheless, an interface reaction does not necessarily result in a lower contact resistance because of the defective nature of exfoliated TMD flakes. However, a complete transformation of the TMD below the contact might mitigate the effect of contact resistance. Kappera et al.[213] demonstrated low contact resistance in a $MoS_2$ FET varying the phase of $MoS_2$ below the contact from semiconductive (2H) to metallic (1T). Similarly, here we showed a Ni-$PtSe_2$ alloy at the contact and $PtSe_2$ in the channel region. However, in this work, a contact resistance analysis was not possible. The $PtSe_2$ under study had a thickness of ~6-10 nm, and in this thickness

range the $PtSe_2$ behaves as a semimetal, therefore it is not contact-resistance limited. Once the $PtSe_2$ growth processes are tuned further to achieve few-layer (<3L) films a more detailed contact resistance study could be performed. Also, the annealing temperature and ambient need to be optimised in order to control the diffusion/reaction of Ni.

A behaviour similar to Ni and $PtSe_2$ has also been observed for $Ag/MoS_2$.[229] In that work, the samples were annealed between 250 $^oC$ and 350 $^oC$ in a rapid thermal annealing furnace for 300 s and the contact resistances values decreased after the thermal treatment, due to Ag diffusion and doping below the contact regions. Although Ag does not react with $MoS_2$ at room temperature,[253] Souder and Brodie[230, 231] showed that Ag diffused in bulk $MoS_2$ after annealing at 400-600 $^oC$ for 5 min, estimating a concentration of approximately $10^{19}$ $cm^{-3}$.

It is unclear if the Ni is acting as a dopant for $PtSe_2$, however, the metal-TMD reaction could be of great interest to improve the contact resistance of TMD-based devices.

## 5.5 CONCLUSIONS

In this study, the Ti-$PtSe_2$ and Ni-$PtSe_2$ interfaces were explored, along with the impact of post-metallisation anneals in forming gas and inert ambient. Electrical and chemical characterization show that Ti is unreactive after annealing, even at relatively high temperature, while Ni readily reacts with $PtSe_2$ to form $NiSe_x$ and reduced $PtSe_x$-Pt-metal. The reaction is enhanced with high temperatures or a hydrogen rich environment, which can cause the Ni to diffuse laterally into the $PtSe_2$.

The metal/$PtSe_2$ alloying is a possible solution for reducing contact resistance in few-layer devices based on $PtSe_2$ and other TMD materials.

# Chapter 6: TCAD MODELLING AND ANALYSIS OF $MoS_2$

This chapter is adapted from the following publications and conferences:

**Mirabelli, G.**; Gity, F.; Monaghan, S.; Hurley, P. K.; Duffy, R. In Impact of impurities, interface traps and contacts on $MoS_2$ MOSFETs: Modelling and experiments, 2017 47th European Solid-State Device Research Conference (ESSDERC), 11-14 Sept. 2017; 2017; pp 288-291.

**Mirabelli, G.**; Zhao, P.; Bolshakov, P.; McGeough, C.; Gity, F.; Monaghan, S.; Hughes, G.; Hinkle, C. L.; Wallace, R. M.; Young, C.; Hurley, P. K.; Duffy, R., Study of interface defects in top-gated $MoS_2$ FETs: experiments and physics based simulations, IEEE Semiconductor Interface Specialist Conference (SISC), San Diego (CA), 2017.

## 6.1 INTRODUCTION

Device modelling is a key capability for the semiconductor industry, allowing process optimization and insight into the physics of novel architectures and materials difficult to access experimentally. Despite much innovative experimental work, device modelling capabilities for field effect devices based on Transition Metal Dichalcogenide channel materials are at an early stage of development. Properly formulated physics-based models would give a substantial improvement for time- and cost-effective development of TMD devices. Nevertheless, a TCAD model for Transition-Metal-Dichalcogenides, or for 2D-materials in general, is still missing. To date few publications showed the effective use of TCAD modelling for the understanding of 2D-semiconductors.[167, 168, 254, 255] The immaturity of the material system itself causes a certain device-to-device variation, which makes even more difficult the development of a solid TCAD model. Even if the TCAD models on which these studies are based on might not be definitive, the simulations allowed a clear interpretation of the device physics, which would not be otherwise possible.

## 6.2 TCAD MODELLING FOR NEW MATERIAL SYSTEMS

The first step to start a TCAD analysis of any material is to load its "parameter file". This file contains all the necessary basic properties, such as: as bandgap, dielectric constant, band structure, mobility of electrons and holes, electron affinity, which are necessary to opportunely solve the drift-diffusion equations in the device. These parameters are widely known for Silicon, for example, since it is a well mature material system. On the contrary, new material systems as TMDs, graphene or GeSn

are not yet defined. For new material systems a deep literature search is needed to have a complete and accurate parameter set.

The second part is the study of the electrical behaviour of the device. In this case, physical models need to be defined in order to match the physics of the device under test with the experimental data. Considering Silicon as example again, there are several models in order to consider the temperature dependence of its bandgap. Or the Shockley-Read-Hall generation/recombination parameters can be made dependent on the doping concentration. All these physical effects and models are not present for 2D-materials and due to the immaturity of the material system these effects are still unknown. In the case of the above-mentioned examples of bandgap and Shockley-Read-Hall generation/recombination parameters, they will be considered constant. Nonetheless, particular attention was paid to the mobility of $MoS_2$. This parameter is often extracted and characterised in literature, so the TCAD software was used in order to implement these effects in the software and study the impact on the electrical performance. An important question to consider is if models defined previously for 3D-semiconductors work as well for 2D-semiconductors. A simple tuning of the fitting parameters of a mobility model might not be enough, but this will be seen in the later paragraphs.

When both the material, physical and electrical models are defined, the material needs to be connected with other semiconductors (e.g.: pn junctions), oxides (e.g.: FET), or metals (e.g.: metal contacts). These interfaces are mostly defective and characterised by interface traps or Schottky barriers, which needs to be tuned in order to finally match the device behaviour. The structure of this chapter follows this trend, as schematically depicted in Figure 1. First the material properties of $MoS_2$ will be

defined considering both theoretical and experimental studies. Then, a mobility model dependent on unintentional impurities and electric field will be studied. Finally, the developed model will be used to study the defects introduced by the oxide-semiconductor and metal-semiconductor interfaces to improve the modelling capabilities for $MoS_2$ field-effect devices.

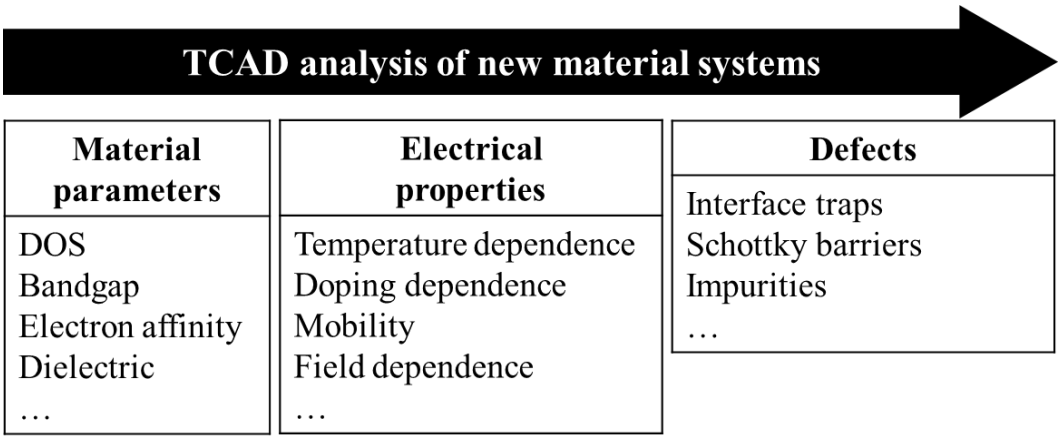


**Figure 1: General schematic showing the steps to undertake in order to develop an accurate TCAD model and analysis for new material systems: define the material parameters, the electrical properties, and finally introduce defects/imperfections.**

## 6.3 BASIC MATERIAL PARAMETERS

Figure 2a shows the variation of the carrier density versus Fermi energy for a single layer of $MoS_2$ and a good agreement is achieved with other studies.[256, 257] Figure 2b, 2c and 2d shows the bandgap[13], electron affinity[258-261], and effective mass variation[262-265] of $MoS_2$, respectively. In these three plots the solid lines show the values that were used in the model. Other parameters are the in-plane dielectric constant[266] and the carrier lifetime.[267] In addition, to model the transport the drift-diffusion equations including Fermi distributions are solved, as discussed in chapter 1.[200, 268] With the exception of the carrier density-Fermi Energy relationships

that is calculated by the TCAD software, the remaining parameters are input of the model and depend on previous theoretical studies or experimental findings.

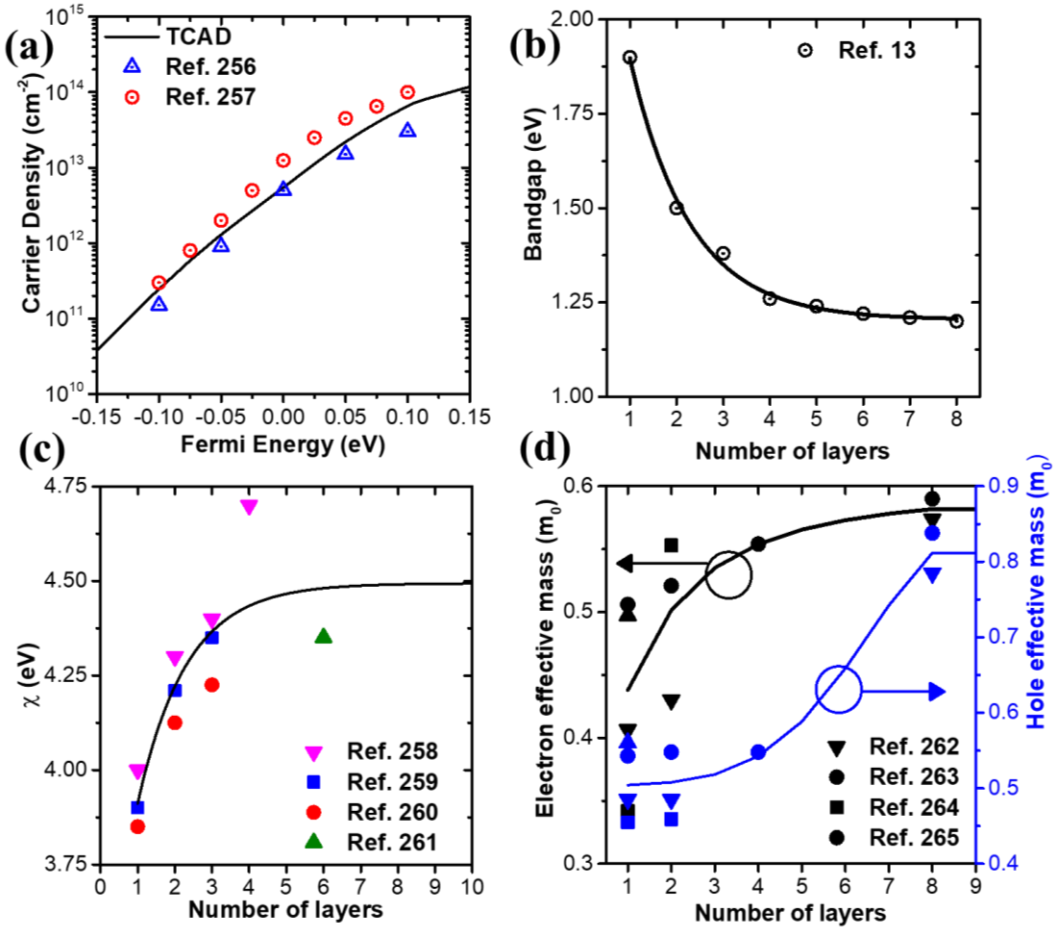


**Figure 2: (a) Carrier concentration variation with respect of Fermi energy of monolayer $MoS_2$ introduced in Sentaurus compared with literature. (b) bandgap, (c) electron affinity and (d) electron/hole effective masses introduced in Sentaurus. Every parameter is thickness dependent, considering either theoretical calculations or experimental results.**

Figure 3 shows a typical device structure implemented in Sentaurus device. The structure is generally set considering the experimental device under consideration.

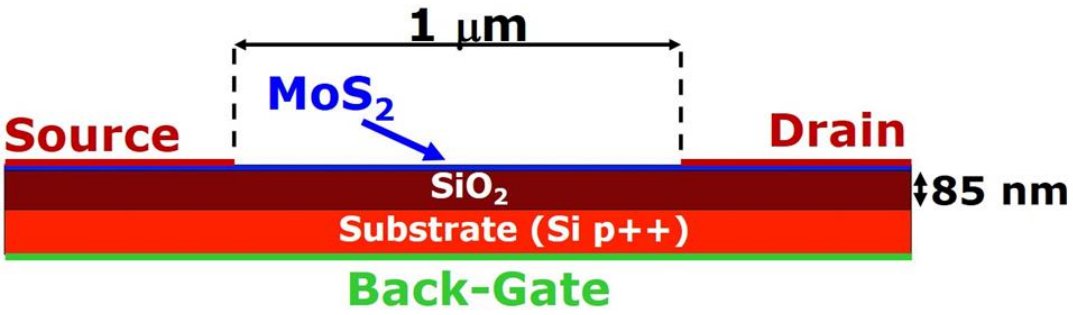


**Figure 3: Schematic of a typical back-gated device structure implemented in Sentaurus device**

## 6.4 MOBILITY MODEL

### 6.4.1 Low carrier density

The electron mobility in the low carrier concentration regime is highly dependent on the impurity concentration present in the material. This was reported to be one of the major scattering mechanisms is single layer $MoS_2$.[269] On this regard, Ma and Jena[92] calculated the mobility of single-layer $MoS_2$ in the relaxation-time approximation of the Boltzmann transport equation, considering the dependency of the dielectric environment and impurity density. This kind of scattering is similar to the one caused by a high doping concentration, since active dopants are charged scattering centres. The only difference is that doping will change the carrier concentration as well. The Arora model was used to take into account this dependency:[270]

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + ((N_{A,0} + N_{D,0})/N_0)^{A^*}} \qquad (1)$$

where $\mu_{dop}$ is the mobility dependent on Coulomb impurities, $N_{A,0}$ is the acceptor concentration, $N_{D,0}$ is the donor concentration and $A^*$, $\mu_{min}$ and $\mu_d$ are fitting

parameters. Figure 4 shows the theoretical model and the TCAD model implemented in Sentaurus. Even if this model was developed for silicon, varying the fitting parameters it is possible to obtain the same behaviour for monolayer $MoS_2$. Clearly mobility is highly limited by the impurity density in the material, as said before. It is also important to notice the mobility dependency on the dielectric environment, since a high-k environment will heavily affect it. This is important especially for FET applications. If one chooses a high-k dielectric to boost gate control, there is a clear drawback in terms of mobility.

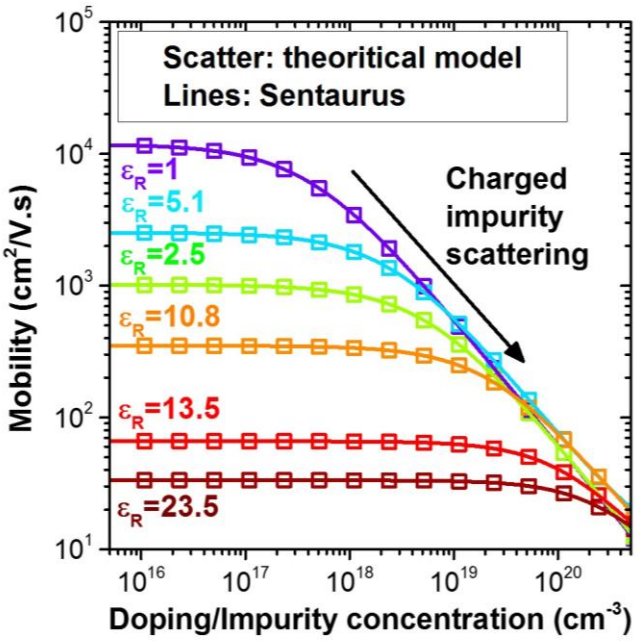


**Figure 4: (a) Mobility versus impurity concentration considering different parameters implemented using the Arora mobility model. The theoretical model is based on DFT calculations for $MoS_2$,[92] while the lines are the results obtained with the TCAD model.**

Table 1 reports the value of each fitting parameter considering each curve in Figure 3. The maximum mobility is obtained for a dielectric environment of 1 (suspended $MoS_2$), around $10^4$ $cm^2/V.s$. This value is rather higher than the

experimental values usually reported. Nonetheless, it can be related to both an immaturity of the material system and a possible overestimation of the theoretical mobility.

**Table 1: Fitting parameters for the Arora model to match the theoretical model of $MoS_2$.**

| $\varepsilon_R$ | $N_0$ [$cm^{-3}$] | A | $\mu_d$ [$cm^2/V.s$] | $\mu_{min}$ [$cm^2/V.s$] |
|---|---|---|---|---|
| **1** | $4.39\times10^{17}$ | 0.97 | 11803.22 | 0 |
| **2.5** | $6.03\times10^{18}$ | 0.98 | 1015.07 | 0.27 |
| **5.1** | $2.78\times10^{18}$ | 0.99 | 2518.34 | 5.84 |
| **10.8** | $2.67\times10^{19}$ | 1.01 | 347.74 | 2.43 |
| **13.5** | $1.38\times10^{20}$ | 1.10 | 62.00 | 4.05 |
| **23.5** | $3.36\times10^{20}$ | 1.14 | 30.30 | 3.09 |

### 6.4.2 **High vertical electric field**

Another cause of mobility degradation is related to high vertical field. $MoS_2$ has shown a high critical electric field of $1.15\times10^5$ $V.cm^{-1}$.[271] However, a strong vertical electric field will shift the charges close to the charged defects associated with the gate dielectric, increasing the scattering rate for carriers degrading the mobility. The data reported in the previous chapter are not useful to evaluate this contribution because of the low electric field applied on the back gate. Nevertheless, a model that takes into account the mobility degradation due to high vertical electric field was reported in literature.[200] Therefore, the results from this report will be used as benchmark to tune the TCAD model. The vertical electrical field degradation model depends on an empirical mobility model developed for Si MOSFETs,[201] similarly to

the model introduced with Sentaurus Device. It considers the mobility degradation observed at the $HfO_2$-semiconductor interface,[202] which was attributed to remote phonon scattering:

$$\mu_{rps} = \frac{\mu_{rps0}}{\left(\frac{F_{\perp}}{10^6\, V/cm}\right)^{\gamma_1}\left(\frac{T}{300K}\right)^{\gamma_2}} \tag{9}$$

where $\mu_{rps0}$, $\gamma_1$ and $\gamma_2$ are fitting parameters and $F_{\perp}$ is the actual vertical field. T is the temperature. This model was validated against experimental results (with T= 300 K), as shown in chapter 3.3.2. Figure 5a shows the extraction of $\gamma_1$ from experimental data and the relationship with the dielectric constant. Figure 5b show the numerical calculation of Equation 9 and the impact of $\gamma_1$ on the mobility degradation. The mobility degradation rate increases for increasing values of $\gamma_1$, therefore low values can be beneficial to avoid low mobility values at high vertical field.

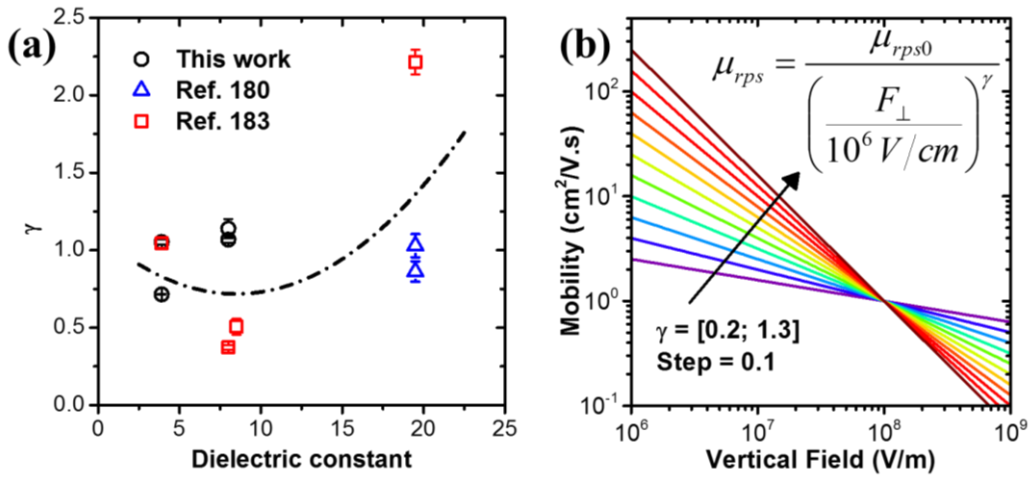


**Figure 5: Model for high vertical electric field proposed in literature[200] and Sentaurus results using the remote phonon scattering model.**

## 6.5 APPLICATION OF THE DEVELOPED MODEL

In the next sections the developed model will be used to understand and quantify the two typical limitations of FET based $MoS_2$ devices: the $MoS_2$-metal interface and the $MoS_2$-oxide interface. Although a fairly good agreement between simulations and experiments is obtained it is important to remember that both the developed model and the material itself are immature. More work from both the theoretical and experimental side will be needed in order to develop a complete TCAD model and extract precise material parameters. Nonetheless, the following analyses give a fair understanding of the main mechanisms limiting the experimental devices, which can be used not only to understand the physics behind a certain behaviour, but are also useful to steer possible experimental plans.

### 6.5.1 $MoS_2$-metal: contact barriers

As shown in chapter 1, the metal-TMD interface often results in high Schottky barriers. Figure 6a shows high energy XPS measurements conducted on $MoS_2$ crystals considering different metals. Even if the workfunction of the metals ranges considerably, the Fermi level at the metal-$MoS_2$ interface pin at approximately the same energy, ≅0.2 eV below the conduction band. The value that will be later used to match the experimental results of the device "Trapezium" (Chapter 3) is 0.17 eV, which is close to experimental values.[142]

Figure 6b shows the effect of the barrier on the simulated transfer characteristic of a typical back-gated single layer $MoS_2$, with doping concentration of $10^{17}$ $cm^{-3}$. It is easy to notice that a decrease in the Schottky barrier would result in a great improvement of the overall behaviour of the device. Also shown is the case of using the Fermi-level pinning model. Considering a value of pinning of 0.2 and a work

function of 4.33 eV (Titanium), the result is similar to using a Schottky barrier of 0.6 eV (from Equations 5 and 6 of Chapter 1). That is because considering the said parameters, the equivalent barrier at the contact using the Fermi-level pinning model is ~0.6.

Therefore, for the sake of modelling the contacts, Schottky barriers will be considered as a variable for each device under consideration. The Fermi-level pinning model sets a fixed barrier height considering the pinning level, work function of the metal, electron affinity of the semiconductor and charge neutral energy level. Nonetheless, due to the variability of 2D-semiconductors, the actual barrier could differ from this value.

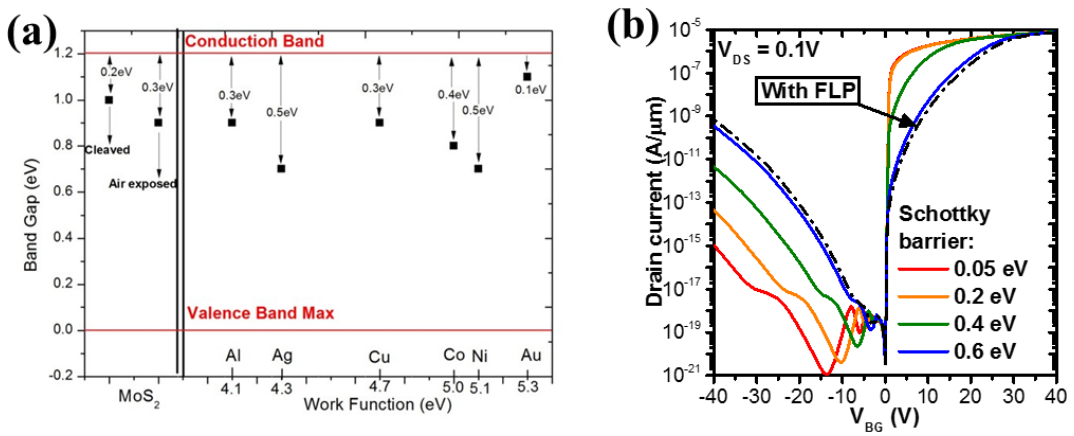


**Figure 6: (a) High energy XPS measurements conducted on $MoS_2$ crystals with different metals. (b) Simulated transfer characteristics varying the Schottky barrier at the source and drain contacts. The structure of the simulated device is as reported in Figure 2: 1L of $MoS_2$ with 1 μm of channel length.**

### 6.5.2 $MoS_2$-oxide: interface traps

#### 6.5.2.1 Back-gated $MoS_2$

The subthreshold behaviour of the device is dependent on interface traps located at the oxide/$MoS_2$ interface. To model the subthreshold slope of the experimental transfer characteristic, acceptor like interface states are introduced close

to the $MoS_2$ conduction band edge. In particular, the device under consideration is the device "Trapezium". The electrical characteristics of this device were reported in Chapter 3. In order to match the subthreshold behaviour of the Trapezium, four trap energies are introduced, with energy levels at $E_{t1}$=1.25kT, $E_{t2}$=2.5kT, $E_{t3}$=5kT and $E_{t4}$=10kT from the conduction band and with concentration of $8\times10^{11}$, $3\times10^{11}$, $2.5\times10^{11}$ and $1\times10^{11}$ $cm^{-2}$, respectively (Figure 7a). Thanks to the software it is possible to selectively choose which interface traps are active. Figure 7b shows how the transfer characteristic of the device would look like if there were no interface traps, if only the traps close to the conduction band were active ($E_{t1}$ and $E_{t2}$) and if only the traps close to the mid-gap were active ($E_{t3}$ and $E_{t4}$).

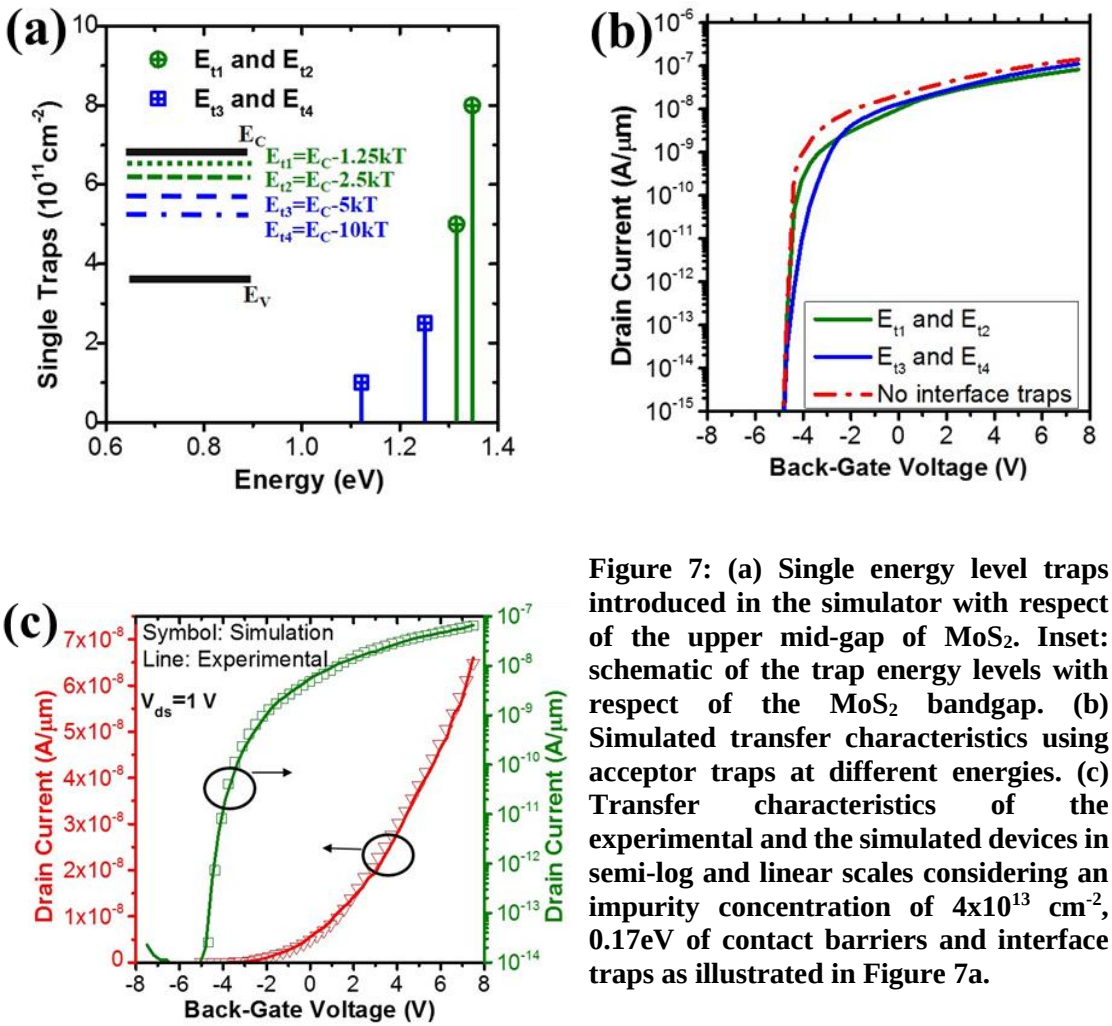


**Figure 7: (a) Single energy level traps introduced in the simulator with respect of the upper mid-gap of $MoS_2$. Inset: schematic of the trap energy levels with respect of the $MoS_2$ bandgap. (b) Simulated transfer characteristics using acceptor traps at different energies. (c) Transfer characteristics of the experimental and the simulated devices in semi-log and linear scales considering an impurity concentration of $4x10^{13}$ $cm^{-2}$, 0.17eV of contact barriers and interface traps as illustrated in Figure 7a.**

Figure 7c compares the experimental and the simulated data, with an impurity concentration of $4\times10^{13}$ $cm^{-2}$, contact barrier of 0.17 eV and the interface traps as shown in Figure 7a. It is important to consider that in this case the interface traps are varied after modelling the contact (Schottky barrier at the drain/source contact) and mobility (impurity concentration equal to the one extracted from the mobility, as shown in Chapter 3). Therefore, an error in the contact or mobility modelling will result in an added uncertainty to the extracted density of interface traps. However, these results are still relevant in order to approximately quantify the effect of each non-ideality. For a better understanding of each defect ad-hoc test-structures are needed, as TLMs for contact studies or MOSCAP for the study of the $MoS_2$/oxide interface.

#### 6.5.2.2 Top-gated $MoS_2$

In relation to the interfacial properties, recent results based on impedance spectroscopy analysis of MOS[272] and MOSFET[273, 274,] structures indicate the presence of electrically active defects at the $MoS_2/Al_2O_3$ and $MoS_2/HfO_2$ interface. Considering previous reports,[273, 274] ac physics based simulations were used, in conjunction with experimental $MoS_2$ MOSFETs characteristics, as a metrology approach to profile the density and energy of electrically active defects at the $MoS_2/HfO_2$ interface. The physics-based ac simulations, in conjunction with the experimental data, provides more insight into the density, energy level and carrier capture cross section values of electrically active defects at the $MoS_2$/oxide interface properties in thin channel $MOS_2$ MOSFETs.

Figure 8a shows the optical picture of the device under consideration. Ti/Au contacts are deposited under High Vacuum using photolithography and lift-off. $HfO_2$ was deposited by Atomic Layer deposition after an UV-O3 treatment.[275] Cr/Au was deposited as the metal gate.

Figure 8b shows the structure implemented in the Synopsys Sentaurus TCAD Device simulator. The dimensions are set to match the experimental device[274] (Figure 8a). The dielectric constant and bandgap of $MoS_2$ are set as explained at the beginning of this chapter, while the charged impurity concentration, required for carrier mobility modelling, is taken from fitting of various back-gated $MoS_2$ MOSFETs as explained in the previous chapter. The n-type doping is determined as $1.25\times10^{19}$ $cm^{-3}$. The actual carrier concentration in the flake following exfoliation might be lower, but positive fixed charges in the $HfO_2$ can provide effective electrostatic doping to the thin $MoS_2$ channel. The dielectric constant (k) of the ALD $HfO_2$ is determined to be 13 based on the experimental C-V accumulation capacitance and a $HfO_2$ thickness of 13 nm derived from cross-sectional transmission electron microscopy measurements.[273, 274] An alternative approach is to take $HfO_2$ with k=17 and consider a van der Waals gap of 0.3 nm (k=1) at the $MoS_2/HfO_2$ interface.[276] The $Ti/MoS_2$ Schottky barrier height set as 0.12 eV considering previous studies[142] and high energy XPS measurements.

Figure 9b shows the experimental and simulated transfer characteristics. The curves are in excellent agreement, except for gate voltages higher than -1V, likely related to the modelling of the contacts, which is not the primary aim of this work. In order to match the simulated and experimental behaviour, acceptor traps were added at the $MoS_2/HfO_2$ interface (Fig. 9a). A constant trap energy in the upper mid-gap of $MoS_2$ was introduced, with concentration of $3.5\times10^{12}$ $cm^{-2}eV^{-1}$. In addition, three

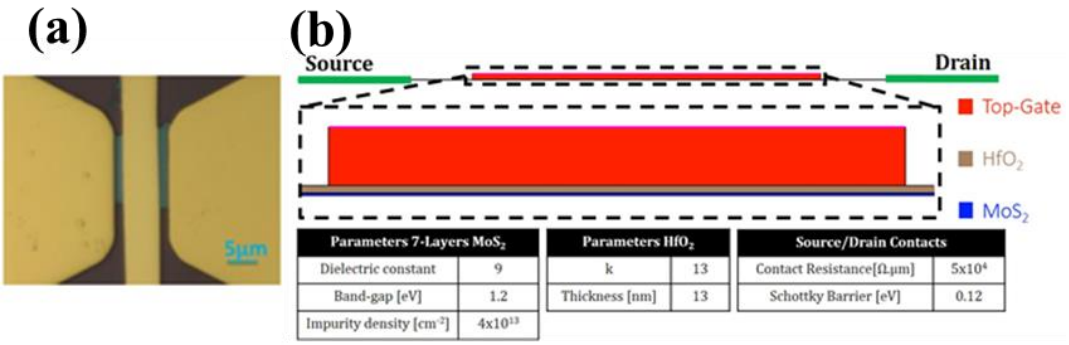


**Figure 8: (a) Optical view of the top-gated MoS2 flake.[273, 274] Ti/Au contacts are deposited under High Vacuum using photolithography and lift-off. $HfO_2$ was deposited by Atomic Layer deposition. Cr/Au was deposited as the metal gate. (b) Schematic of the structure implemented in the Sentaurus physics-based device simulator. The tables show the parameters selected for $MoS_2$, $HfO_2$ and the Ti/$MoS_2$ contacts.**

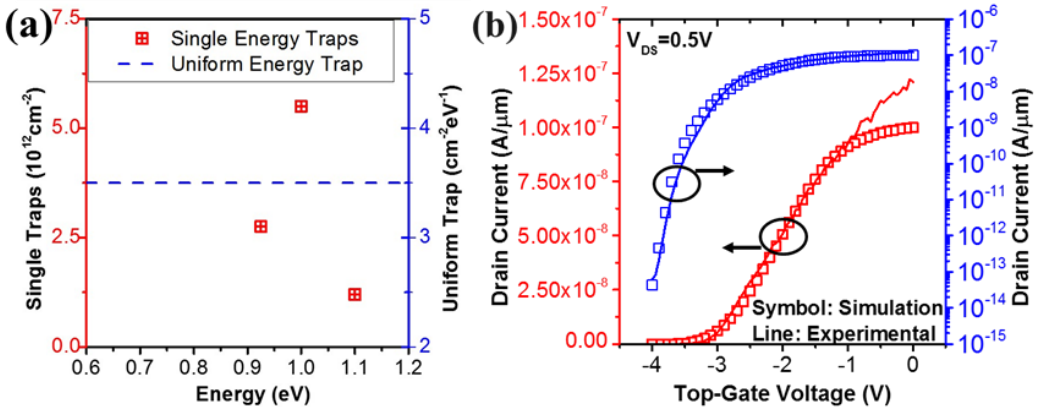


**Figure 9: (a) Trap distribution with respect to the valence band edge of $MoS_2$. The traps span from the mid-gap (0.6 eV) to the lowest energy in the $MoS_2$ conduction band. (b) Transfer characteristics of the experimental and the simulated devices in log (blue) and linear (red) scales. The fit of the simulated response to the experimental transfer characteristic is obtained using the interface trap distribution shown in Figure 6a.**

single energy level traps are added, at energies 0.925, 1.0 and 1.1 eV, with concentrations of $2.75\times10^{12}$, $5.5\times10^{12}$ and $1.2\times10^{12}$ $cm^{-2}$ respectively. The corresponding fitting is close to the experimental density of interface traps (Dit).[273, 274] With the $D_{it}$ energy and density obtained from the DC device characteristics, these

same parameters were employed to determine if they can reproduce the observed experimental multi-frequency gate-to-channel C-V response. One of the advantages of the physics-based ac simulations model is the ability to selectively turn "on and off" the frequency dispersion of each trap, by selecting low ($<10^{-24}$ $cm^2$) trap cross-sections. Unfortunately, 2D-materials in general were not deeply studied through CV analysis, therefore a value for trap cross-section is not present yet. Therefore, the cross-section will be used as a variable.

Figures 10a and 10b shows the effect of the single energy traps located at 0.925 and 1.0 eV respectively at different cross-sections at a frequency of 1 kHz. The cross-section range were set in order to see the most variation of the CV curve related to the particular trap. Both shows a similar signature because of the single energy level. The main difference between the two is the position of the peak with respect of the gate voltage.

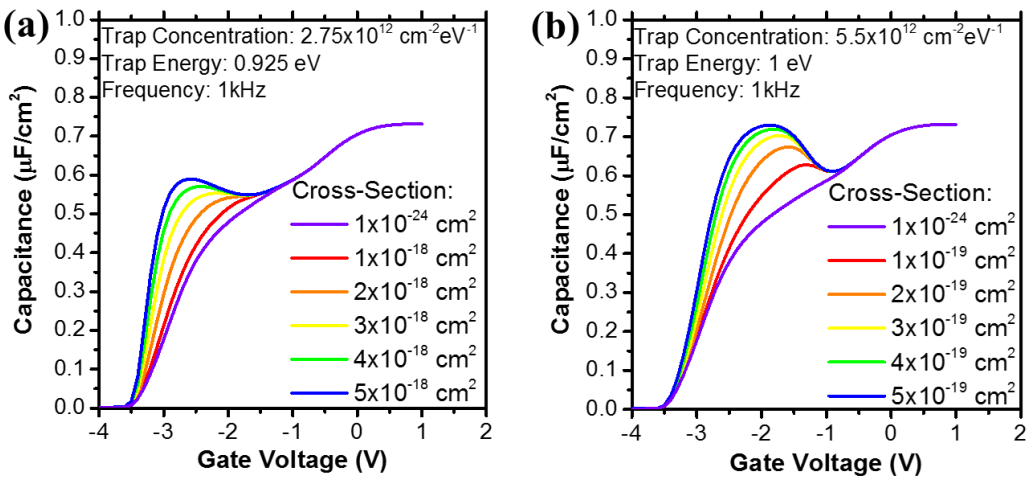


**Figure 10: CV simulations of the single energy level trap located at (a) 0.925 eV and (b) 1 eV. Cross-section is used as a variable in a range when the effect of the trap is clear.**

Figure 11a shows the experimental CV result. By comparison, it is possible to understand which of the trap levels introduced before (Figure 8a) is the responsible of the experimental CV response. As is clear from comparing Figure 10a and 10b with the experimental response in Figure 11a, the trap located at 1 eV is too close to the conduction band to give a CV response similar to the experimental one. Similarly, the trap located at 1.1 eV can be ruled out.

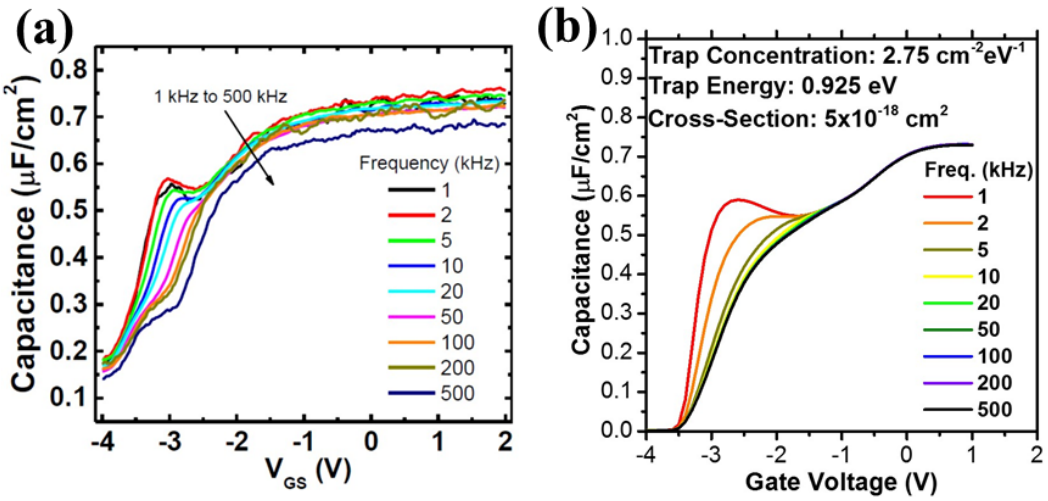


**Figure 11: (a) Experimental[274] and (b) simulated CV response. The simulated CV response consider the trap at energy 0.925 eV, with concentration 2.75x10$^{12}$ cm$^{-2}$ and a cross-section value of 5x10$^{-18}$ cm$^{2}$.**

Therefore, the simulations indicate that the single energy trap located at 0.925 eV is the responsible of the experimental CV behavior. This energy level is consistent with previous reports, in which CV analysis of thick $MoS_2$ was conducted by Therman method.[272] In particular, the energy range of Sulphur vacancies, the most common defect in exfoliated $MoS_2$, is usually 0.9-1 eV. Of course, it is possible to notice that there is still a certain difference between the experimental and the simulated CV, as the experimental behavior is most certainly due to a combination of several traps.

Nevertheless, considering more traps can be difficult, because of the higher number of variables and the sensitivity of the CV response on the trap cross-section.

Lastly, it is possible to evaluate the effect of the uniform trap, which was not evaluated so far. Figure 12 shows the CV responses varying the cross-section of the uniform trap, considering also the single energy level traps at 0.925 eV. From Figure 12a to 12c the cross-section of the uniform trap increases from $5x10^{-18}$ $cm^2$, to $5x10^{-17}$ $cm^2$ and to $10^{-15}$ $cm^2$. An increase in the trap section results in a major dispersion towards more negative gate voltages. This results in an even similar response with respect of the experimental results. Nevertheless, as said before, experimental values of trap sections are not yet present in literature. Even if the software is useful to understand which is the approximate energy related to the trap responsible of the CV response, considering more than one trap might lead to wrong conclusions as there might be too many variables to take into account. On top of that, CV responses are highly sensitive to trap cross-sections.

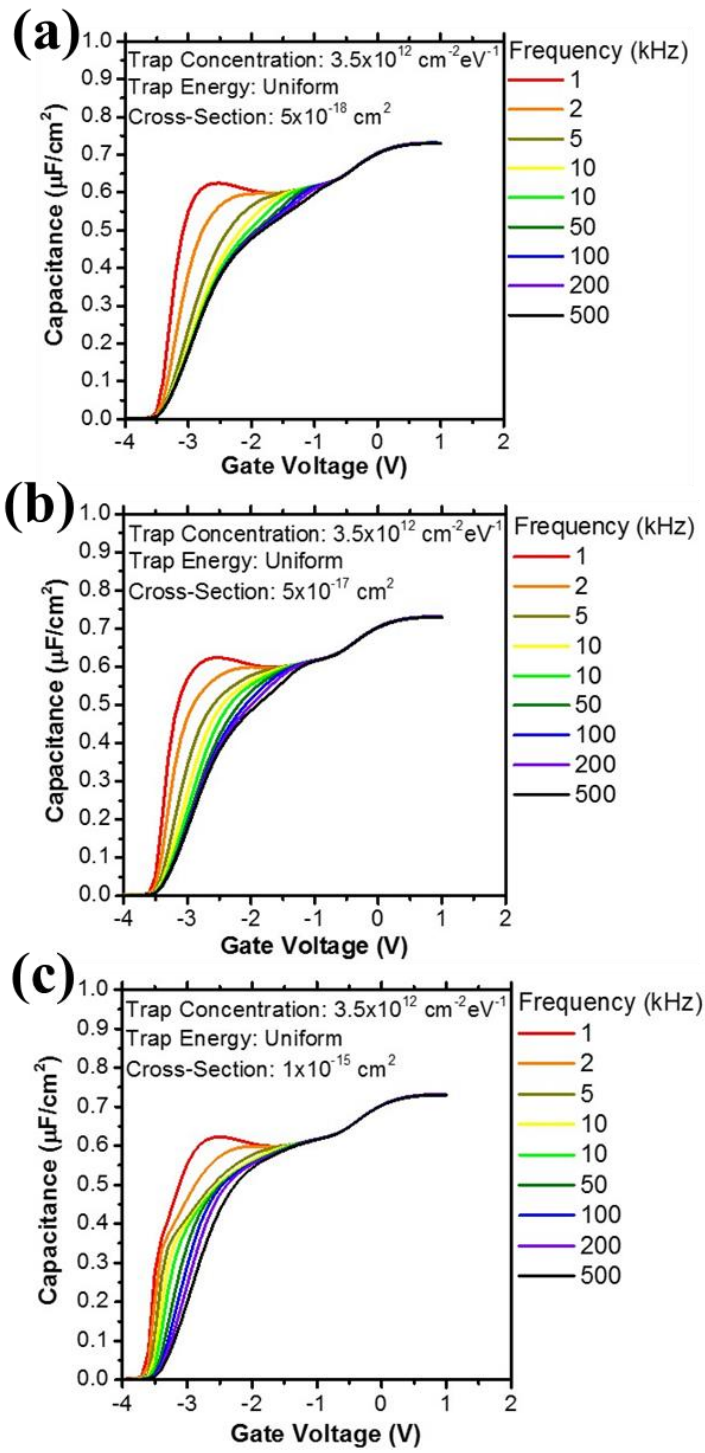


**Figure 12: Simulated CV response of the single energy level traps at 0.925 eV in addition to the uniform trap, which cross-section: (a) $5x10^{-18}$ $cm^2$, (b) $5x10^{-17}$ $cm^2$ and (c) $10^{-15}$ $cm^2$.**

## 6.6 CONCLUSIONS

In conclusion $MoS_2$ FETs were electrically characterized from which continuum-based models and parameter sets were developed. It has been shown that the experimentally extracted field-effect mobility values are strongly dependent on the high impurity concentration present in the material, which limit its true potential. Furthermore, with the combination of CV analysis and TCAD simulations the CV response of a top-gate $MoS_2$ FET was explained considering a single energy level trap, related to sulphur vacancies. Very good agreement between the model and the experimental results has been achieved. Even if promising results are shown to date, the true TMD device performance is still masked by imperfections, which can be tackled by purifying and optimizing the growth and device processing conditions to reduce impurities and improve TMD stoichiometry.

# Chapter 7: THE LAYERED STRUCTURE CONCEPT

This chapter is adapted from the following publications and conferences:

**Mirabelli, G.**; Hurley, P. K.; Duffy, R., Physics-based modelling of $MoS_2$: the layered structure concept, SISPAD, Austin (TX), 2018.

**Mirabelli, G.**; Hurley, P. K.; Duffy, R., Physics-based modelling of $MoS_2$: the layered structure concept. Semiconductor Science and Technology 2019, 34 (5), 055015.

## 7.1 INTRODUCTION

Previous publications investigating continuum-based modelling in $MoS_2$ have accounted for the 2-Dimensional structure based on highly asymmetric mobility in-plane and out-of-plane, while maintaining a homogenous structure. In this work, instead of using a continuous slab of semiconductor, as previously reported, we introduce in a TCAD tool the "layered structure", which takes into account both in-plane drift and diffusion currents and a tunneling process through the Van-der-Waals gap (VdW-gap) between the layers of the 2D-semiconductor. This type of layered-modelling with a TCAD tool is still missing in the state of the art, even if the layered structure is a fundamental feature of TMDs or any other 2D-material and modelling might benefit from its introduction. For this study of transport in 2D-semiconductors the continuum-based Synopsys Sentaurus Device software was used.[146]

The analysis is calibrated using previous experimental findings based on vertical transport through $MoS_2$. The results show that 2D-semiconductors can be modelled by a TCAD tool and the layered structure can be particularly important when a few layers of material are considered, as the layered characteristics of the material have a greater impact with reducing 2D film thickness.

Figure 1a shows a representative TEM image of 3-layers of $MoS_2$ taken in the channel region of a back-gated $MoS_2$ MOSFET, where it is possible to notice the characteristic layered structure of the semiconductor. The structure is represented schematically in Figure 1b in order to emphasize the division between each $MoS_2$ layer. This same layered representation is used in the TCAD (Figure 1c) where the layers of semiconductors are alternated by VdW-gaps. The green stripes are the $MoS_2$ layers, while the light-blue layers are the VdW-gaps. The Van-der-Waals gaps are set

between the layers of the $MoS_2$ only, and not between the $MoS_2$ and the oxide or the $MoS_2$ and the contact. These effects are outside the scope of this work which is the carrier transport in the $MoS_2$ layers.

The thickness of the $MoS_2$ and the gap layers in Figure 1c is set initially to 0.32 nm and 0.29 nm respectively, close to the values that are usually visible by TEM analysis or calculated by X-ray diffraction.[278] However, the effective electrical thicknesses might be different. Previous studies have shown that there exists an overlap of the wave functions and an exchange interaction between nearby $MoS_2$.[279] During the analysis the thickness of one layer of $MoS_2$ and one VdW-gap will be constant and equal to 0.61 nm, which is the known thickness of monolayer $MoS_2$. Nevertheless, the effective electrical thickness of the two sub-components will change as it is a variable that needs to be benchmarked against experimental data.

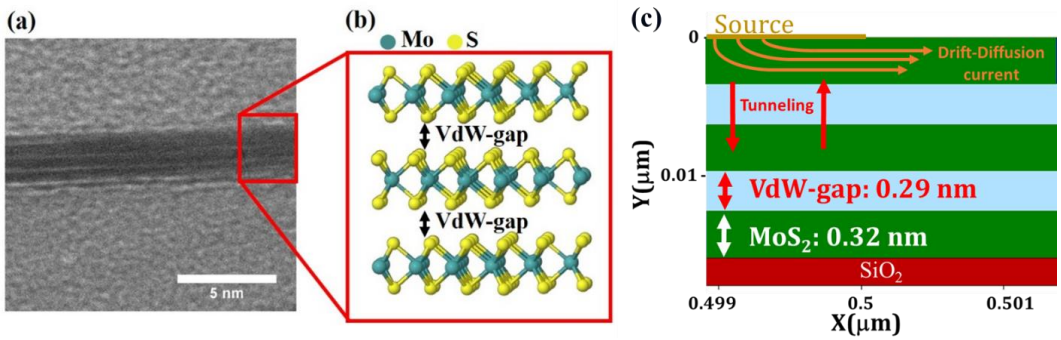


**Figure 1: (a) Representative TEM image showing the layered structure of $MoS_2$. (b) Representation of the structure of $MoS_2$ showing the Van-der Waals gaps between the layers.[277] (c) Schematic of the layered structure implemented in the Sentaurus physics based device simulator.**

In general there will be two kind of currents: (1) parallel current in the $MoS_2$ layers, which is modelled by the drift-diffusion equations, and (2) perpendicular

transport in between layers due to direct tunneling through the gaps, which act as tunneling barriers.

Figure 2b shows the conduction band energy of 5 layers of $MoS_2$ considering a uniform (red) and a layered structure (black). For the layered structure, it is clear that, to have conduction from the top to the bottom of the device, tunneling through the VdW gaps is necessary. Note that the VdW-gaps are aligned with the vacuum level, while the workfunction of the $MoS_2$ layers are equal to 4eV at this thickness, as evaluated experimentally. Similarly, Figure 2c shows the electrostatic potential variation in 5 layers of $MoS_2$. Due to the presence of the VdW gaps, the variation for the layered structure is not linear with distance, as in the uniform structure, but exhibits two distinct gradients of potential for the $MoS_2$ region and the VdW region, based on their respective dielectric constant.

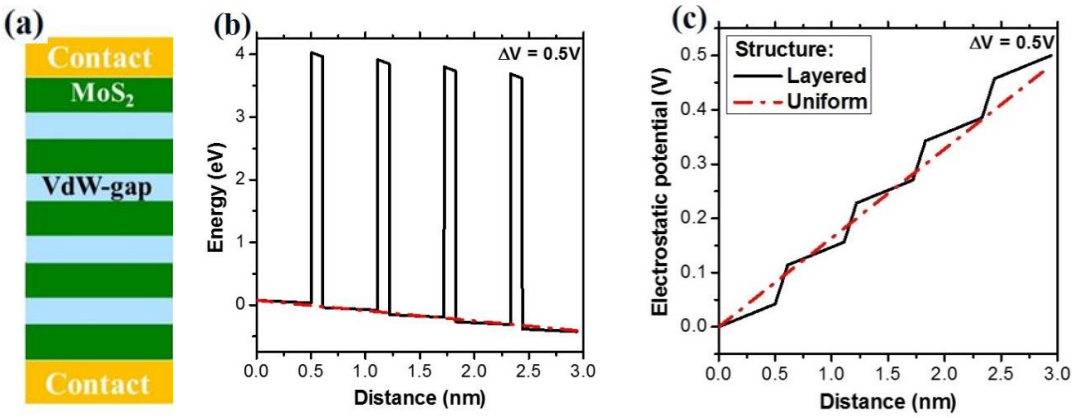


**Figure 2: (a) Device structure considered. (b) Conduction band energy and (c) electrostatic potential variation in the layered and uniform structure, with a voltage of 0.5V applied across the device. For these simulations the VdW-gap is 0.11 nm and the $MoS_2$ thickness is 0.5 nm. The dielectric constant of $MoS_2$ is equal to 3.**

The dielectric constant of each VdW gap was set to 1. The dielectric constant of $MoS_2$ was experimentally measured and the values for different thicknesses are

known.[266] For samples thicker than 10 nm, which is the case of the experiments that will be considered in this work, the value is initially 10.5. Nevertheless, as will be later explained, it will be considered as a variable since for previous calculations $MoS_2$ was considered as a uniform semiconductor. Other basic parameters are set considering reported theoretical and experimental results.

## 7.2 METHODOLOGY DEVELOPMENT

The methodology adopted in this work is to first model the vertical transport through the layered $MoS_2$, and to use this to subsequently model transport of a back gated $MoS_2$ MOSFET structure. In relation to the Figure 1b, the vertical transport will be determined by direct tunneling process through the VdW gaps. The model implemented for direct tunneling in Sentaurus is determined by: the barrier height to tunneling (see Figure 2b), the tunneling effective mass of the electron in the VdW gap, and the potential difference between the two $MoS_2$ layers.[280] The potential difference between two consecutive layers will be determined by the vertical dielectric constant assumed for the single layer of $MoS_2$. As we assume the VdW gap is vacuum, the barrier to electron tunneling is set at 4eV. Consequently, the parameters to be determined are the dielectric constant of the $MoS_2$ and the effective electron mass during tunneling. To obtain these values we calibrate the model against published experimental data for vertical transport through $MoS_2$.[281, 282]

In the experimental work which will be used to calibrate the tunneling model,[282] $MoS_2$ was exfoliated on a gold metal pad and $SiO_2$ or HSQ was patterned by lithography on top of the flake as an isolation layer. The top metal was Ni/Au. In this way it was possible to consider only the perpendicular conduction in $MoS_2$. Based on an analysis of the experimental data assuming the $MoS_2$ as a homogeneous

semiconductor a Schottky barrier of 0.3 eV at the contact was determined for the $Au/MoS_2$ contact, while the effective perpendicular mass was evaluated to be 0.18 $m_0$. Both these values will be considered in our simulations as well.

The TCAD software solves the drift-diffusion equations in both the parallel and perpendicular direction (along the x- and y-axis respectively of Figure 1c). The parallel mobility will be set according to experimental findings as we will explain in a later section. For the modelling of the perpendicular transport, the aim is that this conduction component is limited by tunneling through the VdW-gaps. To achieve this, the perpendicular electron mobility is increased to a point where it no longer affects the conduction.

Figure 3a reports the experimental and simulated perpendicular drain current at 3V as a function of the total thickness of the $MoS_2$. The figure shows 3 curves where the individual layer thickness of the $MoS_2$ is varied (and the VdW-gap thickness accordingly). The results at 3V, with a $MoS_2$ individual layer thickness between 0.5 and 0.55 nm are in reasonable agreement with experiments. The data from Zhu et al.[281] at 1V were also considered, which show less agreement with the simulations. One reason might be the different top contact used for the devices, Ti instead of Ni, which is known to form a layer of $TiO_2$ at the $MoS_2$ interface.

Figure 3b shows the current density considering a variation of the Schottky barrier at the contact from 0.15eV to 0.45eV. The value of 0.3eV is the barrier height used for Figure 2a. A variation in the barrier causes the current density to move almost rigidly along the y-axis. At a voltage of 3V the barrier has little effect on the simulations because the voltage is considerably higher than the Schottky barrier.

Figure 3c shows the variation in the current density when modifying the dielectric constant of $MoS_2$, from 3 to 20. The value of 10.5 is the one used initially. The variation in dielectric constant has a significant effect, and a reasonable fitting is obtained with a dielectric of 3, which is consistent with previous theoretical studies.[283] A variation in the dielectric constant will change the partition of the electric field in the device. A lower dielectric in the $MoS_2$ will increase the potential drop between consecutive $MoS_2$ layers, which increases the direct tunneling current. Based on this analysis, while not fully optimized, the following section takes a perpendicular dielectric constant of the $MoS_2$ as 3, the thickness for the $MoS_2$ layer will be 0.5 nm, with a 0.11 nm VdW-gap.

Figure 3d shows the vertical current from two experimental devices with different layers of $MoS_2$, in comparison with the TCAD model. It is noted that while the parameter tuning process was performed at a fixed voltage (3V) there is a good agreement with the experimental data across the full voltage range and for the two value of $MoS_2$ thickness.

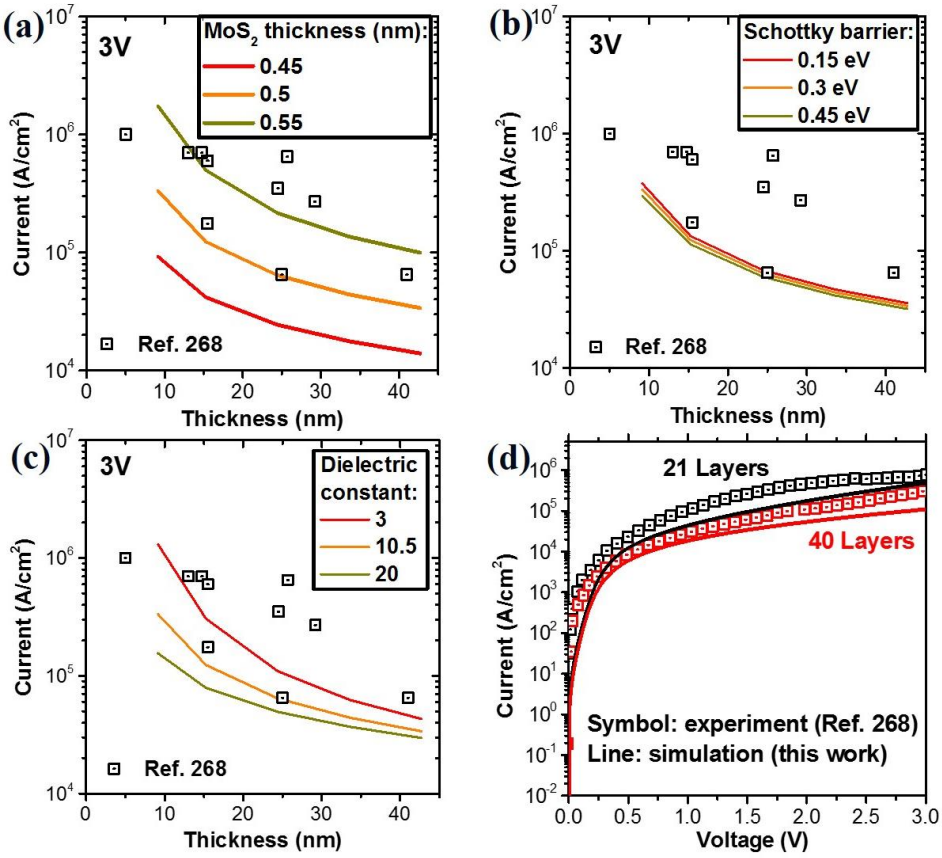


**Figure 3: Current density at 3V for different thickness considering a variation of: (a) $MoS_2$ thickness, (b) Schottky barrier and (c) perpendicular dielectric constant of $MoS_2$. Unless specified, a dielectric constant of 10.5 and a thickness of 0.5 nm were used for the $MoS_2$, with a Schottky barrier of 0.3eV. (d) Comparison of the simulated and experimental vertical current for two different thicknesses reported by Zhang et al.[282].**

Generally, the differences between simulations and experiments can be related to the immaturity of the material itself, which can cause experimental error in the extraction of the Schottky barrier or the dielectric of $MoS_2$. The Schottky barrier can differ from the value of 0.3eV for different samples due to different thickness,[126] impurities and defects, which are highly present in TMDs in general. As reported by McDonnell et al.[143], a defect density of 0.3%, common in TMDs, can be sufficient to dominate the contact resistance and it can also cause device-to-device variation. Furthermore, the dielectric constant of $MoS_2$ might differ from the experimental

extracted value as it is not only dependent on the number of layers, but first-principle calculations showed a certain dependency on the perpendicular electric field as well.

## 7.3 APPLICATION OF THE DEVELOPED MODEL: BACK-GATED $MoS_2$

Using the parameters for the vertical $MoS_2$ transport obtained in the previous paragraph, the implications of the layered $MoS_2$ structure to the characteristics of a back-gated $MoS_2$ MOSFET are considered in this section. For the purpose of this study, which is comparative study between the homogeneous and the layered $MoS_2$ structure, additional effects such as interface traps or Schottky contacts are not considered. The simulated device is discussed in Figure 4a, the channel length is equal to 0.5 µm, and the device is back-gated with 20 nm of $SiO_2$. The thickness of $MoS_2$ was chosen as 8 layers and a uniform *n*-type doping concentration of $10^{17}$ $cm^{-3}$ was chosen.[197] A constant anisotropic mobility model is used (bias independent). The in-plane parallel mobility depends on previous experimental results (Figure 4b),[284] while the out-of-plane conduction is as described in the previous section. This back-gated structure is typical of many $MoS_2$ FET devices reported in literature. The device characteristics are compared for the case of the layered structure, with the parameters derived from the previous sections, and for the case of a homogeneous $MoS_2$ film. While the parallel mobility will be the same between the two models, for the homogeneous $MoS_2$ case we take a perpendicular mobility of 0.5 $cm^2/V.s$. This is increased from the value of 0.2 $cm^2/V.s$ considered in a previous work.[168] The increase in the perpendicular mobility of 0.5 $cm^2/V.s$ was implemented so that the current level of the two structure is similar to facilitate a qualitative comparison.

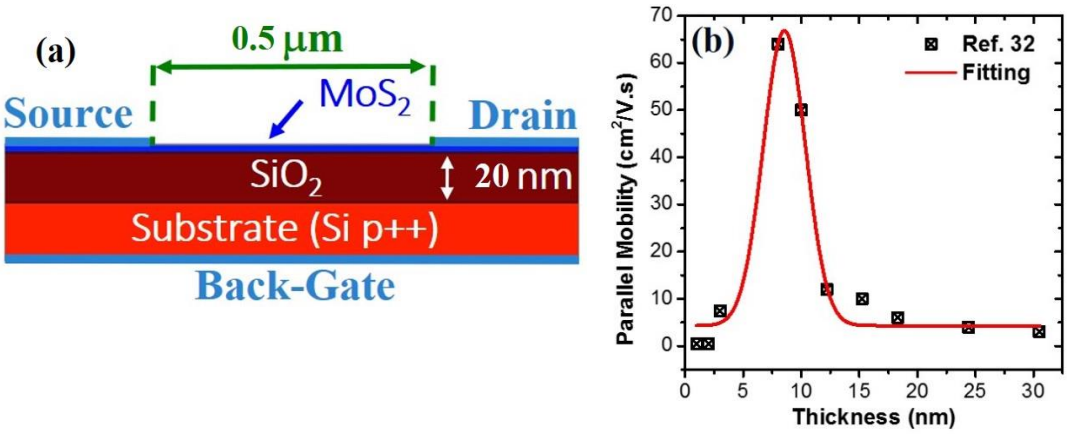


**Figure 4: (a) Schematic of the device structure implemented in Sentaurus device. (b) Layer dependent parallel mobility used for both structures.[284]**

Figure 5a and 5b show the transfer characteristic varying drain voltage for the uniform and the layered structure respectively. The first obvious difference is the current density considering the same applied voltages. The layered structure shows a current almost an order of magnitude higher. Nevertheless, the transition from off to on in the layered structure is much gradual around 0.5-1.0 V. In order to clarify both these points Figure 5 c-h show the current density in the whole device, increasing the drain voltage from 0.5 to 3V at a back-gate voltage of 5V.

Considering first the variation of the current density at any fixed drain voltage it is clear that the current density is mostly limited to the bottom layers. When a drain voltage is applied the current density will increase closer to the drain contact, passing through the whole structure. This is true for both structures, and the increase in drain voltage creates a “path” from the bottom of the semiconductor to the drain contact. From the contour plots at the highest drain voltage for both structures, Figure 5e and 5h, it is clear that below the tip of the drain contact the current density increases. As a result, the difference between the two transfer characteristics is related to how the current vertically passes through the structure. The uniform structure depends on the

perpendicular mobility, while for the layered one depends on direct tunneling through the VdW-gaps. Even if the first option might generate results that are in agreement with experimental data the transport process in a real $MoS_2$ is likely different. Due to a discrete structure formed by separate layers it is unlikely that the process can be simply described by a perpendicular mobility with a drift-diffusion transport model. Also, especially for thin devices the assumption of a perpendicular mobility does not have a physical meaning by definition, since the film thickness will be less than the mean free path between collisions. Therefore, the presence of the VdW-gaps provides a more accurate description of the transport in a real $MoS_2$ film, or 2D-semiconductor in general.

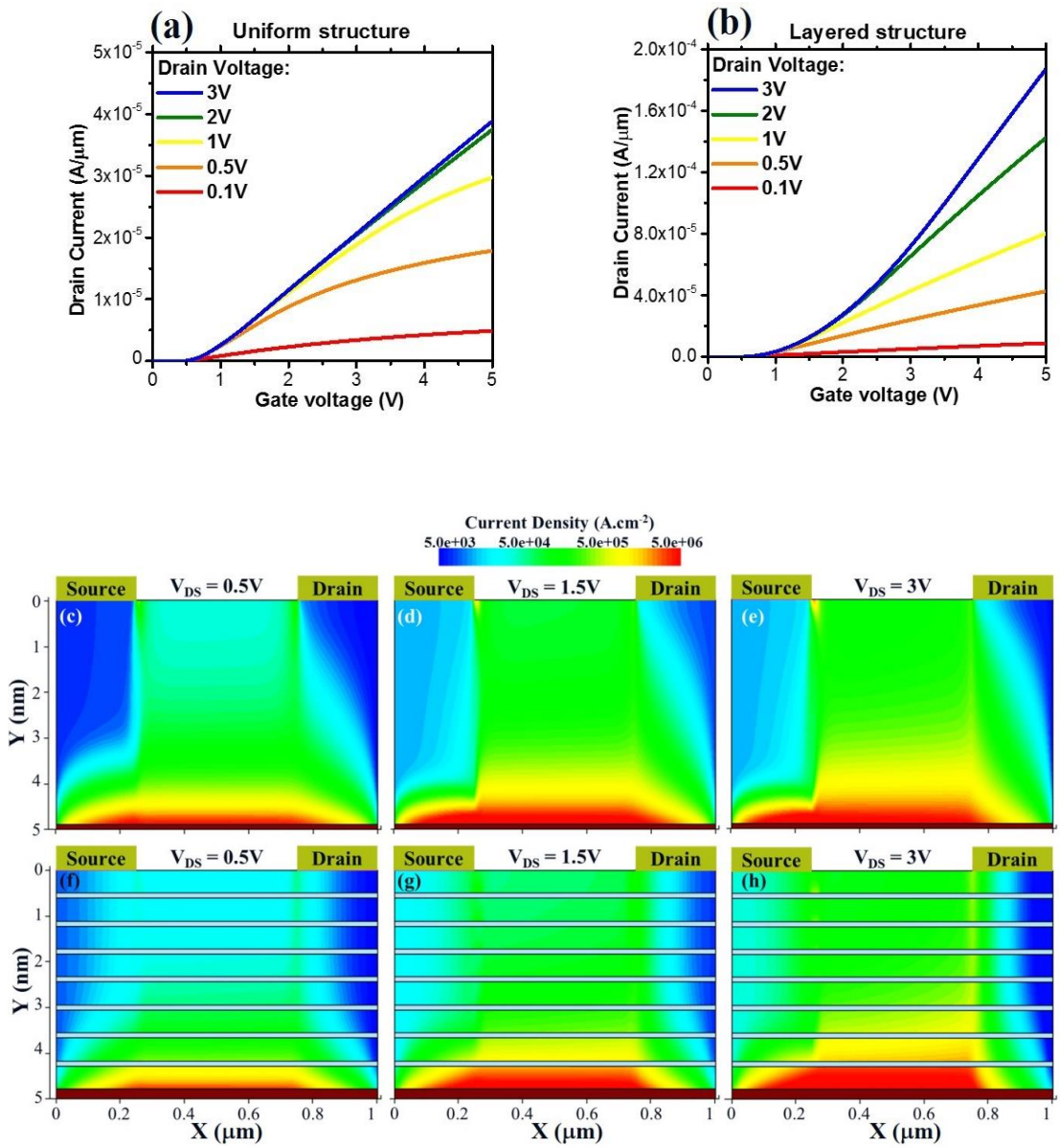


**Figure 5: Transfer characteristic for the (a) uniform and (b) layered structure varying the drain voltage from 0.1 to 3V. Current density contour plot varying the drain voltage from 0.5 to 3V for the (c-e) uniform and (f-h) layered structure. Gate voltage is 5V ($V_{GS}$-$V_T$≅3V).**

## 7.4 METHODOLOGY IMPROVEMENT

Although the model developed in the previous paragraphs is valid, a possible improvement is related to the tunnelling model used for the vertical tunnelling through the VdW-gaps. As said, the model used is the Schenk model,[280] which is a "local

model". This means that only tunnelling of carriers at the interface can participate to the tunnelling current. Another choice is to use a non-local model. In this case the software creates a non-local mesh around the interface and will consider the tunnelling current from each mesh point created. In the $MoS_2$ case, this means that the tunnelling current will come from the all semiconductive layer, not only from the VdW-gap/$MoS_2$ interface.

The advantage of the model is also related to the fact that the vertical tunnelling mass and the conduction mass can be defined separately. The conduction mass can be set considering theoretical studies, as shown before in Chapter 6.3, while the vertical mass is a new parameter that can be tuned to match the experimental values. Other parameters as Schottky barrier and $MoS_2$ dielectric constant will be initially considered as 0.3 eV and 3 respectively considering the results from the previous fitting (Chapter 7.2) and tuned further if needed.

Figure 6a show the fitting of the experimental data considering a variation of thickness for the $MoS_2$ layer from 0.25 to 0.5 nm. Because the model considers the whole $MoS_2$ layer as tunnelling region, the current is generally larger at the same thickness with respect of the local model. Interestingly, considering the trend, a thickness between 0.3 and 0.4 nm is close to fit the experimental data. The other parameter to consider is the effective vertical mass, which trend is reported in Figure 6b, where a thickness of 0.32 nm for the $MoS_2$ was considered. The experimental data are well fitted considering a thickness for the $MoS_2$ of 0.32 nm and vertical mass of 0.2 $m_0$. The value of 0.32 nm for the $MoS_2$ is the same as the sulphur-to-sulphur distance, while the 0.2 $m_0$ is very close to the value 0.18 $m_0$ extracted

experimentally.[281] It was not necessary to change the dielectric constant or the Schottky barrier from their initial values of 3 and 0.3 eV, respectively.

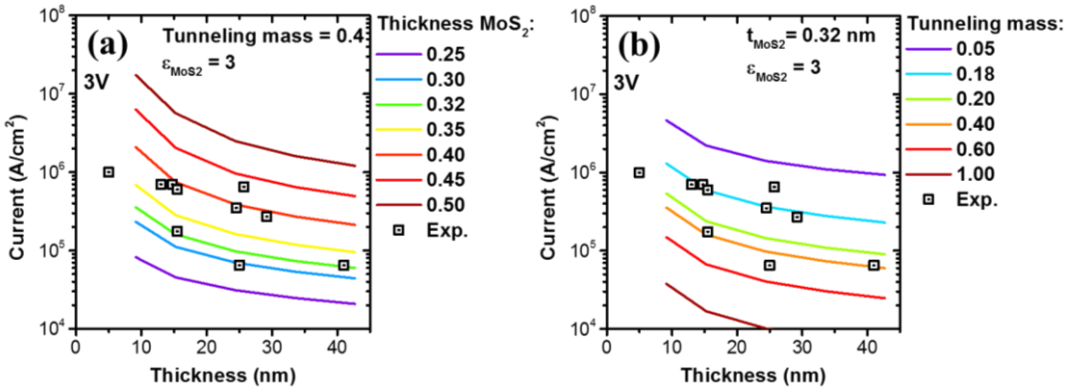


**Figure 6: Current density at 3V for different thickness considering a variation of: (a) $MoS_2$ thickness with a fixed tunneling mass of 0.4, and (b) tunneling mass with a fixed thickness for the $MoS_2$ layer of 0.32 nm.**

## 7.5 JUNCTIONLESS AND INVERSION-MODE TRANSISTORS

Considering the developed model is now possible to answer important questions regarding the potential application of $MoS_2$ in scaled devices for future electronics, focusing on two main architectures, the junctionless transistor (JNT) [181, 265] and the classic inversion mode transistor (IM).

JNTs are characterised by uniform high doping throughout the channel and have been demonstrated in polysilicon, germanium, GaAs and indium-tin-oxide (ITO).[285-288] One of the main advantages is its very simple architecture. Due to the uniform doping it is not necessary to define doped contact regions, which simplify the associated processing. In addition, the electric field perpendicular to the current flow for the device around the threshold voltage is lower than a corresponding inversion-mode or accumulation-mode transistors. This is advantageous as carrier mobility degrades with the perpendicular electric field.[289]

Therefore, it is very important to compare inversion and junctionless transistor architecture to understand which device architecture is most suited for TMD-based devices. Currently, due to the immaturity of the material system, systematic experiments comparing an inversion-mode with a junctionless transistor architecture would be very complicated, because a consistent growth technique, a reliable doping method and a good semiconductor oxide-TMD interface are needed. Although promising results have been shown in literature, the research is still at an early stage. On this matter, TCAD simulations are a useful tool in order to assess the device performance in a timely manner. However, it is also important to consider that the material parameters on which the TCAD model is based on come from theoretical studies which might not be accurate and are sometimes not consistent between each other. For example, the effective mass calculated by advanced calculations and shown before (Chapter 6, Figure 2d) show a certain variation between the different references, which will in turn introduce a certain error in the TCAD model as well. Although these results will inevitably be affected by these small uncertainties, they can be considered as a first step towards the understanding of 2D-FET at scaled dimensions.

Hence, a series of TCAD simulations are carried out considering 3 layers of $MoS_2$. The reason of choosing this thickness is because experimental data have shown a better mobility and contact resistance with respect to thinner devices. Therefore, in terms of scaled devices it is likely that 3-5 layers of $MoS_2$ might be preferred to 1-2 layers.

Figure 7 show the architecture schematics that will be considered. As said, one is the classic "Inversion Mode" (IM) transistor, where the channel is undoped and the contact regions are highly doped. This structure is similar to what shown by Kappera et al..[213] The second one is the JNT architecture, in which the doping concentration is uniformly distributed. The doping will vary between $6\times10^{18}$ and $4\times10^{19}$ $cm^{-3}$. This structure is similar to those works where $MoS_2$ was doped by high-k, chemically or by substitutional doping, as the doping interested the whole channel. Both these architectures will be considered in a single-gate (SG) and double-gate (DG) configuration. Due to the low thickness of the channel the DG mode can be considered close to a gate-all-around architecture. The density of states, energy gap and all the parameters for the $MoS_2$ are detailed in Chapter 6.3. The equivalent oxide thickness (EOT) is 1 nm. The parameters varied are the spacer length (from 3 to 7 nm) and the gate length (8 to 20 nm).[109] The ITRS roadmap was used as guideline to set these values.[109]

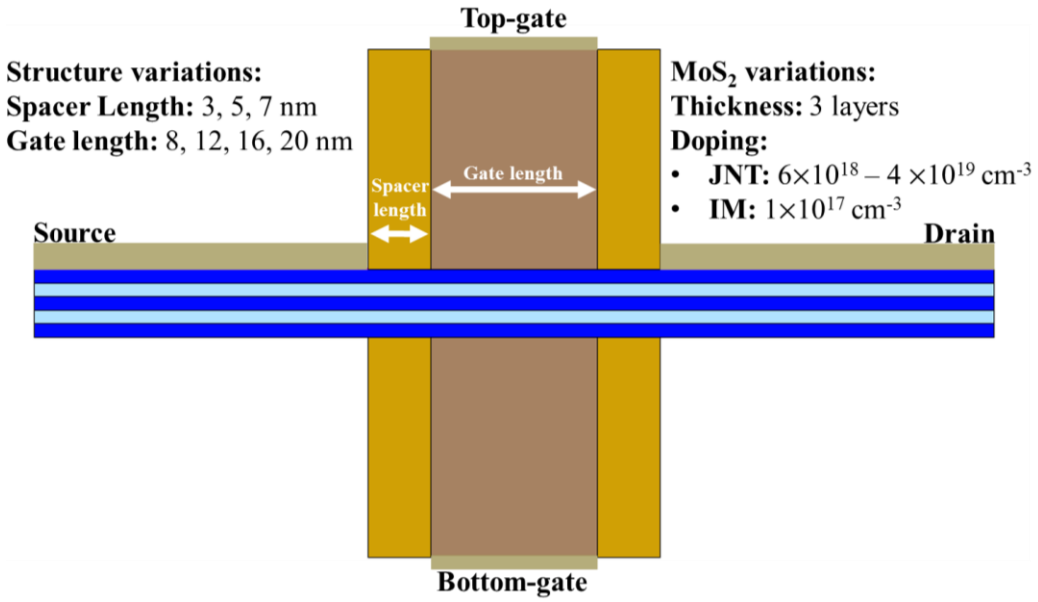


**Figure 7: Double gate device structure considered for the TCAD simulations. For the IM architecture the source and drain regions will be considered metallic, while the channel will be uniformly doped for the JNT structure.**

Figure 8 shows the mobility model adopted for the simulations. The Arora model[270] was tuned considering mobility values in the low and high doping regime. It was assumed a mobility of 100 $cm^2/V.s$ in the case of low doping ($<10^{17}$ $cm^{-3}$). This upper limit in the low-doping regime was set considering recent studies where these mobility values were extracted from nominally undoped $MoS_2$ crystals with optimised contacts.[225] The mobility at high doping concentration was set considering the experimental values from Chapter 4. Even if these data refer to p-type mobility, the p- and n-type mobility are very close considering heavily doped semiconductors

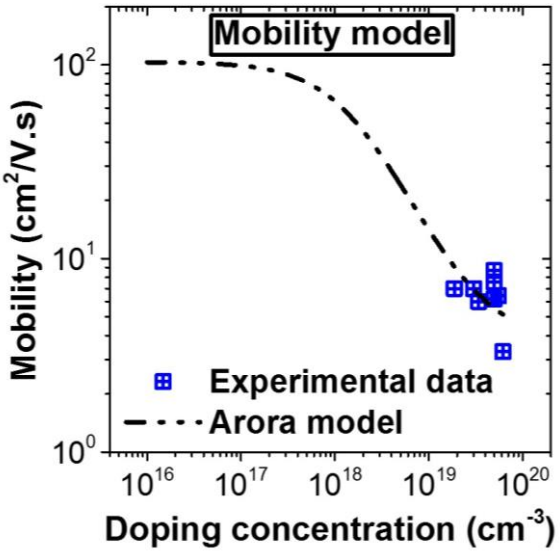


**Figure 8: Mobility model used for the electrical simulations. The Arora model was tuned assuming a mobility value of ~100 $cm^2/V.s$ for a doping concentration of $10^{17}$ $cm^{-3}$ and the experimental data from Chapter 4 for the high-doping region.**

Figure 9a and 9b compare the subthreshold slope (SS) and the drain-induced barrier lowering (DIBL) for the IM and JNT architectures. In both cases the values are very close considering a SG mode. Below 12 nm the SS values exceeds the requirement of the IRDS roadmap for both the JNT and the IM architecture. The DIBL is slightly less for a SG-JNT architecture, although in both cases the values are lower with respect of the ITRS requirements. Instead, considering a DG mode, the JNT

architecture can respect the IRDS standard at a channel length of 8 nm, while the IM architecture is slightly over 65 mV/dec. Although the DIBL values are similar, the ones related to the JNT architecture are lower.

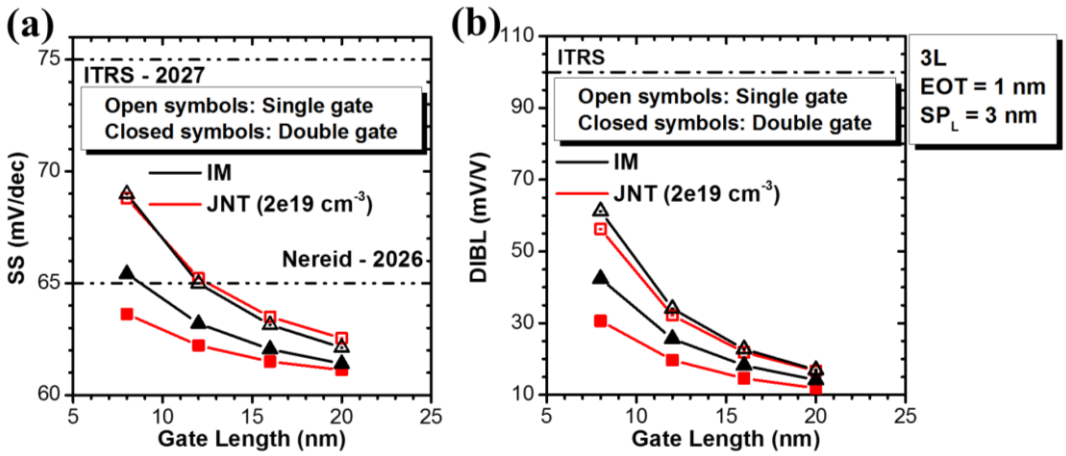


**Figure 9: Comparison of JNT and IM in a single and double gate architecture considering (a) subthreshold slope and (b) DIBL. Same legend applied to both plots.**

A second important parameter is the $I_{ON}$ of the device. Usually, considering the target application the $I_{OFF}$ is fixed at a certain value and the $I_{ON}$ is the value of current at $V_{GS}=V_{DS}=V_{DD}$, where $V_{DD}$ is the operating voltage. In this case the DG mode is chosen. Figure 10a shows the $I_{ON}$ current versus gate length for the IM and JNT architectures. For the JNT data two doping concentrations are considered: $6\times10^{18}$ and $4\times10^{19}$ $cm^{-3}$. For a higher doping concentratio, the $I_{ON}$ decreases. As said, the mobility model chosen for the JNT architecture is a doping-dependent mobility model. A lower doping will guarantee a higher mobility and so better $I_{ON}$. For the same reason the IM values are always higher. For a doping concentration of $10^{17}$ $cm^{-3}$ the mobility is ~100 $cm^2/V.s$.

Figure 10b compare the JNT and the IM architecture at a channel length of 8 nm and spacer length of 3 nm. The dashed lines are the values of $I_{ON}$ from the IRDS

roadmap: 420-470 µA/µm at an $I_{OFF}$ of $10^{-8}$ A/µm at a $V_{DD}$ of 0.7 or 0.65 V. Considering this, the green box shows the region where this condition is respected. Due to the higher mobility of the IM architecture the $I_{ON}$ current is higher with respect of the JNT architecture (doping = $2\times10^{19}$ $cm^{-3}$). The $V_{DD}$ is varied from 0.7 to 0.6 V. Nonetheless, the IRDS condition is respected in a very small window.

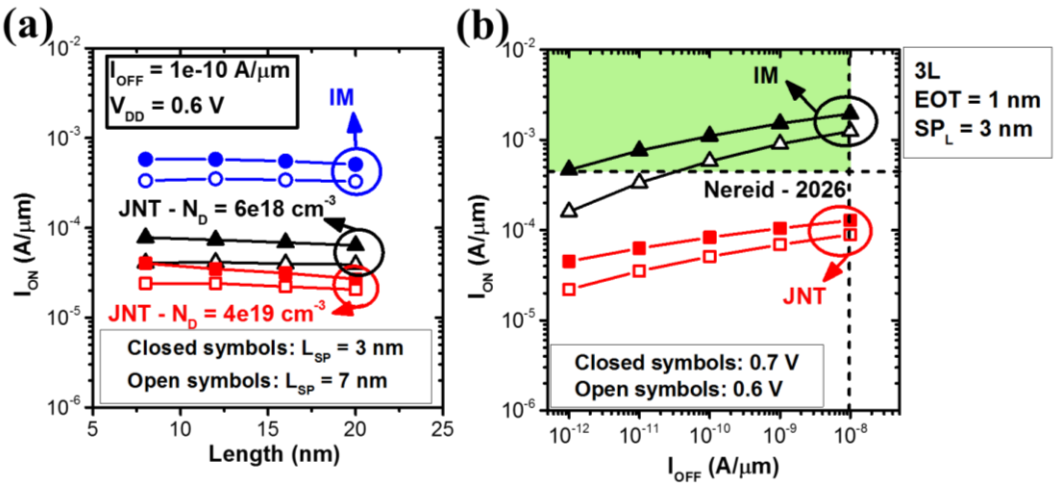


**Figure 10: (a) $I_{ON}$ scaling versus length at $V_{DD}$ = 0.6 V for an $I_{OFF}$ of 1e-10 A/µm and varying the spacer length between 3 and 7 nm. The IM architecture can drive a current almost one order of magnitude higher with respect of the JNT architecture. (b) $I_{ON}$ versus $I_{OFF}$ comparison at a $V_{DD}$ of 0.6 and 0.7 V for the IM and JNT architecture at a channel length of 8 nm. The green box shows the $I_{ON}/I_{OFF}$ region where the condition set by the IRDS is respected.**

## 7.6 DISCUSSION

In order to improve the drive current and satisfy the $I_{ON}$ requirements at short channel lengths is necessary to increase the mobility of the material. In particular, comparing the IM and JNT architectures, the IM mode shows a higher current because of the lower doping and so higher mobility, which might make them the preferable architecture. Nonetheless, the mobility of highly doped 2D-semiconductors might still be increased by other factors. A solution previously adopted for 3D-semiconductors and currently in use in the semiconductor industry is stress engineering.[290] Although previous theoretical studies have shown that strain can induce a higher mobility in

$MoS_2$ or similar TMDs,[111, 291, 292] it is important to consider that a higher mobility is connected with a lower effective mass, which in turn might deteriorate the $I_{OFF}$ or the SS of the device. A similar problem might be solved by the opportune deposition of high-*k* on TMD. Both theoretical and experimental studies have shown how the effect of a high-k can modify the properties of $MoS_2$, improving mobility, as discussed in more detail in Chapter 4 and 6, and reducing contact resistance and variability.[92]

The double-gate architectures modelled in the previous paragraph present both very interesting characteristics in terms of SS and DIBL, which makes $MoS_2$ (or other 2D-semiconductors) a good candidate for scaled devices. The FinFET architecture currently in use might have reached the end for high performance devices after the 5 nm node[293] and the most common substitutes considered nowadays to match the requirements for advanced technology nodes are the nanosheet[294] or nanowire[295] transistors. Nanowires appear as an interesting choice because of the better control with respect of the FinFET architecture. However, they suffer more from scattering and quantization effects due to their small diameter.[160] Both theoretical and experimental studies have shown that nanosheets can outperform nanowire-based FETs.[165, 294, 296] Although 2D-semiconductors are as well affected by quantization effects, they can still maintain considerable performances even at low dimensions, which can make them possible candidates for future electronics. Physical compact models identified $WS_2$ as a promising candidate to meet the 3 nm node requirements, outperforming Si FinFET in term of electrostatic and energy performances.[297] In addition, due to their instrinsic 2D-nature, $MoS_2$ FET were shown to have ~50% lower parasitic capacitance with respect of Si FinFET.[298] This advantage can be useful in order to reduce further the spacer, contact and channel lengths for higher integration, or relax these dimensions for improved performances.

## 7.7 CONCLUSIONS

With a combination of experimental findings and theoretical results a physics-based layered structure model was developed for $MoS_2$. Considering previous reports on the perpendicular conduction in $MoS_2$ devices, a layered structure that considers both the semiconducting layers of $MoS_2$ and the Van-der-Waals gaps in between them was developed and optimized for the first time in a TCAD software. The model was then used to shed light on the current distribution in a back-gated $MoS_2$-based FET and on the scaling behavior of inversion-mode and junctionless FETs. The junctionless transistor architecture, is comparable to the more common inversion-mode architecture in terms of DIBL or SS. However, the high doping required for the junctionless architecture causes a lower mobility, deteriorating the $I_{ON}$ of the device compared to the inversion mode structure. Stress engineering or high-k deposition might be necessary in order to utilize this junctionless architecture.

# Chapter 8: CONCLUSIONS AND FUTURE PERSPECTIVES

The properties and characteristics of 2D-Semiconductors make them very interesting for applications in future electronics. However, certain issues need to be resolved and solutions needs to be found.

Air sensitivity is a major problem for certain 2D-semiconductors. Five different TMDs were studied over a period of 30 days and $MoS_2$ resulted to be the most stable among them. On the contrary $HfSe_2$ is highly unstable. After one day from exfoliation the surface is characterized by Se-rich blisters and an oxidized surface. The high reactivity of this material poses severe challenges on its use in future applications. In order to use more air-sensitive TMDs in future applications, their degradation needs to be contained. Chemical funcionalisation or passivation methods can be interesting solutions, but they need to be optimised to protect the surface from exposure.

Due to the immaturity of the material growth, the mobility of 2D-semiconductors is limited by impurities. Both numerical and SIMS analysis showed a high concentration of a wide range of impurities in exfoliated crystals, which highly degraded the mobility and the electrical performance of TMD-based FETs. This might be solved by more sophisticated growth techniques, as CVD or ALD. In addition, due to the low thickness of the materials, the dielectric environment plays an important role on their electrical performances.

In terms of FET-applications, contact resistance is probably the most important bottleneck to date. In the case of $MoS_2$, it was shown that high-doping concentration can be an optimum way to reduce contact resistance. The results are comparable with both the roadmap for semiconductors (IRDS) and with literature. In the case of $PtSe_2$, forming gas annealing was shown to cause a reaction between the metal and the $PtSe_2$. The 3D-alloy formed can be important for contact resistance optimization. An optimum contact behavior can be achieved by the opportune combination of both these techniques. However, a reliable doping technique needs to be developed for TMDs. Substitutional doping might be introduced only during the growth of the material, therefore chemical or high-k doping might be optimal solutions. In addition, certain pair metal-TMDs might be used to form a TMD-metal 3D-alloy.

Finally, TCAD modelling is an important tool to further study and understand the behavior of new material systems. The model was improved introducing VdW-gaps in the structures and tuning the vertical transport with experimental results. The TCAD model was then used to study the behavior of $MoS_2$-based scaled FETs. Future studies can focus on the optimization of the model by more advanced tools, as quantum Monte Carlo or density functional theory simulations, as well as a proper tuning of more accurate material parameters.

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