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Authors	Caruso, Enrico;Lin, Jun;Monaghan, Scott;Cherkaoui, Karim;Gity, Farzan;Palestri, Pierpaolo;Esseni, David;Selmi, Luca;Hurley, Paul K.
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The Role of Oxide Traps Aligned with the Semiconductor Energy Gap in MOS Systems

Enrico Caruso, Jun Lin, Scott Monaghan, *Senior Member, IEEE,* Karim Cherkaoui, Farzan Gity, Pierpaolo Palestri, *Senior Member, IEEE,* David Esseni, *Fellow, IEEE,* Luca Selmi, *Fellow, IEEE,* and Paul K. Hurley

***Abstract*—This work demonstrates that when inelastic tunneling between oxide traps and semiconductor bands is considered, the traps with energy aligned to the semiconductor bandgap play a significant role in the frequency dispersion of the capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics of metal-oxide-semiconductor (MOS) systems. The work also highlights that a non-local model for tunneling into interface states is mandatory to reproduce experiments when carrier quantization in the inversion layer is accounted for. A model including these ingredients is used to evaluate the energy and depth distribution of oxide traps in a n-$In_{0.53}Ga_{0.47}As/Al_2O_3$MOS system, and is able to accurately fit the C-V frequency dispersion from depletion to weak inversion. The oxide trap distribution determined from the C-V response predicts the corresponding G-V dispersion with frequency.**

***Index Terms*—Oxide Traps, Interface Traps, Defects, C-V, G-V, Multifrequency, Spectroscopy, TCAD, Tunneling, Multi-phonon, InGaAs, Al_2O_3, Quantum Effects, quantization, NMP**

I. Introduction

As conventional silicon based field effect transistors approach the limit of dimensional scaling, new materials and architectures are being investigated to underpin and boost the next generation of integrated circuits. Monolithic 3D co-integration of Silicon CMOS (complementary metal oxide semiconductor), opens up a range of new opportunities to enhance the functionality of systems-on-chip, to reduce power consumption and decrease the overall system cost [1], [2]. In the past decade, important steps have been made towards the integration of memory [3], [4], logic [3], [4], RF [5] and power [6] devices on Silicon wafers, using several candidates semiconducting materials, including: Ge [7], III-V semiconductors [5], [6], semiconducting oxides [4] and 2D semiconductors [8], [9]. However, the thermal budget constraints associated with monolithic 3D integration, or thermal budget limitations from the material system (e.g., III-V semiconductors), precludes the use of high temperature thermal annealing to reduce oxide defect densities in the high dielectric constant (high-κ) oxides used in conjunction with the alternative semiconducting channels [4], [5], [7]. This leads to defective oxides [10], [11] which result in instability, variability and degradation issues. For these reasons, a correct understanding of the physics and characterization of the oxide defects is needed to overcome the challenges related to the fabrication process of the gate stack.

Recent advances in physics based DC and AC modeling of semiconductor/insulator structures have been achieved which allow a fully physics based simulation of MOS systems, including inelastic tunneling from semiconductors to localized defects in insulators [12]. This opens the possibility to simulate, study and extract the density and distribution of electrically active oxide defects from different experimental results. As far as terminology is concerned, oxide defects are often referred to as border traps [13] to emphasize that they are physically close enough (typically < 3 nm) to the border region between the oxide/semiconductor or oxide/metal interface, to allow tunneling between these defect and free carriers in the channel or metal gate. For insulating oxides in current field effect devices, which are frequently $\leq$ 6 nm, all oxide defects are within 3 nm from the metal or semiconductor interface, so there is no distinction between border traps and oxide traps. In this case, we use the general term of oxide defects, with the notation $\mathrm{D_{OX}(E,z)}$ in $[\mathrm{cm^{-3}eV^{-1}}]$ for the density distribution with energy (E) and distance into the oxide from the semiconductor/oxide interface (z).

In this paper, the InGaAs/high-κ MOS system is used as case study, based on the extensive range of literature for this MOS structure combined with the growing appreciation that traps in the oxide (OTs), as well as interface states (ITs), play a significant role in both the C-V and the G-V response. A physics based model for traps is employed to interpret and reproduce the multi-frequency capacitance-voltage (C-V) characteristics, that have been analyzed in several Refs. [14]–[18], even if the physical origin of dispersion and stretch out of the characteristics in depletion is still under debate [15], [16], [18]. Commonly, the frequency dispersion from depletion to inversion is attributed to an interface trap response and the accumulation frequency dispersion to oxide traps aligned at, or above, the majority carrier band edge [14]–[19]. However, using this approach is difficult to accurately reproduce the full C-V/G-V response through simulations [15]. In particular, the frequency dependent "humps" in the region of weak inversion cannot be fitted without a large electron capture time response of interface traps with energy close to the InGaAs valence band edge [16], [18]. The main limitation of this method is the attempt to explain the capacitance and conductance frequency dispersion in depletion using only interfacial states

E. Caruso, J. Lin, S. Monaghan, K. Cherkaoui, F. Gity and P. K. Hurley are with Tyndall National Institute, University College Cork, Cork, Ireland (e-mail:enrico.caruso@tyndall.ie)

P. Palestri and D. Esseni are with the Polytechnic Department of Engineering and Architecture (DPIA), University of Udine, 33100 Udine, Italy

L. Selmi is with University of Modena and Reggio Emilia (DIEF), 41125 Modena, Italy

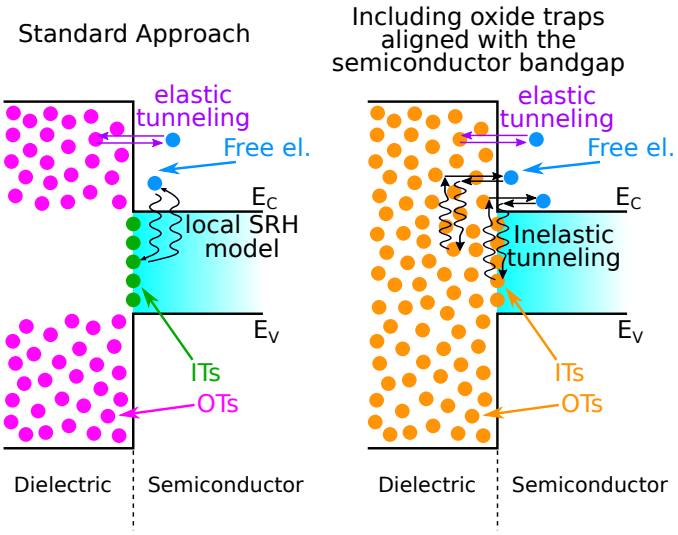

Fig. 1. Sketch of the MOS band diagram including defect and the possible trapping models. In the "standard" approach the simulations rely on the inclusion of interface traps aligned with the semiconductor bandgap, that interact with the free carrier using the local Shockley-Read-Hall (SRH) model (green circles), and oxide traps aligned with the conduction and valence band of the semiconductor, which communicate with the free carrier by elastic tunneling (magenta circles). In this work OTs are included at any energy, also aligned to the semiconductor bandgap. Free carrier and defect communicate through a non-local non-radiative multi-phonon (NMP) model with both elastic and inelastic tunneling (orange circles). In this case, the distinction between ITs and OTs simply relates to the distance from semiconductor/oxide interface.

[14], without providing a full-physical description of the carrier capture/emission process, which has to include both the tunneling through the dielectric barrier and the lattice relaxation at the interface/border trap sites. The comparison between the two different approaches is sketched in Fig. 1 and discussed more in detail in section II.

Building on the work of Ref. [14] we highlight: i) the importance of using OTs energetically aligned with the semiconductor bandgap to reproduce and explain the "humps" of the C-V and G-V curves in weak inversion and ii) the need to use a nonlocal model to describe capture and emission from interface defects when inversion layer quantization effects are taken into account in the physical simulation. It is noted that, while we apply the model to the case of InGaAs/Al_2O_3, it is applicable to all MOS systems.

II. Device and Model Calibration

The experimental samples used in this work are 90 nm Au/ 70 nm Ni/ 6 nm Al_2O_3/ 2 μm n-$In_{0.53}Ga_{0.47}As$/n-InP MOS structures with a nominal S doping concentration of 4×10^{17} cm^{-3} in the InGaAs epitaxial layer, as described in Ref. [20]. The C-V/G-V characteristics have been measured from 1 MHz to 1 kHz with 25 mV signal amplitude, first fixing the the gate bias (V_G) and then performing the AC measurements at various frequencies, and not vice versa. In this way, transient effects due to traps dynamics are minimized yielding experimental conditions closer to the simulation environment, where the linearized small signal AC analysis is carried out after solving the stationary problem. In addition, the C-V/G-V data was measured from accumulation to inversion and was obtained by interpreting the impedance and phase angle data of the measurement system (Agilent E4980A) as a parallel combination of a capacitance and a conductance. This is important, as the impedance and phase angle data generated by the simulation environment is converted to a capacitance and a conductance based on a parallel model.

Sentaurus [21] simulations include Fermi-Dirac statistics and multi-valley/non-parabolic band structure. Generation–recombination processes governing carriers transitions between conduction and valence bands are modeled using the Shockley-Read-Hall (SRH) theory and described by the minority carrier lifetime τ_g. Quantum corrections of the carrier density are taken into account via the modified local density approximation [22] (MLDA). The interface traps distribution ($D_{IT}(E)$ in [$cm^{-2}eV^{-1}$]) is considered in simulations using the SRH extended formalism for phonon-assisted recombination at defects in semiconductor devices. In the SRH model, the recombination center is described either by a capture cross section σ and a trap level E_T or as distributed levels $D_{IT}(E)$. For the case of oxide traps, the models for interaction of the defects with free carriers in the semiconductor conduction and valance bands requires sophisticated models accounting for the tunneling process [23]. Usually, the electrical characteristics are interpreted by modeling the OTs as a distributed network of capacitors/resistors assuming elastic tunneling, as shown in Refs. [15], [17], [24]. However, it has long been understood that charge exchange between oxide states and the channel occurs via a multi-phonon rather than an elastic tunneling process [23], [25]. For these reasons, this work employs the inelastic nonlocal band-to-trap tunneling model used in Ref. [12] which relies on the non-radiative multi-phonon (NMP) theory [23], [26]. In the NMP model, the electrically active defect is described by a trap volume V_T (equivalent to σ for ITs), the Huang-Rhys factor S, the phonon energy $\hbar\omega$, the tunneling mass m_t and either a trap level localized in energy and space $E_{T,z}$ or a distribution of levels $D_{OX}(E,z)$. The Huang-Rhys factor S is linked to the relaxation energy (E_{REL}) of the defect through the relation $E_{REL} = S\hbar\omega$. It represents the energy that is required for the lattice relaxation process to occur [12], [27], determines the capture and emission time constants and their temperature dependence. Moreover it can be useful to identify the physical nature of the defects [28], [29]. E_{REL} is a property of the defect and very little data on Al_2O_3 is available in the literature [28], [30], [31]. To our knowledge, there isn't any experimental data which extracts S and $\hbar\omega$ at the same time, however, the expected value for the Al_2O_3 phonon energy is ~50 meV [32], [33] and the Huang-Rhys factor reported in literature is around 12 [28], [30]. In an amorphous oxide, the parameter E_{REL} is distributed in energy due to the non-uniformity in the local environment of the oxide lattice [34]. Although a distributed E_{REL} reproduce the emission and capture time of the defects more accurately than a single value of E_{REL}, such a fundamental description goes beyond the purpose of this work, as well as beyond the options typically available in a commercial TCAD environment. For this reason, a single value of E_{REL} is employed in the simulations.

TABLE I
SIMULATION PARAMETERS FOR ITS AND OTS: CAPTURE CROSS SECTION (σ), TRAP VOLUME (V_T), TUNNELING MASS (m_t), HUANG-RHYS FACTOR (S) AND PHONON ENERGY ($\hbar\omega$).

		ITs	OTs
	InGaAs	$InGaAs/Al_2O_3$	Al_2O_3
σ	-	10^{-15} cm^2 [a]	-
V_T	-	-	10^{-23} cm^3 [b]
m_t	0.043 m_0 [c]	-	0.23 m_0 [d]
S	-	-	12 [e]
$\hbar\omega$	-	-	48 meV [f]

[a] From Ref. [15] (Large spread of σ in the literature [35], [36]);
[b] From Ref. [20]; [c] From Ref. [37] (same as the electron effective mass);
[d] From Ref. [38]; [e] From Ref. [28]; [f] From Ref. [32]

The capture and emission time constants depend also on the trap volume, which is a property of the defect. Most of the NMP models present in literature use the concept of capture cross section [14], [29], [31] instead of trap volume and more importantly only limited experimental data is available for Al_2O_3 [33]. For these reasons, capture cross section values ranging between 10^{-14} cm^2 and 10^{-16} cm^2 are typically assumed for Al_2O_3 defects. In this work, the cubic V_T is chosen to be 10^{-23} cm^3, whose edge correspond to the radius on an IT with a circular capture cross section σ of 1.46×10^{-15} cm^2, a typical value used for interface and oxide defects. The traps dynamic parameter used in simulations are reported in Tab. I.

III. EXPERIMENTAL RESULTS AND SIMULATIONS

Electrically active interface and oxide traps make the experimental C-V response deviate from the ideal case. Hence, it is instructive to first consider the multi-frequency C-V characteristics of the ideal InGaAs MOS structure and the effect of the quantization model for electrons (dashed and dotted lines in Fig. 2). As expected, quantization reduces the accumulation capacitance in devices with thin oxides due to the shift of the charge centroid from the interface [39] (Fig. 3a).

The deviation between the experiments (solid lines in Fig. 2) and the ideal (no traps) case is significant, and is due to the AC and DC response of electrically active defects in the measured structures. At this point, ITs and OTs are introduced in simulations to reproduce the experimental data, using the typical approach embraced in the literature, *i.e.* ITs inside the InGaAs bandgap and OTs in the oxide with energies aligned with the InGaAs conduction and valence band [15]–[18], [24]. The quantum correction model is important to simulate correctly the accumulation capacitance. However, it is incompatible with IT models based on the local SRH theory because a local calculation of the emission rate relies on the carrier density at the interface [21]. When quantization is accounted for, the electron surface concentration drops dramatically for all bias regions (Fig. 3) and so does the associated emission rate.

To correctly simulate the capture and emission rates of interface traps it is then necessary either to i) neglect quantization effects, making an error in the value of the accumulation

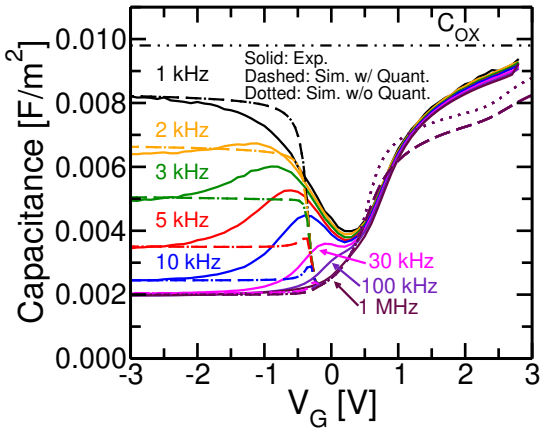

Fig. 2. Experimental multi-frequency C-V (solid lines) at 300 K compared with ideal simulations (without traps). Simulations obtained with/without quantization for electrons are reported with dashed and dotted lines respectively. Simulations use a doping value of $N_D = 4.6 \times 10^{17}$ cm^{-3} (from ECV measurements [20]) and an InGaAs minority carrier lifetime of τ_g=80 ps calibrated in order to match the experimental C-V in inversion. The C_{OX} value used in simulations is shown with the dash-dot-dotted line and assumes an oxide thickness t_{OX}=6.3 nm (from TEM measurements [20]) and a dielectric constant of ε_{OX}= 7 [20].

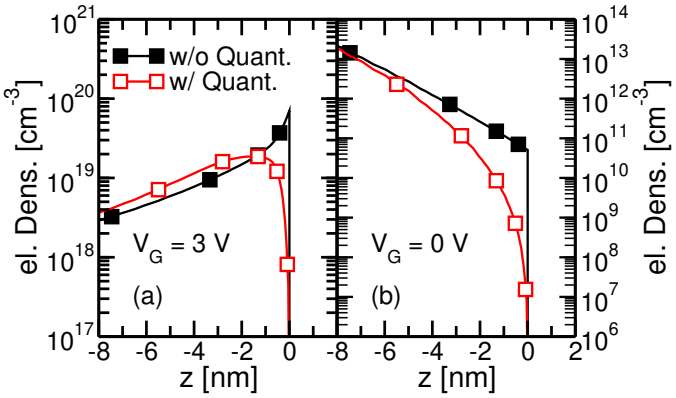

Fig. 3. Comparison between the electron densities extracted from simulations of Fig. 2 along the MOS structure in strong accumulation (a) and in depletion (b). The $InGaAs/Al_2O_3$interface is located at z=0 nm.

capacitance and consequently in the density of oxide traps needed to reproduce experiments or ii) include the quantization and then use a nonlocal model for the interaction between the defects' states and the carriers in the semiconductor.

First, we analyze the consequences of using the SRH model for ITs and neglecting the quantization effects. Fig. 4 compares the experimental C-V with simulations (without quantization) including $D_{IT}(E)$ within the InGaAs bandgap and $D_{OX}(E,z)$ traps at energies primarily above E_C in the InGaAs, shown in Fig. 5. Excellent agreement with the accumulation frequency dispersion can be achieved using the oxide trap energy/depth distribution shown in Fig. 5b. However, even if the simulated peak height of the "humps" in weak inversion match the experimental ones (Fig. 4), the width cannot be reproduced, as also reported in Ref. [15]. In fact, in order to further stretch out the "humps" an unphysically large $D_{IT}(E)$ would be necessary which, in turn, would then result in capacitance "humps" much larger than the ones observed in experiments.

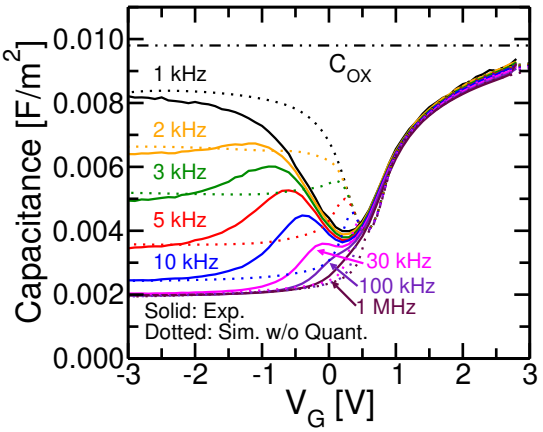

Fig. 4. Experimental multi-frequency C-V (solid lines) and simulated one (dotted lines) including $D_{IT}(E)$ and $D_{OX}(E,z)$ shown in Fig. 5. Simulations use $N_D = 3.0 \times 10^{17}$ cm^{-3} and $\tau_g = 80$ps. Quantization is not active.

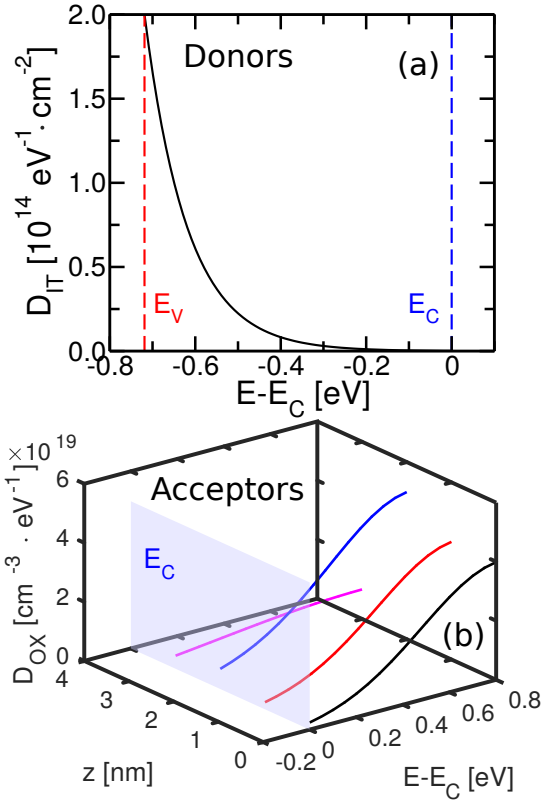

Fig. 5. (a) Donor $D_{IT}(E)$ at the InGaAs/Al_2O_3 interface and (b) acceptor $D_{OX}(E,z)$ inside the Al_2O_3 used in Fig. 4. The energy distributions are referred to the InGaAs conduction band edge (E_C). ITs are defined with energies within the InGaAs bandgap, while OTs above E_C.

It may be noticed in Fig. 5b that OTs located beyond 3 nm into the oxide are not considered. For our device, in fact, the maximum tunneling distance corresponding to an AC signal frequency of 1 kHz, is about 3 nm, so that oxide traps beyond this distance do not contribute to the measured C and G values. In the real device, defects may be located deeper in the oxide, however, their density and distribution cannot be determined beyond this distance due to the experimental conditions. Lower AC signal frequencies for the C-V/G-V measurements, 1/f noise below 1 kHz in MOSFET structures, or C-V hysteresis measurements are required to profile $D_{OX}(E,z)$ beyond this depth.

From the physical point of view there is no reason why the traps in the oxide should not be aligned to the InGaAs bandgap. Most works in the literature do not consider oxide traps aligned with the semiconductor bandgap, as an elastic tunneling model is employed for oxide traps [24]. As a consequence, oxide defects in this energy window are not effective since there are no semiconductor free carriers to interact with the OTs in this energy range. However, there is a large number of reports in literature based on different experiments [40], *i.e.* low frequency noise [41], gate leakage current [42], hysteresis [10], [43] etc., which show the presence of defects in the dielectric aligned to the bandgap of the InGaAs, whose existence has been also predicted by DFT calculations [44]. Finally, many of these experiments suggest that the transitions between the free carriers in the semiconductor and ITs/OTs are governed by inelastic processes assisted by multi-phonons [23], [25], [33]. Following all these considerations, OTs aligned to the semiconductor band gap and an inelastic nonlocal model for interaction of the defects states with electrons/holes in the semiconductor must be included in the simulations to correctly represent the physics of the experiment.

The simulated C-V response is shown together with the experimental response in Fig. 6a, where the results have been obtained by considering the $D_{OX}(E,z)$ distribution shown in Fig. 7 and a nonlocal model for electron and hole interaction with oxide defects. Consequently, quantization effects can be taken into account, and are included in the simulation. It is important to note that this fit to the experimental data is achieved using only oxide traps which extend to the oxide/InGaAs interface. No specific distribution to represent $D_{IT}(E)$ is included at the interface (z=0).

By assuming the same oxide trap distribution used in Fig. 6a the corresponding G-V response (Fig. 6b) is predicted with remarkable accuracy and without any adjustment of the simulated parameters, suggesting again the congruity of the approach and the physics. The agreement between simulations and experiments is good, although second-order adjustments on $D_{OX}(E,z)$ may allow us to further improve the agreement. The inclusion of the OTs aligned to the InGaAs bandgap and extended up to the surface (z=0) and without any need of an additional $D_{IT}(E)$ has improved the agreement in the transition between depletion to weak inversion capacitance and conductance, which has not previously been achieved to this extent [15].

Similar conclusions, on the use of an extended OTs distribution up to the surface (z=0), without using any specific $D_{IT}(E)$, is recently presented in Ref. [45], where a RF characterization of the OTs is carried out for $In_{0.53}Ga_{0.47}As/Al_2O_3$ nanowires.

It should be noted that the energy profile of $D_{OX}(E,z)$ at a given coordinate z (Fig. 8) has shape and values similar to those obtained in other experiments and devices [10], [14], [40], [41], showing a consistency between results extracted with different approaches. It must be stressed that in the stan-

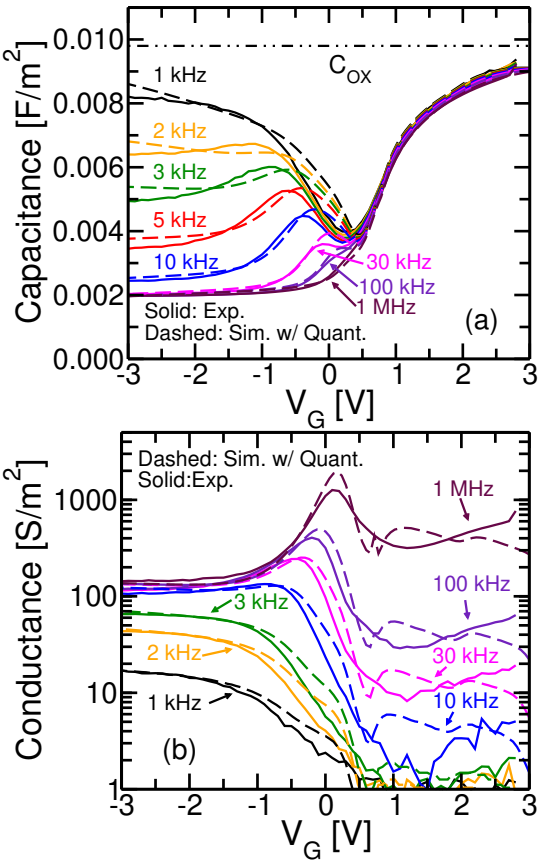

Fig. 6. Experimental (solid lines) multi-frequency C-V (a) and G-V (b) compared with simulated data (dashed lines) including quantization correction and nonlocal model for traps. Simulations use the $D_{OX}(E,z)$ shown in Fig. 7, $N_D = 3.0 \times 10^{17}$ cm^{-3} and $\tau_g = 80$ps. N_D and τ_g have been calibrated in order to match the experimental C-V in strong inversion.

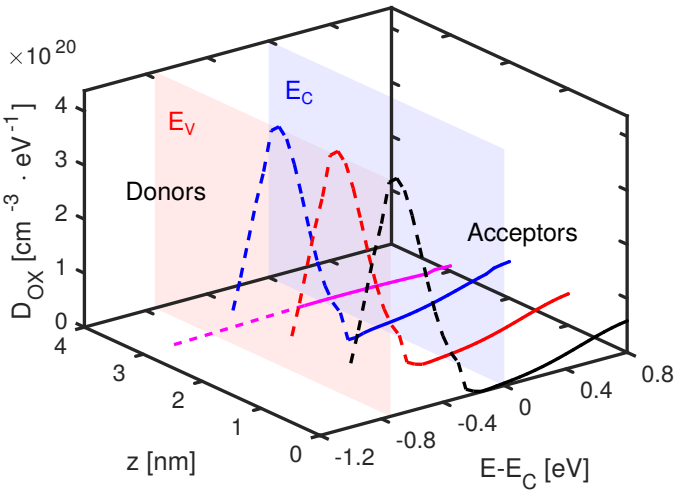

Fig. 7. $D_{OX}(E,z)$ inside the Al_2O_3 of donor and acceptor traps used in simulations of Fig. 6. The energy distributions are referred to the InGaAs conduction band edge (E_C). It is noted that the density of donor states aligned with the InGaAs band gap, and the acceptor states at energies above E_C, both exhibit a gradual increase with depth into the oxide (z).

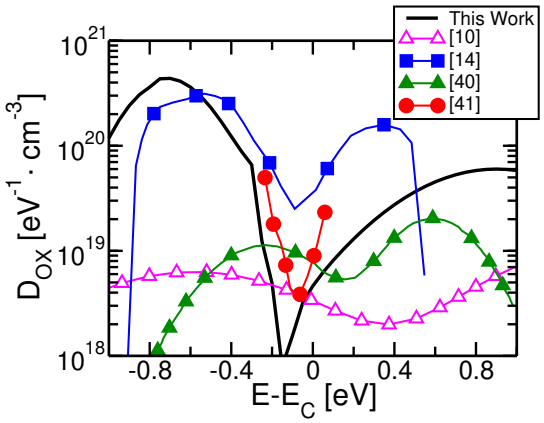

Fig. 8. Comparison between the value OTs density $D_{OX}(E)$ of Fig. 7 at 1 nm inside the Al_2O_3 and the OTs distribution reported in the literature from other devices and extracted from different experiments. OT distributions extracted in [40], [41] (triangle symbols) are based on DC charge trapping measurements (hysteresis and BTI), which assume a uniform distribution of the defect through the whole oxide. Therefore, the extracted effective distribution of OTs (averaged along the oxide) depends on the charging time used in the measurements and thus on the actual occupation of the deep defects in the oxide. If the charging times are not long enough to fill all the defects through the oxide, the resulting $D_{OX}(E)$ might be underestimated. The energy distributions are referred to the InGaAs conduction band (E_C).

dard extraction method based on C-V and G-V response [19], *i.e.* Terman, high-low frequency and conductance methods, all deviations from the ideal C-V/G-V response are interpreted as interface states. As a result, these techniques yield an effective $D_{IT}^{eff}(E)$ which consists of conventional interface states, in addition to a projection to the semiconductor/oxide interface of all oxide traps in the oxide which can respond to the DC sweep and the AC signal at a given frequency. Most of the papers that use these techniques report a rapidly increasing $D_{IT}(E)$ towards and beyond the valance band edge [15], [16], [18], [46], likely due to the projection of the 'z' distribution of OTs on the interface. To illustrate this point Fig. 9 shows the effective IT distribution ($D_{IT}^{eff}(E)$), obtained by spatial integration of $D_{OX}(E,z)$ at flat band condition (no band bending), weighing the contribution of each trap in the oxide in such a way it has the same electrostatic effect of a trap placed at the interface (z=0), that is: $D_{IT}^{eff}(E) = \int_0^{t_{OX}} [D_{OX}(E,z)\,(t_{OX}-z)/t_{OX}]\,dz$. These results are fairly consistent with our present work but they don't provide the spatial distribution of defects into the oxide.

IV. Conclusions

In this work we examined the role of oxide defects aligned with the semiconductor bandgap in MOS structures. As interactions between oxide defects and free carriers in the semiconductor involve multi-phonon transitions, oxide defects at energies aligned with semiconductor bandgap do contribute to the small signal AC response of the MOS structure. In addition it is shown that, when quantum corrections are considered in the numerical calculations, the SRH model for interface states yields incorrect values of the time response. If a non-local model based on NMP theory is introduced instead, the interaction between semiconductor free carriers

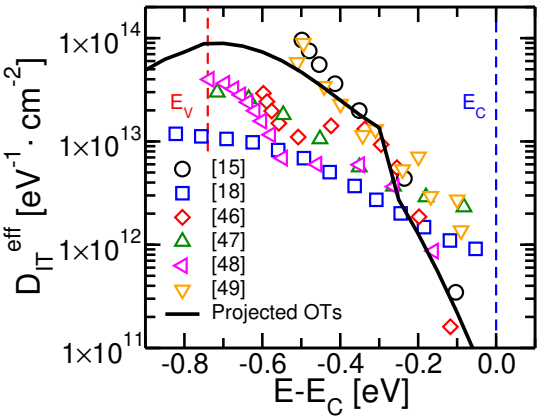

Fig. 9. Comparison between the effective $D_{IT}^{eff}(E)$ obtained from Fig. 7 by the projection of all the electrically active traps at the semiconductor/oxide interface (solid black) and the $D_{IT}(E)$ reported in the literature extracted from different devices and using standard extraction method based on C-V and G-V response. The energy distributions are referred to the InGaAs conduction band edge (E_C).

and oxide defects (either at the interface or in the oxide) is via an inelastic tunneling process, and the distinction between interface states and oxide traps simply relates to the distance from semiconductor/oxide interface.

The model was applied to the InGaAs MOS system, which is known to exhibit a high density of electrically active defect states in the gate insulator. When OTs aligned to the semiconductor bandgap are included, the simulated response of the C-V with frequency can accurately reproduce the experimental characteristics, which is not possible when only ITs are used. The oxide trap density distribution, determined from a fit to the C-V data, also independently reproduces the corresponding G-V response over the frequency range, which is not trivial. While the model was applied to an InGaAs MOS structure in this work, the approach is generic, and is applicable to interpret the data of any MOS system affected by oxide traps.

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