Low-Complexity FPGA-Accelerated NN-Based Adaptive Equalizer for 100 Gb/s IMDD PON

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***Abstract*—We demonstrate a low-complexity, field-programable gate array (FPGA)-based adaptive neural network equalizer to mitigate nonlinear impairments caused by semiconductor optical amplifier (SOA) gain saturation in a 100 Gb/s intensity modulation with direct detection (IMDD) passive optical network (PON). The proposed equalizer employs a 32-tap feed-forward neural network (FFNN) for multi-symbol detection. This approach incorporates both offline training and adaptive learning techniques to ensure real-time adaptability. To enhance FPGA efficiency, the model is quantized to an 8-bit fixed-point format, and the FFNN core is parallelized to achieve a 100 Gb/s throughput. Experimental results show a dynamic range of 27.8 dB and a sensitivity of -22.8 dBm. This approach improves real-time digital signal processing and establishes a foundation for future machine learning-based solutions in next-generation PON systems, addressing key performance challenges.**

***Index Terms*—neural network, FPGA, equalizer, passive optical network,**

I. Introduction

Neural network (NN)-based equalization techniques have gained considerable attention due to their superior ability to compensate for nonlinear impairments where conventional feed-forward equalizers (FFEs) fall short. In particular, these NN-based approaches are poised to play a critical role in future high-speed passive optical networks (PONs). These networks are responsible for delivering high-speed fiber broadband in a cost-effective manner to millions of homes and businesses across the world. A PON system is illustrated in Fig. 1, and comprises an optical line terminal (OLT), usually situated at the service provider's central office, and up to 64 or more optical network units (ONUs) that connect end-users. The OLT functions as the central hub, managing downstream signal transmission to all connected ONUs while simultaneously receiving upstream data from these units. Upstream communication in PON is complex, as multiple ONUs must share the same upstream channel using time-division multiple access (TDMA), requiring them to transmit data in short, intermittent bursts during burst-mode operation.

The ITU-T G.9804.3 PON standard published in 2021 outlines a 50 Gb/s line rate [1]. However, upcoming bandwidth-intensive applications such as AR/VR and 8K video streaming, as well as 5G/6G mobile backhaul deployment scenarios, are motivating research into 100 Gb/s systems. In order to achieve this, bandwidth-efficient modulation in the form of 4-level pulse amplitude modulation (PAM4) is being considered. However, the 29 dB optical loss budget outlined in the standard presents a challenge for PAM4, given its high signal-to-noise ratio (SNR) requirements and the need to support legacy infrastructure. A possible solution for achieving the optical loss budget in 100 Gb/s PAM4 PON is the use of semiconductor optical amplifiers (SOAs) as pre-amplifiers at the OLT [2]. While effective at boosting signal strength, SOAs are prone to gain saturation at high input power levels [3]. This issue is particularly problematic in PON systems, where upstream signals received at the OLT can vary widely in power, due to differing distances and splitter losses between the OLT and individual ONUs. As a result, the OLT receiver dynamic range is a critical performance metric and is defined as the ratio between the weakest and strongest burst packet optical power that an OLT receiver can support without distortion. Signal distortions arising from the SOA gain saturation effect are therefore an obstacle to achieving the minimum 19.5 dB dynamic range required by the 50G PON standard at higher bit rates.

SOA-based optical power equalization methods have been proposed for dynamic range extension while avoiding SOA nonlinearity [4]. However, these methods require additional high-speed circuitry such as a photo-diode and automatic gain controller (AGC) that must be able to adjust the SOA gain within a guard time of tens of nanoseconds on a packet basis.

NN-based equalizer design techniques, such as those using feed-forward or recurrent neural networks (RNNs), offer a powerful approach to mitigating nonlinear impairments and enhancing overall system performance [5], [6]. Recently, our group proposed a novel RNN-based equalizer for 100 Gb/s PAM4 SOA-preamplified PONs, which has been demonstrated to be a highly effective nonlinear equalizer [7]. This solution can simultaneously address the SOA nonlinearity and fiber dispersion impairments in PON, to deliver a large OLT receiver dynamic range of 21 dB. However, the hardware implementation of the equalizer was not discussed, and in particular, the feedback loops intrinsic to RNN architectures are of particular concern, given the significant challenges of implementing these with sufficient throughput on hardware. The authors of [8] struggled with this issue and instead implemented a parallel, fully connected equalizer on a field-programable gate array (FPGA) to compensate for fiber nonlinearities of a 100 Gb/s O-band SOA-preamplified PON. However, the approach

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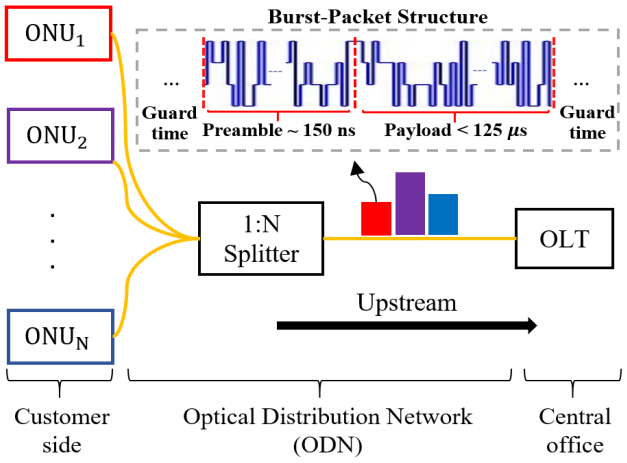

Fig. 1. The upstream transmission architecture in a PON, including an optical line terminal (OLT), an optical distribution network (ODN) containing passive components - such as optical fiber and splitters - and multiple optical network units (ONUs). Additionally, a detailed structure of a burst frame is provided.

in [8] did not assess the equalizer's effectiveness in mitigating SOA nonlinearities. Furthermore, the adaptive training of such NN-based equalizers targeting burst-mode upstream PON deployment, and its implementation in hardware, has not been widely addressed.

In this work, we present a novel adaptive NN equalizer, which employs multi-symbol prediction and leverages the skip connection technique introduced in [7] to facilitate adaptive training. We further demonstrate the feasibility of implementing the proposed equalizer on an FPGA by optimizing resource utilization and reducing computational complexity through the quantization of NN weights and biases to an 8-bit resolution. This study represents, to the best of our knowledge, the first FPGA design of a large dynamic range equalizer for 100 Gb/s intensity modulation with direct detection (IMDD) PON that conducts part of the training within the hardware, signifying a key advancement towards real-time digital signal processing (DSP) solutions for future PON deployments.

II. Experimental Setup

Fig. 2 shows the experimental setup employed in this study. A 50 Gbaud PAM4 signal is generated using a 100 GSa/s digital-to-analog converter (DAC), which includes linear precompensation to account for system bandwidth limitations up to 33 GHz. The high-power C-band transmitter (Tx) is configured using a Mach-Zehnder modulator coupled with an erbium-doped fiber amplifier (EDFA) booster amplifier. The modulated signal is introduced into the SOA (model: CIP-SOA-S), which is biased at a constant current of 100 mA. The input power is adjusted between −26 dBm and +5 dBm using a variable optical attenuator (VOA) to simulate the loss experienced in an optical distribution network (ODN). A 4 nm band-pass filter (BPF) is employed to suppress the amplified spontaneous emission (ASE) noise. An ideal receiver (Rx) configuration is used, comprising an EDFA preamplifier and a 50 GHz photodiode. Waveforms are captured using a

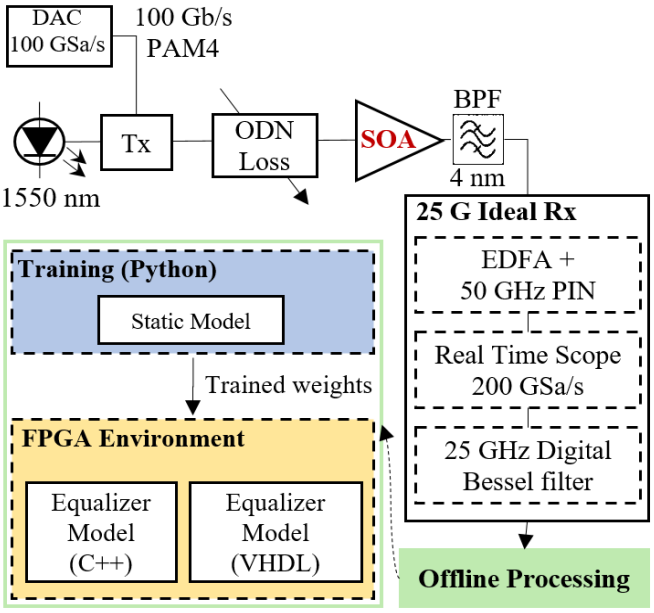

Fig. 2. 100 Gb/s PAM4 back-to-back experimental setup utilizing an SOA preamplifier. DAC: digital-to-analog converter, ODN: optical distribution network, BPF: band-pass filter; SOA: semiconductor optical amplifier; EDFA: erbium-doped fiber amplifier; FPGA: field-programmable gate array

200 GSa/s real-time oscilloscope for subsequent processing and equalization. A 25 GHz 4th-order Bessel filter is utilized to replicate the characteristics of 25 G class optoelectronics. This study utilizes a back-to-back configuration, excluding fiber dispersion, to focus on the nonlinear patterning effect induced by SOA gain saturation. The offline processing block consists of two primary stages: model training in Python and FPGA design environment. In the Python training stage, the proposed feed-forward neural network (FFNN) equalizer is developed to produce the trained neural network parameters. In the FPGA environment, both the adaptive training and inference of the FFNN equalizer are intended for execution on the AMD VC709 FPGA platform [9]. Although this implementation has not been physically executed on the FPGA board, the feasibility of the proposed model is assessed through simulation, synthesis, routing, placement, and bitstream generation stages. Further details regarding the hardware implementation of the equalizer are presented in a dedicated section.

III. FFNN Equalizer Model

A. Multi-Symbol Computation Core Design

The core architecture of the proposed adaptive FFNN equalizer is depicted in Fig. 3(a). The design incorporates 32 input taps and 2 hidden layers with 12 and 8 neurons, respectively. The output layer comprises 5 neurons, adaptively trained within a single FPGA using the multi-input multi-output gear-shifted least mean square (MIMO GS-LMS) algorithm [10]. As the information required to compensate for SOA nonlinearity is mainly in the past symbols, only 32 input taps are needed for the FFNN including 25 past symbols, 2 post symbols, and 5

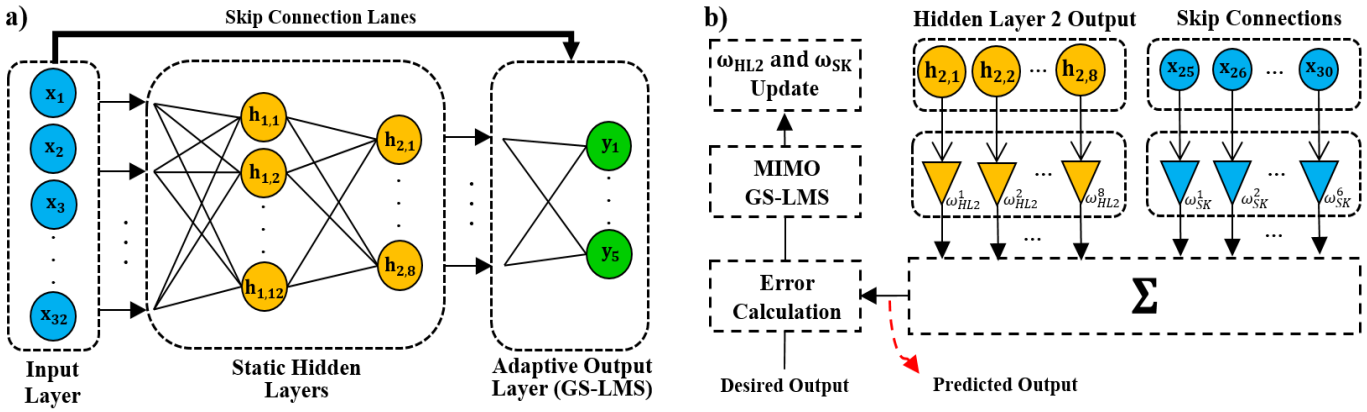

Fig. 3. a) Proposed adaptive FFNN equalizer with skip connection lanes including 32 input taps, two hidden layers with 12 and 8 neurons, respectively, and the adaptive output layer with 5 neurons b) Adaptive training of the FFNN utilizing MIMO GS-LMS algorithm assuming 1 output neuron for simplicity. MIMO GS-LMS: multi-input multi-output gear-shifted least mean square.

predicted PAM4 symbols. This configuration ensures that the most relevant data is used for effective equalization of the SOA patterning impairment. Increasing the number of predicted output symbols in the final layer directly enhances system throughput, as more symbols can be processed simultaneously. However, this improvement comes with trade-offs, requiring a careful balance between resource constraints, potential increases in latency, and maintaining performance accuracy. The hidden layers use the rectified linear unit (ReLU) activation function, due to their computational efficiency in hardware implementations, while the output layer employs a linear activation function to generate real-valued sample predictions for multi-symbol detection. Offline training is performed in Python, using signal data collected at an SOA input power of +4 dBm, a level at which the SOA operates in its nonlinear regime. The training adjusts the weights and biases of the hidden layers to mitigate the SOA's patterning effects at this saturating input power. These weights and biases are then fixed during hardware design, while the output layer weights remain adaptive and are trained within the FPGA. The proposed design also includes skip connections from the input taps to the output layer, facilitating faster convergence and improved accuracy during adaptive training.

Fig. 3(b) shows the adaptive training section, where a MIMO GS-LMS algorithm dynamically updates the output layer weights based on data coming from 14 lanes: 8 lanes from the second hidden layer output and 6 lanes directly from the input taps via the skip connections. In this work, only the sample inputs from 25 to 30 are fed to the output layer through skip connections. After performing the multiply-accumulate (MAC) operation on the data lanes, the MIMO GS-LMS algorithm dynamically adjusts the learning rate to achieve faster convergence and more accurate weights. Finally, the output layer weights obtained during adaptive training on hardware are employed in the inference phase which is carried out on the same FPGA. In the proposed FFNN equalizer, skip connections are utilized to enhance performance for low-power input signals, where the SOA is operating in its linear regime. Skip connections allow direct pathways for the input taps to bypass the nonlinear hidden layers, and feed directly into the output layer. Therefore, the core hidden layers are used to equalize signals affected by SOA nonlinear patterning, while the skip connections allow for effective equalization when the SOA nonlinearity is less severe, or not present. These skip connections are vital, since without them, the hidden layers trained on highly saturated signal data would act to corrupt such unimpaired signals. By providing a direct pathway for input symbols, skip connections allow the model to better handle variations in SOA power levels, ensuring faster convergence and improved performance across a range of operating conditions.

By feeding past and current symbols directly to the output layer, the equalizer can mitigate simpler impairments or mild nonlinearities without engaging the more computationally expensive hidden layers. This reduces the overall complexity and computational load of the network in real-time scenarios. When SOA nonlinearity is low, the equalizer can still maintain accuracy and performance by focusing on the most relevant input symbols (through the skip connections), thereby avoiding unnecessary backpropagation through the entire network.

B. Quantization Analysis

To optimize FPGA resource utilization and reduce system complexity, neural network parameters—such as weights, and biases—are quantized from a 32-bit floating-point format to a fixed-point format with a customized bit resolution. Prior to hardware design, the FFNN equalizer is quantized in MATLAB to identify the optimal allocation of integer and fractional bits for the model weights and biases. Fig. 4 presents the bit error rate (BER) curve, a critical metric for assessing system reliability, across various bit widths, measured with the SOA input power set to +4 dBm. A bit width of up to 6 is insufficient to achieve a BER below the hard-decision forward error correction (HD-FEC) threshold. Although a bit width of 7 is adequate, in this work, all weights and biases of the FFNN equalizer are quantized to 8-bit precision to ensure satisfactory performance. In cases of severe hardware resource limitations, the bit width can be reduced to 7, while still preserving performance within an acceptable range. This comprehensive quantization approach

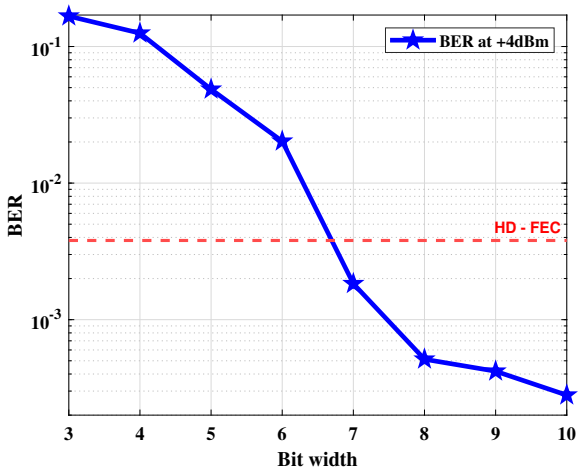

Fig. 4. Quantization analysis of the FFNN equalizer. The BER corresponds to the scenario in which the input power to the SOA is set at +4 dBm.

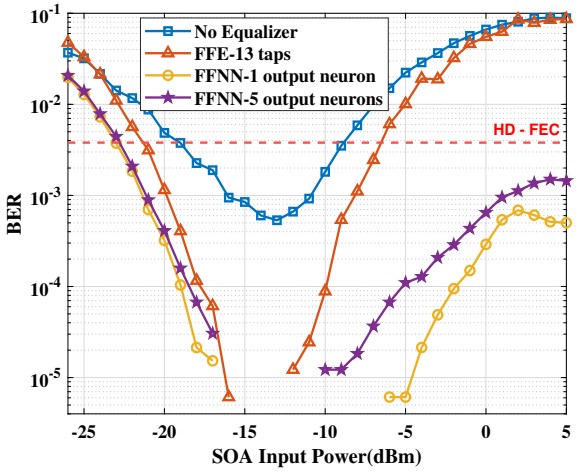

Fig. 5. BER performance, estimated by counting errors over 163k symbols, is compared for the proposed feed-forward neural network (FFNN) equalizer with 1 and 5 output neurons, a conventional 13-tap feed-forward equalizer (FFE), and without equalization in a 100 Gb/s PAM4 PON transmission as the SOA input power increases.

ensures that the neural network model remains resource-efficient within hardware constraints, achieving a crucial balance between computational accuracy and hardware efficiency that facilitates smooth integration into hardware deployments.

IV. FPGA Implementation and Results

FPGA prototyping for DSP solutions is frequently used to evaluate the feasibility of a design before proceeding with the development of an application-specific integrated circuit (ASIC). The implementation of the adaptive FFNN equalizer on an FPGA is carried out in two key phases. Initially, high-level synthesis (HLS) is performed using the AMD Vitis HLS tool [11]. In this process, the design is described in C++, and its behavioral functionality is confirmed through a series of simulations. In the second phase, the design is imported into the AMD Vivado tool [12] for synthesis, routing, and placement on the FPGA, ultimately leading to the bitstream generation. In FPGA design, it is crucial to specify the target chip prior to implementation on the selected evaluation board, as each chip comes with its unique constraints. Hereafter in this paper, the term "implementation" on FPGA refers to all hardware-related steps carried out before deploying the design on an actual board. This approach not only validates the design's feasibility but also ensures that all critical hardware requirements for implementing the equalizer on the FPGA board are addressed, ensuring that the results align with those obtained from implementation on the physical board. Therefore, the FPGA resource utilization obtained from this stage indicates that the design is ready for deployment on an evaluation board.

A critical aspect of neural network implementation on FPGAs is the choice of activation function. While functions like hyperbolic tangent or Sigmoid demand resource-intensive approximations, such as piecewise linear methods or Taylor series expansion [13], ReLU is computationally efficient due to its simplicity. ReLU only involves a simple comparison operation that takes the maximum of the input and zero, making it ideal for FPGA-based implementations. Upon implementing the equalizer core on the FPGA, the design successfully meets all timing requirements at a clock frequency of 70 MHz. This frequency represents the maximum frequency that ensures timing closure—a condition where all signals reach their destinations within the designated time frame for each clock cycle. Applying efficient pipelining techniques, which divide long signal paths into shorter, manageable segments, mitigates critical path delays and enables stable performance at this frequency. To achieve a throughput of 100 Gb/s, the FFNN structure must be parallelized within the FPGA. However, the level of parallelization cannot be excessively high, as increasing parallelization demands more hardware resources. Therefore, an optimal balance must be established between the selection of the number of output neurons and the level of parallelization to ensure efficient resource utilization. The throughput obtained through hardware implementation can be expressed as

$$T_{HW} = CLK \times k \times N_O \times PF \tag{1}$$

where CLK represents the maximum operating frequency achieved in the FPGA, k denotes the number of bits per symbol where k = 2 for PAM4, N_O signifies the number of output neurons, and PF stands for the parallelization factor. According to equation 1, with 5 neurons in the output layer, parallelizing the FFNN core at 143 levels in the FPGA will result in a throughput of approximately 100 Gb/s. It is important to note that the number of output neurons is constrained by the available skip connection lanes. In the case of the FFNN equalizer with 6 skip connection lanes, the maximum number of output neurons is limited to 5. Exceeding this limit would significantly degrade the performance of the system.

Fig. 5 provides a comparison of the BER performance across different SOA input power levels for the proposed adaptive FFNN equalizer with 1 and 5 neurons, a conventional FFE with 13 taps, and the scenario without an equalizer. The x-

TABLE I
FPGA RESOURCE UTILIZATION ON AMD VC709 EVALUATION KIT FOR THE FFNN EQUALIZER WITH 5 OUTPUT NEURONS.

	Training	Inference	**Overall Utilization**
Lookup Tables	25467 (5.88%)	26981 (6.23%)	**52448 (12.11%)**
Flip-Flops	11872 (1.37%)	11634 (1.34%)	**23506 (2.71%)**
Block RAMs	48 (3.26%)	92 (6.3%)	**140 (9.56%)**
DSP Slices	604 (16.78%)	594 (16.5%)	**1198 (33.28%)**
Operational Clock (MHz)	70	140	**70**
Parallelization Factor	**143**		
Throughput (Gb/s)	**100**		

axis represents the SOA input power, ranging from −26 dBm to +5 dBm, which is crucial for PON systems because it reflects the range of optical power levels the SOA is likely to encounter in real-world deployment. In 100 Gb/s PONs, SOAs are used as preamplifiers to boost signals, but they suffer from gain saturation at higher power levels, leading to severe nonlinear impairments. This experiment emulates such conditions, with the goal of assessing the equalizer's ability to mitigate and adapt to these nonlinearities. The dynamic range can be inferred from the figure by noting the range of input power levels over which the system maintains a low BER below a certain threshold. While the conventional FFE offers moderate improvements over the no-equalizer case, it struggles to effectively handle the nonlinear effects. In contrast, the proposed FFNN equalizer maintains a significantly lower BER, demonstrating its superior capacity to compensate for SOA-induced impairments. The system achieves a dynamic range of 27.8 dB and a sensitivity of −22.8 dBm, which are critical for maintaining signal integrity over long distances and variable power levels in PONs. This makes the FFNN equalizer a highly practical solution for next-generation PONs, enabling reliable high-speed data transmission even under challenging optical conditions.

In terms of hardware resource efficiency, the inclusion of 5 output neurons results in a throughput five times higher than that of a single output neuron, facilitating real-time processing at 100 Gb/s PAM4 PON transmission. While this increases FPGA resource utilization slightly, the trade-off is justified by the substantial gains in system throughput. Table I provides a detailed breakdown of FPGA resource utilization on AMD VC709 Evaluation Kit, illustrating how the system efficiently balances performance and hardware constraints to achieve 100 Gb/s throughput. During the training phase, the adaptive output layer leverages the GS-LMS algorithm, which primarily uses MAC operations, reducing the demand for extensive FPGA resources. This resource-efficient approach allows the system to optimize hardware usage without compromising performance. As indicated in the results in Fig. 5, managing nonlinear impairments in PONs operating at 100 Gb/s is a critical challenge. By integrating the proposed adaptive FFNN equalizer with an FPGA platform, the system demonstrates real-world applicability, offering a high-performance solution with scalable hardware implementation. The ability to achieve low BER while sustaining a high dynamic range and sensitivity highlights the effectiveness and practicality of this approach for high-speed optical access networks.

V. CONCLUSION

In this study, we developed a novel, low-complexity adaptive NN-based equalizer for 100 Gb/s IMDD PON and evaluated the feasibility of its implementation on an FPGA platform. To enhance FPGA resource efficiency, NN equalizer parameters were quantized to an 8-bit fixed-point format. By employing adaptive training, multi-symbol detection, and parallelizing the equalizer architecture in hardware, the system achieved a 100 Gb/s throughput. The experimental results further indicate that the BER remained below the HD-FEC threshold, with a sensitivity of −22.8 dBm and a dynamic range of 27.8 dB. This development represents a major step forward in the realization of real-time DSP solutions for next-generation high-speed PONs.

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