CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

Title	Mathematical analysis of prime modulus quantizer MASH digital delta-sigma modulator
Authors	Hosseini, Kaveh;Kennedy, Michael Peter
Publication date	2007-12-01
Original Citation	Hosseini, K., Kennedy, M.P., 2007. Mathematical analysis of prime modulus quantizer MASH digital delta-sigma modulator. IEEE Transactions On Circuits and Systems II - Express Briefs, 54 (12), pp.1105-1109.
Type of publication	Article (peer-reviewed)
Link to publisher's version	10.1109/TCSII.2007.905877
Rights	©2007 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.
Download date	2026-10-12 06:05:53
Item downloaded from	https://hdl.handle.net/10468/141

UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Mathematical Analysis of a Prime Modulus Quantizer MASH Digital Delta–Sigma Modulator

Kaveh Hosseini, *Student Member, IEEE*, and Michael Peter Kennedy, *Fellow, IEEE*

***Abstract*—A MASH digital delta–sigma modulator (DDSM) is analyzed mathematically. It incorporates first-order error feedback modulators (EFM) which include prime modulus quantizers to guarantee a minimum sequence length M. The purpose of this analysis is to calculate the exact sequence length of the aforementioned MASH DDSM. We show that the sequence length for an lth-order member of this modulator family is M for all constant inputs, and for all initial conditions, where M is the sequence length of the constituent first-order prime modulus quantizer EFMs.**

***Index Terms*—Digital delta–sigma modulator (DDSM), MultistAge noise SHaping (MASH), prime modulus quantizer and fractional-N frequency synthesizer.**

I. Introduction

THE DIGITAL delta–sigma modulator (DDSM) is a building block which can be used effectively to implement fractional division in frequency synthesis applications [1]–[4]. Fig. 1 shows the block diagram of a delta–sigma controlled fractional-N phase-locked loop (PLL) synthesizer. It includes a phase frequency detector (PFD), a charge pump, a loop filter and a voltage controlled oscillator (VCO) in the forward path, and a DDSM-controlled multi-modulus divider (MMD) in the feedback path. The DDSM digitally controls the division modulus of the MMD so that the average division ratio over many periods of the reference frequency is the prescribed fractional value.

The input to the DDSM may be a high resolution constant digital word X which sets the fractional division ratio; its output is a low resolution sequence $y[n]$ which controls the MMD value. In this case, the output spectrum of the DDSM contains the desired input dc tone, which sets the fractional part of the division, plus additional frequency components resulting from the digital re-quantization which are collectively called quantization noise. The quantization noise is high-pass filtered by the spectral shaping properties of the DDSM so it can be removed by the low-pass operation of the PLL [3]. MultistAge noise SHaping (MASH) is a popular configuration of the DDSM which is used for high-order filtering in this application [4]. In this brief, we focus on a particular MASH DDSM architecture [5] with a constant input.

It is usually assumed that the quantization noise of the quantizer of a DDSM is additive, white and aperiodic. Note, however, that the fact that the DDSM is a finite-state machine (FSM) means that it always produces a *periodic* output sequence (a cycle) when the input is a constant. In this case, the quantization noise sequence is also periodic. In general, the period depends on the input, the initial conditions, and the architecture of the DDSM. When the sequence length[1] is short, the power of the sequence is distributed among a limited number of tones (so-called "spurious tones") that appear in the DDSM output spectrum. The powers of the spurious tones (spurs) can be significantly higher than the noise-shaping curve predicted by the simplifying assumption that the internal quantizer(s) can be modelled as an aperiodic additive white noise source.

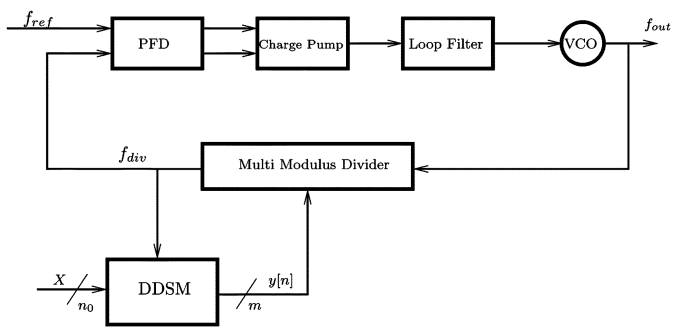

Fig. 1. Block diagram of the DDSM controlled fractional-N frequency synthesizer.

Previous work has investigated extensively the periodic behavior of different configurations of DSMs with constant input. Hein and Zakhor [6] presented analytical and approximate techniques to aid the analysis and design of discrete-time analog double-loop and higher order single-loop modulators. Hyun and Fischer [7] used state-space matrices to describe constant input single-stage single-bit DSMs in order to characterize and validate the limit cycles. Recent work [8] and [9] used state-space descriptions of higher order single-bit feedforward and feedback topologies to develop an exact mathematical framework with which to analyze the structure of limit cycles.

Friedman [10] investigated second-order single-loop modulators and showed that due to the finite word lengths of the arithmetic units in the case of a digital implementation, a constant input to these modulators is represented by a rational number and the modulators always converge to a limit cycle. Gray showed [11], that for a first-order modulator with a dc input, the output spectrum consists of discrete spurs whose locations and amplitudes depend on the input value. This analysis was extended to higher order MASH modulators in [12] and [13]. The authors of [12] and [13] have proven mathematically that, in a higher order MASH modulator, the additive white

Manuscript received May 25, 2007. This work is supported in part by Science Foundation Ireland under Grant 02/IN.1/I45. This paper was recommended by Associate Editor G. Manganaro.

The authors are with the Department of Microelectronic Engineering, University College Cork, and Tyndall National Institute, Cork, Ireland (e-mail: kaveh.hosseini@ue.ucc.ie; peter.kennedy@ucc.ie).

Digital Object Identifier 10.1109/TCSII.2007.905877

[1]In this brief, we use the term *sequence length* instead of period (or cycle length) unless otherwise stated.

1549-7747/$25.00 © 2007 IEEE

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 11:43:40 EDT from IEEE Xplore. Restrictions apply.

noise source assumption for the quantizer error from the last stage is correct when *irrational* dc inputs are employed.

These mathematical analyses [11]–[13] of modulators were performed with the assumption of zero initial condition on the integrators. For the case of irrational dc inputs, the asymptotic behavior of the quantizer error is not affected by the initial conditions [11]–[14]. Kozak and Kale [14] provide an exact analysis for higher order MASH DSMs with rational dc inputs (the DDSM case) and nonzero initial conditions. Their statistical approach shows that an irrational initial condition imposed on the first accumulator guarantees a tone-free output spectrum for third-order and higher order MASH modulators driven by rational dc inputs.

In attempting to extend their theoretical results to the case of *rational* initial conditions (the DDSM case), Kozak and Kale suggest that if the internal digital word length of a fixed-point DDSM is relatively high (> 15 for third-order or higher order MASH DDSMs), irrational initial conditions can be approximated using odd numbers.

Recent work [15] and [16] recommends setting an odd initial condition on the first accumulator of the MASH DDSM in order to maximize the sequence length. In fact, setting the initial condition of the first stage yields a maximum guaranteed minimum sequence length for all constant inputs [15]. If the modulator word-length is large, the lengths of the sequences become large. The modulus of the quantizers in this case is equal to 2^{n_0}, where n_0 is the accumulator's word length.

One way to disrupt short sequences in DDSMs is to apply dither. Dithering breaks up the cycles and increases the effective sequence length, resulting in smoother noise-shaped spectra. While it increases the sequence length, as required, dithering inherently adds noise to the spectrum; care must be taken to minimize the contribution of this additional noise. A state of the art solution is to add shaped pseudorandom least single bit (LSB) dither to the input of the MASH DDSM [17].

Another way to maximize the minimum sequence length for all constant inputs is to use a prime number as the modulus of the quantizer [5]. In this brief, we investigate this method from the perspective of sequence lengths. Exploiting this observation, a first-order error feedback modulator (EFM) has been proposed in which the quantization interval is a prime number [5]. The sequence length for this first-order EFM is always M, which is equal to the quantizer interval. Based on this architecture, Level *et al.* [5] proposed a higher order MASH DDSM. Considering this system as a finite state machine and applying the methods of discrete-time dynamical systems, we calculate its steady-state sequence length. We prove that cascading stages of this type to build a higher order MASH does not increase the sequence length when the input is a constant. Rather, the sequence length is always equal to that defined by the first stage. Nevertheless, the advantage of the prime modulus MASH architecture is that it has a maximum guaranteed minimum sequence length for all constant inputs and for all initial conditions. Although stages after the first do not increase the sequence length, they do contribute to whitening the quantization noise.

In Section II, we describe the first-order EFM with a prime interval quantizer and the MASH structure [5] based on this first-order modulator. We then calculate the sequence length of this MASH DDSM in Section III. We prove that the sequence length is M for all constant inputs, for all initial conditions, and for all orders of MASH of this type. We summarize our contribution in Section IV.

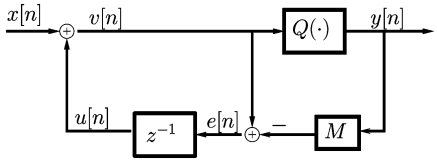

Fig. 2. Block diagram of the first-order EFM (EFM1); all the signals are integers.

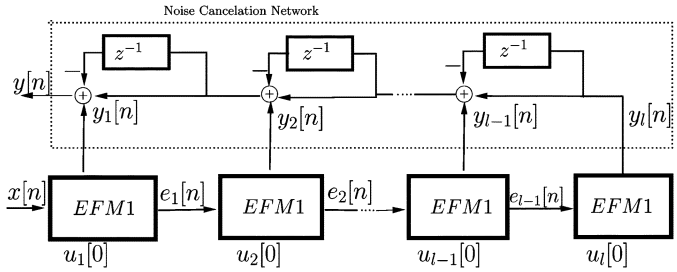

Fig. 3. Prime modulus quantizer MASH; EFM1 corresponds to the block shown in Fig. 2.

II. Prime Modulus Structure

The block diagram of a first-order EFM is shown in Fig. 2. The digital input to the modulator can be a constant value or a sequence of digital values with n_0-bit resolution. The quantizer input-output relationship is

$$y[n] = Q(v[n]) = \begin{cases} 0, & v[n] < M \\ 1, & v[n] \geq M \end{cases} \tag{1}$$

where M is the modulus of the quantizer and $v[n]$ is the input to the quantizer. The sequence length of this structure is determined by solving the following condition [16]:

$$(NX) \bmod M = 0 \tag{2}$$

where N is the sequence length and X is the constant digital input to the modulator. If the greatest common divisor of X and M is equal to 1, then the sequence length is M. Therefore, if M is a prime number then the sequence length N is always equal to M, for all constant inputs. Also, N is independent of the initial condition since the latter does not appear in (2). Based on the prime modulus quantizer EFM, a higher order MASH modulator can be developed. Fig. 3 shows an example of an lth-order prime quantizer MASH inspired by the third-order structure described in [5]. In the figure, all the first-order stages are identical and have prime modulus quantizers. We will prove that the sequence length of this structure is equal to that of the first-order modulator. In other words, while the sequence length is fixed for all constant inputs and for all initial conditions, adding stages to the MASH does not increase the sequence length.

III. Calculation of Sequence Length

In this section, we calculate mathematically the sequence length of the lth-order MASH discussed in the previous section. We write the state equations where $e_i[\cdot]$ is the state variable

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 11:43:40 EDT from IEEE Xplore. Restrictions apply.

associated with stage i. Referring to Fig. 2 and (1), we write for the first stage of Fig. 3

$$e_1[n] = v_1[n] \bmod M \tag{3}$$

where M is the modulus of the quantizer. Writing the equation at the input summing node, we obtain

$$e_1[n] = (x[n] + e_1[n-1]) \bmod M \tag{4}$$

where $x[n]$ is the input to the first stage. We can rewrite the above equation as

$$e_1[n+1] = (x[n+1] + e_1[n]) \bmod M. \tag{5}$$

Repeating the same process for the ith stage, we obtain

$$e_i[n+1] = (e_{i-1}[n+1] + e_i[n]) \bmod M \tag{6}$$

where $e_{i-1}[n+1]$ is the error of the previous stage $i-1$ applied as the input to the stage i. Starting from (5), assuming a constant input $x[n] = X$ (for all n), and expanding the indexes of (6) from 1 to l, we derive a set of equations which we write in matrix form as

$$E[n+1] = (AE[n] + BX) \bmod M \tag{7}$$

where the lower triangular matrix A and the vectors B and E are

$$A = \begin{pmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & & & \vdots \\ 1 & 1 & \cdots & 1 & 0 \\ 1 & 1 & \cdots & 1 & 1 \end{pmatrix}_{l \times l} \tag{8}$$

$$B = \begin{pmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{pmatrix}_{l \times 1} \quad \text{and} \quad E = \begin{pmatrix} e_1 \\ e_2 \\ \vdots \\ e_l \end{pmatrix}_{l \times 1}. \tag{9}$$

Using (7) and expanding it over its indexes from $E[n+2]$ to $E[n+N]$, we obtain

$$\begin{aligned} E[n+2] &= (AE[n+1] + BX) \bmod M \\ &= (A(AE[n] + BX) \bmod M + BX) \bmod M \\ &= (A(AE[n] + BX) + BX) \bmod M \\ &= (A^2 E[n] + (A^1 + A^0)BX) \bmod M. \end{aligned} \tag{10}$$

For index $n+3$, we write

$$E[n+3] = (AE[n+2] + BX) \bmod M. \tag{11}$$

Substituting (10) into (11) and following the same process for achieving (10), we obtain

$$E[n+3] = \left(A^3 E[n] + \left(\sum_{k=0}^{2} A^k \right) BX \right) \bmod M. \tag{12}$$

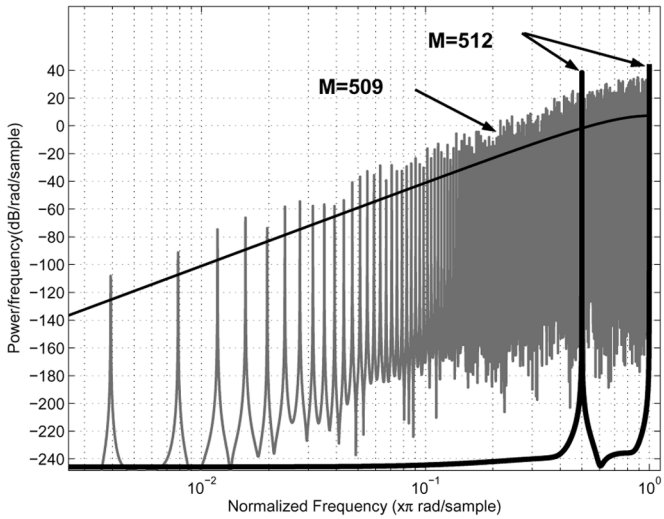

Fig. 4. Output spectra of MASH1–1-1 with zero initial and input 256 for two cases of $M = 512$ and prime $M = 509$. The solid curve represents the expected spectrum, assuming additive white quantization noise.

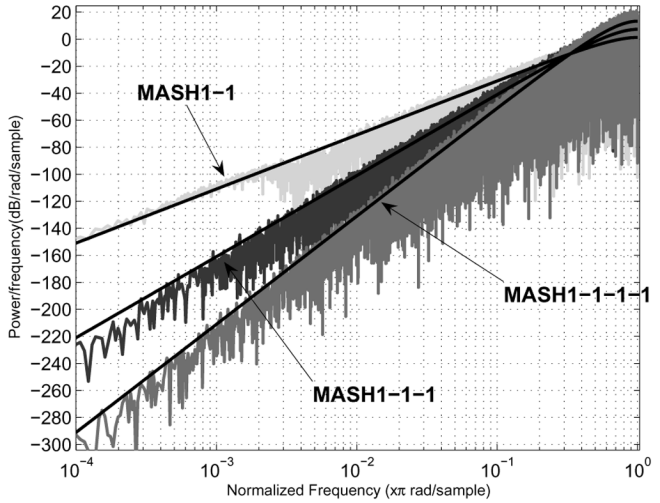

Fig. 5. Output spectra of MASH1–1, MASH1–1-1 and MASH1–1-1–1 with input 1. The quantizer interval is $2^{17}-1$. The solid curves represent the expected spectrum, assuming additive white quantization noise.

Finally, for index $n+N$, we have

$$E[n+N] = \left\{ A^N E[n] + \left(\sum_{k=0}^{N-1} A^k \right) BX \right\} \bmod M. \tag{13}$$

We substitute the identities shown in

$$A^N = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ C_1^N & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & & & \vdots \\ C_{l-2}^{N+l-3} & C_{l-3}^{N+l-4} & \cdots & 1 & 0 \\ C_{l-1}^{N+l-2} & C_{l-2}^{N+l-3} & \cdots & C_1^N & 1 \end{bmatrix}_{l \times l} \tag{14}$$

$$\sum_{k=0}^{N-1} A^k = \begin{bmatrix} C_1^N & 0 & \cdots & 0 & 0 \\ C_2^N & C_1^N & \cdots & 0 & 0 \\ \vdots & \vdots & & & \vdots \\ C_{l-1}^{N+l-3} & C_{l-2}^{N+l-4} & \cdots & C_1^N & 0 \\ C_l^{N+l-2} & C_{l-1}^{N+l-3} & \cdots & C_2^N & C_1^N \end{bmatrix}_{l \times l} \tag{15}$$

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 11:43:40 EDT from IEEE Xplore. Restrictions apply.

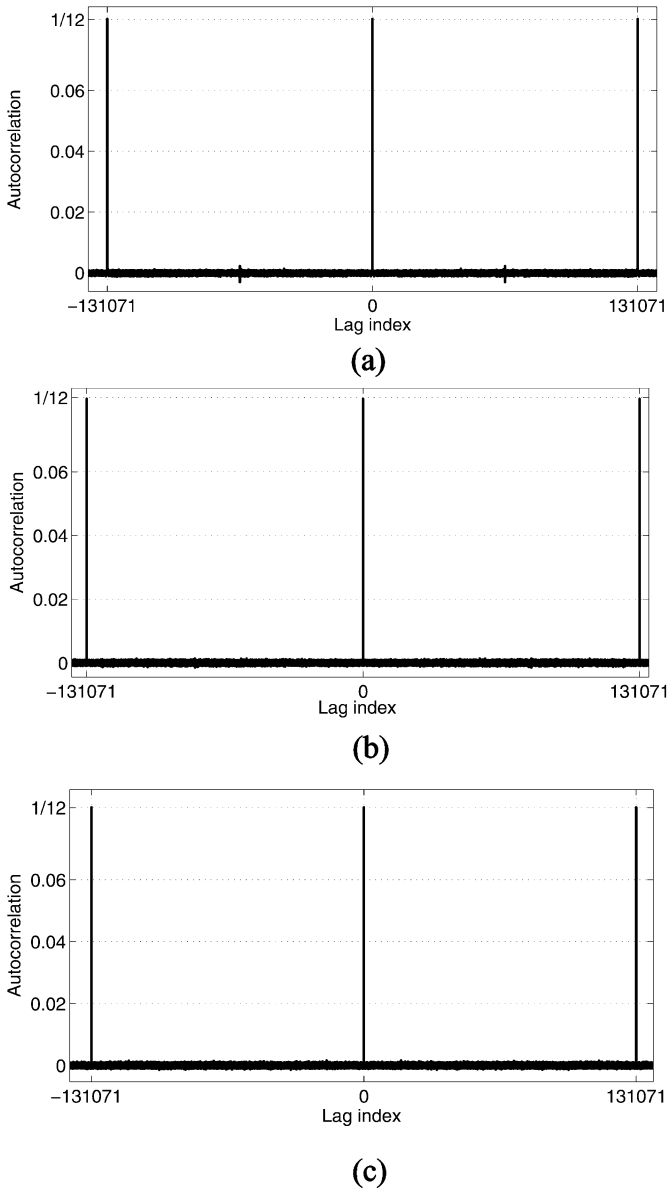

Fig. 6. Autocorrelation functions of quantizer errors for stages 2, 3 and 4 of MASH1–1–1–1.

$$\left(\sum_{k=0}^{N-1} A^k\right) B = \begin{pmatrix} C_1^N \\ C_1^N + C_2^N \\ \vdots \\ C_1^N + C_2^N + \cdots + C_l^{N+l-2} \end{pmatrix}_{l\times 1} = \begin{pmatrix} C_1^N \\ C_2^{N+1} \\ \vdots \\ C_l^{N+l-1} \end{pmatrix}_{l\times 1} \tag{16}$$

into (13) where $C_k^n = n!/k!(n-k)!$. In simplifying (16), we used Pascal's rule

$$C_k^n + C_{k+1}^n = C_{k+1}^{n+1}. \tag{17}$$

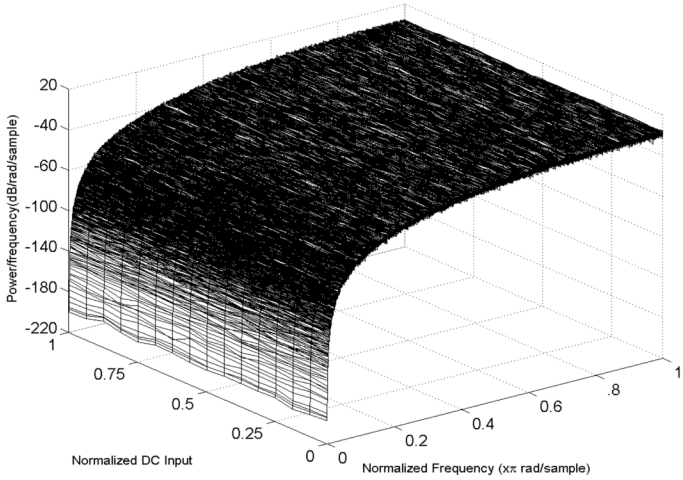

Fig. 7. Output quantization noise spectra of MASH1–1-1 for a range of dc inputs. The quantizer interval is $2^{17}-1$ and all initial conditions are set to zero.

Setting $n = 0$ in (13), we obtain

$$E[N] = \left\{ A^N E[0] + \left(\sum_{k=0}^{N-1} A^k\right) BX \right\} \bmod M. \tag{18}$$

If the system is periodic with period N, then we have that $E[N] = E[0]$; therefore, the following set of equations holds:

$$\begin{aligned} e_1[0] &= \left(e_1[0] + C_1^N X\right) \bmod M \\ e_2[0] &= \left(C_1^N e_1[0] + e_2[0] + C_2^{N+1} X\right) \bmod M \\ &\vdots \\ e_l[0] &= \left(C_{l-1}^{N+l-2} e_1[0] + C_{l-2}^{N+l-3} e_2[0] \right. \\ &\qquad \left. + \cdots + e_l[0] + C_l^{N+l-1} X\right) \bmod M \end{aligned} \tag{19}$$

where $e_i[0]$ is the initial condition of the ith stage. If this time-invariant system starts from state $(e_1[0], \ldots, e_l[0])$ and returns to this state after N steps, then it is periodic with period N. Therefore, in order for the above equations to be true, the following constraints must be satisfied:

$$\begin{aligned} &\left(C_1^N X\right) \bmod M = 0 \\ &\left(C_1^N e_1[0] + C_2^{N+1} X\right) \bmod M = 0 \\ &\vdots \\ &\left(C_{l-1}^{N+l-2} e_1[0] + C_{l-2}^{N+l-3} e_2[0] \right. \\ &\qquad \left. + \cdots + C_1^N e_{l-1}[0] + C_l^{N+l-1} X\right) \bmod M = 0. \end{aligned} \tag{20}$$

We pick the first and the lth equations and write them as

$$\begin{aligned} &(NX) \bmod M = 0 \\ &N\left\{ \frac{(N+1)\cdots(N+l-2)}{(l-1)!} \right. \\ &\qquad \times e_1[0] + \cdots + e_{l-1}[0] \\ &\qquad \left. + \frac{(N+1)\cdots(N+l-1)}{l!} X \right\} \bmod M = 0. \end{aligned} \tag{21}$$

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 11:43:40 EDT from IEEE Xplore. Restrictions apply.

If we choose the modulus of the quantizers M to be prime, then the minimum integer solution for N in the first equation is $N = M$, with $0 < X < M$. Now, consider the last term inside the braces in the second equation. We know that the product of l consecutive integers is divisible by $l!$. In other words, $l!$ divides $(N+1)(N+2)\cdots(N+l-1)(N+l)$. If N is a prime integer and $N > l$, $(N+l)$ is not divisible by l; therefore, $l!$ must divide $(N+1)(N+2)\ldots(N+l-1)$; hence, $(N+1)\ldots(N+l-1)/l!$ is an integer. With a prime N and $N > l$, all the other terms inside the braces of the second equation are integers for the same reason. Consequently, the solution of the lth stage is also $N = M$. In conclusion, if the quantizer modulus M is a prime number and if it is greater than the number of the stages l, then the sequence length is always M, independently of the initial conditions $e_i[0]$, the constant input X, and the order l of the MASH DDSM.

To illustrate the effect of this guaranteed minimum sequence length, we provide some examples. Fig. 4 shows the spectra of two MASH1–1-1 DDSMs, where $M = 512$ and $M = 509$, with the initial conditions of all stages set to zero, and with the input set to 256. The word lengths are 9 per stage Note that the modulator with prime modulus distributes the quantization noise over significantly more tones resulting from the longer sequence length compared to the case of just two tones when $M = 512$. In order to achieve smoother noise-shaped spectra, one can increase M. As an example, Fig. 5 shows the spectra of MASH1–1, MASH1–1-1 and MASH1–1-1–1 modulators of the type shown in Fig. 3 with decimal input 1 when $M = 2^{17}-1$. In this case, the wordlength is 17 bits per stage. As expected, the spectra are smooth and spike-free. The solid curves show the expected shaped noise spectra, assuming additive white quantization noise.

Fig. 6 shows autocorrelation functions of the quantization errors $(e_i[n])$ of the second, third, and fourth stages in the MASH1–1-1–1. The distances between the large spikes in the figure are equal to $2^{17}-1$ which exactly matches the lengths of the quantizer error sequences. In the case of the second stage, there is a small spike between each of the two large spikes, showing a small amount of correlation for half way lags. In the case of the third and fourth stages, for lags other than 0 and integer multiples of the period, the autocorrelation function is very small, providing a good approximation to white noise.

Fig. 7 shows interpolated output quantization noise spectra of a MASH1–1-1, where $M = 2^{17}-1$ for inputs 2^k, $1 \leq k \leq 16$, with zero initial conditions. Regardless of the input, the noise-shaped spectra are smooth and spike-free.

In order to implement a prime modulus quantizer, the technique in [18] can be adopted. Alternatively, [19] describes a technique to maximize sequence lengths by adding simple feedback to the first-order EFM to give an effective prime modulus while the modulus of the quantizer itself is a power of two.

IV. Conclusion

In this brief, we calculated mathematically the sequence length of a MASH structure [5] comprising first-order EFMs with prime modulus quantizers. Our calculations show that the sequence length of an lth-order member of this family with a constant input is equal to that of the first stage (M) for all initial conditions and for all constant inputs. In other words, adding stages to this prime modulus MASH DDSM [5] does not increase its sequence length.

Acknowledgment

The authors gratefully acknowledge discussions with Dr. C. Lyden (Analog Devices) and Prof. P. Fitzpatrick (University College Cork). They are also grateful to the reviewers of an earlier draft of this manuscript for providing a comprehensive list of related work and suggested improvements.

References

[1] B. Miller and R. J. Conley, "A multiple modulator fractional divider," *IEEE Trans. Instrum. Measur.*, vol. 40, no. 6, pp. 578–583, Jun. 1991.

[2] T. A. D. Riley and M. A. Copeland, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[3] I. Galton, "Delta-sigma fractional-N phase-locked loops," in *Phase-Locking in High-Performance Systems from Devices to Architectures*, B. Razavi, Ed. Piscataway, NJ: IEEE Press, 2003.

[4] B. D. Muer and M. Steyaert, *CMOS Fractional-N Synthesizers: Design for High Spectral Purity and Monolithic Integration*. Norwell, MA: Kluwer Academic, 2003.

[5] P. Level, S. Ramet, and L. Camino, "Digital to Digital Sigma–Delta Modulator and Digital Frequency Synthesizer Incorporating the Same," U.S. Patent # 6 822 593 B2, Nov. 23, 2004.

[6] S. Hein and A. Zakhor, "On the stability of sigma delta modulators," *IEEE Trans. Signal Process.*, vol. 41, no. 7, pp. 2322–2348, Jul. 1993.

[7] D. Hyun and G. Fischer, "Limit cycles and pattern noise in single-stage single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 5, pp. 646–656, May 2002.

[8] D. Reefman, J. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 6, pp. 1211–1223, Jun. 2005.

[9] D. Reefman, J. Reiss, E. Janssen, and M. Sandler, "Description of limit cycles in feedback sigma-delta modulators," in *Proc. AES 117th Convention, 2004*, San Francisco, CA, Oct. 28–31, 2004.

[10] V. Friedman, "The structure of the limit cycles in sigma delta modulation," *IEEE Trans. Commun.*, vol. COM-36, no. 8, pp. 972–979, Aug. 1988.

[11] R. M. Gray, "Spectral analysis of quantization noise in a single-loop sigma-delta modulator with dc input," *IEEE Trans. Commun.*, vol. 37, no. 6, pp. 588–599, Jun. 1989.

[12] P. W. M. Wong and R. M. Gray, "Two-stage sigma-delta modulation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 38, no. 11, pp. 1937–1952, Nov. 1990.

[13] W. Chua, P. W. M. Wong, and R. M. Gray, "Multi-stage sigma-delta modulation," *IEEE Trans. Inf. Theory*, vol. 35, no. 7, pp. 784–796, Jul. 1989.

[14] M. Kozak and I. Kale, *Oversampled Delta-Sigma Modulators, Analysis, Applications and Novel Topologies*. Norwell, MA: Kluwer Academic, 2003.

[15] M. J. Borkowski, T. A. D. Riley, J. Hakkinen, and J. Kostamovaara, "A practical delta–sigma modulator design method based on periodical behavior analysis," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 10, pp. 626–630, Oct. 2005.

[16] K. Hosseini and M. P. Kennedy, "Mathematical analysis of digital MASH delta-sigma modulators for fractional-N frequency synthesizers," in *Proc. PRIME'06*, Otranto, Italy, Jun. 2006, pp. 309–312.

[17] S. Pamarti and I. Galton, "LSB dithering in MASH delta-sigma D/A converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 779–790, Apr. 2007.

[18] M. F. Keaveney and W. P. Hunt, "Variable Modulus Interpolator, and a Variable Frequency Synthesizer Incorporating the Variable Modulus Interpolator," U.S. Patent # 6 927 716, Aug. 9, 2005.

[19] K. Hosseini and M. P. Kennedy, "Maximum sequence length MASH digital delta–sigma modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

Authorized licensed use limited to: UNIVERSITY COLLEGE CORK. Downloaded on March 26,2010 at 11:43:40 EDT from IEEE Xplore. Restrictions apply.