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On the calculation of effective electric field in $In_{0.53}Ga_{0.47}As$ surface channel metal-oxide-semiconductor field-effect-transistors

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The effective electron mobility of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors with HfO_2 gate oxide was measured over a wide range of channel doping concentration. The back bias dependence of effective electron mobility was used to correctly calculate the vertical effective electric field. The effective electron mobility at moderate to high vertical effective electric field shows universal behavior independent of substrate impurity concentration. © *2011 American Institute of Physics*. [doi:10.1063/1.3588255]

Because of their exceptional electron mobility and reasonable bandgaps,[1] $In_xGa_{1-x}As$ alloys are considered to be promising materials for future generation n-channel metal-oxide-semiconductor field-effect-transistor (MOSFETs) for low power logic applications. Recent reports on very short channel devices on $In_xGa_{1-x}As$ substrates demonstrate excellent electronic transport characteristics.[2–5] However, for device modeling and performance analysis, a quantitative knowledge of the inversion layer effective mobility (μ_{eff}) and its dependence on various device operating conditions are required. The vertical effective electric field (E_{eff}) is a critical parameter for the appropriate calculation and comparison of the inversion layer electron mobility of surface channel MOSFETs.

The inversion layer electron mobility can be separated into three dominant scattering regimes as a function E_{eff}.[6] At low E_{eff} the mobility is limited by scattering by doping atoms and charges at the semiconductor/oxide interface (Coulomb scattering).[7] At relatively higher E_{eff}, phonon scattering dominates over Coulomb scattering. At even higher E_{eff}, surface roughness scattering limits the total mobility.[7] Though a significant amount of work has been previously performed on modeling electron and hole mobility along with the determination of E_{eff} for Si surface channel MOSFETs,[8–12] little work has been done for III-V MOSFETs. In this work we present the correct calculation of the E_{eff} experienced by the inversion layer electrons in $In_{0.53}Ga_{0.47}As$ MOSFETs. The effective electron mobility (μ_{eff}) of surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs with HfO_2 gate dielectric was measured over a wide range of channel doping concentration (N_a). The mobility data at moderate to high electric field plotted against the E_{eff} fall on a single line for all doping concentrations confirming that the model is correct.

A fully isolated, nonself aligned, gate last process has been used to fabricate the $In_{0.53}Ga_{0.47}As$ devices. A 2 μm p-doped $In_{0.53}Ga_{0.47}As$ channel layer was grown by metalorganic vapor phase epitaxy on InP p+ substrate with standard precursors (trimethyl-aluminum/gallium/indium in purified N_2 carrier gas and purified AsH_3) in a commercial horizontal system managed and constantly monitored to guarantee low unintentional impurity levels.[13] Several epitaxial layer doping concentrations (Zn doped, $\sim 1\times10^{16}$ cm^{-3} $\leq N_a \leq 1\times10^{18}$ cm^{-3}) have been used for the device fabrication. The effective doping concentration was confirmed using the minimum-maximum MOS capacitance-voltage technique.[14] After performing a standard degrease with acetone, methanol and isopropanol solution (1 min each), a 300 nm plasma enhanced chemical vapor deposited (PECVD) SiO_2 was deposited as an isolation oxide. Source and drain (S/D) regions were selectively implanted with 1×10^{14} cm^{-2} Si dose at energy of 40 keV followed by 600 °C, 60 s activation anneal in N_2. After a patterned buffered-oxide-etch of the field oxide from the channel region and a deionized water rinse, the surface was cleaned with a room temperature soaking in 10% $(NH_4)_2S$ solution for 10 min. Approximately 10 nm of atomic layer deposited (ALD) HfO_2 gate oxide was deposited using tetrakis-dimethylamido-hafnium and H_2O precursors at 250 °C followed by a postdeposition anneal (500 °C, 60 s in N_2). Pd gate metal was deposited using e-beam evaporation and patterned using a lift off process. The S/D contacts were formed using e-beam evaporation of a Ni/Ge/Au metal stack. A 350 °C rapid thermal anneal (RTA) for 30 s in N_2 was used as the final postmetal anneal.

Figure 1(a) shows the comparison of source current-gate voltage (I_s-V_G) characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs as a function of N_a. A strong dependence of the drive current on N_a is observed. The decrease in drive current with increasing N_a is generally attributed to the increased impurity scattering yielding reduced carrier mobility. The defect density at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface was measured using the subthreshold slope corrected for peripheral leakage (SS), charge pumping, and pulsed current-voltage hysteresis.[15] The results indicate that the defect density is independent of substrate doping ($SS \sim 150$ mV/decade, $D_{it} \sim 1\times10^{13}$ cm^{-2} eV^{-1}, oxide bulk trap density of $\sim 3\times10^{12}$ cm^{-2}). The device threshold voltage (V_t) was experimentally determined by linearly extrapolating the I_s-V_G curves at the peak transconductance. Figure 1(b) shows both the experimental (star symbol)

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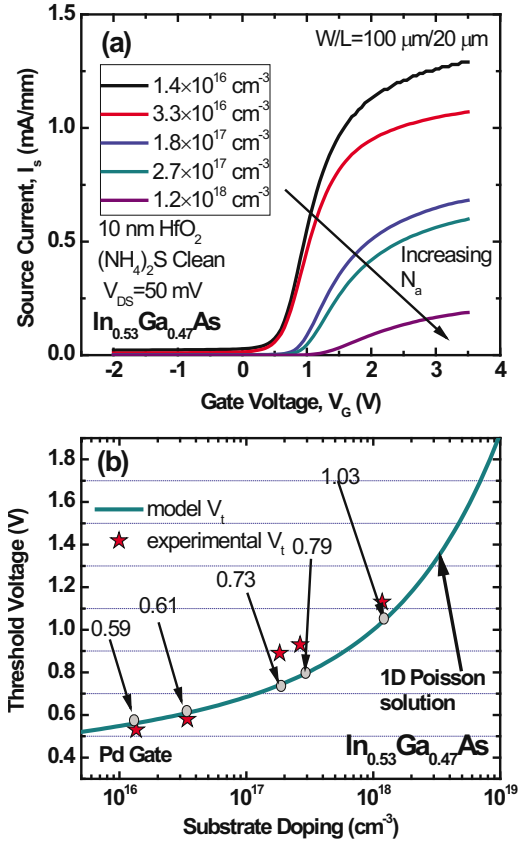

FIG. 1. (Color online) (a) I_s-V_G characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs as a function of substrate doping. Results show that the drive current decreases with the increase in substrate doping. (b) Modeled and experimental threshold voltage as a function of channel doping.

and modeled (circle and line) V_t as a function of N_a. The modeled V_t was calculated using,

$$V_t = \phi_{ms} + 2\phi_b + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_b)}}{C_{ox}}, \tag{1}$$

where φ_{ms} is the metal-semiconductor workfunction difference, φ_b is the semiconductor bulk potential calculated self-consistently using Poisson's equation,[16] ε_s is the semiconductor dielectric constant, and C_{ox} is the oxide capacitance. The modeled V_t were calculated assuming zero oxide and interface state charge and show good agreement with the experimental values. Given the high D_{it}, the theoretical V_t fits the experimental data surprisingly well. The results indicate the fixed charge density is small and the interface traps are donorlike (neutral near threshold) as suggested elsewhere.[17]

According to Gauss' law, the electric field experienced by an electron at any point x, $(0<x<x_i)$ within the inversion layer can be expressed as,

$$E(x) = \frac{N_{dpl}}{\varepsilon_s} + \frac{q}{\varepsilon_s}\int_x^{x_i} n_{inv}(z)dz, \tag{2}$$

where $n_{inv}(z)$ is the inversion carrier density along an axis normal to the semiconductor surface, and N_{dpl} is the calculated depletion charge density.[8–10] It is well known that the inversion electron distribution has a Gaussian-like profile with a peak below the semiconductor surface due to quantization effects. Therefore, an average electric field which governs the transport of the total inversion carrier density (N_{inv}) can be described by:

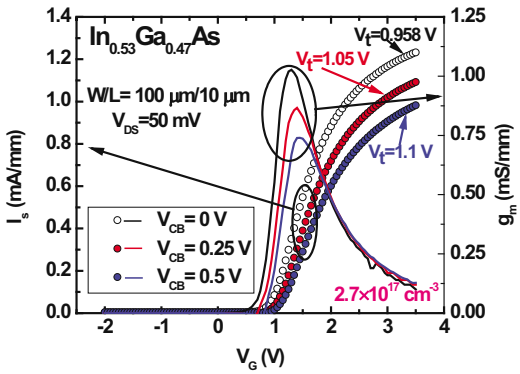

FIG. 2. (Color online) I_s-V_G characteristics for drain-source voltage (V_{DS}) of 50 mV as a function of V_{CB}. The threshold voltage shifts to the positive voltage direction with increasing V_{CB}.

$$E(x) = \frac{1}{\varepsilon_s}(N_{dpl} + \eta N_{inv}), \tag{3}$$

where η is a fitting parameter which should depend only on the band structure of the semiconductor (i.e., the details of the electron distribution in space and energy). The value of η does not depend on N_a, back bias voltage (V_{CB}), or details of the gate dielectric processing but only on the band structure of the semiconductor. However, changing the bandstructure of the material through strain, use of buried channels or use of semiconductor-on-insulator structures can result in a different value for η.[18]

Following the methodology described in Ref. 8, back bias voltages were applied during the I_s-V_G measurements to modulate the relative magnitude of N_{dpl} and N_{inv}. The effective mobility limited by phonons and surface roughness (mobility at moderate to high electric field) depends only on the E_{eff} and not on the relative magnitude of N_{dpl} or N_{inv}. Therefore, modifying V_{CB} allows for the independent determination of η. An increase in $|V_{CB}|$ will increase the depletion region width under the inverted region. For a constant gate to channel voltage, the total gate charge will remain unchanged. As the gate charge remains same, and more ionized acceptor atoms are available in the depletion region to contribute to the balancing action, fewer electrons are needed in the inversion layer. Figure 2 shows the I_s and transconductance (g_m) versus V_G characteristics of an $In_{0.53}Ga_{0.47}As$ device as a function of V_{CB}. With the increase in the $|V_{CB}|$, N_{inv} decreases resulting in less screening of Coulombic scattering centers and a concomitant decrease in drive current and peak g_m. Figure 3 shows the extracted mobility versus the electric field for the devices shown in Fig. 2. The μ_{eff} versus E_{eff} was calculated from I_s-V_G, with N_{inv} and N_{dpl} extracted from fitting of gate-channel capacitance measurements corrected for the interface trap response as described in detail in Ref. 19. The E_{eff} was calculated using Eq. (3) for three different values of $\eta(=1.0, 0.5, 0.25)$. Figure 3(c) shows that the μ_{eff} curves converge at moderate to high field when plotted as a function of E_{eff} calculated with $\eta=0.25$. The same mobility data when plotted as a function of the $E_{surface}$ ($\eta=1$) and E_{eff} ($\eta=0.5$) yields three separate curves in Figs. 3(a) and 3(b), respectively. As the mobility at moderate to high field should

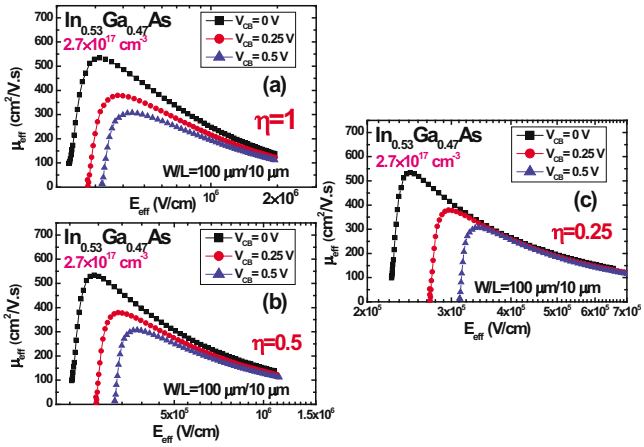

FIG. 3. (Color online) The mobility curves for a given device at different back bias voltages plotted as a function of E_{eff} (η=0.25) become identical whereas the same mobility data yield separate curves for η=0.5 and 1.

depend only on E_{eff} and not the relative magnitude of N_{dpl} and N_{inv}, $\eta=0.25\pm.05$ is the correct value for these $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs.

Figure 4 shows the E_{eff} (calculated with η=0.25) dependences of μ_{eff} at 300 and 77 K for the various substrate doping concentrations. These results show that μ_{eff} plotted against the E_{eff} (calculated with η=0.25) is independent of N_a. The use of other values for η does not result in a convergence of mobility for different N_a. At moderate to high field, the free inversion electrons screen the dopants and the total mobility should be limited only by phonons and surface roughness. As the oxide charge density is similar as a function of doping and assuming similar surface roughness, the total mobility at the same E_{eff} should be independent of substrate doping. The results confirm the E_{eff} model determined using the back bias measurements. The inversion layer charge centroid depends inversely on the effective mass of the semiconductor. For a given inversion carrier density, a deeper charge centroid will result in a lower E_{eff} for the average inversion carrier. Therefore, a lower value of η for

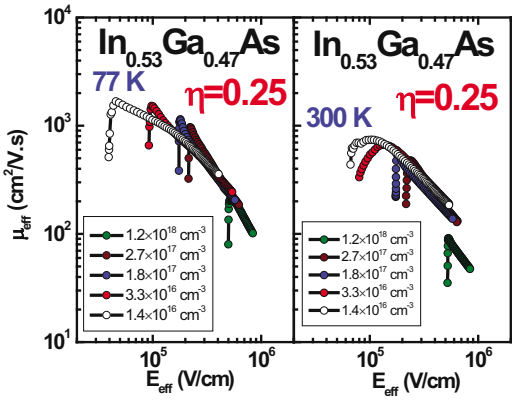

FIG. 4. (Color online) Inversion layer electron mobility at 300 and 77 K vs E_{eff} for different substrate doping densities. Here, E_{eff} is defined by, $E_{eff}=q(N_{dpl}+\eta\times N_{inv})/\varepsilon_s$ with η=0.25.

$In_{0.53}Ga_{0.47}As$ compared to the silicon value of η=0.5 is consistent with the lower effective mass of $In_{0.53}Ga_{0.47}As$.

In summary, the dependence of mobility on substrate doping and the dependence of mobility on back bias have both shown that $\eta=0.25\pm0.05$ results in μ_{eff} versus E_{eff} independent of substrate doping and back bias at moderate to high E_{eff}. This value of η is consistent with the inversion layer charge centroid expected for $In_{0.53}Ga_{0.47}As$.

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