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Ultra-low loss integrated magnetics platform for high frequency power delivery networks

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Abstract

The future smart systems are envisaged to continue shrinking in size and weight, while integrating more features and functionalities, leading to significant increase in power density and efficiency requirements. In addition, devices such as mobile phones and tablet computers require a large reduction in electronic component height. While SMT chip power inductors may have thicknesses as low as 0.6mm; thin film power inductors offer an incremental height of ~50µm. This paper introduces an ultra-low loss integrated magnetics platform for the next generation power systems on-chip (PwrSoC) and in-package (PwrSiP) applications. The integrated magnetics-on-silicon inductors and transformers have been designed, fabricated using conventional CMOS fabrication processes, and characterized, demonstrating industry-leading performance metrics.

1 Introduction

The rapid proliferation of portable electronics, smart devices and systems over the past decade has sparked significant interest in industry and academia towards the miniaturization and integration of power delivery subsystems, while maintaining efficiency, achieving a low profile and meeting the dynamic power requirements of today's application system-on-chip (SoC) ICs. In order to reduce the volume and weight of power delivery networks, the size of passive magnetic devices needs to be reduced, while the power density needs to be increased. This is enabled by increasing the switching frequency of point-of-load (POL) DC-DC converters and integrated voltage regulators (iVR for SoC). While high switching frequency allows for smaller inductors and transformers, it also leads to increased core and conduction losses, adversely affecting the conversion efficiency. Therefore, low-profile, small footprint integrated magnetics-on-silicon (MoS) inductors and transformers capable of operating at high frequency with very low loss are essential for highly integrated iVR and POL applications [1], [2]. This paper presents the development of a range of high frequency (20–100 MHz), high-Q (16–25) thin-film magnetic inductors and transformers for iVR and POL converter applications.

The thin-film MoS devices developed in this work employ a solenoid structure using a single magnetic core layer encapsulated within copper trace windings. Solenoid inductors offer the benefits of scalability and compatibility with the back end of line (BEOL) process options in semiconductor foundries. This opens up the possibility of monolithic integration of ultra-low loss passive magnetics in CMOS power converter ICs, enabling a substantial gain in power density, performance and efficiency.

2 Device design specifications

A number of test device designs (single and coupled inductors, transformers) have been developed in order to investigate the suitability of the ultra-low loss integrated magnetics platform. The device electrical parameters are targeted for integrated power delivery and conversion systems such as SOC iVR and POL DC-DC converters where compact form-factor, low-loss and high efficiency operation are key requirements. The Table 1 lists the target electrical parameters of the test device designs.

Table 1 Design specifications for single and coupled inductors and transformers

Device type	Device ID	Parameters			
		L [nH]	k12	Footprint [mm^2]	f_{SW} [MHz]
Single inductor	SL1	10.4	-	0.5	40
	SL3	105.7	-	2.1	40
	SL4	243.4	-	4.1	40
Coupled inductor	CL2	53.6	0.7	2.6	40
	CL3	104.6	0.8	4.4	40
Transformer	TX1	103.5	0.9	5.1	30
	TX2	40.2	0.9	2.3	30

A schematic cross-section of the solenoid thin-film magnetic devices are illustrated in Figure 1. The devices are fabricated on silicon substrate, and a planar laminated magnetic core is encapsulated within top and bottom copper traces connected through vias. Dielectric layers are used to electrically isolate the copper traces from the core and the substrate.

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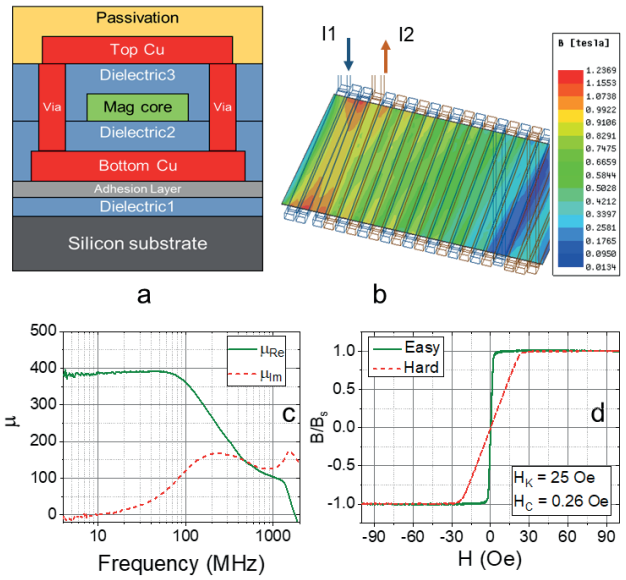

Figure 1 a) Graphical illustration of the cross-section of the thin-film magnetics on silicon (tf-MoS) integrated inductor. b) FEM model of coupled inductor showing magnetic flux density in the core. c) Complex relative permeability spectrum, and d) B-H loop of the laminated magnetic film.

An Analytical model-based design optimization (based on expressions for inductance and resistance given in [3]) and finite-element electromagnetic simulation is used as part of the design workflow.

The design optimization tool incorporates the magnetic properties of the core material stack (Figure 1) and the design rule constraints in order to identify the physical design parameters that satisfy the target design specifications. The anisotropic cobalt-alloy based laminated multilayer core exhibits stable relative permeability up to 100 MHz frequency. Following the analytical design optimization, the optimized design parameters are used to develop three-dimensional electromagnetic finite element models for accurate estimation of device electrical parameters.

3 Device fabrication

The inductors and transformers developed in this work incorporate a solenoidal construction, with the thin-film magnetic core encapsulated within several turns of copper trace windings. The devices are fabricated in a CMOS compatible back-end-of-line (BEOL) process involving photolithography and electrodeposition of the copper traces and vias. The soft magnetic cores of the solenoid devices are fabricated by multiple layers of sputter deposited cobalt-based amorphous alloy and dielectric material layers. The multi-layer laminated core structure significantly reduces the eddy current losses in the core resulting in an improved high-frequency performance. The copper conductors and the magnetic core are electrically isolated by a photo-definable polymer resin with low dielectric constant, which also serves as the passivation material.

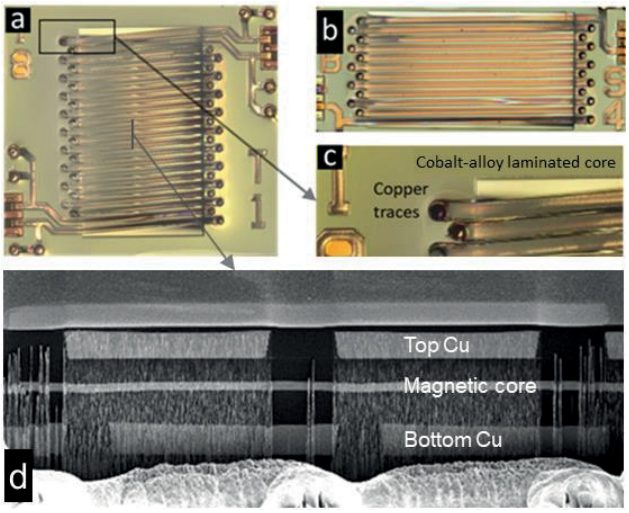

Figure 2 Fabricated devices a) Transformer, b) Single inductor, c) Enlarged view of cobalt-alloy based laminated core enclosed by copper traces in solenoid construction. d) SEM of the fabricated micro-inductors cross-section.

4 Device characterization

Wafer-level small-signal electrical test are carried out using a 4-port vector network analyser and standard RF probes in the 1MHz – 1GHz frequency range. The electrical parameters (AC inductance, resistance, quality factor, coupling coefficient) of the devices are extracted from the measured 4-port S-parameter data. The inductance of the single inductors remains stable over a broad range of frequency (1 – 100 MHz), with the peak quality factor 24.7 occurring at 106 MHz for the SL1 (10 nH) inductor (Figure 3).

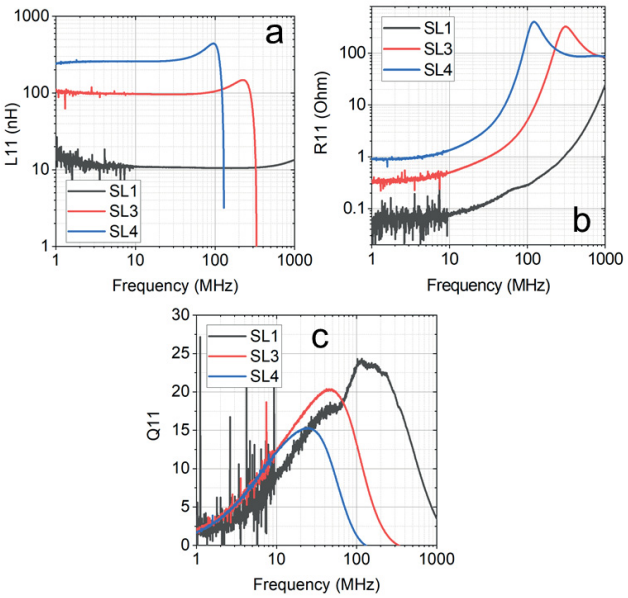

Figure 3 Small signal frequency responses for a) inductance, b) resistance, and c) quality factor of single inductors SL1, SL3 and SL4.

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The AC inductance and coupling coefficient of the coupled inductors and transformers remain stable over a broad frequency range from 1 MHz to 80 MHz. All of these devices exhibit peak quality factors in the range of 16 – 18, at frequencies from 30 MHz – 80 MHz (Figure 4, Figure 5).

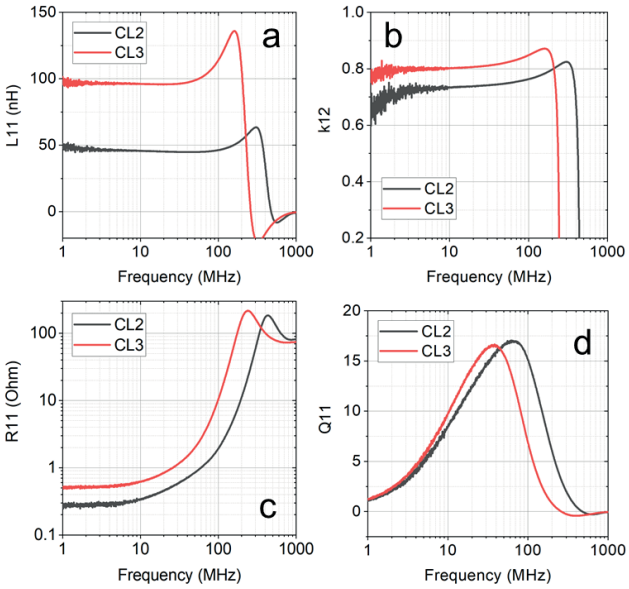

Figure 4 Small signal frequency response for a) Inductance, b) coupling coefficient, c) resistance, and d) quality factor of coupled inductors CL2, CL3.

These performance metrics confirm that the on-silicon inductors and transformer devices are suitable for a variety of power system on-chip (PwrSoC) applications.

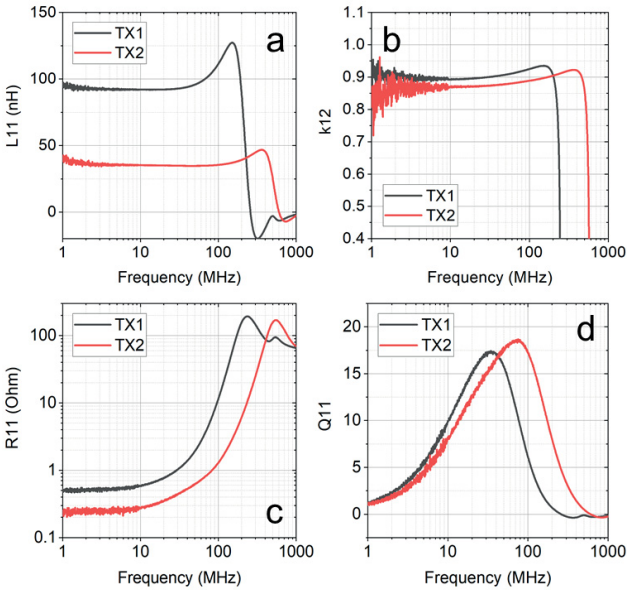

Figure 5 Small signal frequency response for a) inductance, b) coupling coefficient, c) resistance, and d) quality factor of transformers TX1 and TX2.

The current-handling capability of single and coupled inductors are limited by the saturation of the inductor core with applied current. Figure 6 shows the dependence of the inductance of SL1, SL3, SL4 on the DC bias current super-imposed on the AC small signal current. The saturation DC-bias current (10% degradation in inductance) is 450 mA for SL1 and SL3, and 400 mA for SL4 (Fig 6).

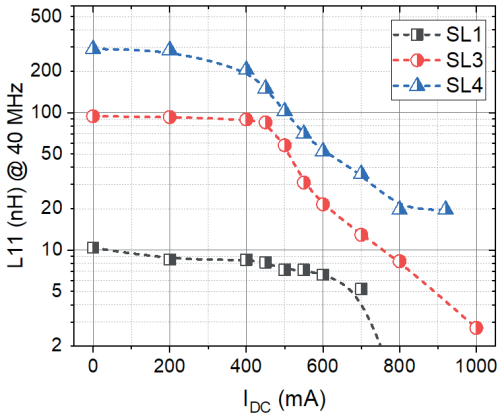

Figure 6 Inductance vs. DC current for the single inductors SL1, SL3, and SL4.

The coupled inductors offer higher current-handling capability in comparison to the single inductors. This is achieved by driving the DC components of the currents through the coupled inductor windings in opposite phases, such that the magnetic flux in the core is reduced substantially.

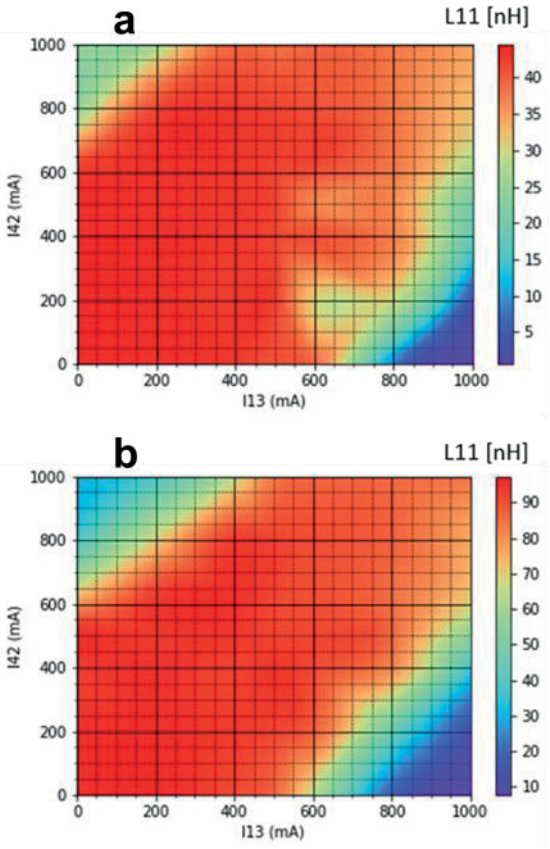

Figure 7 Inductance at 40 MHz vs DC current for the coupled inductors a) CL2, and b) CL3.

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The contour plots in Figure 7 show the inductance of the coupled inductors CL2 (k12 = 0.7) and CL3 (k12 = 0.8) with applied DC-bias currents. The current-handling capability of the coupled inductors is enhanced to higher than 1A by balancing the field induced by the DC currents (Fig 7).

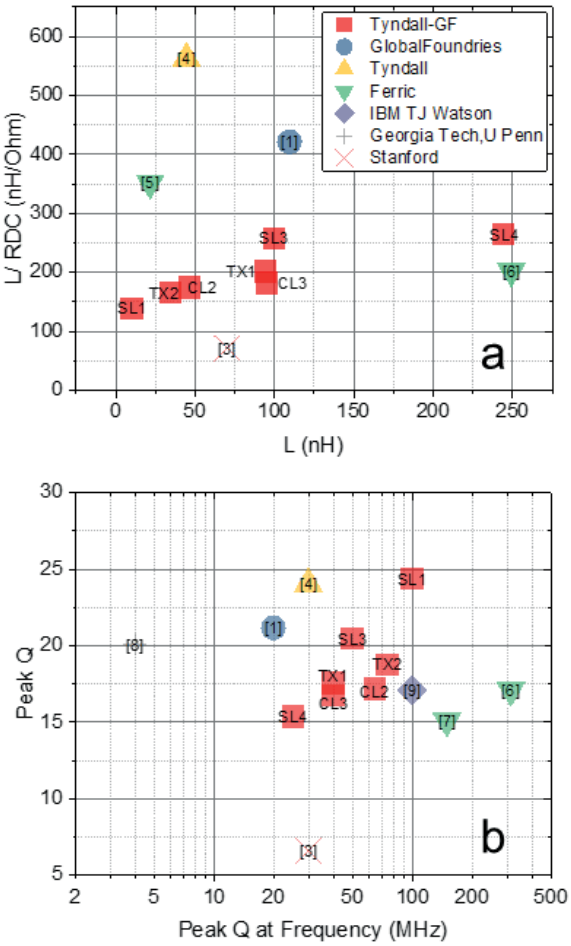

Figure 8 a) L/R_{DC} vs. inductance, and b) peak quality factor vs. frequency plots for magnetics-on-silicon solenoid inductors. The red squares represent the performance metrics of the devices developed in the present work.

A comparative study of the device performance metrics is presented in Figure 8. The graphs plot the L/R_{DC} vs. L and peak quality factor vs. frequency of peak quality factor for other magnetics-on-silicon solenoid inductors. The devices developed in the present work exhibits high L/R_{DC} ratio of 150 – 260 nH/ohm across a wide range of inductance values (10 – 250 nH). In addition, the devices demonstrate high quality factors (15 - 25) at frequencies ranging from 30 – 100 MHz. These metrics highlight the capability of ultra-low loss operation at high switching frequencies for the thin-film magnetics on silicon devices.

5 Conclusion

The low profile, ultra-low loss, high Q-factor magnetics-on-silicon devices allow on-chip integration of iVR (SoC) and POL PMIC converter inductors, while still maintaining very high overall converter efficiencies. The step function benefits in switching frequency, in inductor areal density and in L/R_{DC} metrics additionally enables large dynamic performance improvement or battery life extension.

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