Optical Pitch Transformer Chiplet: Enhancing Packaging Beachfront Density

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Abstract—We propose the use of optical pitch transformer chiplets for beachfront density enhancement, eliminating the need for optical interconnects on devices to match that of fibre array units. Such chiplets can be fabricated separately and micro transfer-printed onto glass interposers. This work focuses on evanescent coupling between SiN tapers and ion-exchanged waveguides, and we observed that optical coupling behaves differently depending on functionality of SiN taper as an emitter or a receiver.

1. INTRODUCTION

The growth of silicon photonic integrated circuit (Si-PIC) industries has been tremendous over the last decade, with almost all major foundries (both commercial and research centres) having their dedicated process and design kits (PDKs) released and made available to customers, driven by an ever-increasing list of functionalities and applications. However, packaging and integration of Si-PIC systems remain an under-studied field, with majority of the activities focusing only on achieving the best fibre-to-PIC coupling efficiency [1], either through design improvements or machine enhancements [2]. We opine that attention should also be paid to the next stage of photonic systems integration [3, 4] that involves a) higher density of components with different functionalities within a package and b) the possibility of wafer/panel level integration of such systems.

An area of interest is beachfront density of PIC, due to its potential to reduce the overall size of PIC component [5] or packing more functionalities. This would allow the realization of heterogeneous integration in which various components fabricated from different foundry nodes can be put together to form a photonic systems-in-package. However, to increase beachfront density of PIC, fibre array unit (FAU) must shrink in sizes too. Although there have been development works that goes down to 82 µm v-groove pitch, 127 µm pitch remains the standard that most user would adopt with confidence and at lower cost. Alternative approaches include transforming FAU into 2D structures such as [6] for surface coupling.

2. CONCEPT AND APPROACH

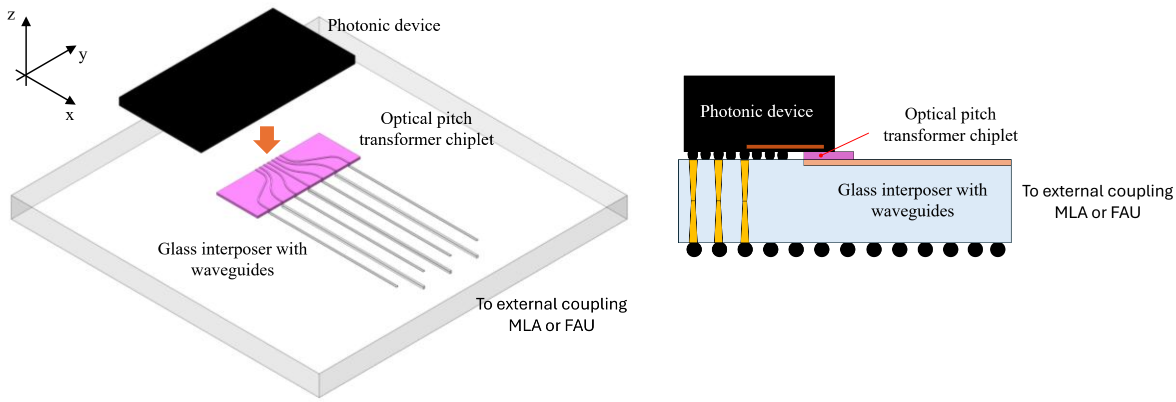

Fig. 1. Illustration of the optical pitch transformer concept – 3D and cross-sectional views.

Fig. 1 shows the concept of the optical pitch transformer chiplets (patent pending), which can be fabricated separately on a source wafer. These chiplets are then released from the bulk substrate or carrier and micro-transfer-printed onto a glass or silicon interposer. One end of the chiplet can have waveguide pitches matching that of PIC, while the other end matching that of the FAU and microlens array (MLA) for in-plane or out-of-plane coupling [7]. The thickness of the chiplet can be varied with multiple layers of waveguides incorporated, eliminating the need for additional cavity formation on interposer for electrical interconnects. Having multiple layers of photonic waveguides on the chiplet could potentially allow for 2D edge coupling from the PIC and the glass interposer. Moreover, passive optical components can be implemented on the chiplet as needed. The interposer on the other hand would have straight passive optical waveguides, such as polymer waveguides [8] or ion-exchanged waveguides [9] incorporated onto it. The interposer would also have typical electrical interconnects such as bond pads with under bump metallization (UBM) on top and bottom surfaces, redistribution lines and layers (RDL) and through vias (TGV or TSV). Low temperature transient liquid phase bonding (TLP) such as [10] can also be used as electrical interconnects between PIC and interposer.

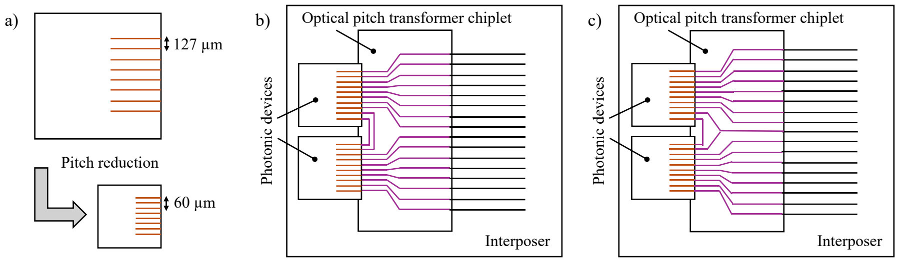

Fig. 2a). Illustration of pitch reduction on photonic device from 127 µm to 30 µm, effectively reducing the size of the component. 2b). Illustration of multi-devices on pitch transformer chiplet allowing optical connections between two devices. 2c). Illustration of signal mixing/splitting on pitch transformer chiplet between two devices.

Fig. 2a) illustrates the concept of pitch reduction on devices, for example, by scaling down the waveguide pitch from standard 127 µm to 30 µm while keeping crosstalks in check. Fig. 2b). further illustrates the example of multiple PIC assembly onto the optical chiplet with loops connecting the PICs, potentially allowing for optical interconnect standardization, similar to UCIe approach in the electronics industries [11]. Fig. 2c) on the other hand illustrates the concept of optical signal mixing or splitting between PICs. Multiple electronics components can also be integrated onto the glass interposer to form a photonic systems-in-package. Moreover, the optical chiplet can be used on standard electrical interposer without additional optical waveguides, by placing it at the edges for direct FAU or MLA coupling.

3. SIMULATION AND ANALYSIS

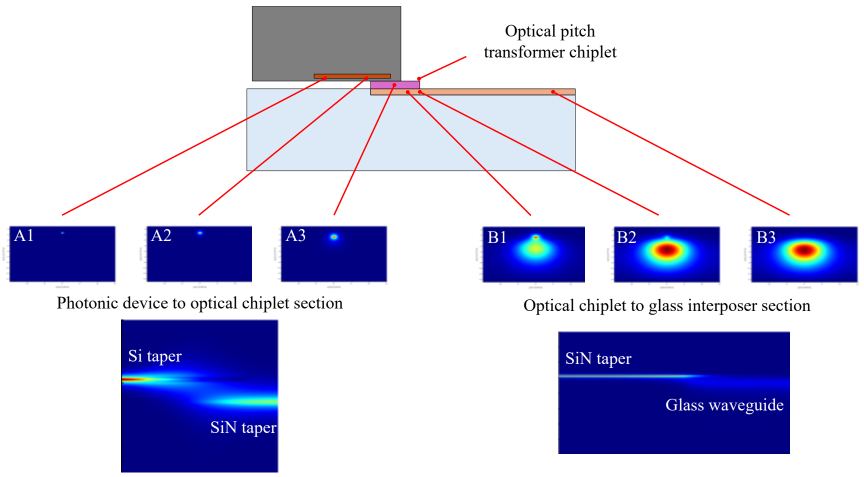

Fig. 3. Mode transition from photonic device, through optical chiplet, and to glass interposer. A1-A3 shows transition from Si taper to SiN taper. B1-B3 shows mode transition from SiN taper to ion-exchanged waveguide.

The current configuration assumes a) silicon waveguide and taper on the PIC, b) single layer silicon nitride waveguide and taper on the optical chiplet, and c) ion-exchanged waveguide embedded in the glass interposer. There is a layer of adhesive between the PIC and optical chiplet and between optical chiplet and glass interposer, which can be spin-coated and patterned. The optical transmission from the PIC to interposer would occur evanescently through the chiplet as shown in Fig. 3.

To better understand the coupling behaviors at 1550 nm wavelength, we first ran EME for basic taper parameters sweeping and then FDTD simulations due to its ability to differentiate directionality [12]. Coupling studies between Si and silicon nitride (SiN) are widely available in the literatures; thus, we look only at the evanescent coupling effect between SiN and ion-exchanged waveguides in this work. We study the behavior of 1mm long SiN taper as an emitter (coupling into ion-exchanged waveguide) and receiver (coupling from ion-exchange waveguide) incorporating lateral misalignment, adhesive layer thickness and adhesive refractive index differences. We fixed the SiN layer thickness to 0.2 µm and its taper length to 1 mm to limit the computational requirements of FDTD. We assume standard material parameters of both Si and SiN at 1550nm wavelength, while for ion-exchanged waveguide, we estimated those from [13, 14].

A. EFFECT OF SiN TAPER WIDTH AND OXIDE TO ADHESIVE THICKNESS RATIO

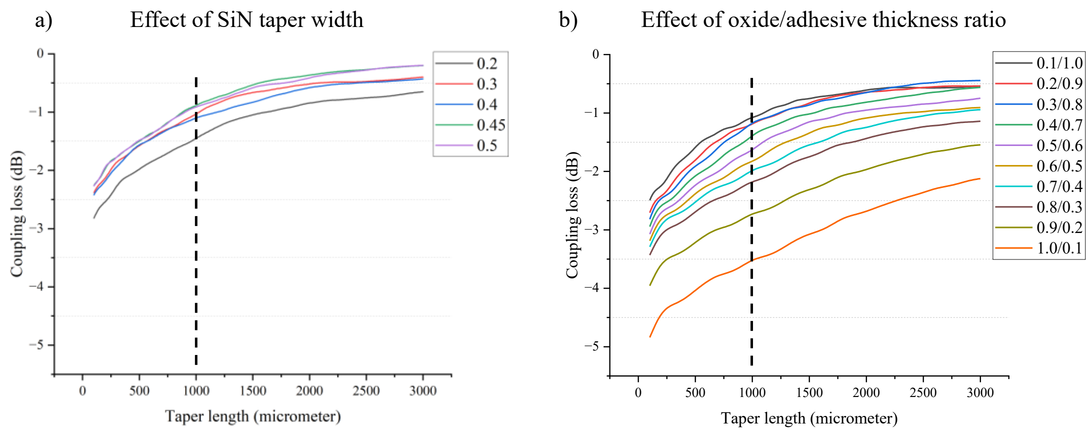

Fig. 4a). Effect of SiN taper width, ranging from 0.2 to 0.5 µm, showing that 0.45 µm has more balanced coupling efficiency across various length. 4b). Effect of oxide to adhesive thickness ratio underneath SiN layer, showing that the thicker the oxide layer, the higher the coupling loss between SiN taper and ion-exchange waveguide.

We first studied the taper width design using EME, assuming no oxide underneath SiN layer and constant 1 µm adhesive thickness (RI of 1.475). Simulation shows that a taper width of 0.45 µm provides the best coupling efficiency (Fig. 4a). From processing point of view, we opined that a layer of oxide underneath SiN layer is needed, thus we set a minimum thickness of 0.1 µm. Next, we studied the effect of oxide to adhesive thickness ratio while keeping the total gap constant at 1.1 µm (Fig. 4b). With 0.1 µm oxide and 1 µm adhesive thickness, a coupling loss of -1.08 dB can be reached. With 0.5 µm oxide and 0.6 µm adhesive, the loss increases to 1.63 dB, and finally 3.52 dB with 1 µm oxide and 0.1 µm adhesive.

B. BEHAVIOR OF SiN TAPER AS TRANSMITTER AND RECEIVER

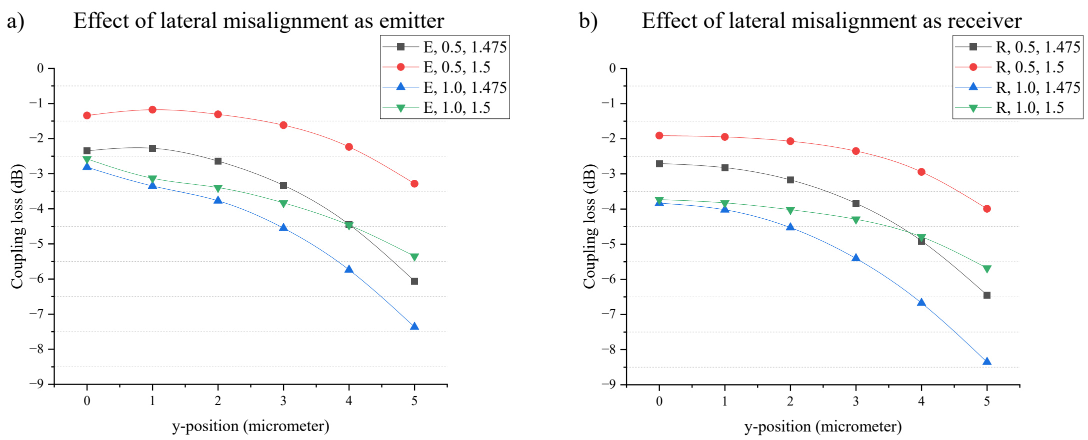

Fig. 5a). Effect of lateral misalignment as an emitter, showing that losses increase as the SiN taper moves away from the centre of the ion-exchange waveguide. 5b). As a receiver, the lateral position of SiN taper follows similar trends, but with higher losses.

We then moved on to FDTD simulation using the optimum taper design from EME and keeping 0.1 µm of oxide underneath the SiN layer to evaluate the taper's coupling performance, either as an emitter (coupling into the ion-exchanged waveguide) or as a receiver (coupling from the ion-exchanged waveguide) due to substantial differences between refractive index of the layers. We can see that SiN taper is sensitive to lateral misalignment regardless of functionality (Fig. 5). However, coupling from ion-exchanged waveguide into SiN taper (as a receiver, Fig. 5b) incurs higher losses compared to the former (Fig. 5a). For example, considering the case with 0.5 µm adhesive thickness and refractive index of 1.5. With perfect alignment (y-position = 0), coupling loss of a SiN emitter is 1.34 dB but is 1.91 dB as a receiver. Increasing the adhesive layer thickness from 0.5 µm to 1µm also increases the coupling loss by almost twice regardless of functionality. From the simulation results, SiN taper will likely have to be designed from a functionality perspective instead of a common design for both emitter and receiver, which had not been differentiated through EME. Similarly, the adhesive thickness should be kept as thin as possible.

C. EFFECT OF ADHESIVE THICKNESS

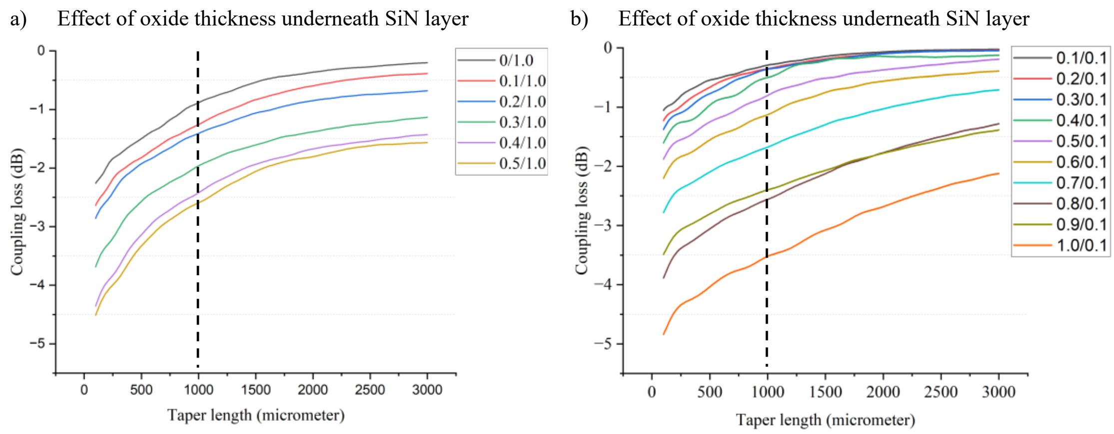

Fig. 6a). Effect of oxide thickness with 1µm adhesive layer, showing that losses increase as the oxide thickness increases due to total gap increases. 6b). Effect of oxide thickness with 0.1µm adhesive layer, follows similar trend, but less sensitive due to smaller total gap increases.

Lastly, we compared the effect of oxide thickness underneath the SiN layer under the scenario of 1 µm and 0.1 µm adhesive thickness (Fig. 6) using EME simulation. For both cases, total gap (oxide plus adhesive thickness) increases led to increased coupling loss. However, with thinner adhesive thickness, the effect is less profound. For example, with 1 µm adhesive thickness, 0.1 µm oxide thickness gave a coupling loss of 1.26 dB, but with 0.1 µm adhesive thickness, the oxide thickness can be increased to 0.6 µm, and the coupling loss is only 1.13 dB. Results also show that with thinner adhesive layer, the coupling loss can be as low as 0.29 dB for a SiN taper length of 1000 µm.

4. OPTICAL CHIPLET PROCESSING AND IMPLEMENTATION

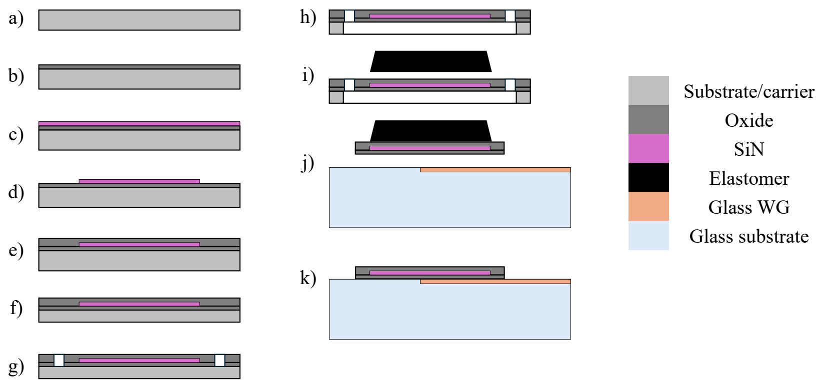

Fig. 7. Proposed optical pitch transformer chiplet processing and implementation.

We further explored the potential route of chiplet processing and implementation, taking advantage of etching selectivity between silicon and oxide layers (Fig. 7). The process begins with (a) a blank substrate or carrier, followed by (b) oxide deposition and (c) SiN deposition. (d) SiN taper is then patterned and (e) covered by a protective oxide layer. (f) Substrate is then thinned down, and (g) oxide tether is then patterned and etched through, stopping at the substrate layer. (h) Substrate underneath the chiplet is then patterned and etched through, stopping at the oxide layer and (i) ready to be transferred to the glass substrate. At this stage, the chiplet is floating on the carrier and held by oxide tethers. Some of the challenges that must be studied further include maximum size of the chiplet that can be processed using this route, tether design and size that can suspend the chiplet safely during substrate etching, residue cleaning and handling.

Prior to chiplet printing, thin layer of adhesive is spin-coated onto the glass substrate. During chiplet transfer, an elastomer post came into contact of the surface and breaks the tether during retraction (j). Once the chiplet has been printed onto the glass substrate, the elastomer post retracts, leaving only the chiplet firmly adhered onto the substrate (k). The substrate with printed chiplet is then cured, followed by a descum step to remove adhesive layer from exposed areas for subsequent assembly processes. The challenge here then would be to find an optical adhesive with suitable refractive index, can be spin-coated down to 0.1 µm and remain sticky for the chiplet to adhere to before final curing.

5. CONCLUSION

We proposed the concept of optical pitch transformer chiplet for photonics integration platform and explored the coupling feasibility to ion-exchanged waveguide. While the current simulation results were limited to 1 mm coupling length due to available computational resources, there is a possibility of increasing it to improve the coupling efficiencies, together with better taper designs. Results showed that SiN inverted taper behaves differently depending on its functionality, and two separate designs may be needed as emitter and receiver respectively. We have also shown that by reducing the thickness of the adhesive and oxide layers, the coupling efficiency can be increased to less than 0.3 dB loss even with a 1 mm taper length.

ACKNOWLEDGMENT

This activity is funded by the European Union's Horizon Europe under Grant Agreement # 101213727.

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