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Effects of the Semiconductor Substrate Material on the Post-Breakdown Current of MgO Dielectric Layers

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The post-breakdown (BD) current-voltage (I-V) characteristics in MgO/Si and MgO/InP stacks with metal gate were investigated. We show that both stacks exhibit the soft and hard BD conduction modes and that the magnitude of the post-BD currents depends statistically on the substrate material, being larger in the case of the InP samples. This is contrary to what happens with the current in the fresh devices, which irrespective of the InP surface treatment, is larger for the Si samples. A comparative analysis of the post-BD conduction characteristics and direct evidence of the localized thermal effects on the metal gate electrode of both structures is also presented.

Introduction

Even though much work has been done in the past to characterize the post-BD conduction in a large number of different gate stacks, to our knowledge, the role played by the semiconductor substrate material has never been explored before. On the other hand, the effect of the gate electrode material was investigated in Ref. (1) but in all cases with Si substrates. In this paper, we present experimental results examining the soft (SBD) and hard (HBD) breakdown currents in 20 nm-thick layers of magnesium oxide (MgO) deposited on Si and InP substrates. We have chosen to investigate these systems in particular because MgO has been pointed out as an appealing material not only for use as an alternative gate insulator in MOS devices (2) but also as part of other devices such as spin valves and magnetic tunnel junctions (3). The main features of MgO can be summarized as follows: a large band gap in the range 7.3 eV (4)- 7.8 eV (5), a medium dielectric permittivity κ ranging from 6.7 (6) to 10 (5) depending on the preparation method, high thermal conductivity and breakdown field (12 MV/cmv for epitaxial growth) (4), and significantly, its chemical properties, which seems to improve the abruptness of the transition layer between the oxide and the semiconductor material (2). InP is a high-mobility compound semiconductor that has been successfully integrated into advanced stacks for high-speed MOSFETs (7,8). Moreover, it has been reported that the interface of MgO films grown on p-type InP substrates is very smooth at the atomic scale with no evidence of interfacial reaction (9), a fact that enhances the interest in this material combination.

SBD and HBD failure modes correspond to the electron transport through localized spots distributed over the device area and their names reflect the magnitude of the total leakage current (10). Under such circumstances, the current does not scale with the gate area so

that the current density is no longer a useful descriptor for the device conduction characteristics. From a physical degradation point of view, the number of spots per unit area is not a good indicator of the leakage current since the transmission properties of the spots may be very dissimilar. Both modes can occur simultaneously in different locations on the same sample and while SBD is often related to the formation of a percolation path across the dielectric layer without significant thermal effects, HBD is associated with larger damaged areas and lateral propagation of discharge events (11).

This paper is organized as follows: first, we compare the fresh I-V characteristics of the MgO on Si and InP samples for both injection polarities. In this latter case, we show the effects of using different surface cleaning processes. Second, we analyze a large number of SBD I-V curves in order to detect any statistical dependence on the substrate material and third, we focus the attention on the HBD I-V characteristics. We show that for this latter failure mode there is a remarkable difference in the leakage current magnitude of both structures. Finally, we show experimental results which demonstrate that even for SBD conduction the thermal effects cannot be neglected. The opened spots leave permanent prints on the gate electrode that permit to localize the BD events. Further stress leads to the lateral propagation of the damage in the form of random walks.

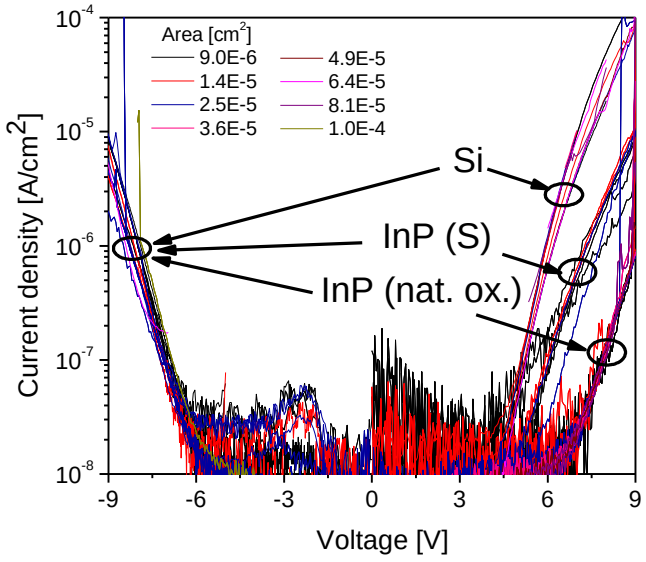

Figure 1. Current density as a function of the gate voltage for the three samples under investigation. The colors indicate the area of the devices.

The Samples

The samples used in this study are MgO films with nominal t_{ox}=20 nm deposited by e-beam evaporation from 99.9% MgO pellets at a rate of 0.2 Å/s at 180 ºC on n-type Si (10^{15} cm^{-3} P doped) and n-type InP ($3x10^{18}$ cm^{-3} S doped) substrates. In the case of InP, we have considered samples with no clean (native oxide) and with ammonium sulfide clean (S). The MgO/Si and MgO/InP samples were capped *in-situ* with 100 nm of amorphous silicon (α-Si) using a second e-beam source. For the NiSi gate process, nickel

was deposited by e-beam evaporation (~80 nm) through a patterned resist mask followed by a lift-off process. The rapid thermal annealing is a one step process at 500 ^{o}C for 30 s in N_2. The area of the devices tested ranges from $9.0x10^{-6}$ to $1.0x10^{-4}$ cm^2. From the C-V measurements, the permittivity of the MgO films on Si was calculated as 8.1. All the post-breakdown I-Vs were obtained by ramped voltage stress.

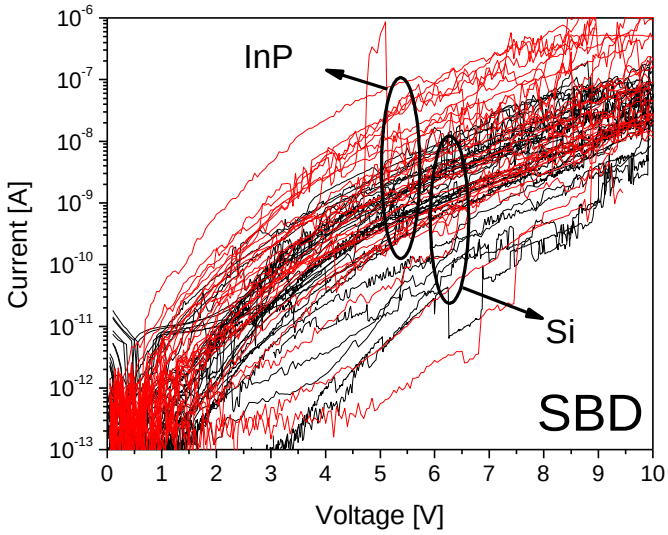

Figure 2. Current-voltage characteristics of the MgO/Si (black traces) and MgO/InP (red traces) stacks corresponding to the SBD failure mode. Some of the curves were measured in the same device after stressing it further by applying successive voltage ramps.

Experimental Results and Discussion

Figure 1 shows the current density profiles from the fresh MgO/Si and MgO/InP stacks. The current scales with the area of the devices indicating uniform current flow and dielectric thickness uniformity over the whole device. Interestingly, while the currents for positive gate injection depend not only on the substrate material but also on the surface cleaning process, the current density profile for negative gate voltages are very similar in the three cases considered. The fact that for negative gate injection the current density is insensitive to the particular features of the substrate points out that the charge transport is mainly due to electron injection from the gate electrode. It also confirms (assuming tunneling conduction) the thickness uniformity of the deposited dielectric. The difference for positive gate injection is more difficult to explain since, at first glance, the current in the InP (E_G=1.34 eV) samples should be larger than in the Si (E_G=1.12 eV) ones because of the lower potential barrier height expected for the MgO/InP system. The difference between the leakage current magnitudes may be in part a consequence of the large surface state density at the MgO/InP interface since, as shown in Fig. 1, the shift reduces with the passivation treatment of the InP surface (from 3V to 1V@10^{-7}A/cm^2). This is consistent with capacitance-voltage measurements (not shown here). In this regard, it has been demonstrated that the cleaning process has a major impact on the electron affinity of this material (12). A possible explanation to account for the origin of the large current difference is that when in accumulation conditions, the interface states in the

semiconductor band gap become charged so that they partially screen the applied voltage therefore reducing the oxide field or the free electron density available for tunneling injection. Accordingly, a larger interface state density would result in a shift of the I-V characteristic towards higher voltage values as observed in Fig. 1. Based on the shift of the I-V characteristics we have estimated that a lower bound for the interface state density in the InP samples would be in the range from 10^{12} to 10^{13} cm^{-2}.

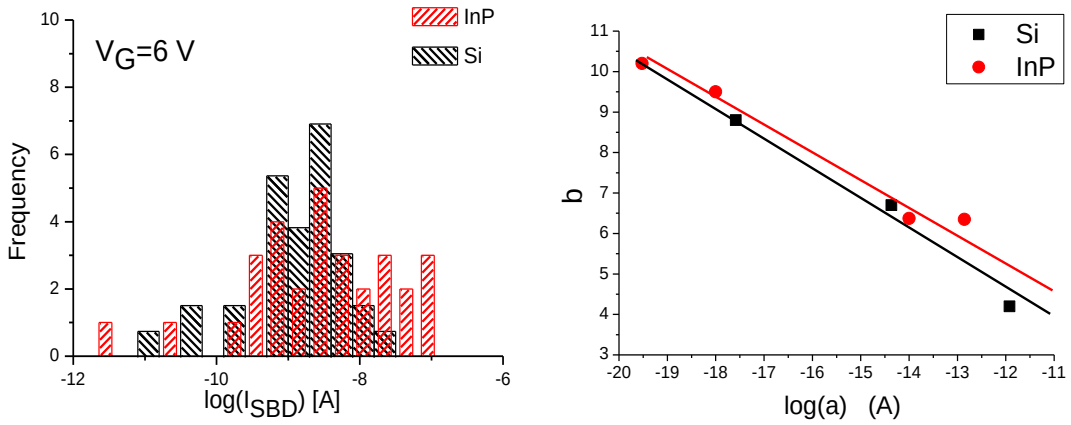

Figure 3. Histogram corresponding to the SBD currents at V_G=6 V for InP and Si shown in Fig. 2. The second figure shows the correlation between the parameters of the power-law model $I=aV^b$. The data was extracted from the I-Vs in Figs. 4.

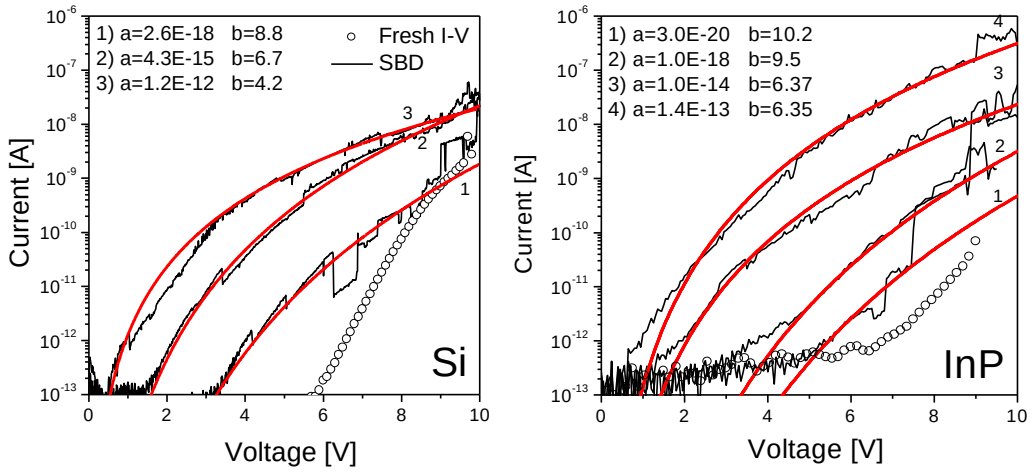

Figure 4. Evolution of the SBD current-voltage characteristics (black lines) measured in the same Si and InP substrate samples. The circles are the fresh I-Vs while the red lines correspond to the fitting results using the power-law model.

On the contrary, as shown in Fig. 2, the SBD currents in the InP stacks are somewhat larger than those in the Si stacks. It is worth pointing out that not all the I-Vs were measured in different devices so that some of the curves were obtained by applying

successive voltage ramps to the same device. As illustrated in Fig. 3, the SBD curves are mainly limited to a band (from 10^{-11} to 10^{-7}A@V_G=6V) and further stressing leads to large current jumps which are associated with the direct transition to HBD. No correlation with the area of the devices nor with the InP surface treatment has been observed. Nevertheless, caution should be exercised with the analysis of the data since the increased leakage current distribution can be attributed not only to the higher doping level of the InP substrate (the oxide barrier does not play any role after BD) but also it may be a consequence of a larger/more conducting damaged area. Preliminary results indicate that the number of spots in the MgO/Si and MgO/InP systems is very similar and it is likely to be limited by the potential drop in the effective series resistance connected to the oxide capacitance.

In order to verify that we are strictly dealing with the SBD conduction mode we have fitted some I-V characteristics measured in the same device (see Fig. 4). To this end, we have adopted the power-law model $I=aV^b$, where *a* and *b* are constants. This model has been related to the conduction properties of percolative nonlinear resistance networks (13). We have found that the power *b* is in the range from 4 to 10 and in agreement with what was previously reported for the SiO_2/Si system (14), *b* decreases for more damaged areas (see Fig. 3). In particular, there is a linear correlation between *b* and log(*a*), which has been explained in terms of the mesoscopic theory of electron transport through confined conducting paths (15). The fact that the curves in Fig. 4 are associated with the creation of additional spots in the same device is confirmed by the images shown in Fig. 5, which were taken during degradation from devices in the SBD stage. As it can be seen, the BD spots appear as scattered points distributed over the device area and correspond to a permanent physical damage in the gate electrode. For comparison, Fig. 6 shows the distribution of spots in the two structures under investigation. In order to detect the spots on the metal gate of the Si samples, a large contrast must be used. On the contrary, the prints in the InP samples are much more well defined and do not require any special image treatment. This demonstrates that not only HBD but also SBD is associated with thermal effects. Curiously, as shown in Fig. 5 (photo 6), there are no spots under the voltage probe so that it could effectively behave as a thermal sink.

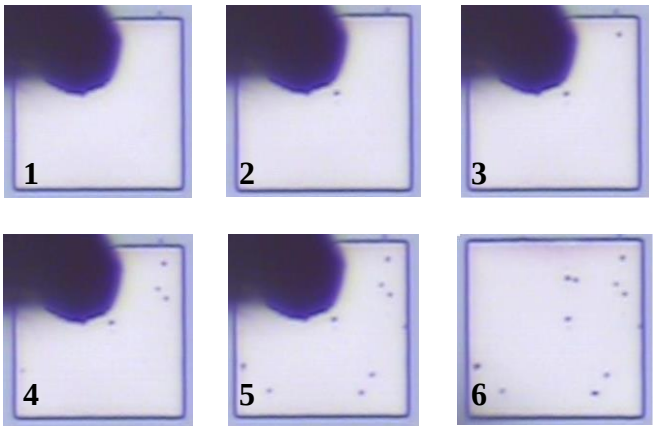

Figure 5. Creation of BD spots in the InP substrate samples by the application of successive voltage ramps. The dark shadow corresponds to the voltage probe.

For HBD (see Fig. 7), the currents in the MgO/InP stacks are unquestionably higher in all the cases. The current reaches the compliance limit nearly at the outset of the measurement and the degradation process is accompanied by large thermal effects which are also visible in the gate electrode. The lateral propagation of the damage seems to be related to the connection of BD spots so that the final result is a kind of random walk (see Fig. 8). Similar behavior was reported before for thick SiO_2 layers on Si substrates (11) and was attributed to the diffusive propagation of the damage. This particular degradation pattern may be caused by surface currents originated by an out-of-equilibrium lateral potential distribution occurring at the very moment of the BD runaway. Sometimes, large on-off current fluctuations can be detected during the voltage sweep but their origin is still unknown.

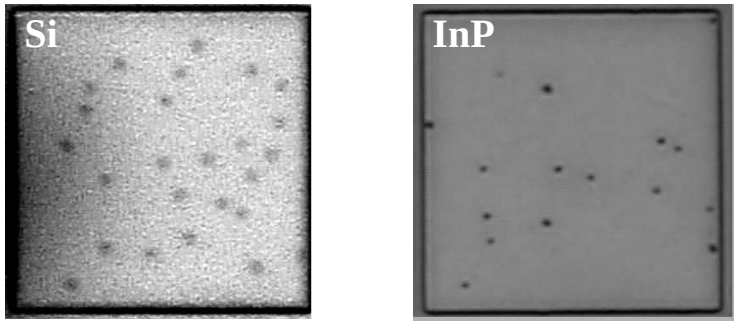

Figure 6. Typical images of the SBD spots taken from Si (left image) and InP (right image) substrate samples. Note that the spots are much well defined in the InP sample. The number of spots cannot be increased beyond certain limit because of the potential drop in the series resistance.

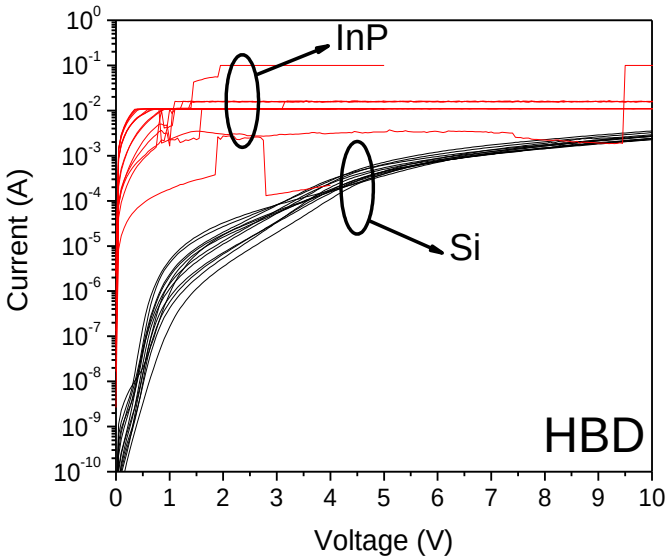

Figure 7. Current-voltage HBD characteristics measured in different Si and InP samples. Notice the switching events in the InP curves, which reflect the partial opening and closing of the BD paths.

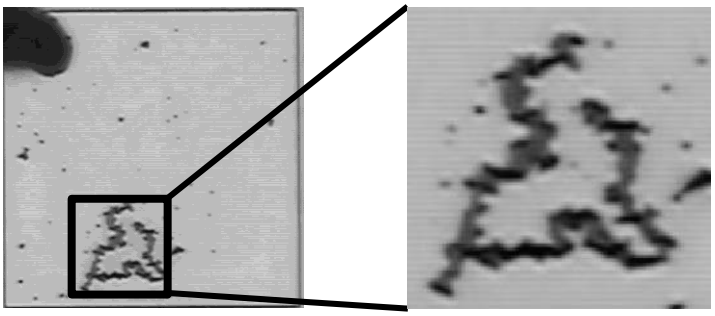

Figure 8. Photographs taken from the InP samples in the HBD state after the application of a high-field voltage sweep. Notice the lateral propagation of the damage in the form or random walks. The dark image in the upper corner of the left image corresponds to the voltage probe.

Conclusions

The post-breakdown current in MgO layers deposited on Si and InP substrates were investigated. It was shown that the substrate material plays a role in the leakage current distribution after soft breakdown and that the difference is much more dramatic in the case of hard breakdown. We have also demonstrated that both breakdown modes exhibit thermal effects which become visible as permanent damage in the gate electrode area.

Acknowledgments

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