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Heterogeneous III-V on silicon nitride amplifiers and lasers via microtransfer printing

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The development of ultralow-loss silicon-nitride-based waveguide platforms has enabled the realization of integrated optical filters with unprecedented performance. Such passive circuits, when combined with phase modulators and low-noise lasers, have the potential to improve the current state of the art of the most critical components in coherent communications, beam steering, and microwave photonics applications. However, the large refractive index difference between silicon nitride and common III-V gain materials in the telecom wavelength range hampers the integration of electrically pumped III-V semiconductor lasers on a silicon nitride waveguide chip. Here, we present an approach to overcome this refractive index mismatch by using an intermediate layer of hydrogenated amorphous silicon, followed by the microtransfer printing of a prefabricated III-V semiconductor optical amplifier. Following this approach, we demonstrate a heterogeneously integrated semiconductor optical amplifier on a silicon nitride waveguide circuit with up to 14 dB gain and a saturation power of 8 mW. We further demonstrate a heterogeneously integrated ring laser on a silicon nitride circuit operating around 1550 nm. This heterogeneous integration approach would not be limited to silicon-nitride-based platforms: it can be used advantageously for any waveguide platform with low-refractive-index waveguide materials such as lithium niobate. © 2020 Optical Society of America under the terms of the OSA Open Access Publishing Agreement

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1. INTRODUCTION

Owing to its wide optical transparency range, silicon nitride (Si_3N_4) has been recognized several decades ago as a suitable candidate for photonic integrated circuits (PICs). Originally, it was used in sensing applications at visible wavelengths. Later on, interest also spiked for applications in the near-infrared. Silicon nitride holds a number of advantages over silicon in this wavelength range. The first is the absence of nonlinear losses such as two-photon absorption and the associated free-carrier absorption. This gives silicon-nitride-based PICs the ability to handle much higher on-chip optical intensities. When proper care is taken to reduce scattering and impurities in the core and cladding, silicon nitride waveguides are capable of carrying several watts of optical power without suffering damage [1]. The second advantage is the lower sensitivity to fabrication errors, due to the lower index contrast as compared to silicon photonic circuits, enabling high-performance passive filters. Thirdly, ultralow waveguide losses can be achieved. Nowadays losses below 10 dB/m around 1550 nm are measured [1–5]. However, the integration of active devices on silicon nitride waveguides remains challenging. Phase modulators on silicon nitride have been demonstrated using materials with closely matched refractive indices such as lithium niobate (LN, $n \simeq 2.2$ at 1550 nm) [6] and lead zirconate titanate (PZT, $n \simeq 2.3$ at 1550 nm) [7]. The integration of III-V materials with higher refractive indices is essential to include photodetection and light sources or light amplification on the platform. The large refractive index difference between Si_3N_4 and indium phosphide (InP)-based materials ($\Delta n \sim 1.3 - 1.5$) makes it challenging to make use of the adiabatic coupling schemes that were developed for the heterogeneous integration of III-V components on the silicon-on-insulator (SOI) platform [8,9]. As such, in device demonstrations with ultralow loss Si_3N_4, light is typically coupled to and from the Si_3N_4 waveguide through edge-coupling. Hybrid single-mode lasers with sub-kilohertz intrinsic Lorentzian linewidths have been demonstrated with edge-coupling, enabling integrated light sources with unprecedented purity [10–12]. In order to increase the functionality of a single photonic chip, multiple active devices need to be interfaced with the passive circuit. Since the edge-coupling method does not allow densely integrated active components, there is a need for alternative schemes such as flip-chip or heterogeneous integration. Recently, the flip-chip integration of an InP semiconductor optical amplifier (SOA) on a low-loss Si_3N_4 platform was demonstrated [13]. Another promising approach is to cointegrate a silicon nitride waveguide

layer and a silicon waveguide layer in one platform, either by depositing Si_3N_4 on a patterned and planarized SOI wafer [14,15] or by using wafer-bonding technology, whereby SOI wafers are bonded on the Si_3N_4 circuits [2,16]. Using the latter approach, photodiodes were integrated at the output of an arrayed-waveguide grating in a low-loss Si_3N_4 platform [17]. The first demonstrations of heterogeneously integrated amplifiers and lasers on Si_3N_4 occurred more recently, first using the method proposed in this paper [18,19] and later on also using wafer-bonding technology [20]. In this work, we present a novel strategy for the heterogeneous integration of InP-based components on Si_3N_4 through microtransfer printing. The large index difference between the Si_3N_4 and the III-V material is bridged by an intermediate layer of hydrogenated amorphous silicon (a-Si:H), deposited using plasma-enhanced chemical vapor deposition (PECVD). The light can be locally coupled out of the Si_3N_4 layer into an a-Si:H waveguide, onto which the active device can be microtransfer printed. Microtransfer printing technology combines several advantageous aspects of wafer bonding and flip-chip integration. It allows for an efficient use of the expensive active materials, massively parallel integration of pretested devices and the cointegration of diverse material stacks for different functionalities on a single target substrate [21]. Here, we use this strategy to integrate an InP/InAlGaAs-based multiple-quantum-well (MQW) SOA on a straight silicon nitride waveguide and in a silicon nitride ring laser cavity. The paper is organized as follows: In Section 2, the design of the tapering structure from the Si_3N_4 layer to the SOA is elaborated. In Section 3, the concept of microtransfer printing is explained, after which the sample fabrication is discussed. The characterization of the fabricated devices is discussed in Section 4.

2. DESIGN

A two-stage taper is designed to locally couple the light out of the Si_3N_4 waveguide into a waveguide in the a-Si:H layer and consecutively to a mode that overlaps with the quantum wells in the III-V stack. A schematic layout of the taper is shown in Fig. 1(a). The starting point of the design is the first taper from the Si_3N_4 to the a-Si:H. The 300-nm-thick Si_3N_4 layer is deposited using low-pressure chemical vapor deposition (LPCVD) on a silicon substrate with 3.3 μm of thermally grown silicon oxide (TOX). Second, using PECVD, a silicon oxide (SiO_2) spacer layer of 100 nm is deposited on the Si_3N_4, followed by 370 nm of a-Si:H. The value of the refractive index of the a-Si:H was determined to be $n = 3.40$ at 1550 nm through ellipsometry. The purpose of the SiO_2 spacer is to decrease the perturbation of the mode in the Si_3N_4 at the a-Si:H taper tip, as well as to act as an etch-stop layer, as explained in Section 3. The thickness of the a-Si:H layer is chosen such that efficient coupling is possible between all three layers in the taper. The Si_3N_4 waveguide is made 3000 nm wide ($w_{Si_3N_4}$) before the transition to the a-Si:H, to further reduce the perturbation at the taper tip. To minimize parasitic reflections and unwanted cavity effects, the taper tip should be made as narrow as possible in a reproducible way. Its width $w_{aSi,1}$ is targeted at 120 nm, which is still compatible with deep-UV lithography. The reflection at the taper tip was simulated using 3D finite-difference time-domain (FDTD) simulations,

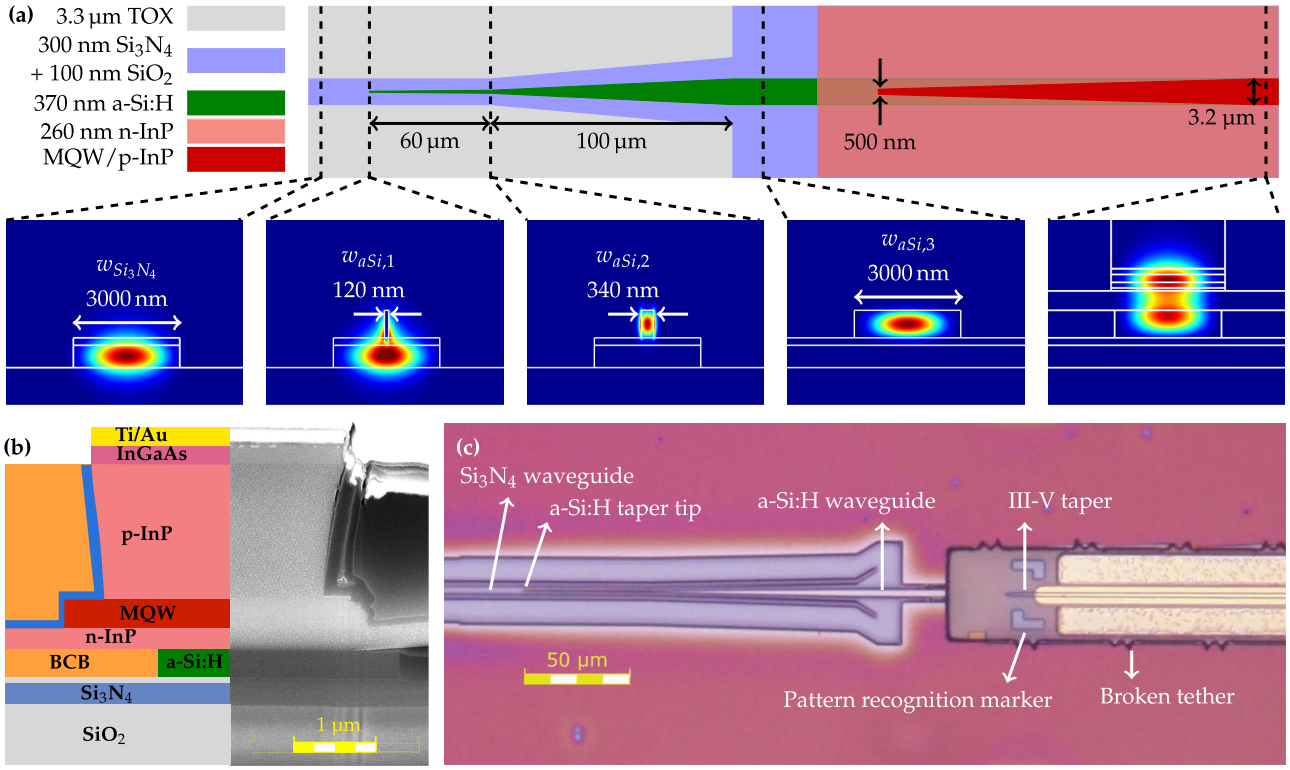

Fig. 1. (a) Schematic layout of the two-step taper from the Si_3N_4 waveguide to the InP/InAlGaAs amplifier. The fundamental TE mode is shown at different stages in the taper. The first two modal distributions are plotted with the same color scale to illustrate the mode matching at the a-Si:H tip interface. (b) SEM image of a cross section of a microtransfer printed III-V amplifier on an a-Si:H waveguide, overlaid with a schematic drawing of the stack. A lateral misalignment of ~650 nm between the SOA and the a-Si:H waveguide is visible. (c) Optical microscope image of a microtransfer printed SOA coupon on an a-Si:H waveguide coupling to the Si_3N_4 layer.

for the case of perfect alignment of the taper to the Si_3N_4 waveguide. On the side of the Si_3N_4 waveguide, −50 dB is reflected back into the fundamental TE mode. In the a-Si:H waveguide, the reflection is −41 dB. When the a-Si:H waveguide becomes 340 nm wide ($w_{aSi,2}$), the mode has transitioned completely from the Si_3N_4 to the a-Si:H. This transition length is designed to be 60 μm. A second broadening to a 3-μm-wide ($w_{aSi,3}$) multimode waveguide with lower scattering losses is done over a length of 100 μm. Eigenmode expansion simulations show that this configuration leads to a coupling efficiency over 99%, for lateral taper misalignments up to 200 nm.

The layer stack of the SOA is similar to the one reported in Ref. [22], only differing in the release layer, which in this work consists of 50 nm InGaAs on top of 500 nm InAlAs, as will be explained in Section 3. A scanning-electron microscope (SEM) image of a focused ion beam (FIB) cross section of the final heterogeneously integrated device is given in Fig. 1(b), together with a schematic drawing of the layer stack, showing the different device layers. The III-V stack features an N-type InP cathode, InAlGaAs separate confinement heterostructure (SCH) layers, six InAlGaAs quantum wells and barriers, and a P-type InP and InGaAs anode. The taper of the III-V waveguide was designed to be tolerant to misalignments up to 1 μm, when the width of the waveguide underneath is constant [23]. Therefore, the a-Si:H waveguide width remains constant at 3000 nm throughout the length of the amplifier. As shown in Fig. 1(a), the taper tip of the III-V waveguide is 500 nm wide. Three-dimensional FDTD simulations show that the total reflection loss on the side of the a-Si:H waveguide at the tip is −47 dB, of which only −60 dB is coupled back into the fundamental TE mode. The reflection back in the III-V taper is −21 dB, of which −36 dB couples into the fundamental TE mode. Eigenmode expansion simulations indicate that the coupling efficiency of this taper is 93% for perfect alignment. The efficiency goes down to 75% for a misalignment of 1 μm. In the hybrid a-Si:H-III-V fundamental TE mode at the center of the SOA, the mode confinement per quantum well is 0.93%. This value remains largely unaffected by moderate lateral misalignments (up to 1 μm) of the SOA relative to the a-Si:H waveguide. A microscope image of a device during the processing, in which the two described tapers are visible, is shown in Fig. 1(c).

The a-Si:H waveguide losses are inevitably higher than those in the Si_3N_4: ∼5 dB/cm for a 3000-nm-wide a-Si:H waveguide using our current process. This loss is mainly due to bulk absorption and scattering mechanisms, as well as scattering on the roughness of the top surface. It can be reduced by polishing the surface after deposition and optimizing the deposition conditions to limit the formation of voids and defects. The losses of the Si_3N_4-a-Si:H transition were measured after the processing of the full chip, using several identical Si_3N_4 waveguides with increasing numbers of pairs of direct and inverse a-Si:H tapers on them. Figure 2 shows the measured losses per taper. For the tapers with 120-nm-wide tips, the measured transmission per transition is −0.66 dB. The transmission spectra of these waveguides did not feature clear interference fringes, indicating that the reflections are weak, as predicted by the simulations.

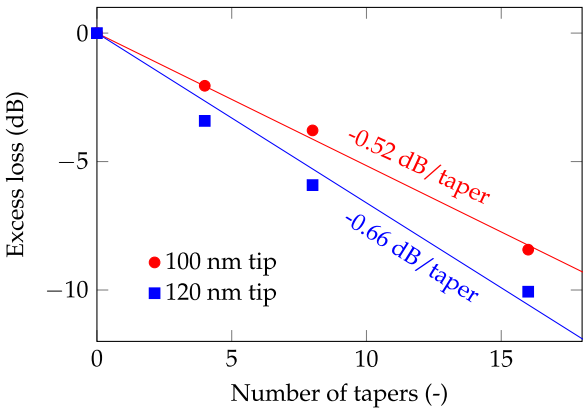

Fig. 2. Measured excess loss per taper tip for two designed tip widths, extracted from identical Si_3N_4 waveguides with increasing numbers of tapers at fixed intervals.

3. FABRICATION

A. Microtransfer Printing: Source Sample Preparation

Microtransfer printing is an integration technology based on the switchable adhesion from a device of interest to an elastomeric stamp [24]. The adhesion to the stamp increases with the stamp's peeling velocity owing to its viscoelasticity. Provided that the adhesion of the device to its native substrate can be reduced to a sufficiently low level, the device's adhesion to the stamp can be kinetically turned on or off. This process was introduced to integrated photonics for the heterogeneous integration of active III-V devices on silicon photonic circuits [21,25,26]. The process of microtransfer printing starts with the definition of active devices (referred to as coupons) on a III-V wafer (the "source" wafer). This is schematically shown in Figs. 3(a)–3(d). These active devices can then be transferred to a non-native substrate, the "target" wafer. The III-V source wafer is densely populated with arrays of SOA coupons of various lengths. Around 1000 SOAs with different lengths fit on 1 cm^2 of the III-V wafer in this design. One source wafer can thus be used to add amplifiers to a great number of target wafers. The layer stack needed for the active devices on the source is epitaxially grown on a 50 nm InGaAs on top of 500 nm InAlAs release layer, which can be etched with a high selectivity against InP [Fig. 3(a)]. The definition of the devices starts with the patterning and formation of the III-V SOA mesa and the active region using optical contact lithography and a mixture of dry and wet etch processes [Fig. 3(b)]. The sidewalls of the MQW layer and the p-InP mesa are passivated using a layer of PECVD-deposited silicon nitride. A lift-off process is used to deposit Ni/Ge/Au contacts on the n-InP cathode. The wafer is then planarized using divinylsiloxane-bis-benzocyclobutene (DVS-BCB, or BCB). The InGaAs contact layer is opened up, and Ti/Au contacts are deposited on the anode. To define the coupon boundaries, the BCB and n-InP layer are patterned in a dry etching step, exposing the release layer next to the coupons. The exposed release layer is patterned, and openings are etched down to the InP substrate in a dry etching step. The devices are then covered with a patterned photoresist encapsulation, which is resistant to the release layer etchant [Fig. 3(c)]. The photoresist is attached to the III-V substrate with thin tethers, while leaving the release layer accessible for the etchant to be able to underetch the coupons. The release layer is then etched in a $FeCl_3 : H_2O$ solution at 7°C, leaving the coupons suspended by means of the encapsulation [Fig. 3(d)]. The release layer etch reduces the adhesion strength of the active device to its substrate to the mechanical strength of the weakest point in the tethers. After the release layer etch, the coupons are ready to be microtransfer printed onto the target wafers.

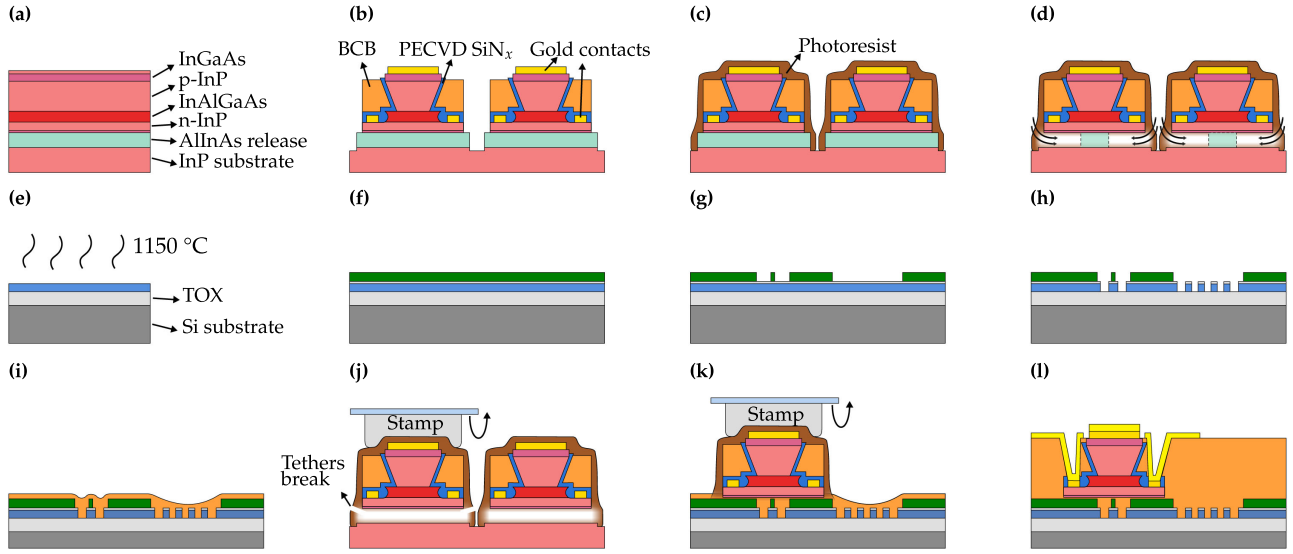

Fig. 3. Schematic process flow of the definition of active devices on the (a)–(d) III-V-substrate for microtransfer printing, (e)–(h) the target substrate preparation, and (i)–(l) the heterogeneous integration and postprocessing. (a) III-V epitaxial layers; (b) device definition on source; (c) coupon encapsulation; (d) release layer etch; (e) LPCVD Si_3N_4 deposition; (f) PECVD a-Si:H deposition; (g) patterning a-Si:H layer; (h) patterning Si_3N_4 layer; (i) spincoating adhesive BCB layer; (j) pick coupon from source; (k) print coupon on target; (l) electrical contacting.

B. Target Sample Preparation

In this work, the target is a Si_3N_4-on-insulator wafer with locally defined a-Si:H tapers and waveguides. The fabrication steps to prepare the target wafer for the microtransfer printing, starting from a blank wafer, are shown in Figs. 3(e)–3(h). The target starts from a polished 4" silicon wafer, onto which 3.3 μm of thermal oxide is grown. Afterward, a 300-nm-thick stoichiometric Si_3N_4 layer is deposited using LPCVD, and the wafer is annealed at 1150°C in a N_2 atmosphere to let the hydrogen diffuse out of the material [Fig. 3(e)]. This reduces the N–H overtone related absorption peak at 1520 nm. The high-quality Si_3N_4 layer resulting from this process is transparent from 400 nm [27]. Subsequently, the wafer is cleaved into individual chips for further processing. Using PECVD, a layer of 100 nm SiO_2 is deposited at 270°C, followed by a layer of 370 nm a-Si:H at a temperature of 180°C [Fig. 3(f)]. In this first demonstration, the circuit is defined using e-beam lithography in a top-down fashion to avoid the need for planarization steps. In a first exposure step, the microtransfer printing sites for the III-V amplifier (a straight 3-μm-wide a-Si:H waveguide) and the a-Si:H tapers are defined using a positive e-beam resist (AR-P 6200.13). In the same step, a large area is also cleared where the Si_3N_4 waveguides will be defined in the next exposure step. Apart from two 3-μm-wide trenches around the a-Si:H waveguide, the area around the printing site remains flat [Fig. 3(g)]. This is needed in order to be able to microtransfer print the III-V amplifier on the waveguide. The a-Si:H is etched anisotropically using reactive ion etching with a mixture of CF_4, SF_6, and H_2. This results in straight waveguide sidewalls and taper tips. The etch rate is controlled to stop etching at the SiO_2 layer, such that the top surface of the Si_3N_4 is not damaged. The resist mask is then stripped with oxygen plasma, and afterward the Si_3N_4 circuit is defined in a second step of e-beam lithography using the same type of resist, spincoated at a lower speed for a higher thickness [Fig. 3(h)]. The e-beam resist covers the topography of the patterned sample conformally. It is sufficiently thick to protect the previously defined patterns in the a-Si:H, in particular, the taper tips. An alignment precision better than 100 nm can be achieved between the two exposure steps, which ensures a high coupling efficiency of the a-Si:H taper. The exposed pattern is transferred to the Si_3N_4 layer by reactive ion etching with CF_4, SF_6, and H_2. After stripping the resist in oxygen plasma, the target is prepared for the microtransfer printing by spincoating a thin layer of BCB, diluted in mesitylene [Fig. 3(i)]. The mesitylene is evaporated during a prebaking step at 150°C. The BCB acts as an adhesive layer that relaxes the requirements in terms of surface roughness, and improves the yield of the microtransfer printing process. The influence of the layer depositions and etching on the Si_3N_4 waveguide losses was investigated using a cutback method. The waveguide losses were measured on a reference Si_3N_4 sample on which no SiO_2 or a-Si:H was deposited (waveguide lengths 2 cm and 12 cm), and on the target sample after the full processing (waveguide lengths 1 cm, 2 cm, 3 cm, and 4 cm). The losses increased from 0.61 ± 0.15 dB/cm to 0.8 ± 0.15 dB/cm at 1570 nm for a 3-μm-wide waveguide. This increase can be attributed to the introduced roughness on the waveguide's top surface due to the SiO_2 spacer layer and absorption in the BCB cladding.

C. Microtransfer Printing Process

After processing the source and target samples, the active devices can be microtransfer printed onto the a-Si:H landing sites. The total coupon size of the used amplifier is 1186.5 μm × 47.5 μm. The total length of the active layers is 1148 μm, consisting of a central straight section of 700 μm long and 3.2 μm wide, and two adiabatic tapers, each 224 μm long. The source and target wafers are loaded into an X-Celeprint μTP-100 tool. An elastomeric polydimethylsiloxane (PDMS) stamp with a single 1200 μm × 50 μm post can be used to pick up a single coupon from the III-V source wafer. The stamp is laminated against a coupon, followed by a rapid upward acceleration, during which the adhesion of the coupon to the stamp increases and the tethers break at their weakest point. This is schematically shown in Fig. 3(j), and the broken tethers are

visible on the fabricated device in Fig. 1(c). Printing a coupon on the target wafer happens in the opposite way. The coupon is laminated against the target, after which the stamp is retracted slowly, leaving the coupon behind on the target [Fig. 3(k)]. An extra shear force can be applied during the retraction to facilitate the release of the stamp. Both steps are carried out at room temperature. The printing process of III-V devices on PICs typically requires careful alignment. Markers for digital pattern recognition are therefore defined on the source coupon and near the target printing site. The markers on the coupon are visible on the device in Fig. 1(c). State-of-the-art microtransfer printing tools offer an alignment accuracy of ± 1.5 μm (3σ) for printed arrays and <1 μm for single coupons. Although the process shown here is sequential, dedicated stamps can be fabricated with posts matching the design of the source and target wafers to parallelize the microtransfer printing process. After the transfer printing, the photoresist encapsulation is removed, and the adhesive BCB layer is cured at 280°C. This is the highest temperature needed for the postprocessing of the microtransfer printed coupons. After planarizing the sample with a thick layer of BCB, the N- and P-contacts are opened up, and electrical contacts are added. The result of these last steps is shown in Fig. 3(l).

This integration technique combines the advantages of two established integration approaches: (heterogeneous) wafer bonding [28] and (hybrid) flip-chip integration [29]. Wafer bonding allows for high-throughput integration of active devices on the host substrate; however, the dense cointegration of different material stacks is not trivial. Furthermore, the III-V devices can only be tested after finishing the fabrication, leading to a compound yield issue. For flip-chip integration, active devices can be characterized prior to the integration; however, typically these devices need antireflective or highly reflective coatings on their facets, resulting in a high cost. Furthermore, the pick-and-placing of the devices is a sequential process, lowering the throughput significantly. Microtransfer printing combines the advantages of both methods. Devices can be fabricated on wafer scale and electrically pretested on their native substrate. Dense arrays of active devices can be printed in a parallel way, leading to a high throughput. Additionally, it is possible to cointegrate diverse material stacks in a dense way on a single target substrate. The pretesting can be done for each individual coupon, provided that it contains sufficiently large contact pads. A faster method consists of estimating the contact resistance of the anodes and cathodes over the whole wafer using transmission line measurements. In this work, the latter method was used for the electrical pretesting of the coupons.

4. DEVICE CHARACTERIZATION

A standalone III/V-on-Si_3N_4 amplifier and a III/V-on-Si_3N_4 ring laser were characterized. The processed sample is placed on a temperature-controlled chuck, which is set to a temperature of 20°C unless mentioned otherwise. The optical output of the devices is extracted through grating couplers in the Si_3N_4 layer, which are probed using cleaved standard single-mode fibers. All devices are accompanied by a nearby reference Si_3N_4 waveguide to calibrate the grating coupler efficiency. The measured peak coupling efficiency is -7.8 dB at 1545 nm, and the 3 dB bandwidth is 60 nm. Two-dimensional FDTD simulations indicate that the reflection in the waveguide at the grating coupler is smaller than -20 dB. The extracted optical output on one end of the device is collected by an optical spectrum analyzer (Anritsu MS9740A), which also acts as a powermeter for the alignment of the fibers at the grating coupler interface. For the measurement of the gain of the amplifiers, an optical input from a tunable semiconductor laser source (Santec TSL-510) is sent through a polarization controller and injected on the other side of the device. The devices are electrically contacted using DC probes. A low-noise current source and voltage meter (Keithley 2400 Sourcemeter) is used to control the applied bias current on the device. Both devices have a low differential series resistance of 10Ω at 80 mA. This bias current level corresponds to a current density in the active layers of 2.11 kA/cm^2.

A. III/V-on-Si_3N_4 Amplifier

Three parameters are swept to characterize the amplifier: the bias current, the optical input power, and the wavelength. Figure 4 shows the gain compression as a function of optical input power at a wavelength of 1570 nm, for different bias currents above transparency. The inset shows the layout of the measured device. At low input power levels, the gain reaches 13.7 dB for a current of 120 mA. We measure a maximum on-chip output power of 7.6 mW output power for an input power of 1.24 mW and 120 mA bias current. The gain compression can be approximated with the following simple relationship [30]:

$$G(P_{\text{in}}) = G_0 \frac{1 + P_{\text{in}}/P_{\text{sat}}}{1 + G_0 P_{\text{in}}/P_{\text{sat}}}. \tag{1}$$

Equation (1) can be used as a model to fit the small-signal gain G_0 and the saturation power P_{sat} for each bias current. The results of these fits are plotted in Fig. 5, together with the optical gain at 1570 nm for several optical input powers P_{in}. The fits indicate that the saturation power reaches 8 mW at 120 mA. For a low on-chip optical input power level of -11 dBm, the noise figure of the amplifier, which indicates the amount of randomly phased amplified spontaneous emission that is added to the signal, is 10.6 dB at a bias current of 100 mA and 12.3 dB at 120 mA. Finally, the wavelength dependence of the gain was measured for different input currents. This result is shown in Fig. 6. The wavelength dependence of the gain can be described using the following relationship:

$$G(\lambda) = G_p \cdot \exp\left[-A(\lambda - \lambda_p)^2\right]. \tag{2}$$

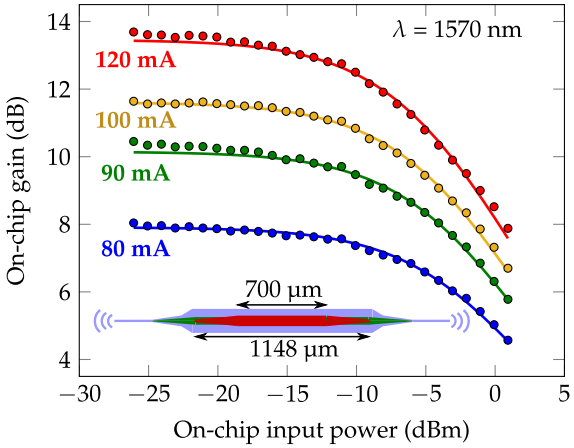

Fig. 4. On-chip gain of the III-V-on-Si_3N_4 amplifier at 1570 nm as a function of on-chip optical input power for different bias currents. The onset of gain compression is visible. The solid lines represent the fit to the gain compression model. The inset shows the layout of the measured device.

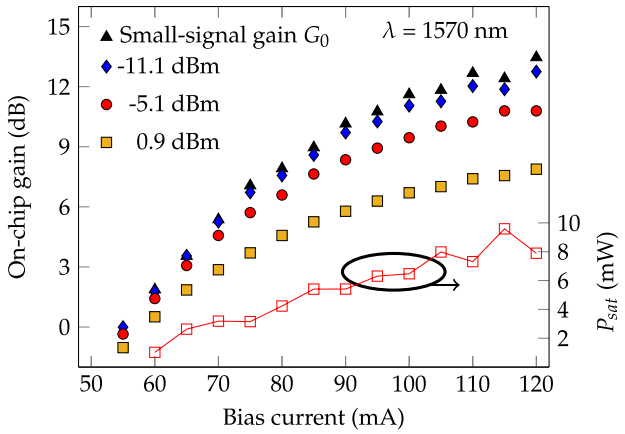

Fig. 5. On-chip gain of the III-V-on-Si_3N_4 amplifier at 1570 nm as a function of bias current for three on-chip optical input levels. The fitting parameters G_0 and P_{sat}—extracted from the fits in Fig. 4—are shown.

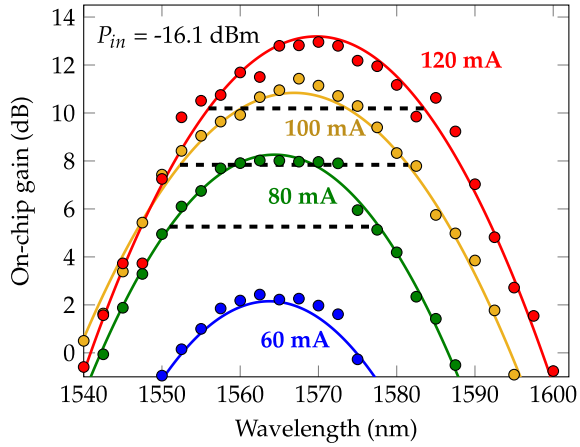

Fig. 6. Wavelength dependence of the gain of the III-V-on-Si_3N_4 amplifier at different bias currents, for an optical input level of −16.1 dBm. The dashed lines indicate the 3 dB gain bandwidth. The gain peak shifts to higher wavelengths for higher currents, indicating the effect of self-heating.

The solid lines in Fig. 6 represent the fits of Eq. (2) to the measured data, from which the peak wavelength λ_p, peak gain G_p, and the 3 dB bandwidth of the gain can be extracted. The latter is indicated by the dashed black lines. The amplifier has a 3 dB gain bandwidth of 28 nm at a bias current of 100 mA. The peak wavelength of the gain shifts from 1564.4 nm at 80 mA to 1569.7 nm at 120 mA. This redshift indicates self-heating, which can be explained by the higher thermal insulation between the device and the substrate in this stack, as compared to active devices integrated on SOI, which typically only has 2 µm of TOX below the waveguide layers. Higher gains and saturation powers can be achieved using longer devices with dedicated III-V epi-stacks and optimized waveguide cross sections [30,31].

B. III/V-on-Si_3N_4 Ring Laser

To demonstrate the potential of the amplifier, a laser cavity was formed by connecting the outputs of an amplifier with a 1-cm-long waveguide in the Si_3N_4 layer. A directional coupler is used to extract around 17% of the power circulating in the cavity. A schematic layout of the laser is shown in Fig. 7. No spectral filters were added in this first demonstration, so the laser is strongly multimode with a free spectral range (FSR) of 10.7 GHz. A detailed calculation of this FSR is given in Supplement 1. For the characterization of the laser, the same measurement setup is used, except the tunable laser input is replaced by a second optical power meter (HP 8153A Lightwave Multimeter). The laser is characterized by measuring the optical output power and spectrum as a function of bias current at three different temperatures: 15°C, 20°C, and 25°C. The measured voltage and single-sided on-chip optical output power at all three temperatures are plotted against the bias current in Fig. 8. The differential series resistance is the same at each temperature. It can be observed that the lasing threshold increases with temperature: from 59 mA at 15°C, over 63 mA at 20°C to 69 mA at 25°C. At threshold, the loss and gain of a longitudinal mode in the cavity match. The gain is reduced at higher temperatures. As shown in the supplementary information, thermal roll-off occurs at an electrical power dissipation around 230 mW. Reducing the series resistance will allow pumping of the device with higher current densities. Single-sided on-chip optical powers up to 350 µW are reached. This sub-milliwatt value can be explained by the combined effects of a low output coupling, cavity losses, and variability in the transfer printing alignment accuracy, which leads to a varying coupling efficiency between the III-V and the a-Si:H waveguides. Lasing spectra below and above

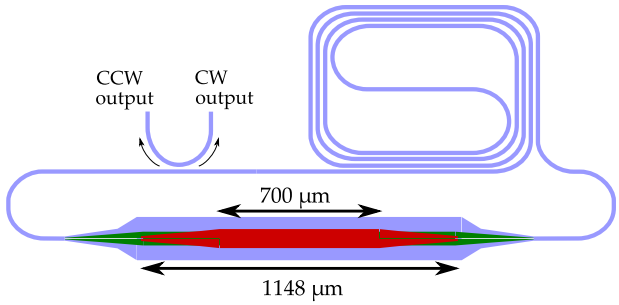

Fig. 7. Schematic layout of the laser. It comprises the same type of amplifier as characterized in Section 4.A. The amplifier's outputs are connected to a 1-cm-long spiral in the Si_3N_4 layer. A directional coupler is used to extract about 17% of the optical power circulating in the cavity in the clockwise (CW) and counterclockwise (CCW) direction.

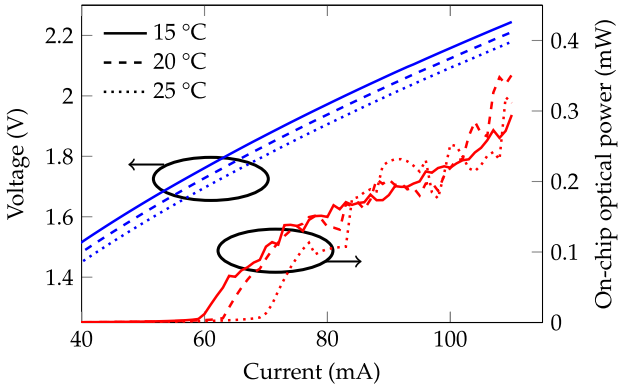

Fig. 8. LIV curves of the device. The estimated slope efficiency just above threshold at 20°C is 0.015 W/A.

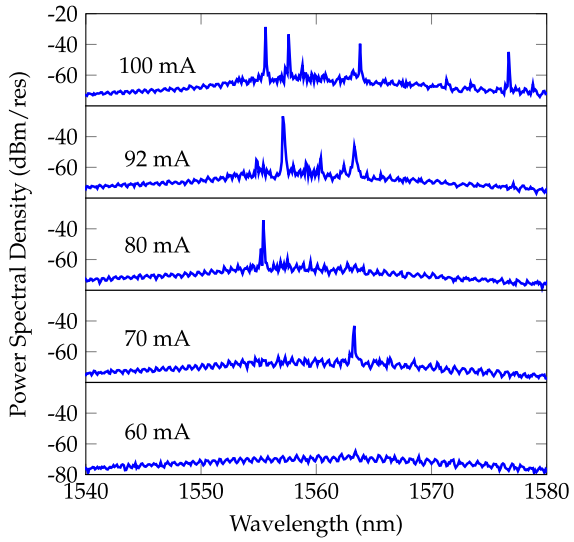

Fig. 9. Spectra of the device below and above threshold at 20°C, recorded with a resolution of 30 pm.

threshold at 20°C are shown in Fig. 9. Just above threshold, the estimated slope efficiency is 0.015 W/A, and only one lasing peak is prominent, with around 18 dB side-mode suppression. At higher bias currents, more modes start lasing. The laser can be made single-mode by adding a spectral filter in the Si_3N_4 cavity [20]. As shown in Supplement 1, the CW mode carries around 7 dB more power than the CCW mode, indicating that the modes are coupled due to spurious reflections in the cavity.

5. OUTLOOK

The demonstrated integration approach can be readily applied to Si_3N_4-based platforms with waveguide thicknesses from below 100 nm to above 700 nm featuring ultralow waveguide losses, or other platforms with low refractive indices such as lithium-niobate-on-insulator. Often, the waveguides in ultralow-loss waveguide platforms are oxide-clad. To apply this integration approach to these platforms, the oxide cladding could be locally removed, and a recess could be etched down to the waveguide layer. Since a-Si:H can be readily deposited using PECVD, there is no need for a wafer bonding step for the intermediate layer, which removes the requirement of having a flat surface. The microtransfer printing method can then be used to print active devices in a recess [32,33]. Therefore, our approach can be used to add adiabatically coupled active devices to a platform in a back-end process, without modifying the front-end process.

6. CONCLUSION

In conclusion, we demonstrate a novel strategy for the heterogeneous integration of III-V amplifiers on a low refractive index platform. Here we show the integration with Si_3N_4 PICs, by means of microtransfer printing active devices on an intermediate layer of a-Si:H. A III/V-on-Si_3N_4 SOA is demonstrated with a small-signal gain up to 14 dB and a saturation power of 8 mW. Using the same type of SOA, a heterogeneously integrated ring laser on a Si_3N_4-based platform is demonstrated. We propose that this strategy can be used to add more active functionality to a range of platforms where integration of III-V materials is currently challenging, such as the lithium-niobate-on-insulator platform.

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See Supplement 1 for supporting content.

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