

Title	Influence of channel material properties on performance of nanowire transistors
Authors	Razavi, Pedram;Fagas, Gíorgos;Ferain, Isabelle;Yu, Ran;Das, Samaresh;Colinge, Jean-Pierre
Publication date	2012
Original Citation	Razavi, P., Fagas, G., Ferain, I., Yu, R., Das, S. and Colinge, J.-P. (2012) 'Influence of channel material properties on performance of nanowire transistors', Journal of Applied Physics, 111(12), 124509 (8pp). doi: 10.1063/1.4729777
Type of publication	Article (peer-reviewed)
Link to publisher's version	<a href="http://aip.scitation.org/doi/10.1063/1.4729777">http://aip.scitation.org/doi/10.1063/1.4729777</a> - 10.1063/1.4729777
Rights	© 2012, American Institute of Physics. This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. The following article appeared in Razavi, P., Fagas, G., Ferain, I., Yu, R., Das, S. and Colinge, J.-P. (2012) 'Influence of channel material properties on performance of nanowire transistors', Journal of Applied Physics, 111(12), 124509 (8pp). doi: 10.1063/1.4729777 and may be found at <a href="http://aip.scitation.org/doi/10.1063/1.4729777">http://aip.scitation.org/doi/10.1063/1.4729777</a>
Download date	2025-07-03 21:55:01
Item downloaded from	<a href="https://hdl.handle.net/10468/4731">https://hdl.handle.net/10468/4731</a>

## Influence of channel material properties on performance of nanowire transistors

Pedram Razavi, Giorgos Fagas, Isabelle Ferain, Ran Yu, Samaresh Das, and Jean-Pierre Colinge

Citation: [Journal of Applied Physics](#) **111**, 124509 (2012); doi: 10.1063/1.4729777

View online: <http://dx.doi.org/10.1063/1.4729777>

View Table of Contents: <http://aip.scitation.org/toc/jap/111/12>

Published by the [American Institute of Physics](#)

---

### Articles you may be interested in

[Electrical performance of III-V gate-all-around nanowire transistors](#)

*Applied Physics Letters* **103**, 063506 (2013); 10.1063/1.4817997

[Mobility improvement in nanowire junctionless transistors by uniaxial strain](#)

*Applied Physics Letters* **97**, 042114 (2010); 10.1063/1.3474608

[Junctionless multigate field-effect transistor](#)

*Applied Physics Letters* **94**, 053511 (2009); 10.1063/1.3079411

[Gate-all-around junctionless silicon transistors with atomically thin nanosheet channel \(0.65 nm\) and record sub-threshold slope \(43 mV/dec\)](#)

*Applied Physics Letters* **110**, 032101 (2017); 10.1063/1.4974255

[Reduced electric field in junctionless transistors](#)

*Applied Physics Letters* **96**, 073510 (2010); 10.1063/1.3299014

---

**AIP** | Journal of  
Applied Physics

Save your money for your research.

It's now **FREE** to publish with us -

no page, color or publication charges apply.

Publish your research in the  
*Journal of Applied Physics*  
to claim your place in applied  
physics history.

# Influence of channel material properties on performance of nanowire transistors

Pedram Razavi, Giorgos Fagas, Isabelle Ferain, Ran Yu, Samaresh Das,  
and Jean-Pierre Colinge

*Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland*

(Received 14 March 2012; accepted 18 May 2012; published online 21 June 2012)

The performance of germanium and silicon inversion-mode and junctionless nanowire field-effect transistors are investigated using three-dimensional quantum mechanical simulations in the ballistic transport regime and within the framework of effective-mass theory for different channel materials and orientations. Our study shows that junctionless nanowire transistors made using n-type Ge or Si nanowires as a channel material are more immune to short-channel effects than conventional inversion-mode nanowire field-effect transistors. As a result, these transistors present smaller subthreshold swing, less drain-induced barrier-lowering, lower source-to-drain tunneling, and higher  $I_{\text{on}}/I_{\text{off}}$  ratio for the same technology node and low standby power technologies. We also show that the short-channel characteristics of Ge and Si junctionless nanowire transistors, unlike the inversion-mode nanowire transistors, are very similar. The results are explained through a detailed analysis on the effect of the channel crystallographic orientation, effective masses, and dielectric constant on electrical characteristics. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4729777>]

## I. INTRODUCTION

According to the international technology roadmap of semiconductors (ITRS) metal-oxide-semiconductor field-effect transistors (MOSFETs) are shrinking rapidly and will reach sub-10 nm regime within the next few years.<sup>1</sup> Scaling device dimensions gives rise to short-channel effects (SCEs) which is caused by a loss in electrostatic control of the channel by the gate. The classical SCEs are an increase of the subthreshold swing (SS), a lowering of the threshold voltage ( $V_{th}$ ) when gate length is reduced, and the drain-induced barrier lowering (DIBL) effect, which manifests itself as a lowering of the threshold voltage when the drain voltage ( $V_d$ ) is increased. All these effects degrade device performance. Reducing short-channel effects is important for being able to scale transistors to decananometer dimensions. To this end, various device structures and materials have been proposed.

Multiple-gate structures (such as the FinFET, trigate,  $\Pi$ -gate,  $\Omega$ -gate, and gate-all-around (GAA) MOSFETs), thin-body silicon-on-insulator (SOI) devices and high- $\kappa$  gate dielectrics are being used to enhance gate control over the channel.<sup>2,3</sup> From a design perspective, devices that resemble nanowires with a very small cross-section are very promising due to their excellent characteristics and a potential for high-density integration. On the materials side, channels made of germanium, carbon nanotubes, and compound semiconductors are being investigated because of high carrier mobilities. Their science and technology have also attracted considerable attention by companies as they have shown to yield enhanced drive current and improvement of electrical performances in nanotransistors.<sup>4-6</sup>

Besides the issue of controlling short-channel effects, modern devices pose other challenges such as the formation of ultrasharp source and drain junctions. At very short channel

length, extremely high doping concentration gradients are needed to form p-n junctions. This results in increasing the cost and the complexity of the fabrication process. Junctionless nanowire transistors (JNTs) are heavily doped gated resistors made using thin  $N^+$  or  $P^+$  semiconductor nanowires and provide full CMOS functionality. The fabrication processes of JNTs are much simpler than in conventional CMOS devices due to the fact that these devices do not need the formation of extremely abrupt source and drain junctions. The main key in the fabrication of JNTs is that the channel region has to be narrow and thin enough to allow for full depletion of carriers to turn off the device.<sup>7</sup>

In JNTs, the conduction mechanism is based on the propagation of most carriers through the bulk of the channel rather than in surface channel.<sup>8</sup> Atomic-scale simulations have confirmed the scalability of JNTs down to sub-5 nm dimensions.<sup>9</sup> Several recent publications on the characterization of JNTs and comparison of these devices with conventional IM devices can be found in the literature.<sup>10-18</sup> Germanium inversion-mode (IM) devices have been previously investigated<sup>19,20</sup> but no quantum mechanical study on the performance comparison of germanium and silicon JNTs has been reported. In this paper, using 3D ballistic quantum mechanical simulations we investigate the effect of different channel materials and orientations, namely,  $\langle 100 \rangle$ - or  $\langle 110 \rangle$ -oriented Ge and Si wires on a (010)-wafer, on the short channel characteristics of N-channel JNTs and compare them with the characteristics of conventional IM nanowire-based FETs. This comprehensive analysis allows us to explain the physical origin of the superior short channel behavior of JNTs and identify the materials properties that affect device performance.

In Sec. II, the device structures and parameters which have been used in the simulations are discussed. Section III introduces the simulation methodology followed by the

presentation of the results in Sec. IV. We conclude with few summary remarks.

## II. DEVICE STRUCTURES AND PARAMETERS

We consider n-type Si and Ge nanowires with channel orientations of  $\langle 100 \rangle$  and  $\langle 110 \rangle$  are made on (010)-oriented wafers. Figures 1(a) and 1(b) show a schematic view of GAA junctionless and inversion-mode nanowire transistors with a square cross-section as well as the doping profile in the longitudinal direction for both devices. The square cross-sections have dimensions of  $W_{Si/Ge} = T_{Si/Ge}$ , where  $T_{Si/Ge}$  ranges from 6 nm down to 4 nm. Gate lengths range from 12 nm to 8 nm and uniform doping concentrations throughout the channel and source/drain regions of the devices have been used. In IM transistors, the source and drain junctions are assumed to be abrupt, and doping concentrations in the source/drain regions and channel are  $1 \times 10^{20} \text{ cm}^{-3}$  and  $1 \times 10^{15} \text{ cm}^{-3}$ , respectively. The doping concentration in JNTs is  $1 \times 10^{19} \text{ cm}^{-3}$  throughout the device. The effective oxide thickness (EOT) is equal to 1 nm for all devices. The supply voltage ( $V_{dd}$ ) is equal to 0.65 V and by tuning the gate workfunction, all transistors are designed to have the same off-current of  $10 \text{ pA}/\mu\text{m}$  which is suitable for low standby power technologies.<sup>1</sup>

The band alignments of the various direct and indirect gaps of Si and Ge at room temperature are shown in Figure 2. In bulk semiconductor devices, valleys which are lower in energy have the largest contribution to transport. As it can be seen in this figure, in bulk silicon, the X-valleys are energetically much lower than the other valleys and, as a result, most of the electrons in the conduction band populate the X-valleys; other valleys can be ignored in the transport simulations. In small dimension

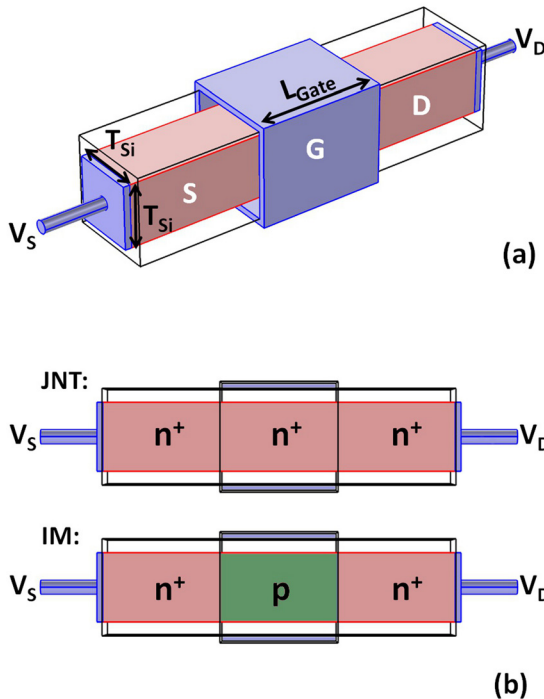


FIG. 1. (a) Bird eye's view of a junctionless and IM nanowire MOSFETs and (b) doping profile in the longitudinal direction in JNTs and IM devices.

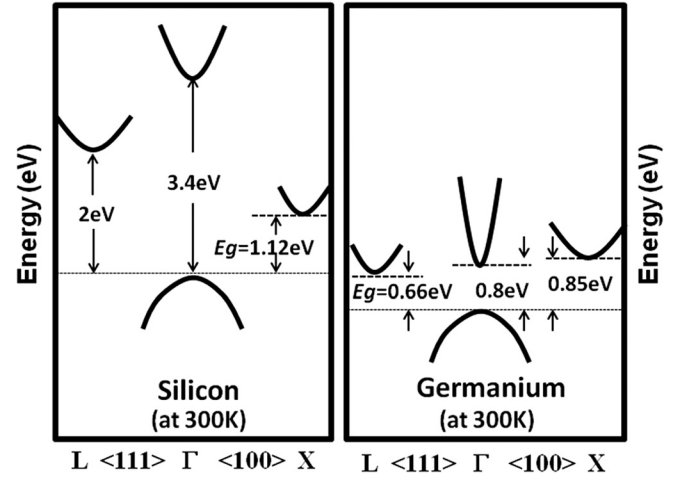


FIG. 2. The various direct and indirect gap values used in the simulations of Si and Ge devices.

nanowires, however, quantum confinement becomes important, and effective masses perpendicular to the wire axis play an important role in determining the valleys that form the energetically lowest subbands. Table I shows the effective masses used in the simulations for Si and Ge nanowires with different crystal orientations. These are expressed through the transverse and longitudinal effective masses used for the X- and L-valleys in bulk Si and Ge as shown in Table II. The  $\Gamma$ -valley in Ge is non-degenerate and has an isotropic effective mass ( $0.038 \times m_0$ , where  $m_0$  is the free electron mass). Using the above band structures and effective masses, we investigate the effect of different wire materials and orientations on the subthreshold swing, DIBL, source-to-drain tunneling and  $I_{on}/I_{off}$  ratio in JNTs and compare them with those of IM devices.

The effect of band-to-band tunneling (BTBT) has not been considered in the simulations as the applied supply voltage is assumed to be 0.65 V which is smaller than the band gap of germanium and silicon. In fact, due to the quantization

TABLE I. Effective masses and subband degeneracy for  $\langle 100 \rangle$ - and  $\langle 110 \rangle$ -oriented semiconductor nanowires. The wafer orientation is (010).

Wire	Valley	$m_{yy}$	$m_{zz}$	$m_{yz}$	$m_x$	Deg
$\langle 100 \rangle$	X	$m_t$	$m_t$	$inf$	$m_l$	2
		$m_l$	$m_t$	$inf$	$m_t$	2
		$m_t$	$m_l$	$inf$	$m_t$	2
	L	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t - m_l}$	$\frac{2m_t + m_l}{3}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_l - m_t}$	$\frac{2m_t + m_l}{3}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{m_l - m_t}$	$\frac{2m_t + m_l}{3}$	2
$\langle 110 \rangle$	X	$m_l$	$m_t$	$inf$	$m_t$	2
		$\frac{2m_l m_t}{m_t + m_l}$	$m_t$	$inf$	$\frac{m_t + m_l}{2}$	2
	L	$m_t$	$\frac{2m_l m_t}{m_t + m_l}$	$inf$	$\frac{m_t + m_l}{2}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{m_t + m_l}{3m_l m_t}$	$\frac{3m_l m_t}{m_t + m_l}$	$\frac{2}{m_t}$	1
		$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{2m_t + m_l}{2m_t + m_l}$	$\frac{3m_l m_t}{\sqrt{2}(m_t - m_l)}$	$\frac{2}{m_t}$	1
	L	$\frac{3m_l m_t}{m_t + 2m_l}$	$\frac{3m_l m_t}{2m_t + m_l}$	$\frac{3m_l m_t}{\sqrt{2}(m_t - m_l)}$	$m_t$	1
		$\frac{3m_l m_t}{m_t + 2m_l}$	$m_t$	$inf$	$\frac{m_t + 2m_l}{3}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$m_t$	$inf$	$\frac{m_t + 2m_l}{3}$	2
	L	$\frac{3m_l m_t}{m_t + 2m_l}$	$m_t$	$inf$	$\frac{m_t + 2m_l}{3}$	2
		$\frac{3m_l m_t}{m_t + 2m_l}$	$m_t$	$inf$	$\frac{m_t + 2m_l}{3}$	2

TABLE II. Transverse and longitudinal effective masses for the X- and L-valleys in bulk Si and Ge used in our simulations.

	Valley	$m_t/m_0$	$m_l/m_0$
Si	X	0.98	0.19
	L	1.7	0.12
Ge	X	0.95	0.2
	L	1.64	0.082

effect the band gap in our devices becomes even larger compared to bulk devices as the channel thickness shrinks. As a result, the BTBT rate decreases.<sup>21</sup> Using larger supply voltages could increase the leakage current and degrade the off-state performance of the devices.<sup>22</sup> A brief introduction of the simulation method that takes into account of the effective masses for arbitrarily oriented wires is discussed in Sec. III.

### III. SIMULATION METHODOLOGY

Simulations were carried out using a fully self-consistent 3D quantum mechanical simulator that uses the effective-mass approximation. Calculation of band structures in Si and Ge nanowires using tight-binding simulations has shown that for devices with a cross-section larger than 4 nm, the change in curvature of electronic bands along transport directions is negligible, and as a result the parabolic approximation is valid and accurate.<sup>20,23</sup> Here, the quantum transport is calculated using the non-equilibrium Green's functions (NEGF) formalism<sup>24</sup> expressed in the mode space (MS) approach.<sup>25</sup> The 3D Poisson equation and 3D Schrödinger equation with open boundary conditions are solved self-consistently. COMSOL MULTIPHYSICS<sup>26</sup> is used to solve the Poisson equation and obtain the electrostatic potential in the device. Using the MS approach, the quantum confinement and transport can be separated to solve the Schrödinger equation in a computationally efficient manner. As a result of this procedure, the 3D Schrödinger equation is decomposed into: (1) a 2D Schrödinger equation which is solved with closed boundary condition in different cross-sections of the nanowire to obtain the wave functions and the electron subbands along the device and (2) a 1D transport equation which is solved using NEGF formalism along source-drain axis to obtain the electron charge density.

The 3D full stationary Schrödinger equation is given by

$$H_{3D}\Psi(x, y, z) = E\Psi(x, y, z), \quad (1)$$

where  $H_{3D}$  is the 3D device Hamiltonian,  $E$  is the energy, and  $\Psi(x, y, z)$  is the 3D wavefunction. In arbitrarily oriented wires, the inverse effective-mass tensor has non-diagonal terms which are due to misalignment of the iso-energy surfaces of the conduction bands with the device coordinate system. Assuming an ellipsoidal parabolic energy band,  $H_{3D}$  is defined as

$$H_{3D} = -\frac{\hbar^2}{2} \left( \frac{1}{m_{xx}} \frac{\partial^2}{\partial x^2} + \frac{1}{m_{yy}} \frac{\partial^2}{\partial y^2} + \frac{1}{m_{zz}} \frac{\partial^2}{\partial z^2} + \frac{2}{m_{xy}} \frac{\partial^2}{\partial x \partial y} + \frac{2}{m_{yz}} \frac{\partial^2}{\partial y \partial z} + \frac{2}{m_{xz}} \frac{\partial^2}{\partial x \partial z} \right) + V(x, y, z), \quad (2)$$

where  $1/m_{ij}$  is the reciprocal effective mass tensor (EMT) in the device coordinate system and  $V(x, y, z)$  is the potential energy. Solving this equation is a computational challenge. By decoupling the associated energies along the confinement and transport directions, one can avoid having to solve the full 3D equation. This can be done using the method described in Ref. 27. By assuming constant confinement along the transport ( $x$ ) direction, the 3D wavefunction can be written as follows:

$$\Psi(x, y, z) = \phi(y, z)e^{ik_x x}, \quad (3)$$

where  $\phi$  and  $k_x$  are the wavefunction in the cross-section and the wavevector in the transport direction, respectively. By writing the transverse part of the wavefunction as follows:

$$\phi(y, z) = \varphi(y, z)e^{ik_x(\alpha y + \beta z)} \quad (4)$$

and choosing parameters  $\alpha$  and  $\beta$  in such a way to cancel the first order derivatives with respect to  $y$  and  $z$  in the 3D Schrödinger equation, we obtain the following equation:

$$-\frac{\hbar^2}{2} \left( \frac{1}{m_{yy}} \frac{\partial^2 \varphi}{\partial y^2} + \frac{1}{m_{zz}} \frac{\partial^2 \varphi}{\partial z^2} + \frac{2}{m_{yz}} \frac{\partial^2 \varphi}{\partial y \partial z} \right) + \left( \frac{\hbar^2 k_x^2}{2m_x} + V(y, z) - E \right) \varphi = 0, \quad (5)$$

where  $m_x$  is the effective mass in transport direction,  $1/m_{ij}$  is the reciprocal EMT in the device coordinate system,  $E$  is the charge-carrier energy, and  $V$  is the confinement potential energy. In this equation, the associated energies in the confined cross-section and in the channel direction ( $x$ ) are decoupled, which allows one to use the NEGF formalism<sup>24</sup> expressed within the MS approach.<sup>25</sup> The 2D Schrödinger equation to be solved for the confined cross-section at each point along the transport direction ( $x$ ) to yield the electron subbands energy levels and modes reads as

$$H_{2D}\Psi^n(y, z; x_i) = E_{sub}^n \Psi^n(y, z; x_i), \quad (6)$$

where

$$H_{2D} = -\frac{\hbar^2}{2} \left( \frac{1}{m_{yy}} \frac{\partial^2}{\partial y^2} + \frac{1}{m_{zz}} \frac{\partial^2}{\partial z^2} + \frac{2}{m_{yz}} \frac{\partial^2}{\partial y \partial z} \right) + V(y, z), \quad (7)$$

where  $E_{sub}^n$  is the subband energy level and  $\Psi^n(y, z; x_i)$  is the corresponding transversal wave function at each slice  $x = x_i$ . Finally, using the mode-space device Hamiltonian and assuming ballistic transport, the retarded Green's function ( $G$ ) of the active device is calculated using

$$G = [EI - H - \Sigma_1 - \Sigma_2]^{-1}, \quad (8)$$

where  $I$  is the identity matrix. The self-energy functions  $\Sigma_1$  and  $\Sigma_2$  account for the open boundary conditions.<sup>28</sup> Using the NEGF formalism and knowing the retarded Green's function then the electron density and current can be obtained.<sup>24,25</sup> Since just the first few subbands are essentially occupied by electron carriers and needed to be taken into



account in the simulations, computation time is significantly reduced.

To benchmark the different devices we use the subthreshold swing and DIBL as performance indicators. The subthreshold swing measures the rate of current increase with gate voltage below threshold and is expressed in millivolts of gate voltage per decade of drain current. It is defined as

$$SS = \frac{dV_G}{d(\log_{10} I_D)}, \quad (9)$$

which for a MOSFET yields

$$SS = n \frac{k_B T}{q} \ln(10) \quad (\text{mV/decade}). \quad (10)$$

Here,  $k_B$  is the Boltzmann constant,  $T$  is the temperature in Kelvin,  $q$  is the absolute value of the electron charge, and  $n$  is the body factor. The body factor presents the efficiency of the gate control over the channel potential and in the best case is equal to 1, which at room temperature ( $T = 300$  K) gives a value of  $SS = 59.6$  mV/decade.

Typically, the depletion regions created in the channel region because of the source/drain junctions decrease the

effective channel length and degrade the gate control over the channel region. The channel potential is no longer controlled just by the gate electrode but also depends on the distance between source and drain regions and the voltage applied to the drain. DIBL is defined as

$$DIBL = (V_{th}|_{V_{DS}=0.05V} - V_{th}|_{V_{DS}=0.65V}) / (0.65 - 0.05). \quad (11)$$

## IV. RESULTS AND DISCUSSION

Simulation results on the effect of channel dimension, orientation, and material and on the characteristics of JNTs and IM devices are presented in this section.

### A. Device characteristics

Figure 3 shows the impact of cross-section dimension on the subthreshold swing and DIBL of Si and Ge JNTs and IM devices. For a fixed gate length, the SS improves towards the ideal value of 59.6 mV/decade as the cross-section decreases for both types of devices. DIBL also decreases with increasing confinement. This is largely expected as the electrostatic control of channel charges by the gate improves

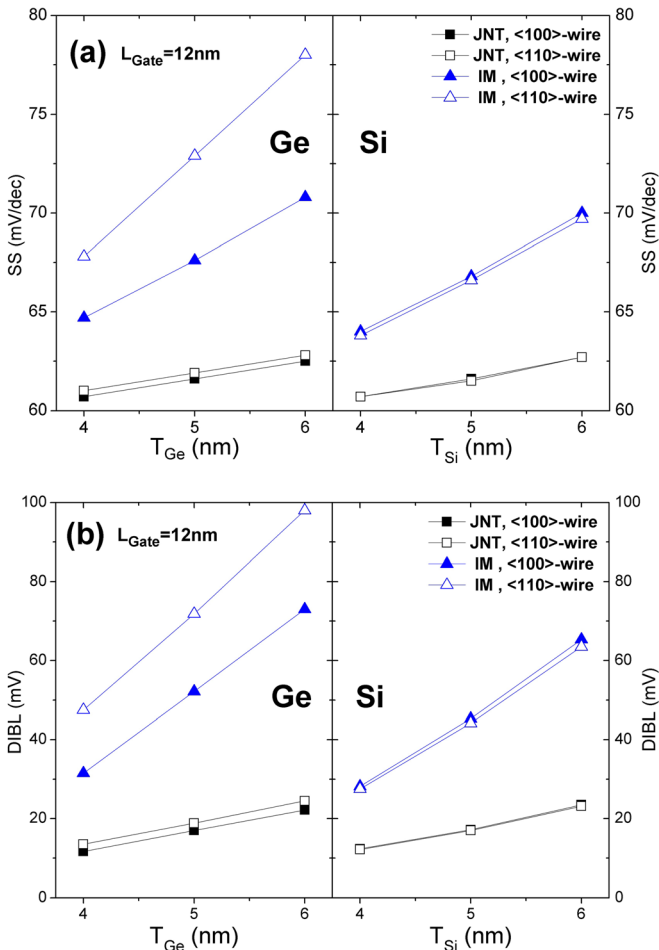


FIG. 3. Impact of the cross-section dimensions on (a) subthreshold swing and (b) DIBL in JNTs and IM devices with germanium and silicon nanowire channels.

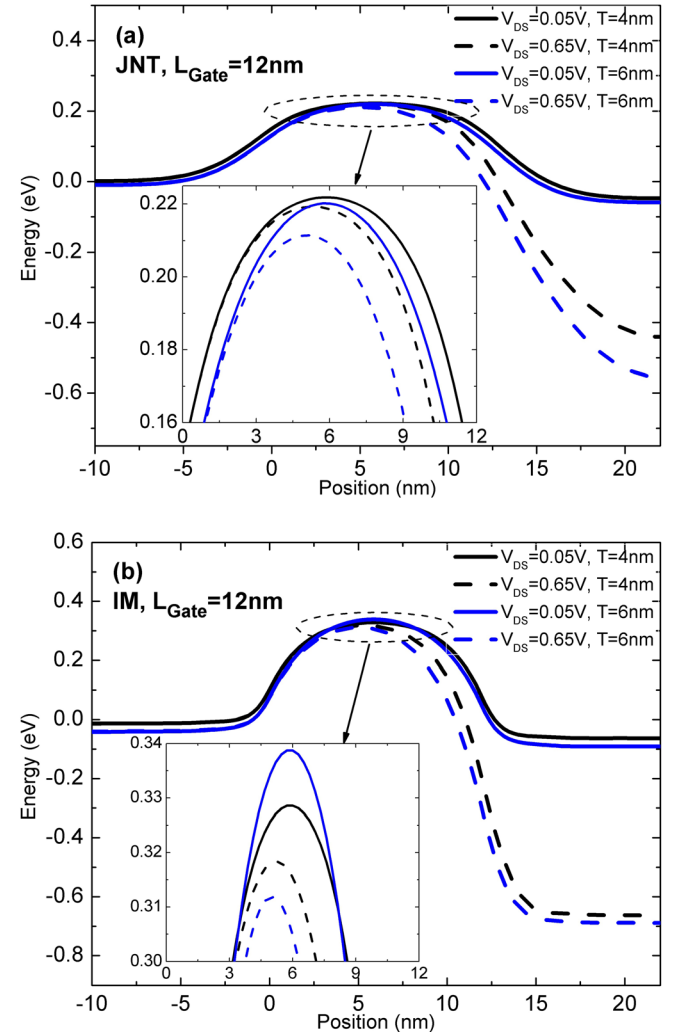


FIG. 4. Decrease of source-channel barrier due to increasing of drain voltage in (a) JNTs and (b) IM devices (Si <100>-oriented nanowires).

with smaller cross-sections. Figure 4 exemplifies the anticipated behaviour; a drop in the source-channel potential barrier with drain voltage is much larger in devices with larger cross-sections. In devices with  $T_{Ge} = 6$  nm, for instance, the subthreshold swings of  $\langle 100 \rangle$ - and  $\langle 110 \rangle$ - oriented wires in JNTs are 12% and 20% better than those of IM transistors, respectively. The respective DIBL is 70% and 75% lower. This is due to the presence of space-charge regions in the channel region of IM devices associated with the source and drain PN junctions and also the increase of the drain space-charge region with drain voltage which results in degradation of gate control over the channel charges in IM devices compared to JNTs. This and the varying sensitivity in orientation for the two different types of devices, that is, IM and JNTs, will be explained in more detail below.

Figure 5 gives a general comparison of drive current characteristics of JNTs and IM nanowire transistors for different wire materials and channel orientations for a gate length of 10 nm. JNTs exhibit a better  $I_{on}/I_{off}$  ratio in every case, for a supply voltage of  $V_{DD} = 0.65$  V. It can also be seen that  $\langle 110 \rangle$ -oriented IM germanium nanowires cannot be properly turned on at  $V_{gs} = V_{dd} = 0.65$  V and have a poor  $I_{on}/I_{off}$  ratio due to a large subthreshold swing. The degradation of the device characteristics in this case results from the effective mass tensor of the Ge channel which determines

the subband properties. There are three L-derived valleys for wires fabricated along the  $\langle 110 \rangle$  direction (see Table I). Those with higher effective masses along the confinement direction have the largest contribution to the total current since they are positioned lower in energy. On the other hand, their lower transport effective mass increases the source-to-drain tunneling, thereby, increasing the off-current. The details of the tunnelling current contribution to the total current are discussed in Sec. IV B.

For completeness, Figure 6 shows how SS and DIBL depend on varying the cross-section in short channel devices, that is, keeping the ratio of gate length to thickness equal to two. As anticipated, short channel effects result in a larger increase in the DIBL and subthreshold-swing degradation in IM nanowire transistors compared to JNTs. Also, whilst Ge JNTs characteristics are comparable to the Si JNTs devices the use of  $\langle 110 \rangle$ -oriented Ge as channel material in IM devices clearly yields the worse performance. An interplay between the larger effective gate length and the lower transport effective mass of the  $\langle 100 \rangle$  Si channel compared to the Ge counterpart yields very similar short-channel behaviour for both JNTs and IM devices made of these materials. Overall, Figure 6 shows that n-type Ge devices may at best be expected to perform equally well with their silicon counterparts.

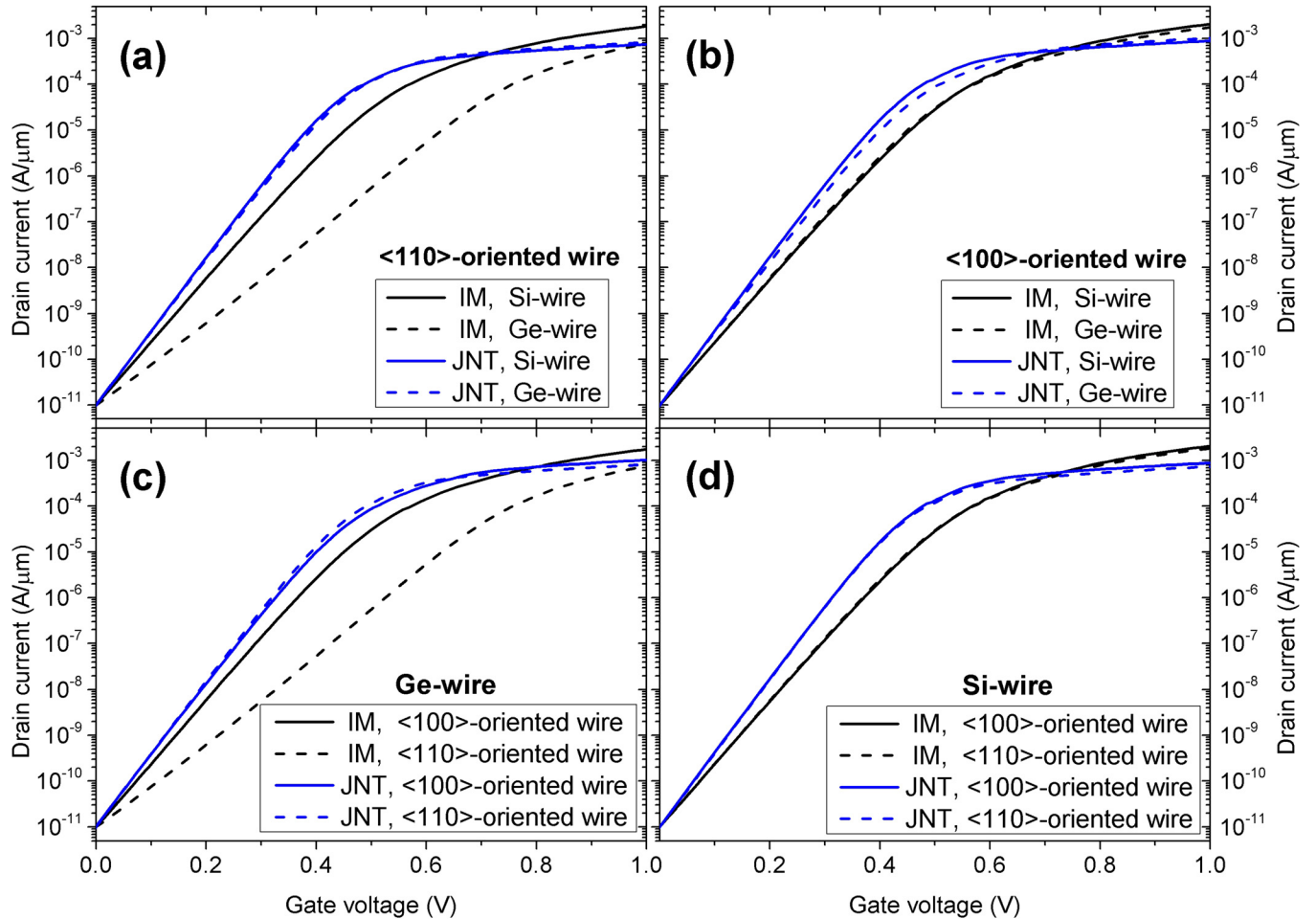


FIG. 5. Comparison of  $I_d$ - $V_{gs}$  for fixed wire orientation ((a) and (b)) and different channel materials ((c) and (d)) in JNTs and IM transistors ( $L_{gate} = 10$  nm, channel cross-section:  $5 \times 5$  nm<sup>2</sup>,  $V_{DS} = 0.65$  V).

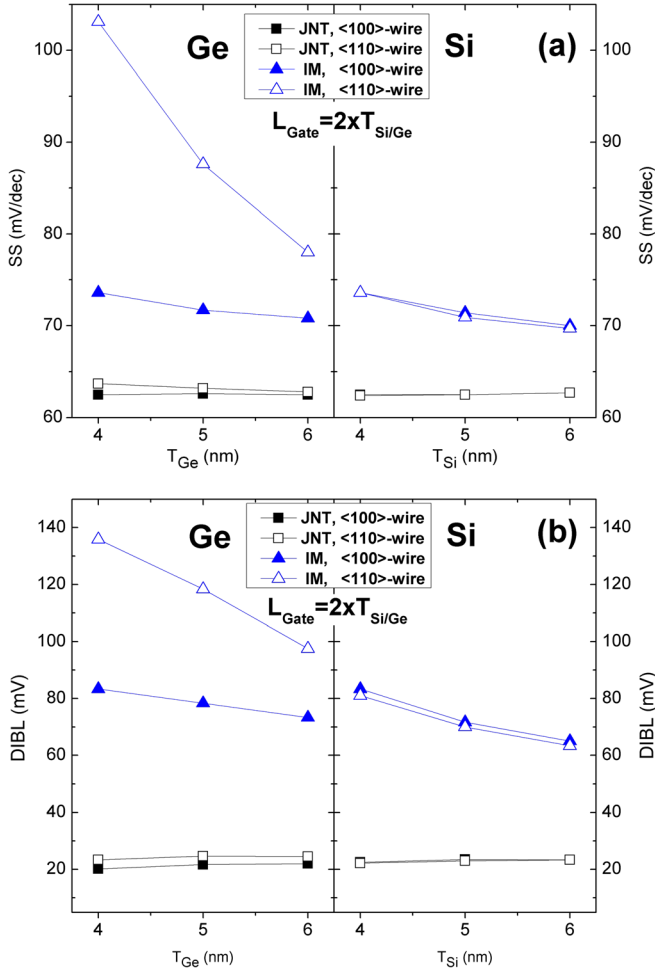


FIG. 6. Effect of wire channel material (Ge and Si), orientation ( $\langle 100 \rangle$  and  $\langle 110 \rangle$ ), and cross-section on (a) subthreshold swing and (b) DIBL in JNTs and IM transistors (the ratio of gate length to wire thickness is equal to two).

## B. Device physics

One reason for the worse short channel effect control in Ge nanowires than in Si devices can be explained by the concept of natural length ( $\lambda$ ). The natural length is a parameter which represents the extension of the electric field lines from the source and the drain into the channel region.<sup>29–31</sup> In gate-all-around devices with square cross-section, natural length is defined by the following expression:

$$\lambda = \sqrt{\frac{\epsilon_{\text{semicon}}}{4\epsilon_{\text{ox}}}} t_{\text{ox}} t_{\text{semicon}}, \quad (12)$$

where  $\epsilon_{\text{ox}}$  is the permittivity of the gate oxide,  $\epsilon_{\text{semicon}}$  is the permittivity of the wire material (Si or Ge),  $t_{\text{ox}}$  is the gate oxide thickness, and  $t_{\text{semicon}}$  is the nanowire thickness. The ratio of effective gate length to the natural length should be large enough for devices to be free of SCEs. According to this expression, short-channel effects can be minimized by: (1) decreasing the gate oxide thickness, (2) decreasing the nanowire thickness, (3) increasing the dielectric constant of the gate oxide material, and/or (4) decreasing the dielectric constant of the wire material. Since  $\epsilon_{\text{Si}} < \epsilon_{\text{Ge}}$  the natural length of Si nanowires is smaller than that of Ge nanowires ( $\lambda_{\text{Si}} = 0.86\lambda_{\text{Ge}}$ )

and, as a result, Ge nanowires are more affected by short channel effects for the same gate length and device parameters.

Another reason for the difference in SCE control between Si and Ge devices lies in the variation of the effective masses and, in particular, their effect in the tunnelling contribution to the total current. Figure 7 shows the contribution of source-drain tunneling current to the total current in the off state and in the on-state. As it can be seen in this figure, for both Si and Ge nanowires, source-to-drain tunneling in the subthreshold regime is much lower in JNTs than in IM devices. In the on-state, the source-to-drain tunneling is almost equal to zero in both Si and Ge JNTs, but not in IM devices. Moreover, the tunneling current is much larger in  $\langle 110 \rangle$ -oriented than in  $\langle 100 \rangle$ -oriented Ge nanowires. This is due to the small effective mass of the L-valleys ( $0.082 \times m_0$  along the transport direction), which carry the largest contribution to the total current. Within the  $\langle 100 \rangle$ -oriented Ge nanowires the transport effective mass is much larger ( $0.601 \times m_0$ ), yielding a lower tunneling current. The smaller tunneling current in JNT compared to the IM nanowire device in the subthreshold regime can be explained by the larger effective gate length of JNTs in the off-state. Figure 8 shows the profile of the first subband of Ge and Si JNTs and IM devices in both the off-state and the on-state. As it can be seen in this figure, when the JNT is in on-state there is no source/channel junction potential barrier, which virtually reduces the tunneling current to zero. As it is

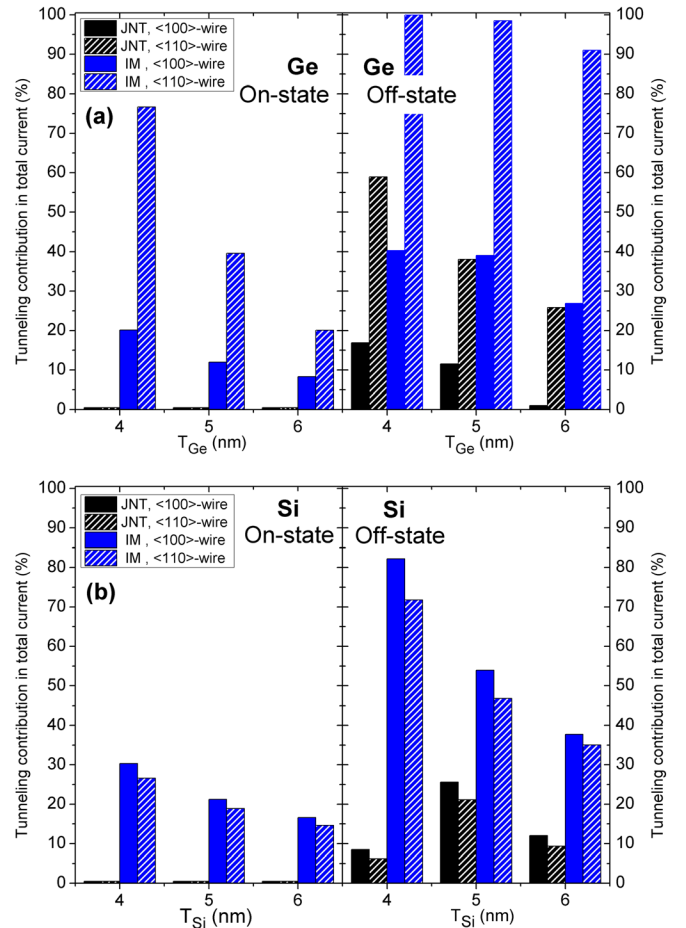


FIG. 7. Contribution of the source-to-drain tunneling current to the total current in the off- and the on-states for: (a) Ge and (b) Si.



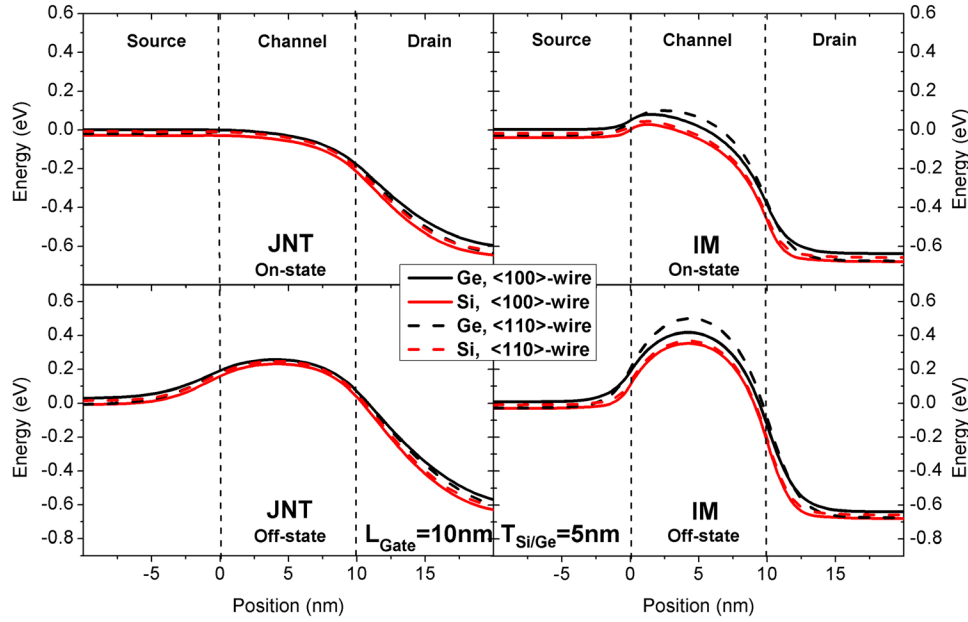


FIG. 8. Profile of the first subband in JNT and IM devices in both off-state and on-state regime for different nanowire materials and orientations ( $L_{gate} = 10$  nm,  $T_{semicond} = 5$  nm).

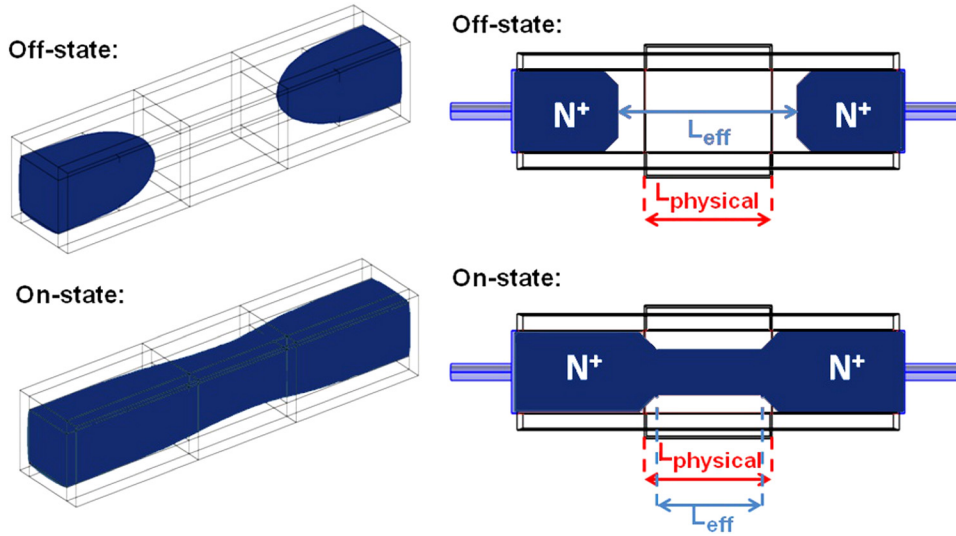


FIG. 9. Illustration of the effective gate length variation from the off-state to the on-state (right) in a JNT using the plot of charge carrier concentration (left). The dark areas are neutral (i.e., not depleted). The depleted region is transparent.

illustrated in Figure 8, the top of the potential barrier in the channel region is lower in the JNT than in the IM device in the off state. In addition, the potential barrier extends from the sides of the physical gate electrode into the source and drain regions, which produces an effective channel length longer than the physical gate length when the device is turned off. As a result, smaller tunneling current is found in JNTs than in IM nanowire transistors even in the off state.

JNTs have a larger effective gate length than the physical gate length ( $L_{eff} > L_{physical}$ ) in the off-state and a smaller effective gate length than the physical gate length ( $L_{eff} \leq L_{physical}$ ) in the on-state. This behavior justifies the highly improved short channel characteristics of JNTs.<sup>32,33</sup> A plot of charge carrier concentrations in the off- and on-states in a JNT illustrates the variation of effective gate length in Figure 9.

## V. CONCLUSION

The current characteristics, subthreshold swing, drain-induced barrier lowering, source-to-drain tunneling, and

$I_{on}/I_{off}$  ratio of inversion-mode and junctionless nanowire field-effect transistors are investigated in the ballistic transport regime using 3D quantum mechanical simulations within the framework of effective-mass theory for different wire materials (germanium and silicon), orientations ( $\langle 100 \rangle$  and  $\langle 110 \rangle$ ), and device dimensions. Our study shows that JNTs with Ge and Si as a channel material and with  $\langle 100 \rangle$ - and  $\langle 110 \rangle$ -oriented nanowires fabricated on (010)-wafers are more immune to short channel effects than conventional IM devices and present smaller subthreshold swing, less DIBL, lower source-to-drain tunneling, and a larger  $I_{on}/I_{off}$  ratio, which is attractive for low-power applications.

We also show that Ge IM devices along the  $\langle 110 \rangle$  direction have much poorer short-channel characteristics than their Si counterparts. In contrast, the material and orientation of the channel does not affect the device performance of JNTs considerably. This is traced back to the larger effective gate length that suppresses source-to-drain tunnelling. As a result, JNTs made of n-type Ge and Si nanowire channels

perform equally good despite the differences in the natural length and effective masses.

## ACKNOWLEDGMENTS

This work was supported by the Science Foundation Ireland Grant Nos. 05/IN/1888 and 10/IN.1/12992, and the European Commission through the SQWIRE project under Grant Agreement No. 257111. This work has also been enabled by the Programme for Research in Third-Level Institutions.

- <sup>1</sup>See <http://public.itrs.net/> for information about the International Technology Roadmap for Semiconductors, 2010.
- <sup>2</sup>J. P. Colinge, "Multi-gate SOI MOSFETs," *Microelectron. Eng.* **84**, 2071–2076 (2007).
- <sup>3</sup>N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "High-performance fully depleted silicon nanowire (diameter  $\leq 5$  nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.* **27**, 383–386 (2006).
- <sup>4</sup>K. Saraswat, C. O. Chui, T. Krishnamohan, D. Kim, A. Nayfeh, and A. Pethe, "High performance germanium MOSFETs," *Mater. Sci. Eng., B* **135**, 242–249 (2006).
- <sup>5</sup>K. C. Saraswat, C. O. Chui, T. Krishnamohan, A. Nayfeh, and P. McIntyre, "Ge based high performance nanoscale MOSFETs," *Microelectron. Eng.* **80**, 15–21 (2005).
- <sup>6</sup>R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-kappa/metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Lett.* **25**, 408–410 (2004).
- <sup>7</sup>J.-P. Colinge, C.-W. Lee, A. Afzal, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.* **5**, 225–229 (2010).
- <sup>8</sup>A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines," in *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European* (2010), pp. 357–360.
- <sup>9</sup>L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer, "Simulation of junctionless Si nanowire transistors with 3 nm gate length," *Appl. Phys. Lett.* **97**, 062105 (2010).
- <sup>10</sup>C.-W. Lee, I. Ferain, A. Afzal, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid-State Electron.* **54**, 97–103 (2010).
- <sup>11</sup>J.-P. Raskin, J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, R. Yan, P. Razavi, and R. Yu, "Mobility improvement in nanowire junctionless transistors by uniaxial strain," *Appl. Phys. Lett.* **97**, 042114 (2010).
- <sup>12</sup>J.-T. Park, J. Y. Kim, C.-W. Lee, and J.-P. Colinge, "Low-temperature conductance oscillations in junctionless nanowire transistors," *Appl. Phys. Lett.* **97**, 172101 (2010).
- <sup>13</sup>D. Jang, J. W. Lee, C.-W. Lee, J.-P. Colinge, L. Montes, J. I. Lee, G. T. Kim, and G. Ghibaudo, "Low-frequency noise in junctionless multigate transistors," *Appl. Phys. Lett.* **98**, 133502 (2011).
- <sup>14</sup>J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Appl. Phys. Lett.* **96**, 073510 (2010).
- <sup>15</sup>C.-W. Lee, A. Borne, I. Ferain, A. Afzal, R. Yan, N. Dehdashti Akhavan, P. Razavi, and J. P. Colinge, "High-temperature performance of silicon junctionless MOSFETs," *IEEE Trans. Electron Devices* **57**, 620–625 (2010).
- <sup>16</sup>R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, L. Chi-Woo, I. Ferain, N. D. Akhavan, Y. Ran, P. Razavi, Y. Ran, A. Kranti, and J. Colinge, "Junctionless multiple-gate transistors for analog applications," *IEEE Trans. Electron Devices* **58**, 2511–2519 (2011).
- <sup>17</sup>C. Seongjae, K. Kyung Rok, P. Byung-Gook, and K. In Man, "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs," *IEEE Trans. Electron Devices* **58**, 1388–1396 (2011).
- <sup>18</sup>P. Razavi, N. D-Akhavan, R. Yu, G. Fagas, I. Ferain, and J.-P. Colinge, "Investigation of short-channel effects in junctionless nanowire transistors," paper presented at the Proceedings of the International Conference Solid States Devices and Materials (SSDM), 2011.
- <sup>19</sup>M. Bescond, N. Cavassilas, K. Kalna, K. Nehari, L. Raymond, J. L. Autran, M. Lannoo, and A. Asenov, "Ballistic transport in Si, Ge, and GaAs nanowire MOSFETs," *IEEE Int. Tech. Dig. - Int. Electron Devices Meet.* **2005**, 526–529.
- <sup>20</sup>W. Jing, A. Rahman, G. Klimeck, and M. Lundstrom, "Bandstructure and orientation effects in ballistic Si and Ge nanowire FETs," *IEEE Int. Tech. Dig. - Int. Electron Devices Meet.* **2005**, 4 and 533.
- <sup>21</sup>D. Kim, T. Krishnamohan, Y. Nishi, and K. C. Saraswat, "Band to band tunneling limited off state current in ultra-thin body double gate FETs with high mobility materials: III-V, Ge and strained Si/Ge," in *2006 International Conference on Simulation of Semiconductor Processes and Devices* (2006), pp. 389–392.
- <sup>22</sup>S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. M. Murali, S. Ganguly, and A. Kottantharayil, "Effect of band-to-band tunneling on junctionless transistors," *IEEE Trans. Electron Devices* **59**, 1023–1029 (2012).
- <sup>23</sup>K. Nehari, N. Cavassilas, J. L. Autran, M. Bescond, D. Munteanu, and M. Lannoo, "Influence of band structure on electron ballistic transport in silicon nanowire MOSFETs: An atomistic study," *Solid-State Electron.* **50**, 716–721 (2006).
- <sup>24</sup>S. Datta, "Nanoscale device modeling: The Green's function method," *Superlattices Microstruct.* **28**, 253–278 (2000).
- <sup>25</sup>J. Wang, E. Polizzi, and M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation," *J. Appl. Phys.* **96**, 2192–2203 (2004).
- <sup>26</sup>See <http://comsol.com> for information about the Comsol Multiphysics Software.
- <sup>27</sup>M. Bescond, N. Cavassilas, and M. Lannoo, "Effective-mass approach for n-type semiconductor nanowire MOSFETs arbitrarily oriented," *Nanotechnology* **18**, 255201 (2007).
- <sup>28</sup>S. Datta, *Quantum Transport: Atom to Transistor* (Cambridge University Press, 2005).
- <sup>29</sup>R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices* **39**, 1704–1710 (1992).
- <sup>30</sup>C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid-State Electron.* **51**, 505–510 (2007).
- <sup>31</sup>J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.* **48**, 897–905 (2004).
- <sup>32</sup>J.-P. Colinge, A. Kranti, R. Yan, I. Ferain, N. D. Akhavan, P. Razavi, C.-W. Lee, R. Yu, and C. Colinge, "A Simulation comparison between junctionless and inversion-mode MuGFETs," *ECS Trans.* **35**, 63–72 (2011).
- <sup>33</sup>P. Chan-Hoon, K. Myung-Dong, K. Ki-Hyun, S. Chang-Woo, B. Chang Ki, J. Yoon-Ha, and L. Jeong-Soo, "Comparative study of fabricated junctionless and inversion-mode nanowire FETs," in *2011 69th Annual Device Research Conference (DRC)* (2011), pp. 179–180.