1-to-*N* Ring Power Combiners With Common Delta Ports

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***Abstract*— In this paper, we present a new 1-to-N way ring combiner that is an adaptation of the ring-hybrid (rat-race) structure. We present the general design guidelines for N-way planar ring combiners based on theoretical analysis of the structures. The proposed 1-to-N way ring structure offers a compact, planar layout that includes a single common delta port. This is beneficial to applications where power monitoring, calibration, or energy recycling can be leveraged. It offers similar loss to other N-way structures. To demonstrate the combiners operation, we present completely passive structures and structures with embedded power amplifiers for 4- and 6-way variants. The designs are optimized for operation in the 5–6 GHz unlicensed bands. The passive 4- and 6-way combiners achieve IL of 1.3 and 1 dB, respectively, with associated port isolations of <-30 dB. The combiners with embedded amplifiers show similar performance and are validated using modulated signals and demonstrate good measured linearity when combining up to 6 amplifiers for output powers >1 W.**

***Index Terms*— Power combiner, power divider, high power amplifier, rat-race combiner, ring-hybrid combiner.**

I. Introduction

COMBINING and dividing circuits are a widespread practice in RF and microwave circuits at both the printed circuit board (PCB) and monolithic microwave IC (MMIC) level. Combiners are especially useful in power amplifier (PA) designs where several lower power PAs can be combined to yield a higher output power, at the expense of extra area and reduction in efficiency due to insertion loss (IL) in the combiner. Hence combiners must operate with low insertion loss to maximize efficiency and should offer high port-to-port isolation and minimal mismatch loss to maximize linearity.

Power combiners are used to combine several power amplifiers [1]–[4], signals from an antenna array [5], or modulating signals in an outphasing amplifier [6]–[8]. Particularly, multi-way combiners are of recent interest, owing to their potential to boost output power and efficiency [9]–[11]. Combiner designs have relied heavily on the both transmission line (TL) and lumped element implementations of the original Wilkinson divider/combiner (WDC) [12]–[14]. This owes to the WDC's relatively low insertion loss (IL), good port matching and high port-to-port isolation. Additionally, Lange couplers have been used in travelling wave configurations [15] and branchline coupler topologies [16] are popular because they offer increased port isolation when compared to WDC based approaches. However, this comes at the expense of reduced bandwidth, an increase in layout area and/or IL. Lange couplers also require an additional connection between coupled lines via wirebonding or airbridges.

WDC, Lange and branchline couplers require ladder structures, radial structures [17] or other cumbersome layouts [12] to realize more than 2-way power combining. In RFICs/MMICs, lumped element transformers are possible, but require use of lossy spirals [18]. In ladder form, each step of the ladder requires a separate isolation resistor to realize port-to-port isolation. An alternative to these combiner approaches are ring combiners (e.g., rat-race [19], multi-port ring [20], [21]), where all inputs/outputs to the combiner branch off of a TL ring. An advantage to ring-based geometries is that they can offer a single point for connection of the isolation resistor. Additionally, combination of more than two amplifiers can be accommodated by expanding the circumference of the ring to add more input/output ports. Ring based combiners can offer comparable layout area, IL, port-matching and port-isolation when compared to the branch and coupled line structures. However, they do operate with narrower bandwidths, and require added complexity in the feeding networks for the ports if used in standalone operation (e.g., with a single, common input). However, in MMICs or other highly integrated applications, the complexity of the feeding networks can be reduced by using signal processing to properly condition the phases of the input signals.

The common-delta port offers distinct advantages in multi-phase applications (e.g., outphasing, [11]), where the energy from deconstructive addition of input vectors is dumped into a load termination. The common-delta port can enable energy harvesting of this delta energy for efficiency enhancement at output power backoff (e.g., LINC [22]). Additionally, it allows for port monitoring for phase alignment calibrations [23], a common port for remote isolation resistors in MMIC applications [24], and switching operations for enhanced signal routing [25], [26].

In this paper, we present a new class of *N*-way ring combiners, as shown in Fig. 1, as well as operation theory and design guidelines that enable the reader to synthesize *N*-way ring combiners. It is noted that combiners and dividers are

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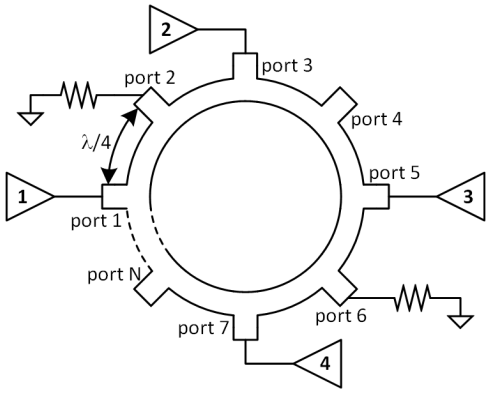

Fig. 1. Proposed N-way ring combiner.

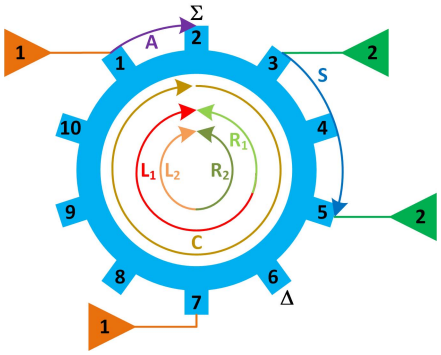

Fig. 2. Example 10-port ring combiner annotated with parameterized dimensions.

typically reciprocal; hence, in this paper, we focus on the power combining aspects of our proposed 1-to-N way ring combiner, but reciprocal operation as a divider is possible. The ring combiner is based on the ring hybrid combiner; however, it requires two distinct phase groups for proper operation. This paper is organized as follows. First, in section II design rules of the presented multi-port rings are provided for operation as combiners/dividers. Next, in section III, port placement and impedance rules are presented. In section IV, individual design examples are presented, followed by measurement results in section V. Finally, conclusions are presented in section VI.

II. N-Way Ring Combiner Design Rules

In the proposed 1-to-N way ring combiner there are two sets of input groups. One input group shares a common relative phase length from input to either output (e.g., Σ or Δ). The other input group has a 180° relative phase difference from input to either output port. With these port designations constructive summation is achieved at the desired output port (e.g., Σ) and de-constructively cancels at the other output port (e.g., Δ). We also note that in our derivations it is assumed that each amplifier group will contain the same number of amplifiers, to enforce symmetry between amplifier groups.

Though the structure works well as a power divider in reciprocal operation, we will focus our discussion and analysis on operation as a power combiner. In the following discussion, we develop a set of sizing rules for a 1-to-N way ring for combining N individual power amplifiers in two different input groups.

A. Scalable 1-to-N Way Ring Combiner Rules

A set of sizing rules for the proposed 1-to-N way ring combiners is now developed, noting that the rules derived are a superset of prior demonstrated ring combiners [20], [21]. The 1-to-N way ring combiner consists of amplifiers in two different phase groups. Relative signal phase at each input is set to either 0° or 180° , depending on the desired output port assignment. The proper input phase of each group can be created using either lumped elements (e.g., polyphase circuits), distributed elements (e.g., delay lines) or using signal processing. A generic 10-port ring is shown in Fig. 2. The circumference of the ring is given by C, while the input port to output port spacing is given by A. The spacing between two amplifiers in one group is given by S. It is noted that signals can propagate around the ring in a clockwise or counterclockwise direction; either path should have the same relative phase delay.

B. Input-to-Input and Output-to-Output Spacing Rules

Rules for input-to-input spacing in an N-way ring combiner can be derived as follows. First, the spacing can be derived as a function of a counter-clockwise or clockwise trip around the ring from one input to another input (e.g. port 3 to port 5), as shown by S in Fig. 2. The figure shows counter-clockwise and clockwise propogation from the input port to the antenna port for amplifiers in group 1 and 2. For instance, R_1 (R_2) represents a counter-clockwise trip from port 5 (port 7) to the output port, port 2. L_1 (L_2) shows a clockwise trip from port 5 (port 7) to the output port, port 2. The total circumference (C) for the combination of paths for each input port to the output port is equal and shown to be the sum of the counter-clockwise and clockwise trips:

$$C = R_1 + L_1 = R_2 + L_2 \tag{1}$$

In-phase signal combination occurs at the output port on the first pass around the ring when the following is true:

$$R_1 = L_1 + n\lambda, \tag{2}$$

$$R_2 = L_2 + m\lambda, \tag{3}$$

where n and m are integers representing the number of sections in the path from an individual input to the output for the clockwise and counter-clockwise directions, respectively.

Solving for the input-to-input spacing (S, Fig. 2) for any combination of L_1 and L_2, is performed as follows:

$$S = L_2 - L_1, \tag{4}$$

Substituting (2) and (3) into (1) yields:

$$L_2 - L_1 = \frac{(n-m)\lambda}{2} \tag{5}$$

Here, we substitute x for n-m. x is an integer representing the difference in the number of sections in between the counter-clockwise and clockwise paths. Hence the spacing is defined geometrically by the following:

$$S = \frac{x\lambda}{2}. \tag{6}$$

Where x is any non-zero positive/negative integer. A negative integer means a counter-clockwise propagating signal, while a positive integer means a clockwise propagating signal. Hence the spacing between ports must be an integer multiple of a half wavelength. This port spacing achieves isolation between input port pairs by creating an out-of-phase null from one port to another.

A similar requirement satisfies the spacing between the two output ports, Σ and Δ (e.g., Fig. 2, ports 2 and 6, respectively). Because of the out-of-phase null created by this half-wavelength spacing, undesirable loading on the ring that can be created by variations of the parasitic loading at each port due to process, voltage and temperature (PVT) variations is minimized.

C. Input-to-Output Spacing Rules

Nulls are established to occur with half-wavelength periodicity around the ring, maxima occur halfway between nulls. To achieve maximum power combination output ports should be located at these maxima, relative to the input port; hence the spacing A, from input-to-output is given by the following:

$$A = \lambda/4 + y\lambda/2. \tag{7}$$

The variable y is any positive/negative integer or zero. Negative integers represent propagation in the counter-clockwise direction and positive integers represent propagation in the clockwise direction.

Minimum spacing between any port is now established to be a quarter wavelength. The number and location of the inputs and outputs for operation is set by application specific requirements.

D. Number of Ports Required for 1-to-N Way Combining

The proposed ring combiners offer a key feature in that they have a single summation port and a single delta port. Hence any ring combiner requires a minimum of 2 ports for outputs. Using the spacing rules derived for input-to-input/output-to-output (e.g., S) and the input-to-output spacing rules (e.g., A) dictates that each amplifier placed at an input requires a minimum equivalent spacing $2A$. It can be shown that the minimum number of ports, P, required to combine N amplifiers in the proposed ring combiner is given by the following:

$$P = 2 \cdot N + 2. \tag{8}$$

The addend of 2 is due to the required output ports. It should be noted that not all ports are populated in a 1-to-N way ring combiner, and those that are not populated are left open to reduce the loading on the ring. It should also be noted that equation (8) simply sets a lower bound for the number of ports that are required; more ports can be added to the ring if desired. Cases where this may be desirable are to allow on-the-fly replacement of amplifier components that fail, increasing mean-time-to-failure at the expense of a large ring size and increase in insertion loss. Additionally, extra ports can be added if discrete power control is required. In such a scheme, amplifiers could be enabled/disabled as the output power requirements change.

E. Ring Circumference

The ring circumference can be determined by the total number of ports that are required for a 1-to-N way combiner, noting that all ports must be separated by a spacing of $\lambda/4$. The ring circumference is then given by the following:

$$C = P \cdot \frac{\lambda}{4}. \tag{9}$$

Substituting (8) into (9) yields the amplifier circumference for 1-to-N way combining to be given in terms of the number of combined inputs by:

$$C = (N+1) \cdot \frac{\lambda}{2}. \tag{10}$$

As was previously noted, an even number of amplifiers is preferred, but N is not expressly limited to be even. It is noted that the traditional Rat-Race coupler [19], or ring hybrid is a special case of this 1-to-N way ring hybrid, where $N = 2$. The Rat-Race coupler utilizes only four of the possible six ports based on quarter-wavelength spacing around its circumference.

III. General N-way Ring Combiner Design Procedure

A. Select Ring Circumference

The ring circumference is now defined based on the number of amplifiers to be combined. Assigning the first input port as port 1, the above equations are only satisfied for inputs into odd-numbered ports. Likewise, outputs will only occur at even numbered ports. Any unused ports are typically left unterminated to reduce parasitic loading effects on the ring. However, the unused ports can be used if reconfigurability is desired.

Ring circumference is dictated by the total number of amplifiers to be combined and the operation frequency, f_0. The circumference of the N-way combiner is thus given by the following:

$$C = (N+1) \cdot \frac{c}{2f_0\sqrt{\varepsilon_r}}, \tag{11}$$

where c is the speed of light in a vacuum and ε_{r} is the relative permittivity of the propagation medium (e.g., dielectric constant of the PCB or substrate).

B. Select Input and Output Ports

Considering the input port spacing (S) and input-to-output port spacing (A), the available input and output ports are alternated around the ring, with a separation of $\lambda/4$ between potential inputs and potential outputs. Typically, the Σ and Δ output ports are chosen to be nearly opposite from one another across the ring, as it is easier to provide symmetry with such a configuration, though this is not a necessary condition for operation. Symmetry allows for more straight forward even/odd mode analysis to determine S-parameters easier to perform, as it enables easier reduction of the even-/ odd-mode circuits.

Due to the number of ports, many valid designs are possible for an N-way combiner. We attempt to provide one such design guideline that provides symmetry between inputs

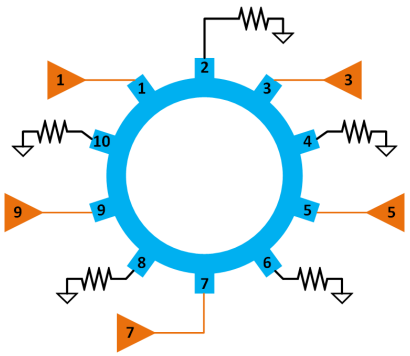

Fig. 3. 10-port ring combiner schematic.

TABLE I
10-PORT RELATIVE PORT PHASES

		Ring Outputs				
		Port 2	Port 4	Port 6	Port 8	Port 10
Ring Inputs	Port 1	90°	270°	90°	270°	90°
	Port 3	90°	90°	270°	90°	270°
	Port 5	270°	90°	90°	270°	90°
	Port 7	90°	270°	90°	90°	270°
	Port 9	270°	90°	270°	90°	90°

and outputs. An example 10-port combiner that can be used as a 4-way combiner is shown in Fig. 3, with all possible inputs and outputs designated.

In combining, potential inputs (shown as amplifiers) are placed at odd numbered ports and potential outputs (shown as load resistors) are placed at even numbered ports. A relative phase table is composed that describes the relative phase difference from each odd-port (e.g., input) to each even port (e.g., output), as shown in Table I. We now discuss choosing ports for a 10-port ring that can accommodate a combination of 4 amplifiers in two input groups. Ports 2 and 6 of Fig. 3 are chosen as the two outputs (Σ and Δ, respectively), which is a choice that will enable symmetry in later analysis. These two columns are shaded in the table. As noted, inputs will only be placed at the odd numbered ports, meaning that there are five potential ports to choose for input; with symmetry being preferred, only four of the ports will be chosen.

We now present one option for port placements that is generalizable to a P-port design, though we note that there are many other designs/port location choices that would realize an N-way combiner. The choices that we propose lead to a symmetric design. In any N-way ring combiner design with an even number of ports there will always be a line of symmetry that can be drawn between ports $P-1$ and $P/2-1$. After the line of symmetry is found, the output ports are selected. The Σ port is placed at port $P/2-3$, while the Δ port is place at port $P-4$. Finally, the input ports are divided into groups A and B. Working above the line of symmetry, input group A will be placed at positions 1 to $P/2-4$ in even increments. Inputs in group B will always be placed at port $P/2-2$. In this way, there are always $N/2-1$ inputs in group A above the line of symmetry and one input in group B above

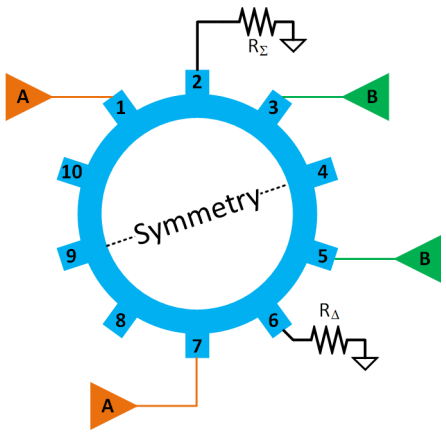

Fig. 4. 10-port ring combiner schematic after port selection.

the line of symmetry. Working below the line of symmetry, there will always be one amplifier in group A placed at port $P-3$. Amplifiers in group B will be placed at positions $P/2$ to $P-5$ in increments of 2. Note that all ports that are not assigned an input or output are left unterminated to minimize loading of the ring.

The designer should note that inputs in some groups may require a phase inversion, typically via a $\lambda/2$ length transmission line. For instance, in the example above, note that ports 3 and 5 are shifted by 180°. This requires that port 3 has an additional $\lambda/2$ phase length in its path. Such lines add size to the design, but using trombone structures, the size impact can be minimized. Addition of these extra TL segments and the size impact can be seen later in Fig. 15, Fig. 17, Fig. 20, and Fig. 22. It should also be noted that in applications where DSP is available to invert the inputs, there is no impact on the size of the ring to achieve proper input signal phasing.

C. Select Ring Transmission Line Impedance

The even and odd mode analysis for an N-way ring combiner begins by breaking the ring on a line of symmetry that includes two open ports. This is possible for all even N-way ring combiners with greater than 2 inputs. For instance, for the 4-way combiner (P=*10*) shown in Fig. 4, the combiner is broken between ports 4 and 9. Using the placement rules defined above, the Σ port is placed at port 2 and the Δ port is placed at port 6. Inputs in group A are assigned to ports 1 and 7, and inputs in group B are assigned to ports 3 and 5. The balance of the ports (e.g., 4, 8-10) are left open. Note that the Table I shows that port 5 has an extra 180° phase shift in its path to port 2 and hence it is inverted. Note also that the Σ and Δ ports can be exchanged if instead port 3 is inverted and port 5 is left non-inverted. This is an extension application of ring combiners.

An N-way even-mode half-circuit can be constructed, as shown in Fig. 5(top). The schematic can be simplified, noting that the open-circuit (O.C.) termination at the left side is transformed by a half-wavelength to an open circuit at the left-most input port. There must always be an even number of quarter-wave segments between input ports to satisfy the

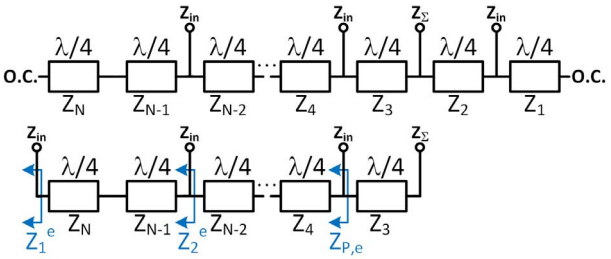

Fig. 5. (Top) even-mode analysis schematic for a 10-way ring combiner. (Bottom) even-mode analysis schematic, with component reduction accounting for $\lambda/4$ rotations of the open-circuit terminations.

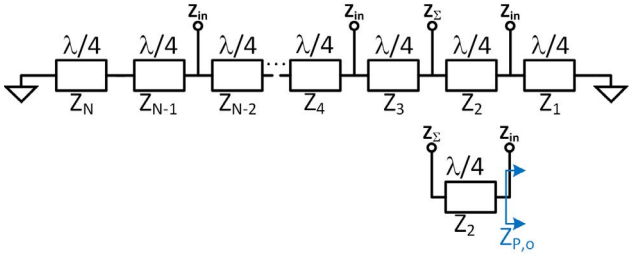

Fig. 6. (Top) odd-mode analysis schematic for a 10-way ring combiner. (Bottom) odd-mode analysis schematic, with component reduction accounting for $\lambda/4$ rotations of the short-circuit terminations.

spacing requirement, S. The open-circuit on the right side is transformed to a short circuit at the right-most input port and again becomes a short at the input closest to the Σ port. One final quarter-wave transform yields an open at the Σ port. It is noted that any number of ports can be added to the left or right side, if they are always separated by an even multiple of quarter-wave TL segments. The simplified even-mode circuit schematic is shown in Fig. 5(bottom).

In a similar fashion, the odd-mode circuit is constructed and shown in Fig. 6(top). The schematic can be simplified, noting that the short-circuit termination on the left side is transformed by an odd number of quarter-wave transmission lines to the Σ port, resulting in an open-circuit at the sum port (e.g., no load on the Σ port). The short-circuit termination on the right side is transformed by one quarter-wave TL, becoming an O.C. before it is transformed by an even-number of quarter-wave TLs to the input port closest to the sum port on the right side. This means that it does not load the input port. Again, it is noted that any number of ports can be added to the left or right side, if they are always separated by an even number of quarter-wave TLs. The simplified odd-mode circuit schematic is shown in Fig. 6(bottom).

With the simplified even- and odd-mode schematics derived for the N-way combiners, analysis of the impedances on the ring is straightforward. The even-mode input impedance Z_1^e (Fig. 5, bottom) of the left most input port rotates is transformed by a half-wavelength TL from the left-most port to equal the same impedance at Z_2^e (e.g., the next left-most port). This transformed impedance is combined in parallel with the impedance at the next left-most input port. The combined impedance then undergoes the same transformation X times, where X is the number of ports to the left of the output in the equivalent circuit. For an N-way combiner, where N is even and $N > 2$, X is given by:

$$X = \frac{N}{2} - 1. \tag{12}$$

The impedance looking into the input port adjacent to the output port, $Z_{P,e}$ is then given by the following:

$$Z_{P,e} = \frac{1}{\sum_{n=1}^{X} \frac{1}{Z_{in}}}, \tag{13}$$

where Z_{in} is the driving impedance of the port. It should be noted that the case of N=2 is a special case that is well analyzed [27]. The even-mode line impedance, Z_{even}, is found by applying a quarter-wave TL impedance transformation between $Z_{P,e}$ and Z_Σ. It is given by the geometric mean between the output port impedance, Z_Σ, and $Z_{P,e}$:

$$Z_{even} = \sqrt{Z_{P,e} Z_\Sigma}. \tag{14}$$

Derivation of the odd-mode characteristic impedance begins with analysis of Fig. 6(bottom). The short-circuit on the left-had side of the figure is transformed through X half-wavelength TLs before undergoing a single quarter-wave transform to an open-circuit at the Σ port. Hence, the left side of the circuit does not load the Σ port.

If the aforementioned port-placement rules are followed, there will always only be one input to the right side of the Σ port. The short-circuit undergoes one quarter-wave transform and hence does not load the input port to the right of the Σ port. Hence, the impedance $Z_{P,o}$ is equal to the port input impedance, Z_{in}. Similar to the even-mode case, the odd-mode line impedance is found by applying quarter-wave TL impedance transformation between $Z_{P,o}$ and Z_Σ. The odd-mode line impedance, Z_{odd}, is given by the geometric mean between the output port impedance, Z_Σ and $Z_{P,o}$:

$$Z_{odd} = \sqrt{Z_{P,o} Z_\Sigma}. \tag{15}$$

The $\lambda/4$ TL segments (Z_1 to Z_N) are designed to have a common impedance, Z_{ring}, selected to have an average impedance of Z_{even} and Z_{odd} to minimize impedance discontinuities around the ring:

$$Z_{ring} = \frac{Z_{even} Z_{odd}}{2}. \tag{16}$$

Shown in Fig. 7 is the designed characteristic impedance, Z_{ring}, of the ring as a function of the number of amplifiers that are combined (e.g., N), for the case where the input impedance matches the output impedance at 50 Ω (e.g., $Z_{in} = Z_{out} = 50\ \Omega$). The derivation matches ADS simulation results closely.

D. 1-to-N Ring Combiner Bandwidth

It is noted that there are no closed-form expressions for the bandwidths of ring-combiners, including the original rat-race (ring hybrid) combiner [19]. The frequency dependence of the ring combiner is based upon the frequency dependence of the transmission line lengths of which the ring is comprised.

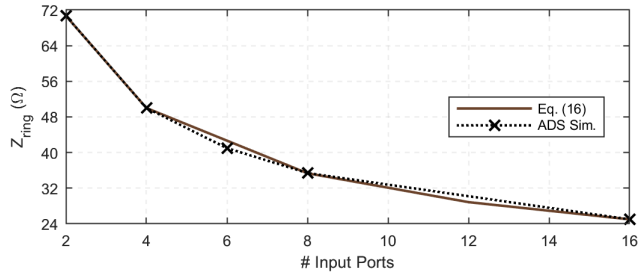

Fig. 7. N-way ring impedance equation vs. simulation results.

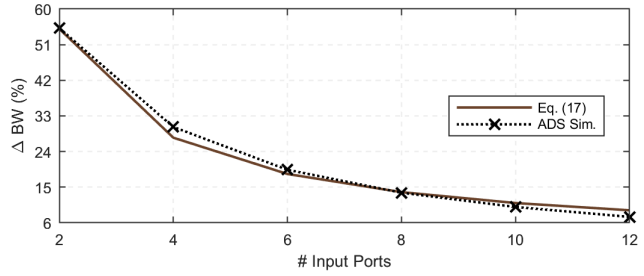

Fig. 8. 1-dB IL fractional bandwidth vs. number of input ports for 1-to-N way ring combiners.

As the number of ring sections are increased to yield higher combining ratios, N, the bandwidth of the ring is reduced.

In general, the bandwidth can be specified in terms of inserion loss (IL), reflection (Γ) or isolation. For the purposes of the proposed work, the bandwidth is specified as the 1-dB IL bandwidth of the combiner, as gain flatness is a desirable quality for most RF and microwave systems.

To quantify the effects of increasing the number of amplifiers, N, to be combined in 1-to-N way ring combiners, we simulate several ideal ring combiners in ADS. The 1-dB IL fractional bandwidth, ΔBW, is plotted as a function of N in Fig. 8. Though an exact expression cannot be derived for the 1-dB IL Δ BW, an estimate is given as follows:

$$\Delta_{1dB} = 110/N. \tag{17}$$

This estimate is also plotted in Fig. 8, and compares well with the ADS simulation results.

IV. Design Examples

A. 4-Way Ring Combiner Analysis

Fig. 9 shows a 4-way combiner implementation that allows for port switching. The splitters are used to allow for a single input for ease of measurement but are not expressly necessary in applications where signal processing can be used to create 6 individual inputs with the correct phase relationships. Note also that the extra circuitry comprised of the switch and 180° segments are not necessary; they are used to enable port switching of the Σ and Δ ports [20].

The port placement rules are given in Section III. Inputs in group A are labeled 1 and 6 and are connected to ports 1 and 7 of the 10-port combiner (Fig. 4). Inputs in group B are labeled 3 and 4 and are connected to ports 3 and 5 of the 10-port combiner. The outputs are labeled 2 and 5 and are connected to ports 2 and 6 of the 10-port combiner. The TL segments are designed to be a quarter-wavelength at the

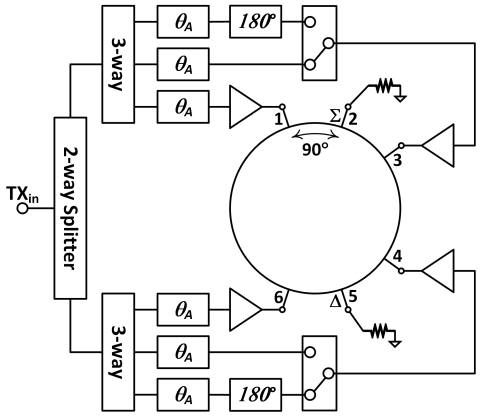

Fig. 9. Example 4-way ring combiner schematic.

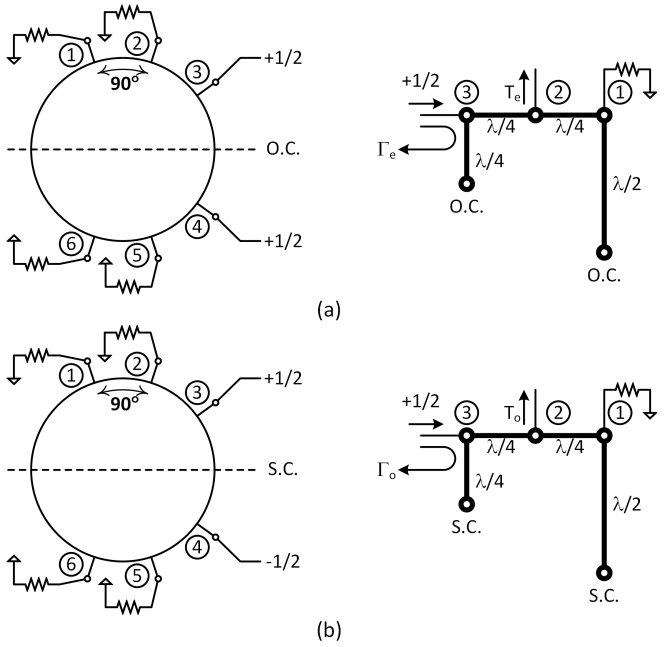

Fig. 10. (a) Even- and (b) odd-mode analysis schematics.

center frequency and the characteristic impedances are chosen according to (16) to be 50 Ω.

The 10-port combiner combines 4 amplifiers using only 6 of the available ports. The S-parameters of the ring combiner can be obtained by even- and odd-mode analysis of the half-circuits shown in Fig. 10, noting that the line of symmetry that exists through the center of the combiner allows ease of calculation due to symmetry. The example in Fig. 10 must be repeated at each of the symmetric ports in the combiner to obtain the full 6×6 S-parameter matrix. Derivations are omitted due to space constraints, but follow a similar method for the rat-race combiner [27]. The S-parameter matrix for the *effective* 6-port 4-way ring combiner is given as follows:

$$S = \frac{1}{2}\begin{pmatrix} -1 & -j & 0 & 0 & -j & 1 \\ -j & 0 & -j & j & 0 & -j \\ 0 & -j & -1 & -1 & j & 0 \\ 0 & j & -1 & -1 & -j & 0 \\ -j & 0 & j & -j & 0 & -j \\ 1 & -j & 0 & 0 & -j & -1 \end{pmatrix}. \tag{18}$$

Note that the S-parameters show non-zero reflection at ports 1, 3, 4 and 6 (e.g., the input ports). Mismatch only occurs if the signals of a common input group are not matched (e.g., have different impedances). If all ports are well matched, there is no port reflection. This is later validated with measurement results. Phase shifts result from the phasing relationships between ports found in Table I.

As is shown in Fig. 9, the 4-way ring combiner is driven by a single input, TX_{in}. The input is split using a 2-way splitter that uses a conventional Wilkinson divider. Each output of the Wilkinson splitter is followed by a modified 3-way T-junction divider that allows for port switching between the Σ and Δ port using single-pole, double-throw (SPDT) switch. The θ_A phase length is a multiple of a half-wavelength such that the path not selected by the SPDT switch is left open circuit and appears as an open circuit at the 3-way splitter (e.g., it does not load the splitter). Ports 5 and 7 have opposite output port phase shifts enabling signals to additively combine at the designated ring output port (e.g., either Σ or Δ). In operation, the switches in this circuit implementation always select opposite polarity paths. When the switches are configured as shown, output 2 is selected as Σ and output 5 is Δ. By inverting both switches the output port functions are swapped. The input/output port reflection validates the calculated S-parameters of the system level design, as shown in Fig. 11.

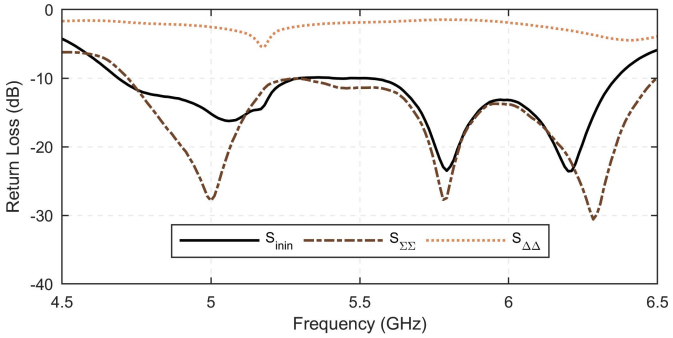

Fig. 11. Reflection coefficients at the input and output ports of the 4-way ring combiner.

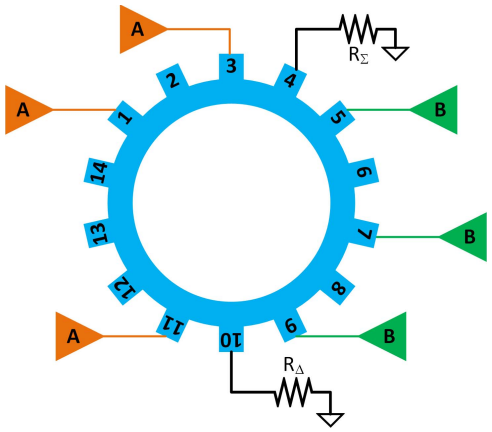

Fig. 12. 6-way ring combiner/divider.

B. 6-Way Ring Combiner Analysis

The 6-way ring combiner presented in [25] is a 14 port combiner, featuring 6 input ports in two groups (e.g., group A: 1, 3, 11; group B: 5, 7, 9) driving two output ports (e.g., $\Sigma = 4$ and $\Delta = 10$) as shown in Fig. 12. Ports 2, 6, 8, 12-14 are left unterminated. The TL sections that define the ring are designed to be a quarter-wavelength at the desired frequency and the characteristic impedances is chosen according to (16) to be 41 Ω.

The designed 6-way combiner (Fig. 13) was not designed for the same port swapping as the 4-way combiner; hence the additional circuitry is omitted from the design. No convenient line of symmetry exists for a simplified half circuit analysis; The S-parameters are derived port-by-port. The analysis yields the following S-parameter matrix: (19), as shown at the bottom of this page, where the scaling factor $A = 1/\sqrt{6}$. Again, note that the S-parameters show non-zero reflection at ports 1, 2, 4, 5, 6 and 8. Mismatch only occurs if the signals of a common input group have different impedances. The input/output port reflection is plotted in Fig. 14 for the combiner of Fig. 13. Note that even though internal ports are not well matched, if properly terminated and driven, the return loss at the design frequency can be <-10 dB.

V. Measurement Results

To validate the performance of the ring combiners 4-way and 6-way passive combiners are fabricated, both with and without amplifiers. All combiner designs are made on PCBs

$$S = \begin{pmatrix} -\frac{2}{3} & -\frac{1}{3} & jA & 0 & 0 & 0 & -jA & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & -jA & 0 & 0 & 0 & jA & -\frac{1}{3} \\ jA & -jA & 0 & -jA & jA & -jA & 0 & jA \\ 0 & 0 & -jA & -\frac{2}{3} & -\frac{1}{3} & \frac{1}{3} & -jA & 0 \\ 0 & 0 & jA & -\frac{1}{3} & -\frac{2}{3} & -\frac{1}{3} & jA & 0 \\ 0 & 0 & -jA & \frac{1}{3} & -\frac{1}{3} & -\frac{2}{3} & -jA & 0 \\ -jA & jA & 0 & -jA & jA & -jA & 0 & -jA \\ \frac{1}{3} & -\frac{1}{3} & jA & 0 & 0 & 0 & -jA & -\frac{2}{3} \end{pmatrix}, \tag{19}$$

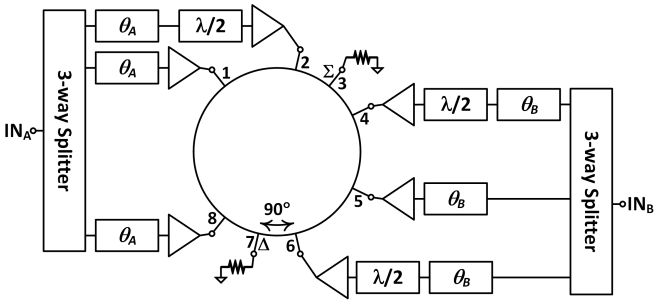

Fig. 13. 6-way ring outphasing amplifier schematic.

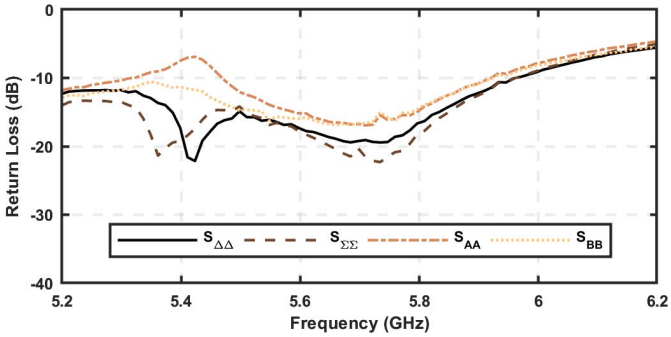

Fig. 14. Reflection coefficients at the input and output ports of the 6-way ring.

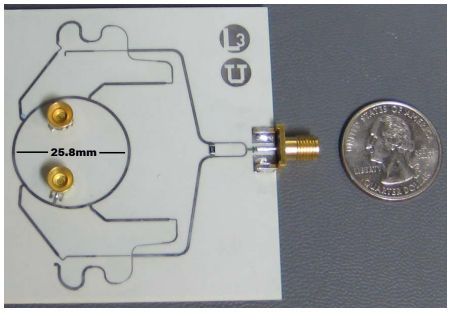

Fig. 15. 4-way passive ring combiner/divider PCB.

using Rogers RO4350 as the substrate. The measurement details for each of the combiners are now presented.

A. 4-Way Ring Combiner

A passive layout of the 4-way ring combiner designed for 5.7GHz center frequency is shown in Fig. 15. The absence in performance variation of active components enables clear comparison of simulated and measured ring combiner performance. There is close correlation between simulation and measured results shown in Fig. 16. The insertion loss (IL) from the common input to the Σ port is measured at −1.2 dB at the center of the band (5.7 GHz) and compares well with the ideal simulated response, shown in Fig. 16(a). Ring combiners have narrower bandwidths than other combiners, owing to multiple cascaded quarter-wave transmission line segments; The bandwidth narrows as the number of amplifiers to be combined is increased. In our design, the insertion loss bandwidth is ∼33%, while the isolation bandwidth (e.g. common input to Δ port) is >10.5% for isolation >30 dB. The simulated isolation matches well with the measured isolation,

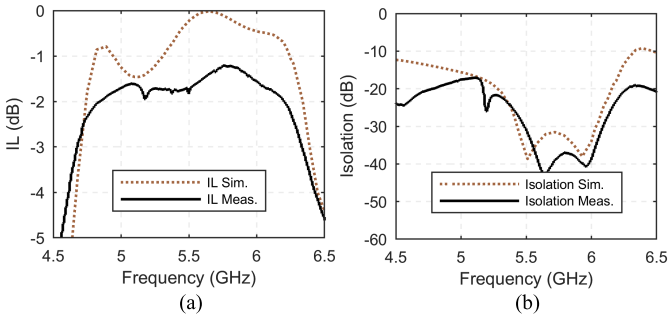

Fig. 16. 4-way passive ring combiner simulated vs. measured (a) small-signal IL at the Σ port and (b) isolation at the Δ port.

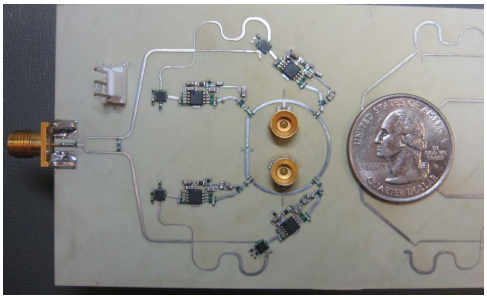

Fig. 17. 4-way active ring combiner PCB.

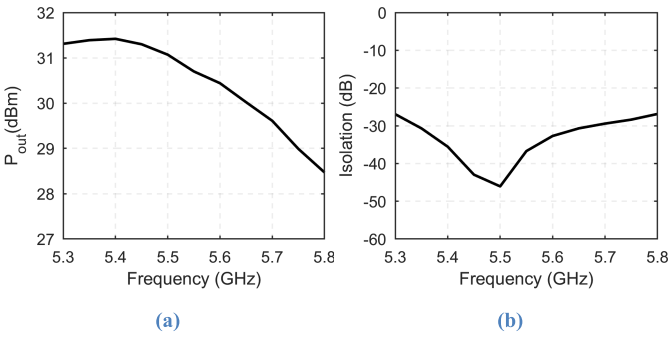

Fig. 18. Measured (a) output power at the Σ port and (b) isolation at the Δ port for the 4-way active ring combiner.

as shown in Fig. 16(b). Note that in this design, the inputs to the ring are derived from a single input port; if we were to drive the two input groups separately, the isolation could be tuned by adjusting the relative phase difference between input groups, as is later demonstrated with the 6-way combiner measurement results.

The 4-way ring combiner is also fabricated with embedded amplifiers as shown in Fig. 17. Four HMC406MS8G devices are combined to produce a net peak of 31.4 dBm output power (P_{out}), which includes all loss from the combiner and mismatch effects due to amplifier process, voltage and temperature (PVT) variations. This is ∼1.6 dB lower than the ideal result, as the HMC406MS8G can output 27 dBm saturated P_{out}, and an ideal 4-way combiner would provide 6 dB increase in output power for an ideal net of 33 dBm. The output power and isolation of the 4-way combiner are plotted in Fig. 18(a) and (b), respectively. The isolation (Δ port) peaks at 5.5 GHz, while the P_{out} (Σ port) ranges from 31.4 dBm at the 5.4 GHz to 28.5 dBm at the 5.8 GHz. The roll-off in P_{out} is

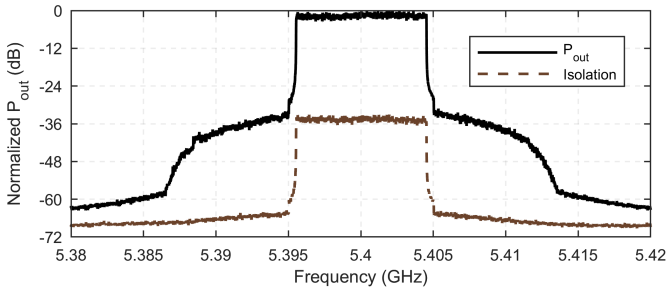

Fig. 19. Measured PSD for a 10MHz, 64 QAM LTE uplink signal at the Σ port and the Δ port.

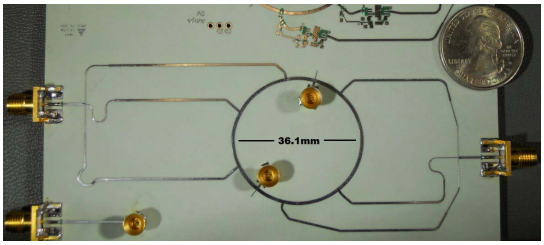

Fig. 20. 6-way passive ring combiner/divider PCB.

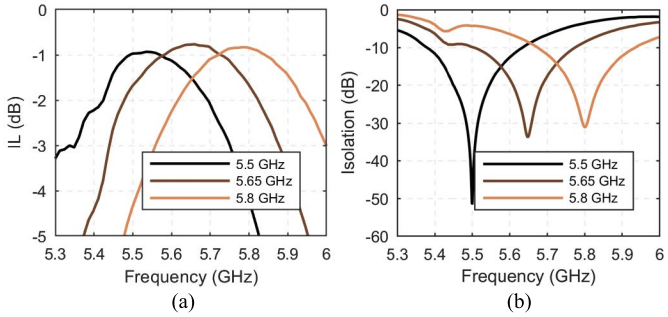

Fig. 21. Measured IL and isolation for the 6-way passive ring combiner.

due to the combiner non-optimally loading the amplifier away from the center frequency. Shown in Fig. 19 is the output of the ring combiner for a 10MHz LTE waveform, with an RF carrier frequency of 5.4 GHz. The measured output power at the Σ port for the LTE signal is 25.5 dBm. The isolation measured at the Δ port is >35 dB. Owing to the switches described in section IV, the signal can be routed to either the Σ or Δ port with similar performance.

B. 6-Way Ring Combiner

To validate the performance of the 6-way ring combiner, a passive only prototype version of the combiner was fabricated on a Rogers RO4350 substrate, as shown in Fig. 20. The insertion loss (Σ) and isolation (Δ) are measured vs. frequency in Fig. 21(a) and (b), respectively. It is noted that though the 6-way combiner has a narrower bandwidth than other combiners, its output center frequency can be adjusted by controlling the relative phase between the group 1 and group 2 inputs, allowing for reconfigurability. The relative phase shift between the input ports (e.g., IN_A and IN_B, Fig. 13) is adjusted by the signal generator input feeding these ports. The IL through the passive combiner is <1 dB when the combiner is tuned to operate at a center frequency of 5.5,

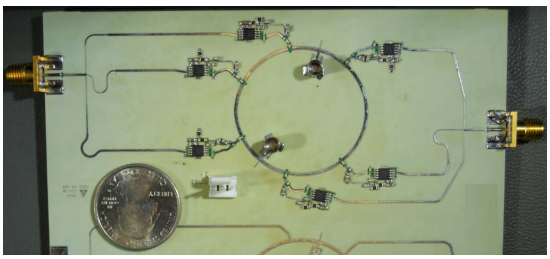

Fig. 22. 6-way active ring combiner/divider PCB.

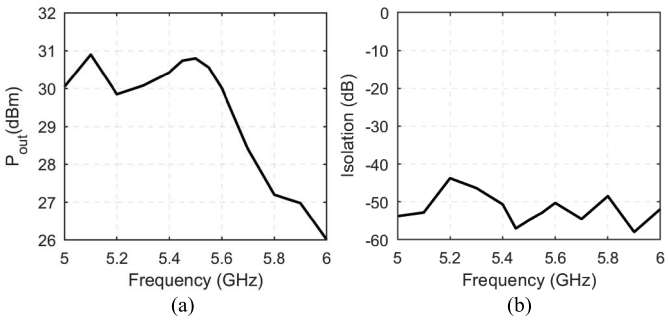

Fig. 23. Measured (a) output power and (b) isolation for the 6-way active ring combiner.

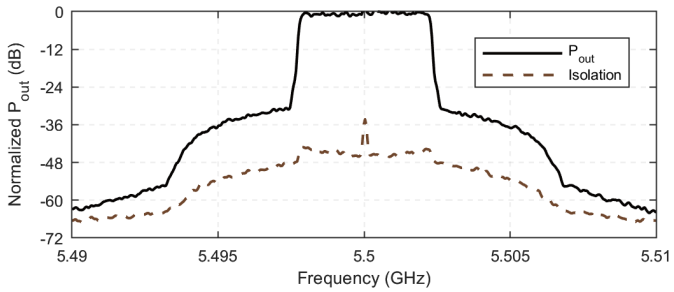

Fig. 24. Measured PSD for a 5MHz, 64 QAM LTE uplink signal at the Σ port (P_{out}) and the Δ port (Isolation).

5.65 and 5.8 GHz. This is obtained by adjusting the phase offset between IN_A and IN_B to 0°, 5° and 20°, respectively. It is noted that this is less than the loss of the previously reported 4-way combiner; this is for two reasons. First, the 4-way combiner included extra circuitry to enable port-switching that is not necessary when only using as a combiner. Second, the phase tuning mechanism used on the 6-way combiner was not available on the 4-way combiner because in the 4-way combiner, all ports were driven with the same source.

Similarly, the isolation at these center frequencies is >25 dB. When tuned to the designed optimal frequency of 5.5 GHz, the measured isolation is >44 dB. This frequency is where the quarter-wave TL segments are centered. Fine phase adjustments can allow for the isolation to be tuned to any frequency in the bandwidth of the ring.

The 6-way active ring combiner is also fabricated with embedded amplifiers as shown in Fig. 22. Six HMC406MS8G devices are combined. The output power and isolation are measured versus frequency in Fig. 23(a) and (b), respectively. A measured peak output power of 31 dBm is produced at 5.5 GHz. The combiner ideally provides a gain of 10log10(6)≈7.8 dB. Accounting for IL, the gain of the

TABLE II
COMPARISON TO PRIOR ART FOR RECENT FOUR- AND SIX-WAY COMBINERS

Specification	[2]	[10]	[28]	[29]	[30]	[31]	This work	This work
# Combined Ports	4	4	6	4	6	6	4	6
Topology	Coupled Line	T Junction Ladder	Branch Wave-guide	N/A	N/A	N/A	Ring	Ring
Size (@f_0)	0.4λ×1.0λ	0.8λ×0.8λ	N/A	0.3λ×0.3λ	0.4λ×0.8λ	1.4λ×1.0λ	1.1λ×1.0λ	0.9λ×2.3λ
Freq. (GHz)	6.0	2.1	32	11.0	10.0	5.0	5.5	5.5
1dB IL BW %	108%	N/A	18%	127%	160%	120%	33%	10%
IL (dB)	1.0	N/A	0.8	0.9	1.6	1.2	1.2	1.0
Output RL (dB)	15.0	N/A	14.0	12.5	11.8	12.7	9.3	14.0
Planar	No	No	No	No	No	No	Yes	Yes
Delta Port	No	No	No	No	No	No	Yes	Yes
Delta Isolation (dB)	N/A	N/A	N/A	N/A	N/A	N/A	<-30	<-25

combiner is ≈6.8 dB. This should yield an output power of 33.8 dBm with the chosen power amplifiers. The additional loss is due to PVT variations due to the assembly and in the output impedance of the amplifiers. The PCB was assembled manually, resulting in inconsistent solder contacts. The PVT variations cause phase mismatch at the amplifier input ports, reducing the peak output power due to out-of-phase summation. This is the prime challenge when attempting to combine many amplifiers, with a single combiner. It is noted that matched amplifiers, phase compensating pre-distortion, integration at mm-wave frequencies on a MMIC, or machine-based assembly would improve the losses due to mismatches in loading, owing to better control of PVT variations.

The isolation can be optimized across frequency by adjusting the static phase difference between the input groups. The measured isolation across the band (Fig. 23(b)) from 5-6 GHz is better than 44 dBc.

To validate the performance with a modulated signal, a 24.1 dBm 5 MHz LTE waveform is measured at 5.5 GHz with >35 dBc ACLR for E-UTRA, as shown in Fig. 24. Note, this is not a single-carrier OFDM signal, hence the peak-to-average power ratio (PAPR) is ≈6.5 dB. The measured isolation to the delta port of the modulated signal is >35 dBc. Note that no digital pre-distortion or other linearization techniques were used in this measurement.

VI. CONCLUSION

A new generalized N-way ring power combiner is presented in this paper, along with a generalized design methodology. The combiner, though narrower band than WDC based combiners, offers a compact, planar layout and offers a single common delta-port that has applications for energy recovery, port monitoring and calibration. It is noted that due to the cascading $\lambda/4$ TL sections, the ring combiner family generally offers lower bandwidth than other combiners and if external circuitry is included is comparable in size. For heavily embedded/integrated applications where DSP can be used to create phase shifts, the ring can be smaller than the other combiners. Finally, two example designs are presented for both a 4-way and a 6-way ring combiner. Each example design uses conventional splitters to enable use of a single input port, but it is noted that in highly integrated designs (e.g., MMICs and RFICs), the splitting network is not necessary. Both designs show measurement results for a passive case, and a case with embedded amplifiers. Measurement results are shown with good correlation to simulation data. Result summaries with comparison to recent 4- and 6-way combiners in the literature [2], [10], [28] and in production [30, p. 4], [31, p. 6], [31] are shown in Table II.

ACKNOWLEDGEMENTS

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REFERENCES

[1] M. Thian, V. Fusco, and P. Gardner, "Power-combining class-E amplifier with finite choke," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 3, pp. 451–457, Mar. 2011.

[2] A. M. Darwish, A. A. Ibrahim, J. X. Qiu, E. Viveiros, and H. A. Hung, "A broadband 1-to-N power divider/combiner with isolation and reflection cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2253–2263, Jul. 2015.

[3] I. Ju, M.-K. Cho, I. Song, and J. D. Cressler, "A compact, wideband lumped-element Wilkinson power divider/combiner using symmetric inductors with embedded capacitors," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 8, pp. 595–597, Aug. 2016.

[4] I. Song, M.-K. Cho, J.-G. Kim, and J. D. Cressler, "A SiGe-BiCMOS wideband (2–22 GHz) active power divider/combiner circuit supporting bidirectional operation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4676–4684, Dec. 2016.

[5] D.-J. Lee, S.-J. Lee, I.-J. Hwang, W.-S. Lee, and J.-W. Yu, "Hybrid power combining rectenna array for wide incident angle coverage in RF energy transfer," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3409–3418, Sep. 2017.

[6] T. Hwang, K. Azadet, R. S. Wilson, and J. Lin, "Nonlinearity modeling of a Chireix outphasing power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 12, pp. 2898–2907, Dec. 2015.

[7] M. Özen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, "A generalized combiner synthesis technique for class-E outphasing transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 5, pp. 1126–1139, May 2017.

[8] K. D. Holzer, W. Yuan, and J. S. Walling, "Wideband techniques for outphasing power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2715–2725, Sep. 2018.

[9] D. J. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1713–1726, Aug. 2011.

[10] T. W. Barton and D. J. Perreault, "Four-way microstrip-based power combining for microwave outphasing power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2987–2998, Oct. 2014.
[11] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-way lossless outphasing system based on an all-transmission-line combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1313–1326, Apr. 2016.
[12] E. J. Wilkinson, "An N-way hybrid power divider," *IRE Trans. Microw. Theory Techn.*, vol. 8, no. 1, pp. 116–118, Jan. 1960.
[13] U. H. Gysel, "A new N-way power divider/combiner suitable for high-power applications," in *IEEE-MTT-S Int. Microw. Symp. Dig.*, May 1975, pp. 116–118.
[14] R. Gómez-García, R. Loeches-Sánchez, D. Psychogiou, and D. Peroulis, "Single/multi-band Wilkinson-type power dividers with embedded transversal filtering sections and application to channelized filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1518–1527, Jun. 2015.
[15] J. M. Schellenberg, "A 2-W W-band GaN traveling-wave amplifier with 25-GHz bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2833–2840, Sep. 2015.
[16] J. Schellenberg, "The evolution of power combining techniques: From the 60s to today," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4.
[17] A. A. M. Saleh, "Planar electrically symmetric n-way hybrid power dividers/combiners," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-28, no. 6, pp. 555–563, Jun. 1980.
[18] F. Wang and H. Wang, "An N-way transformer based Wilkinson power divider in CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.
[19] W. A. Tyrrell, "Hybrid circuits for microwaves," *Proc. IRE*, vol. 35, no. 11, pp. 1294–1306, Nov. 1947.
[20] K. D. Holzer and J. S. Walling, "A multi-channel outphasing ring combiner for multi-mode output and channel aggregation," in *Proc. 46th Eur. Microw. Conf. (EuMC)*, Oct. 2016, pp. 516–519.
[21] K. D. Holzer and J. S. Walling, "A 6-way ring combiner/divider," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 420–423.
[22] D. Cox, "Linear amplification with nonlinear components," *IEEE Trans. Commun.*, vol. 22, no. 12, pp. 1942–1945, Dec. 1974.
[23] R. Darraji and F. M. Ghannouchi, "High efficiency Doherty amplifier combining digital adaptive power distribution and dynamic phase alignment," in *Proc. IEEE WAMICON*, 2013, pp. 1–3.
[24] M. A. Panahi, S. Abdollahramezani, G. E. Ardakani, and R. Safian, "An efficient high power RF dummy-load," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 6, pp. 409–411, Jun. 2015.
[25] K. D. Holzer and J. S. Walling, "A Ku band high-power, low-insertion-loss single pole, triple throw switch," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Oct. 2017, pp. 81–84.
[26] K. D. Holzer and J. S. Walling, "Magnetless ring circulators for full duplex division wireless communication," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Oct. 2017, pp. 77–80.
[27] D. M. Pozar, "The 180° ring hybrid," in *Microwave Engineering*, 2nd ed. 1998, ch. 7, pp. 401–407.
[28] X. Jie, C. Yinjie, Q. Cheng, and L. Wenyuan, "A Ka-band power-combined amplifier based on a six-way quasi-planar power divider/Combiner," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, vol. 1, Dec. 2015, pp. 1–3.
[29] *DC Pass Power Splitter/Combiner—ZN4PD-272+*, Mini-Circuits.
[30] *High Power, DC Pass Power Splitter/Combiner—ZN6PD-272+*, Mini-Circuits.
[31] *Technical Data Sheet—6 Ways Power Divider 2-8 GHz—R434516001*, Radiall Corporation.

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