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# Probing Interface Defects in Top-Gated MoS<sub>2</sub> Transistors with Impedance Spectroscopy

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**Abstract** The electronic properties of the HfO<sub>2</sub>/MoS<sub>2</sub> interface were investigated using multi-frequency capacitance-voltage (C-V) and current-voltage characterization of top-gated MoS<sub>2</sub> metal-oxide-semiconductor field effect transistors (MOSFETs). The analysis was performed on few layer (5 - 10) MoS<sub>2</sub> MOSFETs fabricated using photolithographic patterning with 13 nm and 8 nm HfO<sub>2</sub> gate oxide layers formed by atomic layer deposition after in-situ UV-O<sub>3</sub> surface functionalization. The impedance response of the HfO<sub>2</sub>/MoS<sub>2</sub> gate stack indicates the existence of specific defects at the interface, which exhibited either a frequency dependent distortion similar to conventional Si MOSFETs with unpassivated silicon dangling bonds, or a frequency dispersion over the entire voltage range corresponding to depletion of the HfO<sub>2</sub>/MoS<sub>2</sub> surface,

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3 consistent with interface traps distributed over a range of energy levels. The interface defects  
4 density ( $D_{it}$ ) was extracted from the C-V responses by the high-low frequency and the multiple-  
5 frequency extraction methods, where a  $D_{it}$  peak value of  $1.2 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$  was extracted for a  
6 device (7-L MoS<sub>2</sub> and 13 nm HfO<sub>2</sub>) exhibiting a behavior approximating to a single trap  
7 response. The MoS<sub>2</sub> MOSFET with 4-L MoS<sub>2</sub> and 8 nm HfO<sub>2</sub> gave  $D_{it}$  values ranging from  
8  $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  to  $2 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$  across the energy range corresponding to depletion near the  
9 HfO<sub>2</sub>/MoS<sub>2</sub> interface. The gate current was below  $10^{-7} \text{ A/cm}^2$  across the full bias sweep for both  
10 samples indicating continuous HfO<sub>2</sub> films resulting from the combined UV ozone and HfO<sub>2</sub>  
11 deposition process. The results demonstrated that impedance spectroscopy applied to relatively  
12 simple top-gated transistor test structures provides an approach to investigate electrically active  
13 defects at the HfO<sub>2</sub>/MoS<sub>2</sub> interface and should be applicable to alternative TMD materials,  
14 surface treatments and gate oxides as an interface defect metrology tool in the development of  
15 TMD-based MOSFETs.  
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38 **Keywords** Molybdenum disulfide (MoS<sub>2</sub>), high-*k* dielectrics, interface defects, electrical  
39 characterization, top-gated transistors, capacitance – voltage (C-V).  
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## 46 **Introduction**

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49 Over the past decade, two-dimensional (2-D) materials have attracted considerable attention  
50 due to their atomically-thin structure and their unique electronic, optical and mechanical  
51 properties<sup>1-3</sup>. Among these materials, transition metal dichalcogenides (TMDs) have  
52 demonstrated satisfactory energy bandgap values and promising properties for future  
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3 applications in electronics and optoelectronics <sup>4-17</sup>. Molybdenum disulfide (MoS<sub>2</sub>), as the most  
4 explored TMD material, has been reported to exhibit an electron mobility of 55 cm<sup>2</sup>/V·s in a  
5 top-gated transistor with a single layer of MoS<sub>2</sub> <sup>4-6</sup>, and a theoretical value of 410 cm<sup>2</sup>/V·s at  
6 room temperature <sup>7</sup>. Moreover, compared with monolayer MoS<sub>2</sub>, few-layer MoS<sub>2</sub> has been  
7 predicted and experimentally demonstrated as an excellent channel material to achieve high  
8 mobility and reduced contact resistivity <sup>8-12</sup>. With the ultimate electrostatic control due to the 2-  
9 D structure, an energy gap in the range of 1.2eV to 1.8eV, and the high mobility value, MoS<sub>2</sub> is  
10 especially attractive for high performance, low power-consumption flexible electronics <sup>1,10,18,19</sup>.

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23 As the utilization of high dielectric constant (high-*k*) gate oxide material in conventional  
24 silicon CMOS processing has been demonstrated to reduce the gate leakage and enable further  
25 scaling of transistors, high-*k* dielectrics are also considered extensively for TMD transistors  
26 <sup>5,10,11,16,18-28</sup>. In addition, high-*k* materials can suppress the coulombic scattering in low  
27 dimensional nanostructures, increasing the carrier mobility, as shown in the literature with both  
28 theoretical simulation <sup>20</sup> and experimental evidence <sup>5,11</sup>. Although back gated structures are ideal  
29 for contact and doping research on TMD transistors <sup>8,29,30</sup>, top gate devices are more attractive  
30 for integrated circuit manufacturing. Thus, investigating high-*k* deposition on TMDs and  
31 understanding the interface properties is an important scientific and technological research area.

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45 An obstacle of integrating high-*k* dielectrics on these 2-D materials is the lack of bonds  
46 available at the surface that enables thin film deposition <sup>21,22</sup>. Many top-gated transistors in the  
47 literature adopted thick gate dielectric deposition, usually from 15 nm to 50 nm <sup>5,11,16,23</sup>, to avoid  
48 pin holes and non-uniformity in the dielectric. Recently, multiple surface functionalization  
49 methodologies have been reported for thin, uniform high-*k* dielectric deposition on MoS<sub>2</sub> <sup>22,24-27</sup>.  
50 Metal seed layers <sup>24</sup>, oxygen plasma treatment <sup>22,25</sup> and ultraviolet-ozone (UV-O<sub>3</sub>) treatment <sup>26,27</sup>

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3 are promising pre-deposition approaches to gain a uniform dielectric layer. However, since the  
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5 ultimate goal of these approaches is the enhancement of electronic device performance, detailed  
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7 reports on device performance related to the impacts of these treatments is vital, but only shown  
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9 in a few papers<sup>24,25,31</sup>. Our previous research suggested that defects existed at the high- $k$ /MoS<sub>2</sub>  
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11 interface region after an ex-situ UV-O<sub>3</sub> treatment<sup>28</sup>, but the gate oxide leakage on these large  
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13 area MOS structures affected the analysis, due to the rough surface of the bulk MoS<sub>2</sub> sample and  
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15 relatively large capacitor area. Recently, Azcatl et al.,<sup>26,27</sup> reported that the non-destructive (i.e.,  
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17 no Mo-oxide formation) in-situ UV-O<sub>3</sub> treatment featured a uniform atomic layer deposited  
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19 (ALD) high- $k$  oxide without unexpected interfacial layers for exfoliated MoS<sub>2</sub>.  
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25 Impedance measurements are recognized as one of the fastest and most robust methods to  
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27 investigate properties of a dielectric and its interface with the underlying substrate. However,  
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29 impedance measurements of metal/high- $k$  dielectric/TMD MOS system have only been reported  
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31 in a limited number of works<sup>10,11,18,31–33</sup>. Most publications report capacitance - voltage (C-V)  
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33 curves without further analysis<sup>10,11,32</sup>, or back-gated capacitors with high- $k$  deposited on Si<sup>33</sup>.  
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35 Recently, S. Park et al.<sup>31</sup> reported C-V characteristics of capacitors with Al<sub>2</sub>O<sub>3</sub> on 100-200 nm  
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37 thick MoS<sub>2</sub> yielding  $D_{it}$  values of  $10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup> to  $10^{14}$  cm<sup>-2</sup>eV<sup>-1</sup>. For high- $k$  on chemical-vapor-  
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39 deposited (CVD) MoS<sub>2</sub> thin films, a comprehensive study of dielectric impedance was  
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41 performed, showing  $D_{it}$  extraction and modeling work based on capacitors with 30 nm ALD  
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43 HfO<sub>2</sub> on monolayer MoS<sub>2</sub> with 2nm Al as an interfacial seed layer<sup>18</sup>. Another relevant and useful  
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45  $D_{it}$  extraction work has been reported by Takenaka et al.<sup>33</sup>, which uses the Terman method to  
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47 analyze and compare interfaces of MoS<sub>2</sub> and SiO<sub>2</sub>/HfO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>. The extracted  $D_{it}$  values are  
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49 about  $1 \times 10^{13}$  cm<sup>-2</sup>eV<sup>-1</sup> regardless of the dielectric selection for back-gated devices on semi-bulk  
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51 MoS<sub>2</sub>. However, the device architecture may not be commensurate with the necessary solution  
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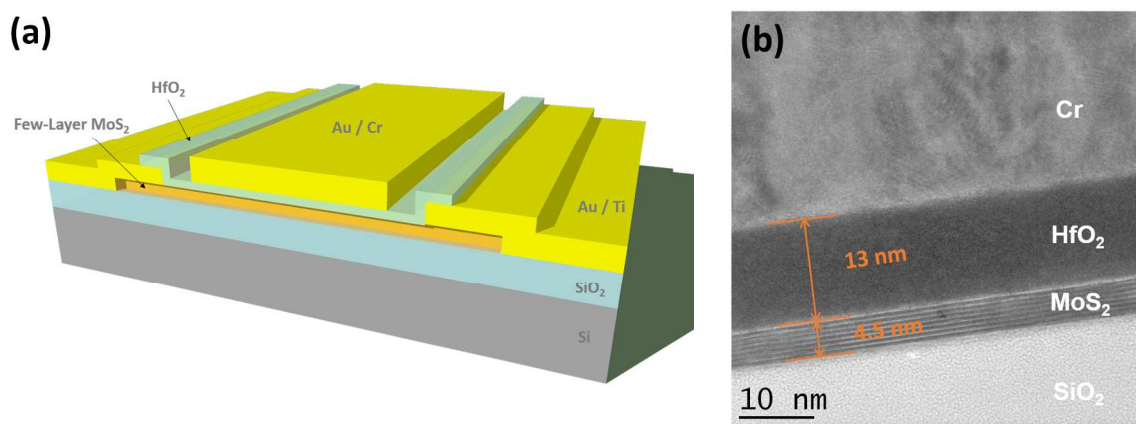
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3 for continued device scaling where top-gated architectures dominate. Here, dielectric/substrate  
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5 interfaces are dependent upon how device fabrication was executed, and therefore, should be  
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7 investigated in this context.  
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11 In this work, we designed and fabricated top-gated transistors on exfoliated, few-layer MoS<sub>2</sub>  
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13 as the test structures, with an in-situ UV-O<sub>3</sub> functionalization<sup>26,27</sup> and 8 to 13 nm ALD HfO<sub>2</sub>,  
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15 which are among the thinnest high-*k* dielectrics on top-gate TMD MOSFETs to date. As we use  
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17 photolithography for source/drain and gate patterning, the gated area is sufficiently large for C-V  
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19 characterization. Both transistor performance and gate-stack interface properties were  
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21 characterized, with an emphasis on the impedance spectroscopy of the dielectric. The interface  
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23 defect density ( $D_{it}$ ) was extracted and analyzed by three different methods. Besides reporting the  
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25 interface properties of our transistors, the methodology can be potentially applied to other TMDs  
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27 and surface functionalization, beyond MoS<sub>2</sub> and UV-O<sub>3</sub> treatment.  
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## 36 **Experimental Methods**

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39 The transistor structure used for the few-layer MoS<sub>2</sub> MOSFETs examined in this work is  
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41 shown in Fig. 1a. Before device fabrication, 270nm SiO<sub>2</sub> was thermally grown on highly doped  
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43 p-type Si wafers as a substrate. Few-layer MoS<sub>2</sub> flakes were mechanically exfoliated from  
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45 commercially available natural MoS<sub>2</sub> crystals and transferred onto the SiO<sub>2</sub>. By using  
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47 conventional photolithography, we aligned a source/drain pattern on the photomask directly on  
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49 the selected flake. After patterning, Au/Ti (380/20nm) was deposited as contacts in an e-beam  
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51 evaporator at  $2 \times 10^{-6}$  Torr, followed by a lift-off process. Thereafter, a 15-minute in-situ UV-O<sub>3</sub>  
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53 surface treatment<sup>26</sup> was performed. The UV-O<sub>3</sub> is generated based on irradiance from the fused  
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3 quartz envelope, low pressure UV Hg lamp employed previously<sup>26,27</sup> and is estimated to be 5  
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5 mW/cm<sup>2</sup> which ensures no etching or Mo-oxide formation according to S. Park et al.<sup>31</sup>  
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8 Following the UV-O<sub>3</sub> surface preparation, HfO<sub>2</sub> was deposited at 200°C in the ALD chamber  
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10 immediately after the treatment without a break in vacuum. The thermal ALD used H<sub>2</sub>O and  
11  
12 TDMA-Hf as the precursors, and started the deposition with a TDMA-Hf pulse. We intentionally  
13  
14 avoided annealing the HfO<sub>2</sub> after deposition to study the effects of the UV-O<sub>3</sub> functionalization  
15  
16 treatment and its role on HfO<sub>2</sub>/MoS<sub>2</sub> interface properties without the impact of any subsequent  
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18 annealing. The final step of fabrication was patterning and evaporating of Au / Cr (250/50nm)  
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20 metal gate. The typical MoS<sub>2</sub> thickness studied in our work was about 5-10 layers (3-6 nm). The  
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22 device size was determined by both lithography and the flake shape. Electrical measurements in  
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24 this work were performed using a Keithley 4200 Semiconductor Characterization System and an  
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26 Agilent E4980A LCR meter at room temperature (25°C) in a shielded probe station.  
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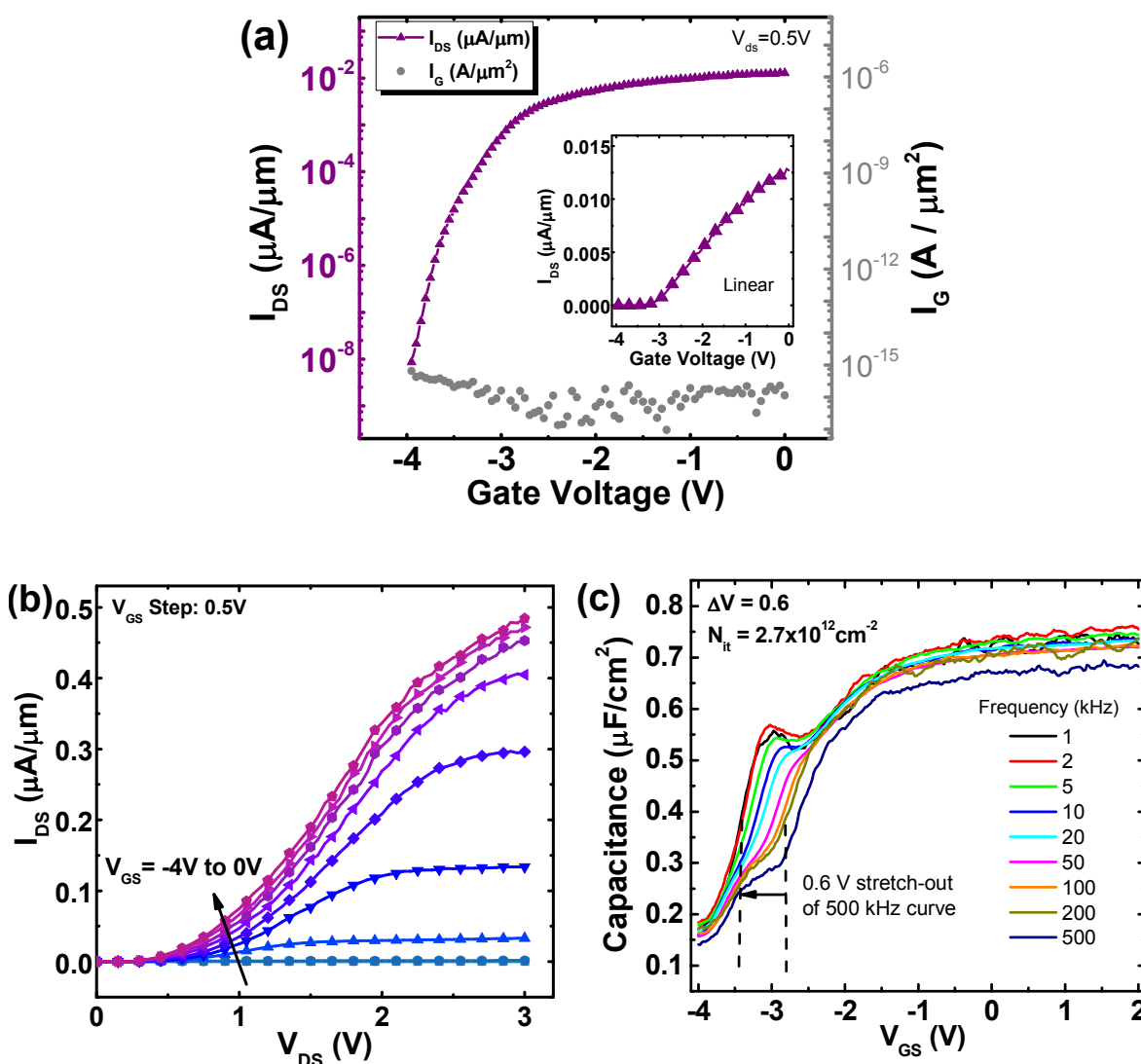
**Figure 1.** (a) Schematic cross section of the top-gated MoS<sub>2</sub> field effect transistor structure used in this work. Gate stack: Au / Cr / HfO<sub>2</sub> / MoS<sub>2</sub>. (b) Cross sectional transmission electron microscopic image of the metal/HfO<sub>2</sub>/MoS<sub>2</sub> transistor gate stack. 13nm HfO<sub>2</sub> is uniformly deposited on a 7-layer MoS<sub>2</sub> flake, showing no evidence of unintentional oxidation of the MoS<sub>2</sub> surface.



## Results and Discussion

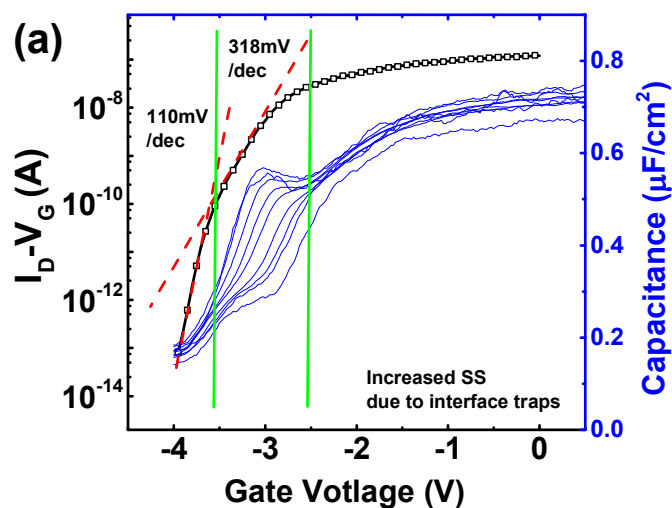
A high-resolution transmission electron microscopic (TEM) image is shown in Fig.1b, illustrating the cross section of a device gate stack with 7 layer MoS<sub>2</sub> and a 13 nm HfO<sub>2</sub> dielectric. The active channel length under the metal gate is 6.5 μm and the channel width is 9.5 μm. Fig. 2a shows the I<sub>DS</sub>-V<sub>GS</sub> and the gate leakage characteristics for this MoS<sub>2</sub> transistor. V<sub>DS</sub> was kept at 0.5V. An excellent on/off ratio of 10<sup>6</sup> was observed, with an ultra-low leakage current on the gate. The MoS<sub>2</sub> was intrinsically n-type doped, consistent with our previous observation<sup>28</sup> and literature reports<sup>5,8,24,29</sup>. The relatively large negative threshold voltage (V<sub>T</sub> = -3V) is possibility due to the fixed positive charge in the dielectric layer(s). Similar large |V<sub>T</sub>| was also observed by other researchers using top-gated MoS<sub>2</sub> transistors with high-*k* dielectrics<sup>11,24</sup>. Since the HfO<sub>2</sub> is deposited at low temperature (200 °C) with no post deposition annealing (to assess the UV-O<sub>3</sub> treatment without convolution from additional annealing), a possible net oxide charge being present in the HfO<sub>2</sub> layer may result. Furthermore, possible contribution of induced charges in the underlying SiO<sub>2</sub> from potential x-rays exposure during the electron beam deposition process – which was used to form the metal gate and source/drain regions – could occur. Thus, both oxide layers could possess trapped charge. Assuming the threshold voltage shift ΔV=-3V originates from oxide charges, the density of the positive fixed charges can be estimated by  $Q_f / q = - C_{ox} \cdot \Delta V / q = 1.4 \times 10^{13} / \text{cm}^2$ . Fig. 2b shows the I<sub>DS</sub>-V<sub>DS</sub> curves with V<sub>GS</sub> swept from -4 V to 0 V. A non-linear region was observed at low V<sub>DS</sub>, likely because of high resistance Schottky barriers at the source/drain contacts associated with this unannealed device<sup>5,34</sup>. This is expected, as there is no intentional doping in the MoS<sub>2</sub> film in the source and drain region. As is the case in conventional 3D semiconductors, increasing the doping

in the MoS<sub>2</sub> film to high concentrations ( $> 1 \times 10^{19} \text{ cm}^{-3}$ ), for example via Nb doping<sup>35</sup>, significantly reduces the specific contact resistivity at the Ti/MoS<sub>2</sub> interface. In addition, it is noted from Fig.1a that the top-gated MOSFET has non-gated regions between the gate edge and the source and drain contacts (approximately 1-2 $\mu\text{m}$  on each side), which is another source of series resistance in the structure.

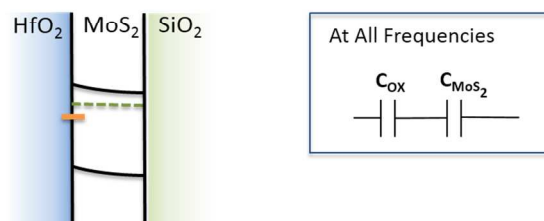


**Figure 2.** Electrical characterization of device with 13 nm HfO<sub>2</sub> and 7-layer MoS<sub>2</sub> (L=6.5 $\mu\text{m}$ , W=9.5 $\mu\text{m}$ ). (a)  $I_{DS}$  -  $V_{GS}$ :  $I_{ON}/I_{OFF} = 10^6$  with ultra-low gate leakage; (b)  $I_{DS}$  -  $V_{DS}$  with  $V_{GS}$  from -4 V to 0 V; (c) C-V: frequency

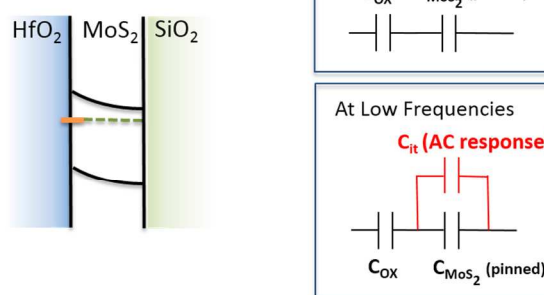
dependence, where a “hump” in the range -2.5 to -3.5 V is indicating an interface defect response. The 0.6 V stretch-out of 500 kHz curve indicates the Fermi energy pinning at MoS<sub>2</sub> / HfO<sub>2</sub> interface.



(b) (i)  $V_{GS} > -2.8$  V in depletion region



(ii)  $-3.4$  V  $< V_{GS} < -2.8$  V ( $E_F$  pinned)



**Figure 3.** (a)  $I_D$ - $V_G$  and multi-frequency C-V overlaid to illustrate the impact of  $D_{it}$  in both measurements occurs at the same  $V_g$ . SS is degraded due to interface traps and  $D_{it} = 1.6 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$  is estimated. (b) Energy band diagram of high- $k$  / MoS<sub>2</sub> interface and equivalent circuits. (i) At gate voltages higher than -2.8 V or lower than -3.4

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3 V, the total AC capacitance is due to the  $C_{ox}$  and  $C_{MoS_2}$  connected in series. (ii) At gate voltage between -3.4 V and -  
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5 2.8 V, the  $E_F$  is pinned at interface, and there is an AC response at low frequencies due to  $D_{it}$  but no AC response at  
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7 high frequencies.  
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10 To investigate the electronic properties at  $HfO_2/MoS_2$  interface, the source and drain were  
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12 connected to one terminal of the LCR meter, while the gate is connected to the other terminal.  
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14 Variable frequency C-V measurements were conducted. The back gate contact was intentionally  
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16 floated to minimize the effect from oxide charge in the underlying  $SiO_2$ . The frequency  
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18 dependence is shown in Fig. 2c. Since this transistor operates in accumulation mode, the reaction  
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20 of the majority carriers (electrons) to the ac signal is observed. In contrast to our previous study  
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22 on the ex-situ UV- $O_3$  treatment and bulk  $MoS_2$  crystals<sup>28</sup>, these C-V frequency dependence  
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24 results showed a highly improved high- $k/MoS_2$  interface, with significantly less dispersion and  
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26 lower gate leakage due to the in-situ UV- $O_3$  treatment and the few-layer TMD thickness. The C-  
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28 V characteristics demonstrate an approximately constant capacitance for positive gate voltage,  
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30 corresponding to the  $HfO_2$  gate oxide capacitance, and a decrease in capacitance in the region -  
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32 2V to -4 V, consistent with depletion of negative charge at the  $HfO_2/MoS_2$  interface. It is noted  
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34 that the region of surface depletion in the C-V response in Fig. 2c, is consistent with the sub-  
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36 threshold region in the transfer characteristics in Fig. 2a. The measured accumulation  
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38 capacitance is  $0.76\mu F/cm^2$ . Based on cross section TEM images, the  $HfO_2$  is 13nm, and assuming  
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40 a  $k$  value of 17 for ALD grown  $HfO_2$ , this would yield a maximum capacitance value of  
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42  $1.1\mu F/cm^2$ . The lower value obtained experimentally, suggests the possibility of a lower  $k$  value  
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44 interface transition region between the  $HfO_2$  and the  $MoS_2$  which is not immediately obvious  
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46 from the TEM analysis.  
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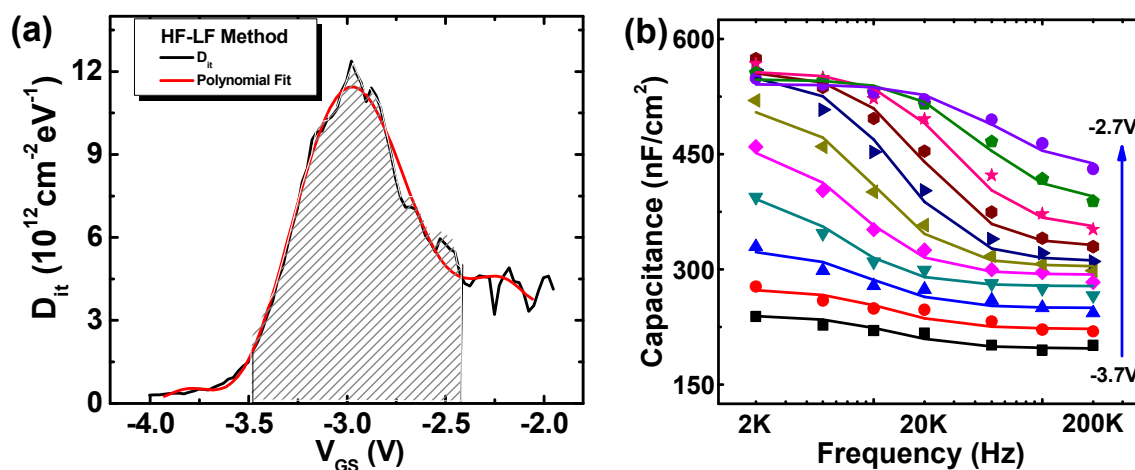
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3 In the capacitance-voltage response in the region -4 V to -2 V, a frequency-dependent  
4 distortion (“hump”) in the depletion region is observed, which is consistent with an electrically  
5 activated trap response at the high- $k$ /MoS<sub>2</sub> interface region. In conventional Si MOSFETs with  
6 either SiO<sub>2</sub> or high- $k$  oxides, this “hump” is usually attributed to interface traps which exhibit a  
7 peak density at a specific energy in the bandgap<sup>36,37</sup>, and usually a forming gas anneal around  
8 400°C can passivate the defects<sup>38,39</sup>, which are primarily silicon dangling bond (P<sub>b</sub>) defects. The  
9 C-V response of Si control sample under the same ALD condition was reported in our previous  
10 work<sup>28</sup>. HfO<sub>2</sub> formed at low temperature (200°C), without any higher temperature annealing in  
11 N<sub>2</sub> or H<sub>2</sub>/N<sub>2</sub> can exhibit gap states which result in C-V hysteresis, interface defect response, and  
12 lower than expected dielectric constant. However, the HfO<sub>2</sub>/Si control sample will not be  
13 representative of the HfO<sub>2</sub>/MoS<sub>2</sub> interface due to the different substrate material and interfacial  
14 condition. (e.g. The Si substrate surface will spontaneously form a SiO<sub>2</sub>-like interfacial layer  
15 during an ALD process, which primarily determines the interfacial property of the HfO<sub>2</sub>/Si<sup>40</sup>).  
16 Published C-V frequency dependence data on a metal / (30nm) HfO<sub>2</sub> / monolayer MoS<sub>2</sub> gate  
17 stack was reported by Zhu et al.<sup>18</sup>, where chemical vapor deposited (CVD) MoS<sub>2</sub> was utilized in  
18 the device structure. Compared with the device based on CVD MoS<sub>2</sub>, this gate stack with  
19 mechanically exfoliated MoS<sub>2</sub> shows much less frequency dispersion, suggesting significantly  
20 fewer interface defects. A limited study of the C-V frequency dependence on semi-bulk MoS<sub>2</sub>  
21 with Al<sub>2</sub>O<sub>3</sub> has also been reported<sup>31</sup>, where interface defects (D<sub>it</sub>) ranging from 10<sup>11</sup> cm<sup>-2</sup>eV<sup>-1</sup> to  
22 10<sup>14</sup> cm<sup>-2</sup>eV<sup>-1</sup> were reported. However, the lateral shift of C-V curves possibly convoluted  
23 positive oxide charge with interface defects in the D<sub>it</sub> extraction process.  
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53 The techniques that we are about to describe to analyze the D<sub>it</sub> are only valid when the device  
54 is not fully depleted, which must be carefully adhered to when using very thin flakes. In this  
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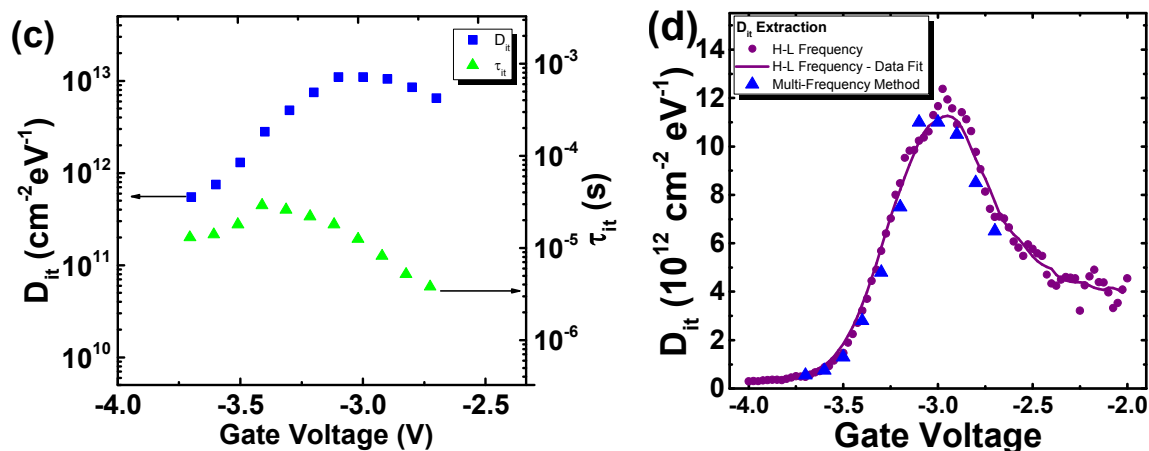
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3 work, the flake is not fully depleted over the bias range where the  $D_{it}$  response is detected. If the  
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5 MoS<sub>2</sub> thin film is fully depleted, the capacitance should be 0 F (or at a constant number over a  
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7 voltage range due to parasitic capacitance components)<sup>41</sup>. As shown in Fig. 3a, at about -3V  
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9 where interface traps are detected, the transistor is not fully turned off (i.e., not fully depleted and  
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11 still has carriers in the flake responding to the AC signal). Further evidence, based on series  
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13 resistance analysis (supporting information Fig. S1, S2), confirms that the device is not fully  
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15 depleted in the  $V_g$  range used to analyze the  $D_{it}$  from the multi-frequency C-V measurements.  
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17 Due to the influence of the interface traps, the inverse subthreshold slope (SS) also increases at  
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19 around -3V. This change of SS is also consistent with the charging of MoS<sub>2</sub>/HfO<sub>2</sub> interface traps  
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21 providing an independent measurement technique indicating that the C-V response is detecting  
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23 interface traps at the corresponding region of the C-V response. SS can be used to roughly  
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25 estimate  $D_{it}$  since  $SS = 60\text{mV} \cdot [1 + (C_{dm} + C_{it})/C_{ox}]$ , where  $C_{dm}$  is the capacitance of depleted MoS<sub>2</sub>  
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27 and  $C_{it}$  is the capacitance due to interface traps. Thus,  $C_{it}$  and  $D_{it}$  ( $C_{it}/q$ ) can be estimated by  
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29 comparing the change in SS around -3.8 V (110 mV/dec) and around -3.2 V (318 mV/dec). The  
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31 calculated result gives  $D_{it} = 1.6 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ .  
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40 Next, we quantified the  $D_{it}$  from the C-V response (Fig. 2c). As the frequency is increased  
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42 from 1 kHz to 500 kHz, this reduces the AC response of the interface defects to the measured  
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44 capacitance, resulting in the dispersion of capacitance with frequency noted in the region from -  
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46 2.5 V to -3.5 V in Fig. 2c. In the limit of increasing frequency, the interface defects will only  
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48 respond to the DC bias (high frequency  $D_{it}$  response), and the interface states will be evident as a  
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50 “plateau” region of the C-V in the case where the interface states are located in a narrow band of  
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52 energies. From Fig. 2c, at frequencies above 100 kHz, an approximate plateau region is observed.  
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54 At 500 kHz this region extends from -2.8 V and -3.4 V. We interpret this 0.6V gate voltage  
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region to be due to the DC response of the defects<sup>42</sup>. This is illustrated in schematic energy band diagrams in Fig. 3b, with surface Fermi level pinning due to interface states with a peak density in a specific energy in the band gap<sup>(1)</sup>. The total density of interface defects, in the areal density units of  $\text{cm}^{-2}$ , can be estimated from the oxide capacitance and the width of the plateau region in the 500kHz CV response, and this yields an interface trap density  $D_{it} = 2.7 \times 10^{12} \text{ cm}^{-2}$ . A more detailed calculation is shown in the supporting information S.3. Although the possibility that the defects still respond with AC signal at 500kHz could not be fully excluded, an abrupt C-V distortion due to peaked distribution of interface defects<sup>42</sup> is consistent with our following  $D_{it}$  extraction and analysis.



<sup>(1)</sup> The plateau region is not a constant capacitance. This would only occur for a mono-energetic defect level at a temperature of zero K.



**Figure 4.**  $D_{it}$  extraction. (a)  $D_{it}$  vs  $V_{GS}$ , calculated by High-Low Frequency method; (b) Re-plotted “Capacitance vs Voltage” to “Capacitance vs Frequency” (dots), and modeling (solid lines); (c)  $D_{it}$  vs  $V_{GS}$  and  $\tau_{it}$  vs  $V_{GS}$ , from the modeling work in (b); (d) Comparison of two  $D_{it}$  extraction methods in (a) and (c), showing similar  $D_{it}$  distribution, with a  $D_{it}$  peak at  $1.2 \times 10^{13} \text{ cm}^{-2} \text{eV}^{-1}$ .

Fig. 4a shows the  $D_{it}$  calculated by the conventional high-low frequency method<sup>42</sup> from equations

$$C_{it} = \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \quad (1)$$

$$D_{it} = C_{it}/q \quad (2)$$

where capacitance of interface traps ( $C_{it}$ ) represents the capacitance when all the traps reacted with AC signal at low frequency;  $C_{LF}$  and  $C_{HF}$  are the capacitance measured at 1 kHz and 500 kHz respectively. In Fig. 4a, the polynomial function is a guide to the eye.  $D_{it}$  ranges from the order of  $10^{12}$  to  $10^{13} \text{ cm}^{-2} \text{eV}^{-1}$ , with a peak value of  $1.2 \times 10^{13} \text{ cm}^{-2} \text{eV}^{-1}$ . The peak value is one order of magnitude lower than what was reported in reference<sup>31</sup> using the same high-low frequency method, and aluminum oxide as the dielectric. It is in the same range as the defect density in literature for exfoliated  $\text{MoS}_2$  by photo-excited charge collection spectroscopy<sup>43</sup>. Translating each gate voltage in Fig. 4a to a corresponding surface potential at the  $\text{MoS}_2/\text{HfO}_2$



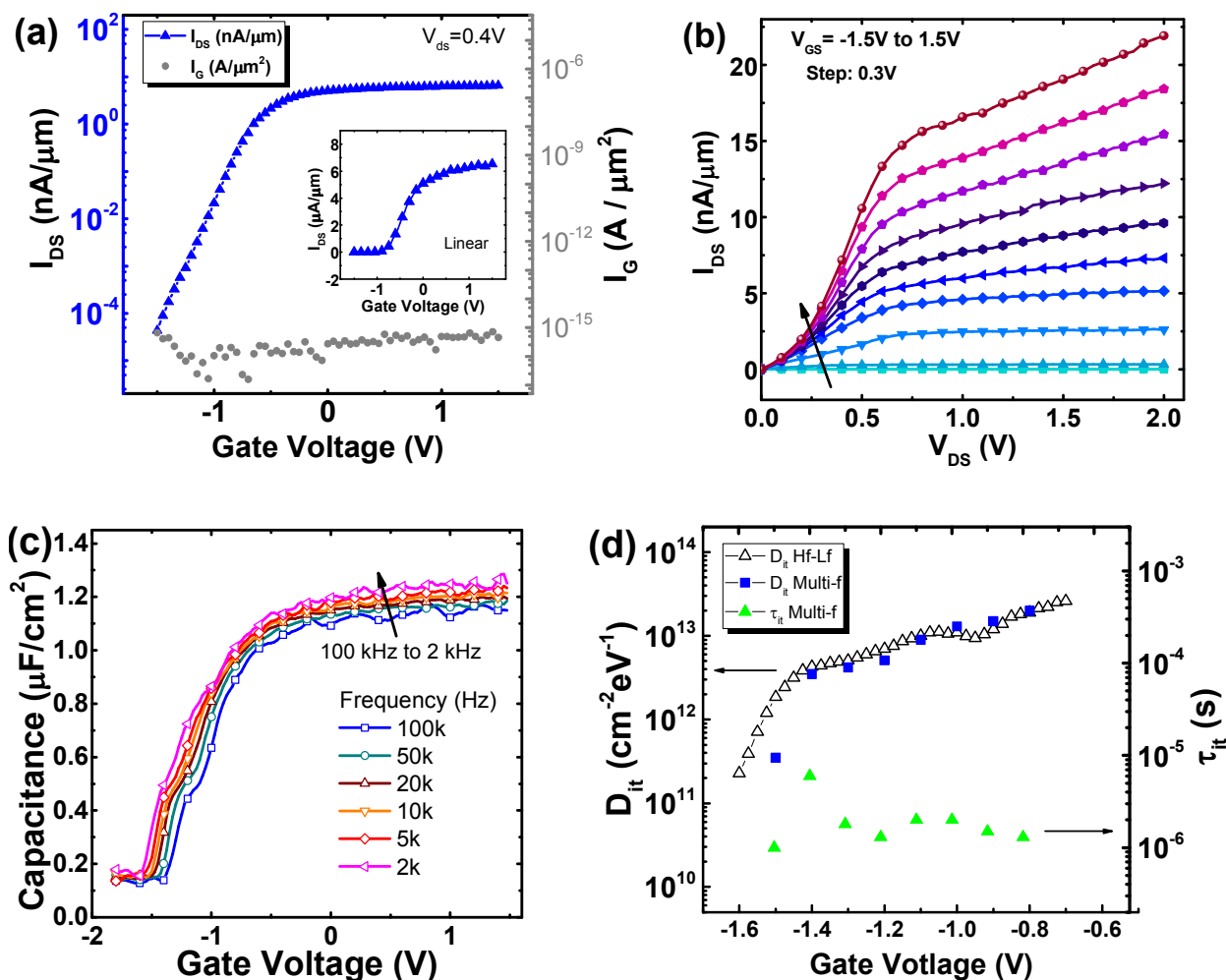
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3 interface, requires a known value of the active *n*-type doping concentration in the MoS<sub>2</sub>. This  
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5 value is not readily known for the geological samples employed here, and as a consequence, the  
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7  $D_{it}$  versus energy in the MoS<sub>2</sub> energy gap cannot be determined for these devices.  
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11 An alternative method was also employed to extract  $D_{it}$ <sup>18</sup>. Instead of only using the C-V data  
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13 of high and low frequencies, data from the complete span of frequencies was used, and using this  
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15 approach both  $D_{it}$  and the trap time constant  $\tau_{it}$  can be extracted. (The importance of  $\tau_{it}$  is that one  
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17 can extract the trap cross section,  $\sigma$ , and trap energy,  $E_T$ , with temperature dependent  
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19 experiments<sup>33</sup> to understand the physical origin of the interface traps, and this is beyond the  
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21 scope of this work.) In this multi-frequency method,  $C_{it}$  is determined by  $D_{it}$  and  $\tau_{it}$  at certain  
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23 voltages.  
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$$C_{it} = \frac{qD_{it}}{1+\omega^2\tau_{it}^2} \quad (3)$$

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31 where  $\omega=2\pi f$ , and  $f$  is the applied AC frequency. Thus, at certain voltages,  $D_{it}$  and  $\tau_{it}$  can be  
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33 extracted from the C-f or C- $\omega$  relationship. Fig. 4b shows the measured data (symbols) and  
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35 model fit (lines) for the capacitance versus frequency for the voltage range corresponding to the  
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37 interface defects response in the C-V characteristic. From Fig. 4b, the values of  $D_{it}$ , and the  
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39 corresponding  $\tau_{it}$  values, can be determined at each gate voltage, and the characteristics are  
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41 shown in Fig. 4c. The two methods are compared in Fig. 4d, demonstrating consistency between  
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43 the two  $D_{it}$  extraction approaches. Detailed modeling work for these two methods can be found  
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45 in S.3 and S.4.  
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**Figure 5.** Electrical characterization and  $D_{it}$  extraction of a device with 8 nm  $HfO_2$  and 4-layer  $MoS_2$ . ( $W=7.2\mu m$ ,  $L=5.6\mu m$ ) (a)  $I_{DS}$ - $V_{GS}$  and gate leakage; (b) Corresponding  $I_{DS}$ - $V_{DS}$ ; (c) C-V: frequency dependence; C-V curves disperse in the entire depletion voltage range, indicating interface traps in range of energy levels; (d)  $D_{it}$  vs  $V_{GS}$  and  $\tau_{it}$  vs  $V_{GS}$ ,  $D_{it}$  ranges from  $2 \times 10^{11} cm^{-2} eV^{-1}$  to  $2 \times 10^{13} cm^{-2} eV^{-1}$ , with both H-L frequency method and multi-frequency method.

Due to possible variation in the electronic properties of exfoliated  $MoS_2$  flakes for differing samples, and within a given crystal, in addition to contaminants and the presence of surface defects<sup>44</sup>, we applied the same methods on a different  $MoS_2$  transistor with 8nm  $HfO_2$  and a 4-layer  $MoS_2$  flake to verify if the C-V analysis method is more broadly applicable. Fig. 5a and 5b shows the  $I_{DS}$ - $V_{GS}$ , gate leakage and  $I_{DS}$ - $V_{DS}$  characteristics of this transistor. The gated area is

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3 width  $\times$  length = 7.2  $\mu\text{m}$   $\times$  5.6  $\mu\text{m}$ . Fig. 5c and 5d shows the C-V frequency dependence, along  
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5 with the extracted  $D_{it}$  with two methods. The C-V frequency dispersion (Fig. 5c) suggests a  
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7 different distribution of interface defects at the  $\text{HfO}_2/\text{MoS}_2$  interface compared to the sample  
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9 analyzed in Fig. 4. The frequency dependent C-V characteristics are consistent with an interface  
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11 state density distributed throughout the  $\text{MoS}_2$  energy gap at the  $\text{HfO}_2/\text{MoS}_2$  interface. Fig. 5d  
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13 shows the  $D_{it}$  and  $\tau_{it}$  extracted using high-low frequency and multi-frequency methods. The  
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15 magnitude of  $D_{it}$  and  $\tau_{it}$  are comparable to the 7-layer  $\text{MoS}_2$  flake MOSFET shown in Fig. 4, but  
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17 in this case no peak in  $D_{it}$  is evident. Similar variation has also been reported in other  
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19 publications using thicker  $\text{MoS}_2$  layers<sup>33</sup>, and the variation from sample to sample (with  
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21 nominally identical processing) is also manifest in the transport properties<sup>32</sup>. This variability in  
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23 interface and transport properties is most likely a consequence of the high density and variability  
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25 of impurities and defects in both geological and grown  $\text{MoS}_2$ .<sup>44,45</sup>  
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32 Interfacial sulfur vacancies<sup>46,47</sup> and other types of surface structural defects<sup>48</sup> are the defects  
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34 often observed by researchers, and can potentially generate these defect responses in the  
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36 impedance measurement. One possible suggestion for the defect level which shows a peak  
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38 response at a specific energy in the band gap (Fig. 4), is that the defect results from sulfur  
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40 vacancies<sup>33</sup>, which is reported to have an energy level of 0.35eV from mid gap, from  
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42 measurements<sup>46</sup>. The alternative behavior of an almost constant  $D_{it}$  across the energy gap (Fig.  
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44 5), observed in this work and in literature<sup>33</sup>, could be a consequence of the area of the certain  
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46 devices not containing S vacancies within the gate area probed. Both cases (peaked  $D_{it}$  &  
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48 uniform  $D_{it}$ ) were also reported in Ref 33, showing C-V response of MOS capacitors on semi-  
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50 bulk  $\text{MoS}_2$  flakes, indicating that the samples that we report in this work are representative. We  
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52 also suspect that the defect response observed in our devices can potentially originate from other  
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3 impurities and defects present in the flake source <sup>44,45</sup> (i.e., the exfoliated MoS<sub>2</sub> crystal), which  
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5 can exhibit equivalent surface density values in the range  $1 \times 10^{12}$  to  $1 \times 10^{13}$  cm<sup>-2</sup>. In addition, it is  
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7 possible that the response could originate from defects located in an interfacial transition region  
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9 between the MoS<sub>2</sub> and the HfO<sub>2</sub> <sup>49–51</sup> because this methodology can also capture border trap  
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11 response. This is also the subject of on-going studies.  
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16 This work provides a relatively easy fabrication procedure and robust electrical  
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18 characterization methodology to study top-gated metal / high-*k* / TMD devices. The multi-  
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20 frequency C-V response of the structure is consistent with the existence of electrically active  
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22 defects at the interface between high-*k* and MoS<sub>2</sub>. By combining with simulation and other  
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24 physical characterization, a route to understand and passivate electrically active interface defects  
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26 in high-*k* gate TMD MOSFETs is possible .  
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## 40 **Conclusion**

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43 In conclusion, we designed and photolithographically fabricated top-gated FETs on exfoliated,  
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45 few-layer MoS<sub>2</sub> flakes, with an in-situ UV-ozone functionalization treatment and 8nm to 13nm  
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47 ALD HfO<sub>2</sub> dielectrics. Both the transistor performance and the gate-stack interface properties  
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49 were characterized electrically. Based on impedance spectroscopy of the HfO<sub>2</sub>/MoS<sub>2</sub> gate stack  
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51 in the MOSFET structure,  $D_{it}$  was extracted from the frequency dependence of the C-V response  
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53 using two different methods. The interface state density values were in the range  $1 \times 10^{12}$  to  
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55  $1 \times 10^{13}$  cm<sup>-2</sup> eV<sup>-1</sup> for the devices studied, with trapping time constants in the range  $1 \times 10^{-5}$  to  
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3  $1 \times 10^{-6}$  s. One device with 7-L MoS<sub>2</sub> and 13 nm HfO<sub>2</sub> as the gate oxide exhibited a C-V response  
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5 consistent with a D<sub>it</sub> distribution peaking at a value of  $1.2 \times 10^{13}$  cm<sup>-2</sup> eV<sup>-1</sup> at a specific energy in  
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7 the MoS<sub>2</sub> band gap. A second device with 4-L MoS<sub>2</sub> and 8 nm HfO<sub>2</sub> yielded D<sub>it</sub> values ranged  
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9 from  $2 \times 10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup> to  $2 \times 10^{13}$  cm<sup>-2</sup> eV<sup>-1</sup> with no peak value of D<sub>it</sub> observed. The device  
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11 performance and interface properties indicate that the UV-ozone functionalization is promising  
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13 for MoS<sub>2</sub>-based devices with high-*k* dielectrics to achieve low leakage, thin and continuous high-*k*  
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15 oxide layers, with interface state density values which allow modulation of the Fermi level at  
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17 the HfO<sub>2</sub>/MoS<sub>2</sub> interface. The relatively simple MOSFET test structure, combined with the gate  
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19 to channel C-V response, indicates the existence of specific electrically active HfO<sub>2</sub>/MoS<sub>2</sub>  
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21 interface defects, and combining these results with simulation and other physical  
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23 characterization methods, will provide an increased understanding of the physical origin of  
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25 defects, as well as a method to monitor the impact of different high-*k* oxides and varying surface  
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27 preparations on the interface state density at high-*k*/MoS<sub>2</sub> interfaces.  
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### 41 **Supporting Information**

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43 Proposed equivalent circuits of C-V characterization; Series resistance analysis and full depletion  
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45 of MoS<sub>2</sub> flake; Number of interface defects (N<sub>it</sub>) extraction from C-V curves; Defects density  
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47 (D<sub>it</sub>) calculation by high-low frequency method; D<sub>it</sub> and traps time constant τ<sub>it</sub> extraction by  
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49 multi-frequency method.  
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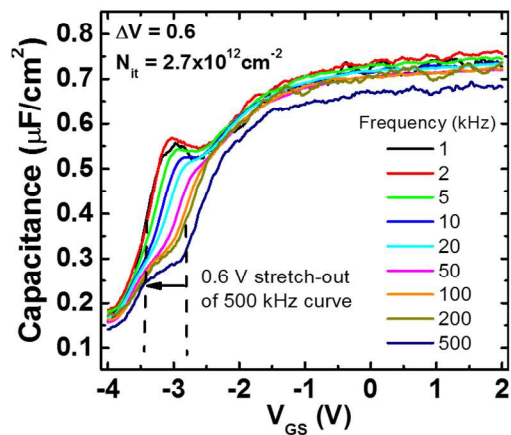
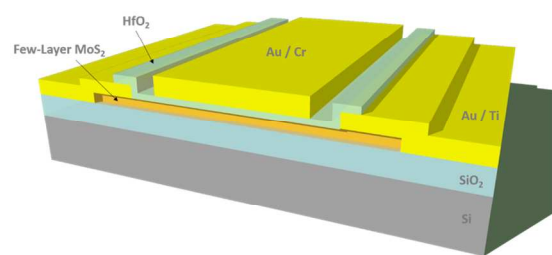
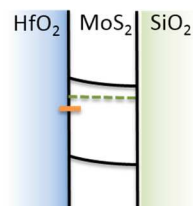


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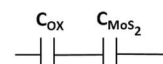
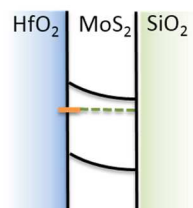
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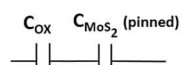
## Graphic for Table of Contents (TOC)

(i)  $V_{GS} > -2.8$  V in depletion region

At All Frequencies

(ii)  $-3.4$  V  $< V_{GS} < -2.8$  V ( $E_F$  pinned)

At High Frequencies



At Low Frequencies

