

Title	Rectifiers, MOS diodes and LEDs made of fully porous GaN produced by chemical vapor deposition
Authors	Carvajal, Joan J.;Mena, Josue;Aixart, J.;O'Dwyer, Colm;Diaz, Francesc;Aguilo, Magdalena
Publication date	2017-09
Original Citation	Carvajal, J. J., Mena, J., Aixart, J., O'Dwyer, C., Díaz, F. and Aguiló, M. (2017) 'Rectifiers, MOS Diodes and LEDs Made of Fully Porous GaN Produced by Chemical Vapor Deposition', ECS Journal of Solid State Science and Technology, 6(10), pp. R143-R148. doi: 10.1149/2.0041710jss
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://jss.ecsdl.org/content/6/10/R143.abstract - 10.1149/2.0041710jss
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Download date	2023-09-30 04:12:58
Item downloaded from	https://hdl.handle.net/10468/6307



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Rectifiers, MOS diodes and LEDs made of fully porous GaN produced by Chemical Vapor Deposition

J. J. Carvajal,^{a,*} J. Mena,^a J. Aixart,^a C. O'Dwyer,^b F. Díaz,^a and M. Aguiló^a

^aFísica i Cristal·lografia de Materials i Nanomaterials, FiCMA-FiCNA, and EMaS, Dept. Química Física i Inorgànica, Universitat Rovira i Virgili, URV, Marcel·lí Domingo 1, E-43007, Spain

^bDepartment of Chemistry, University College Cork, Cork, Ireland

Here we present the fabrication of LEDs based on porous GaN produced by chemical vapor deposition (CVD) and reviewed the work done that allowed demonstrating *p-n* junction rectifiers and MOS diodes in a simple manner and without involving post-growth steps to induce porosity. *p-n* junction rectifiers exhibited stable rectification in the range $\pm 1\text{-}\pm 5$ V, with very stable values of current with time. MOS diodes were fabricated in a single growth step formed by a MgO dielectric interlayer in between Mg-doped porous GaN and a Mg-Ga metallic alloy. Despite the high resistivity observed in the LEDs fabricated, that induced a turn on voltage of ~ 13 V, the emission consisted only in one peak centered at 542 nm. Our porous GaN films exhibit random porosity when compared to arrays of nanostructures, however, their easy deposition over large areas without dominating leakage currents is promising for wideband gap applications.

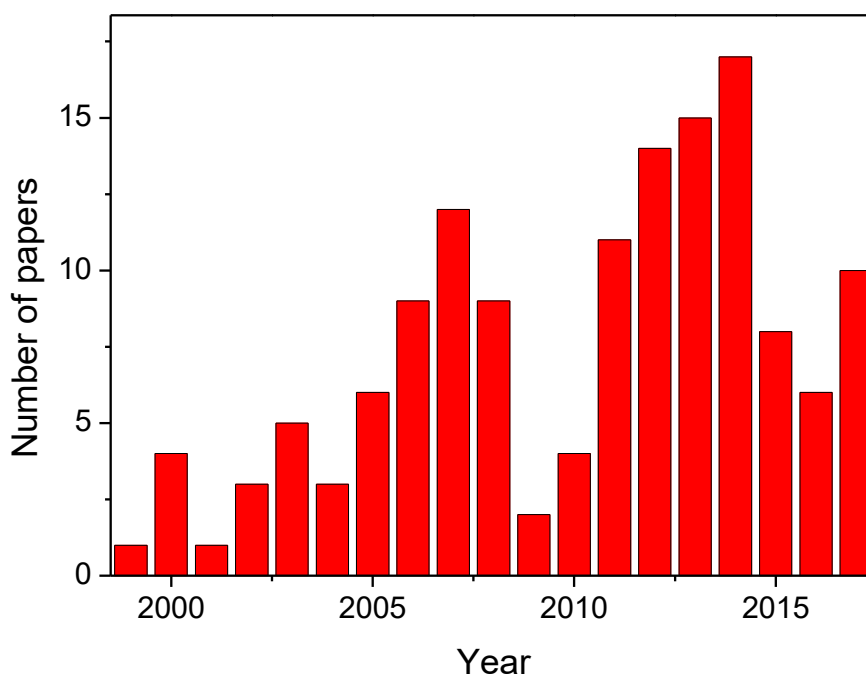
Introduction

GaN is a hexagonal semiconductor, crystallizing in the space group $P6_3mc$ with the wurtzite structure (1). It is considered an important wide band-gap semiconductor for a good number of applications in electronics and optoelectronics (2). It possess a large band gap, that together with its thermal stability and excellent physical properties, make of GaN an excellent candidate for high temperature electronics (3). From another side, GaN exhibits a high heat capacity and a high thermal conductivity, which makes it suitable for high power and high frequency applications (4). Its high stability in front ionizing radiations makes it also good for applications in space, betavoltaics and photovoltaics (5-6).

In its porous form, GaN is particularly interesting for developing optoelectronic devices with improved efficiency, such as LEDs with enhanced efficiency (7-15) and sensors with enhanced sensitivity (16-17). It has also been demonstrated that porous GaN exhibits a reduced structural stress when compared to its non-porous form (18). Despite not being as popular as its bulk counterpart is, the interest in porous GaN has been maintained since the first references in which it was reported, back in 1999, as can be seen in Figure 1, with a tendency to increase the number of papers published about this subject as the time goes by.

Porous GaN is produced typically by (photo)electrochemical etching and chemical etching methods (19-22). An alternative to produce porous GaN we proposed some time ago is the chemical vapour deposition (CVD) method (23), through which we have

50 shown that it is possible to produce nanoporous GaN without any etching or chemical
51 post-growth treatment, with the porosity being present only on the (0001) face of the
52 material. By using this technique, we have demonstrated that it is possible to form low
53 resistivity Ohmic Pt and Au metallic contacts on porous *n*-type GaN by the formation of
54 intermetallic seed layers through the vapour-solid-solid (VSS) mechanism (24). Also, we
55 have been able to develop *p*-type porous GaN by doping it with Mg, with a charge carrier
56 concentration of the order of 10^{18} cm^{-3} (25). By tuning the concentration of Mg,
57 introduced as Mg_2N_3 in the CVD system, we have shown that it is possible to form a
58 polycrystalline high- κ oxide between an Ohmic metallic alloy interlayer contact and the
59 porous GaN, while maintaining a clean interface, that allowed to fabricate MOS-type
60 diodes on silicon substrates in a single growth step (26). Besides, through the careful
61 selection of the substrate it has also been possible to produce porous GaN epitaxial layers
62 (27-28) that allow for the fabrication of high quality partially and fully porous GaN
63 rectifying *p-n* junctions, through a two step CVD process, and show their behaviour as
64 diodes with effective uniform conduction under a green technology (29).



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Figure 1. Number of papers published per year since 1999 about porous GaN (Source: Scopus).

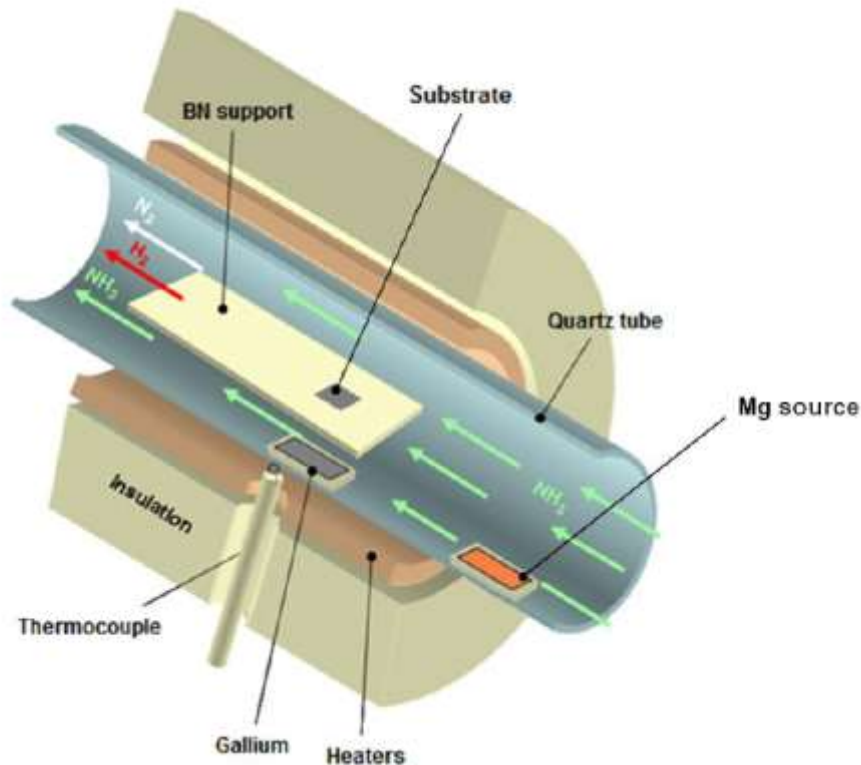
Here, we review the work we have done in porous GaN in the recent years, and present also the promising results we obtained in the light emission of these structures. Thus, we are convinced that these porous *p-n* junctions have potential applications in rectifiers' technology, high power diodes, LEDs with enhanced light emitting properties and high surface area sensors with improved sensitivity.

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Porous GaN rectifiers fabricated by CVD

CVD growth and morphological characterization

Porous GaN layers have been grown on non-porous GaN films ($\sim 5 \mu\text{m}$ thick) on sapphire with *n*-type or *p*-type conductivity, depending on the experiment and the *p-n* junction to be formed. For that we used the direct reaction between Ga and NH_3 in a CVD system (28). Mg_3N_2 was used as the Mg source, located upstream of the Ga source (30). The substrates were placed above the Ga and Mg precursors, when needed, were introduced in the furnace, the reactor was degassed to 1×10^{-2} Torr, prior to the introduction of NH_3 at a constant flow rate of 75 sccm. Figure 2 shows a scheme of the CVD growth setup used. During the reaction, that lasted for 60 min, the pressure of the system was set at 15 Torr, while the reaction was kept at 930 °C. To stop the synthesis process, the ammonia flow was shut down and the temperature was decreased to room temperature. To select and control the areas of the substrate on which the porous GaN layers were deposited, a selective-area growth process was used, covering the substrate with a BN mask. Finally, to activate the *p*-type conductivity of the Mg-doped samples, we annealed them at 700 °C in a nitrogen atmosphere during 20 min.



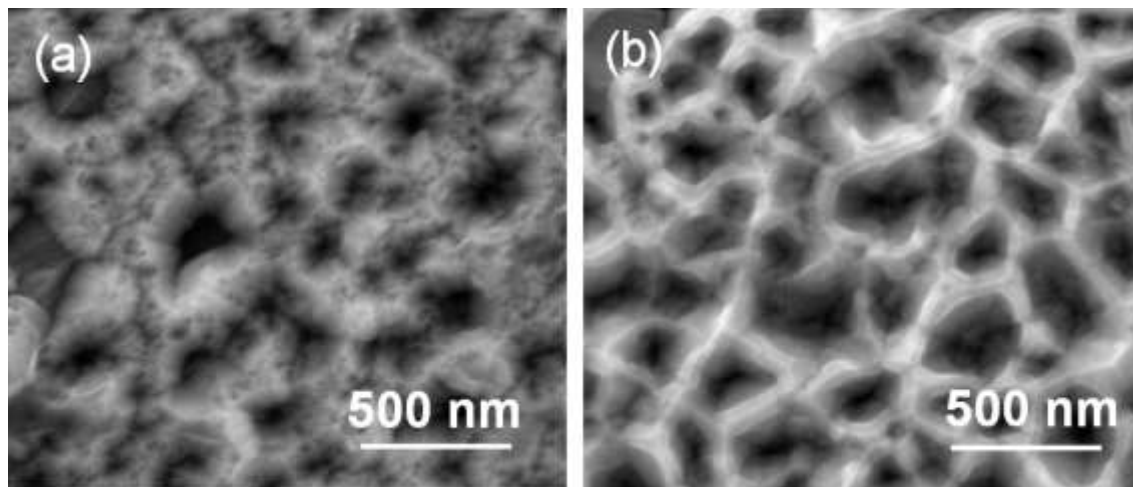
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Figure 2. Schematic representation of the CVD system used for the growth of porous GaN layers.

106 Three types of porous GaN diodes were prepared: (i) undoped *n*-type porous GaN
107 grown on non-porous *p*-type GaN; (ii) Mg-doped porous *p*-type GaN grown on non-
108 porous *n*-type GaN; and (iii) Mg-doped porous *p*-type GaN grown on undoped porous *n*-
109 type GaN previously grown on non-porous *n*-type GaN (28). The last type of diodes were
110 grown on a two crystal growth step process. In the first step, an undoped *n*-type porous
111 GaN film was grown on a non-porous GaN substrate with (0001) crystallographic
112 orientation. Then, the porous Mg-doped *p*-type GaN layer was grown on the top of this
113 undoped porous GaN film.

114 The SEM images recorded for the porous layers obtained reveal a high degree of
115 porosity. However, the diameters of the pores tend to be slightly bigger in the Mg-doped
116 samples when compared to those of the undoped samples. This is even more evident
117 when we compare the diameters of the pores of the two layers constituting the fully
118 porous GaN diode, i.e. the one formed by a Mg-doped porous *p*-type GaN layer grown on
119 an undoped porous *n*-type GaN layer previously deposited on a non-porous *n*-type GaN
120 substrate, as can be seen in Figure 3. This might be due to the exposure of this sample at
121 high temperatures during a longer time. This would widen the pores by a thermal etching
122 effect (31). Another reason that might contribute to the widening of the pores would be
123 their corrugation during the second growth step (32).

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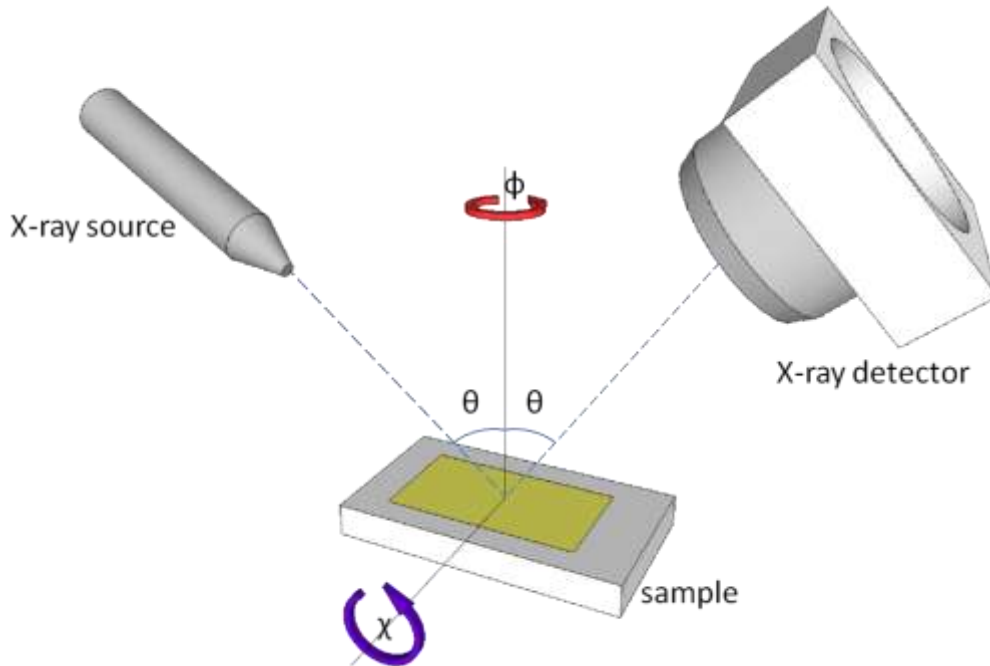
127 Figure 3. High magnification SEM images of the porous structures observed on (a) *n*-
128 type and (b) Mg-doped GaN layers corresponding to the type (iii) diode, i.e. a Mg-doped
129 porous *p*-type GaN layer grown on an undoped porous *n*-type GaN layer previously
130 deposited on a non-porous *n*-type GaN substrate.

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132 An important aspect to be mentioned is that in all cases, the porous GaN layers grew
133 crystallographically oriented along the *c* direction, matching the crystallographic
134 direction provided by the substrates used.

135 This was revealed by the rocking curves corresponding to the $(10\bar{1}2)$ and (0004)
136 reflections of the porous layers. The rocking curves were recorded using a Bruker-AXS
137 D8-Discover diffractometer equipped with a parallel incident beam (Göbel mirror), a
138 vertical θ - θ goniometer, an XYZ motorized stage, and a General Area Diffraction
139 Detection System (GADDS) HI-STAR detector with a multiwire proportional counter of
140 $30 \times 30 \text{ cm}^2$ area and 1024×1024 pixel density. Samples were placed on the sample
141 holder fixed with wax, and the area of interest was selected with the aid of a video-laser
142 focusing system. An X-ray collimator system allows the analysis of an area of $500 \mu\text{m}^2$

143 on the sample. The X-ray diffractometer was operated at 40 kV and 20 mA. For this
 144 purpose, the X-ray source and the X-ray detector positions were settled at the desired
 145 Bragg angle, corresponding to the particular reflection of interest, and 120 frames were
 146 recorded at an integration time of 1 s every 0.05° in ω . The ω -scan was set to start at an ω
 147 angle 3° below the desired Bragg angle, and was finished 3° above that Bragg angle. The
 148 envelope function of the collection of 120 frames was then plotted, obtaining the
 149 corresponding rocking curve. For the identification of the $(10\bar{1}2)$ peak a χ - and a ϕ -scan
 150 were performed to identify the right diffraction conditions. The χ -scan was fixed when
 151 the k vector was perpendicular to the $(10\bar{1}2)$ plane. This χ angle was defined using the
 152 stereographic projection and measuring the angle between the $(10\bar{1}2)$ and (0001) planes.
 153 Then, a ϕ -scan was recorded to find the location of the a (or b) crystallographic axis. This
 154 procedure allowed identifying peaks that are off the plane of the sample when the thin
 155 film was parallel to the ground platform. For this, the X-ray source and the detector were
 156 positioned at a defined θ Bragg angle and then, the sample was rotated in 5 degrees steps
 157 36 times with an integration time of 5 seconds, covering an angle of 180° in ϕ . Once the ϕ
 158 angle was roughly identified following these conditions, a second ϕ -scan was performed
 159 to found more accurately its value, using 1 degree steps 5 times with an integration time
 160 of 5 seconds. Once the ϕ and χ angles were defined the rocking curves were recorded,
 161 with an initial $\omega_1 = 21.19^\circ$ and a final $\omega_2 = 27.19^\circ$ for the $(10\bar{1}2)$ reflection, and an initial
 162 $\omega_1 = 33.44^\circ$ and a final $\omega_2 = 39.44^\circ$ for the (0004) reflection. Figure 4 shows a scheme of
 163 how the rocking curves were recorded.
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 167 Figure 4. Schematic representation of the ϕ , χ and θ (ω) rotations used to record the
 168 rocking curves in the porous GaN samples.
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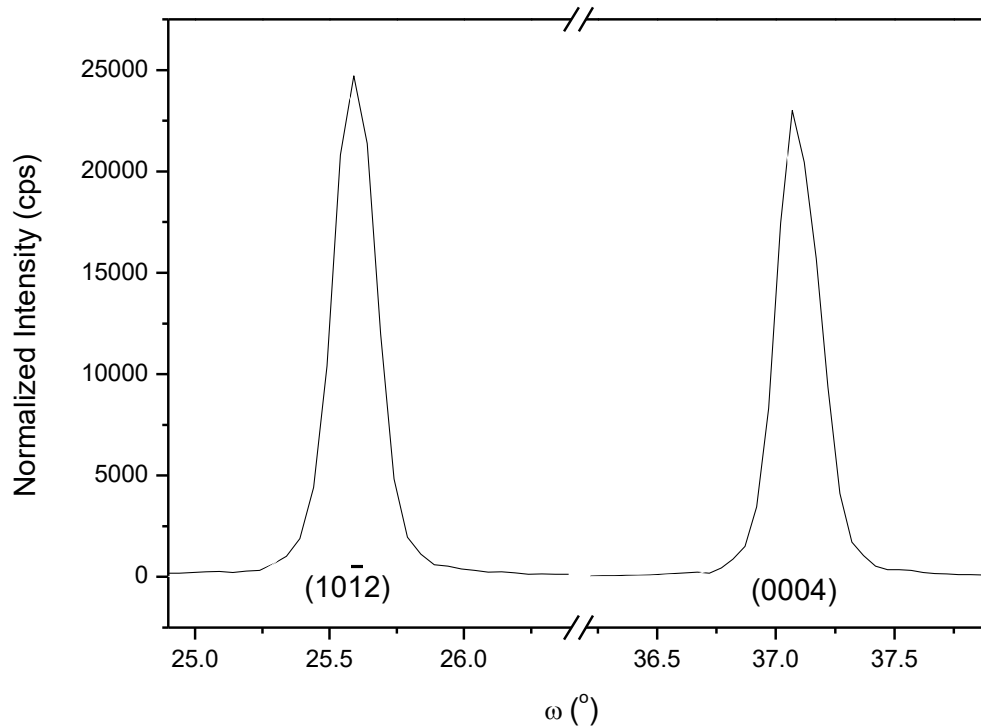
170 As an example, Figure 5 shows the rocking curve corresponding to the undoped
 171 porous GaN layer. From the data extracted from the figure, the position and the full width
 172 at half-maximum (FWHM) of the diffraction peaks of the porous layer could be analyzed.

173 Table 1 lists these data. The FWHM of the rocking curves are similar in both cases,
 174 indicating a good structural quality for the porous layer. In fact, for the non-porous
 175 substrate, similar values were obtained, indicating that the structural quality of the porous
 176 layer is at least as good as that of the commercial substrates.
 177

TABLE I. Peak position and FWHM of the rocking curves shown in Figure 5 recorded for porous GaN.

Reflection	Peak position (°)	FWHM (°)
(10 $\bar{1}2$)	25.54	0.15
(0004)	37.01	0.15

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182 Figure 5. Rocking curves corresponding to the (10 $\bar{1}2$) and (0004) reflections of an
 183 undoped porous GaN grown on a non-porous *p*-type GaN substrate.
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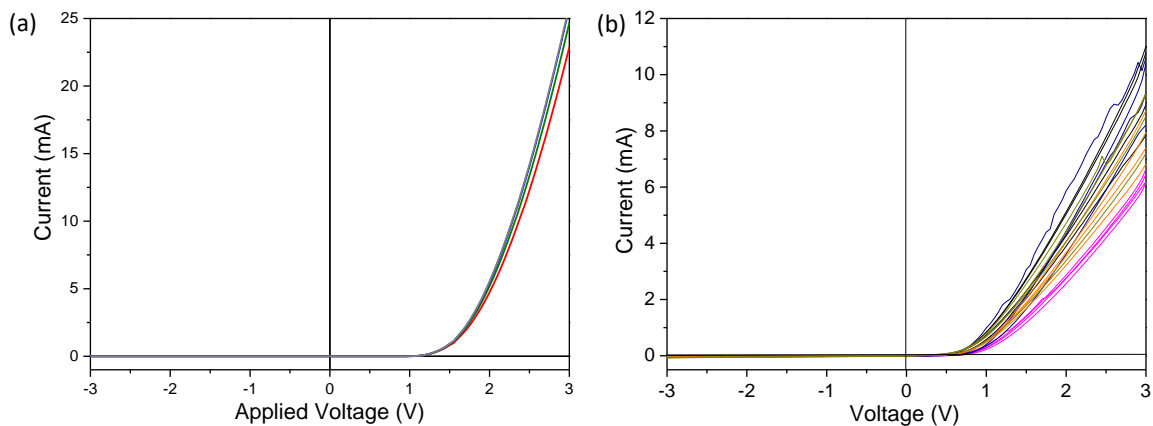
185 Electrical characterization

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187 Electrical characterization of the three different types of porous GaN diodes
 188 fabricated was performed using the two-probe electrical measurements technique. As
 189 contacts we used In/Ga liquid drops placed on the top of the porous GaN layer and the
 190 non-porous GaN substrate, in the case of the diodes formed by an undoped *n*-type porous
 191 GaN layer grown on non-porous *p*-type GaN substrates or by a Mg-doped porous *p*-type
 192 GaN layer grown on non-porous *n*-type GaN substrates, to ensure a good wetting area of
 193 several μm^2 to the rough top-surface of the porous GaN samples. In the case of the Mg-
 194 doped porous *p*-type GaN layer grown on an undoped porous *n*-type GaN film previously
 195 grown on a non-porous *n*-type GaN substrate, the In/Ga liquid drops were placed on the
 196 top of the two porous layers. For the measurements, a Keithley 2400 sourcemeter was
 197 used. Linear voltage sweeps were obtained in the range between -10 and 10 V with a 50

198 mV/s sweep rate. The measurements were repeated with contacts on various points of
199 each sample to ensure repeatability.

200 Figure 6 shows the I-V curves recorded for a diode formed by an undoped *n*-type
201 porous GaN layer grown on the top of a non-porous *p*-type GaN substrate. All the
202 samples exhibited characteristic I-V curves with strong rectification (28). From these
203 curves we found that the barrier to the exponential current increase was lower than the
204 expected GaN diode response, happening below 1 V at around 0.5-0.68 V, in the $(E_g/4q) -$
205 $(E_g/2q)$ range. Figure 5(a) shows the I-V curves recorded in several locations of the same
206 diode, showing the homogeneity in the electrical behavior of the devices. Figure 6(b)
207 shows the I-V curves recorded for 25 different diodes. In this case, despite the current
208 obtained at +3 V for the different devices varies between 6 and 10 mA, the knee voltage
209 is located in the range 0.5-0.68 V in all cases, indicating the good reproducibility of this
210 technique for the fabrication of porous GaN diodes.
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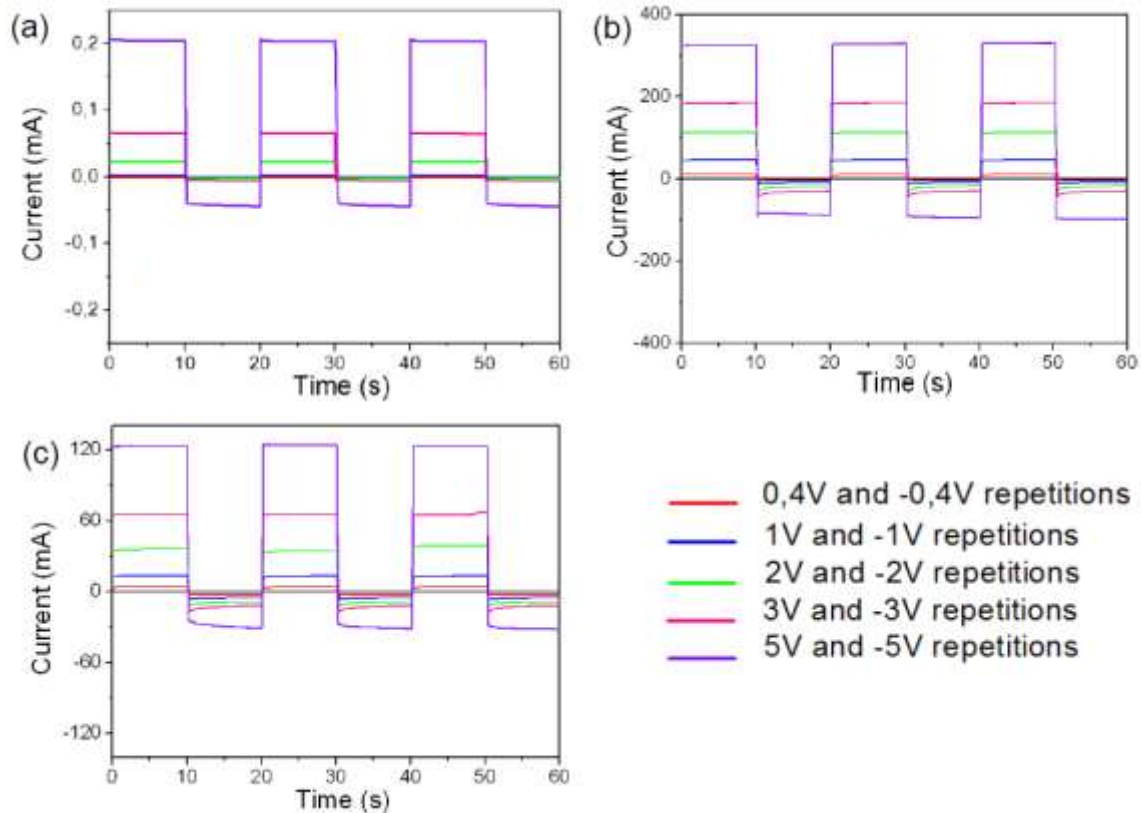


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214 Figure 6. I-V curves recorded for a diode formed by an undoped *n*-type porous GaN
215 layer grown on the top a non-porous *p*-type GaN substrate. (a) I-V curves recorded on
216 different points of the same diode, and (b) I-V curves recorded for different diodes.
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218 An important property of a *p-n* junction is the rectifying effect, which means that it
219 only allows the electric current to flow in one direction. Diode rectification
220 measurements were conducted in the range between -0.4 and +0.4 V, and -5 V and +5 V
221 voltages for forward and reverse bias, respectively. As expected, by applying both
222 reverse and forward bias to the porous GaN diodes, a distinct rectifying behavior was
223 observed (28). Figure 7 shows current vs. time plots recorded at different constant
224 voltages for each of the three porous GaN diodes, after changing the polarity of diode
225 bias with a frequency of 0.1 Hz. All diodes exhibited stable rectification. The I-t
226 characteristics recorded at ± 0.4 V does not show clear rectification behavior, since this
227 voltage is below the turn-on voltage of the porous GaN diodes. At ± 1 V, ± 2 V, ± 3 V and
228 ± 5 V voltages all diodes demonstrate rectifying behavior. The highest leakage voltage
229 and the lowest rectification ratio were observed at ± 5 V. Also, porous GaN diodes
230 demonstrate very stable values of current with time at both, forward and reverse bias. The
231 stability confirms that for porous *p-n* junctions using a single porous layer deposited on
232 an epitaxial continuous GaN film, or from a porous layer grown on another porous layer,
233 a remarkable stability in rectification is maintained. Porous GaN films can exhibit
234 random porosity (compared to arrays of nanostructures), but their ease of deposition over

235 large areas without dominating leakage currents is promising for wideband gap
236 applications, including sensors.
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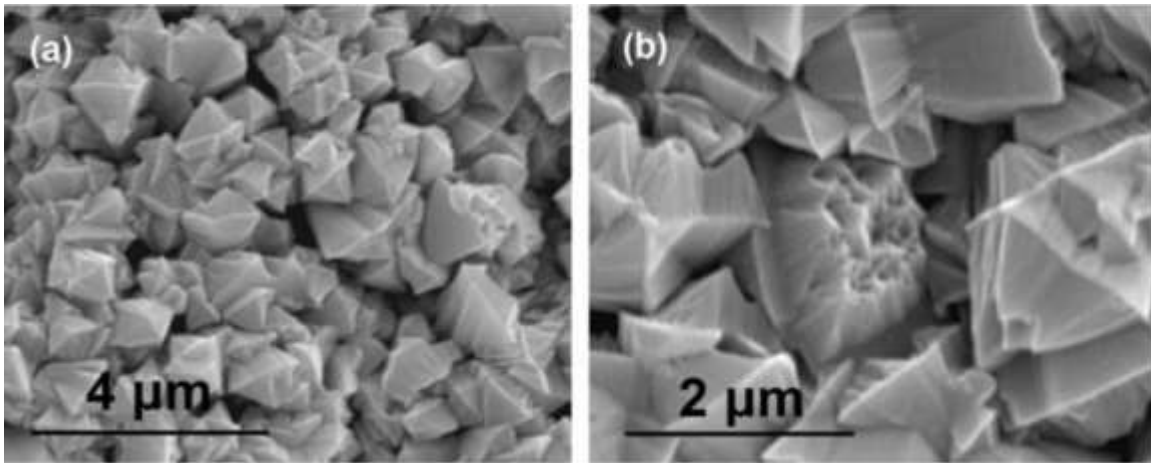
240 Figure 7. Rectification properties of porous GaN diodes formed by (a) an undoped *n*-
241 type porous GaN layer grown on the top a non-porous *p*-type GaN substrate, (b) a Mg-
242 doped porous *p*-type GaN layer grown on a non-porous *n*-type GaN substrate, and (c) a
243 Mg-doped porous *p*-type GaN layer grown on an undoped porous *n*-type GaN film
244 previously grown on a non-porous *n*-type GaN substrate.

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247 Porous GaN MOS diodes fabricated by CVD

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249 By increasing the concentration of Mg_3N_2 in the synthesis of porous GaN we have
250 discovered the possibility of fabricating MgO-GaN metal-oxide semiconductor (MOS)
251 diodes in one single synthesis step (26). The synthesis consisted in using a molar ratio
252 $Mg/Ga = 0.052$, locating the Mg_3N_2 precursor of Mg 4 cm upstream of the Ga source. In
253 this case, Si (100) substrates were used, coated with a thin catalyst layer 20 nm thick of
254 Pt or Au to facilitate the nucleation of the porous GaN particles (24). Under these
255 conditions, a layer of crystalline MgO was formed underneath the Mg-doped GaN layer.
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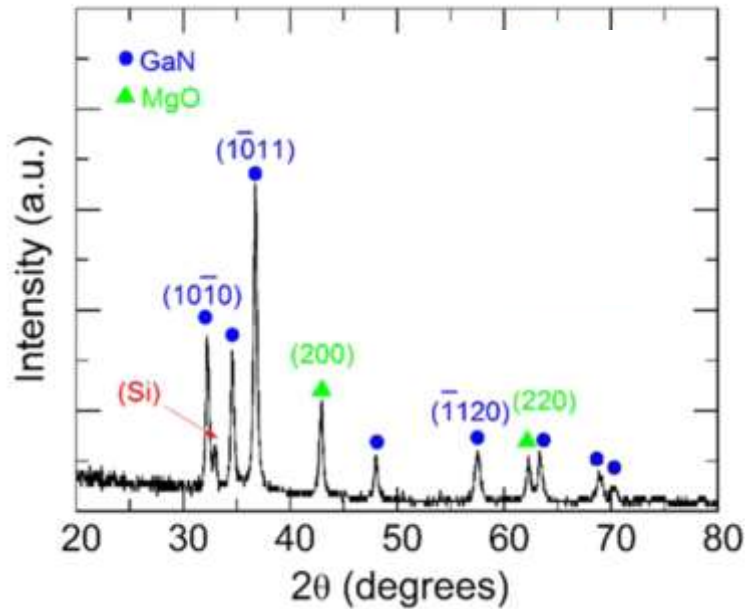


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Figure 8. SEM image of the porous GaN particles nucleated on the top of the MOS structure grown on Si (100) substrates coated with (a) a 20 nm thick film of Au and (b) a 20 nm thick film of Pt.

Figure 8 shows the characteristic morphology of the porous GaN particles, with a mean size of $\sim 1.5 \mu\text{m}$, that nucleated on the top of the MOS structure. In this figure it can be clearly seen the intraparticle and the interparticle porosity, typical of these structures.

The XRD pattern of the MOS diode, shown in Figure 9 shows the presence of polycrystalline wurtzite GaN, as well as MgO on these structures. Even, the peak corresponding to the Si substrate can be seen in this figure.



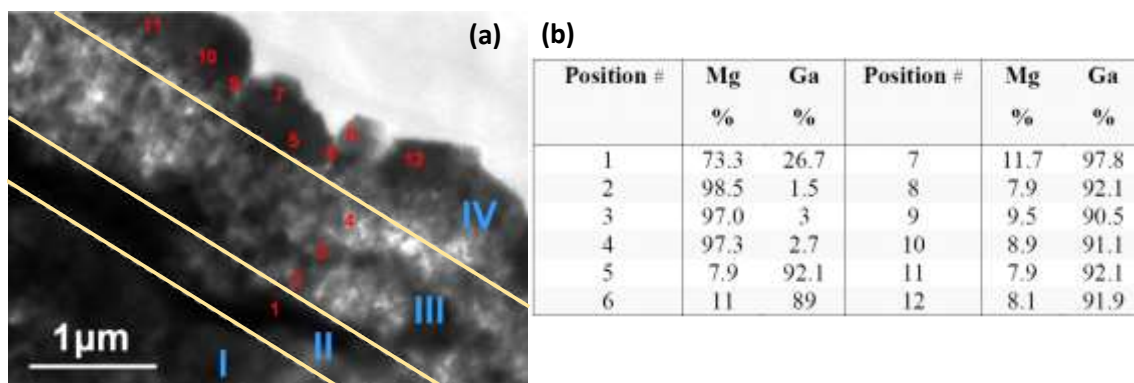
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Figure 9. XRD pattern of the porous MgO-GaN MOS structure grown on a Si (100) substrate.

The combination of cross-section TEM images and energy dispersive X-ray spectrometry (EDX) analysis allowed determine the location of the MgO layer in the structure, just underneath the porous GaN polycrystalline layer (see Figure 10). The TEM

278 image reveals the presence of different regions with a variation in contrast, corresponding
 279 to the different Mg concentration. Through the quantification of the Mg concentration by
 280 EDX, four different spatial regions could be defined in the sample: (i) a region
 281 corresponding to the Si substrate; (ii) a second region (corresponding to point 1 in Figure
 282 10) corresponding to the formation of an intermetallic Mg-Ga (27 % - 73 %) alloy; (iii) a
 283 third layer in which MgO is encountered (corresponding to points 2-4 in Figure 10); and
 284 (iv) the Mg-doped GaN layer (corresponding to points 5-12 in Figure 10).

285 The electrical characterization of the MgO-GaN porous layers formed on silicon
 286 exhibit a diode behavior which is consistent with a MOS system. The I-V curves
 287 recorded, plotted in Figure 11 (a), show a rectifying diode response. We assumed that the
 288 net current is due to the thermionic emission current, as the metal-semiconductor-metal
 289 contact now involves a dielectric on one interface, mimicking the structure of a Schottky
 290 contact with series resistances originated from the MgO and porous *n*-type GaN. We
 291 believe that effective Ohmic contacts can form with *n*-type GaN suggesting that Ohmic
 292 transport is dominated by resistivity through the Mg-Ga alloy interface. However, when
 293 the MgO layer is introduced, since it has a high dielectric constant, the series resistance
 294 increase in an important way even at low voltages. Thus, the system exhibit a diode
 295 behavior but utilizing an Ohmic contact formed by the Mg-Ga intermetallic found under
 296 the MgO layer and biased by the underlying Si substrate. The series resistance, however,
 297 seems to include also tunneling effects (such as Poole-Frenkel tunneling and surface
 298 leakage), since the ideality factor depends strongly on the voltage, becoming quite high in
 299 the region corresponding to high current and high voltage, as plotted in Figure 11 (b).
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 303 Figure 10. (a) Cross-section TEM image of the porous MgO-GaN MOS diode fabricated
 304 by CVD in a single synthesis step on a Si (100) substrate, and (b) EDX content of Mg
 305 and Ga identified in the different layers of the structure.
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307 This method of fabrication of MOS diodes in a single synthesis step might be
 308 extended to growing nanoscale III-N materials and alloys using metals that are not
 309 typically employed for forming electric contacts, to provide an Ohmic response and
 310 fabricate MOS-based systems to be used in high surface area transistors for biosensing
 311 applications that are chemically stable.
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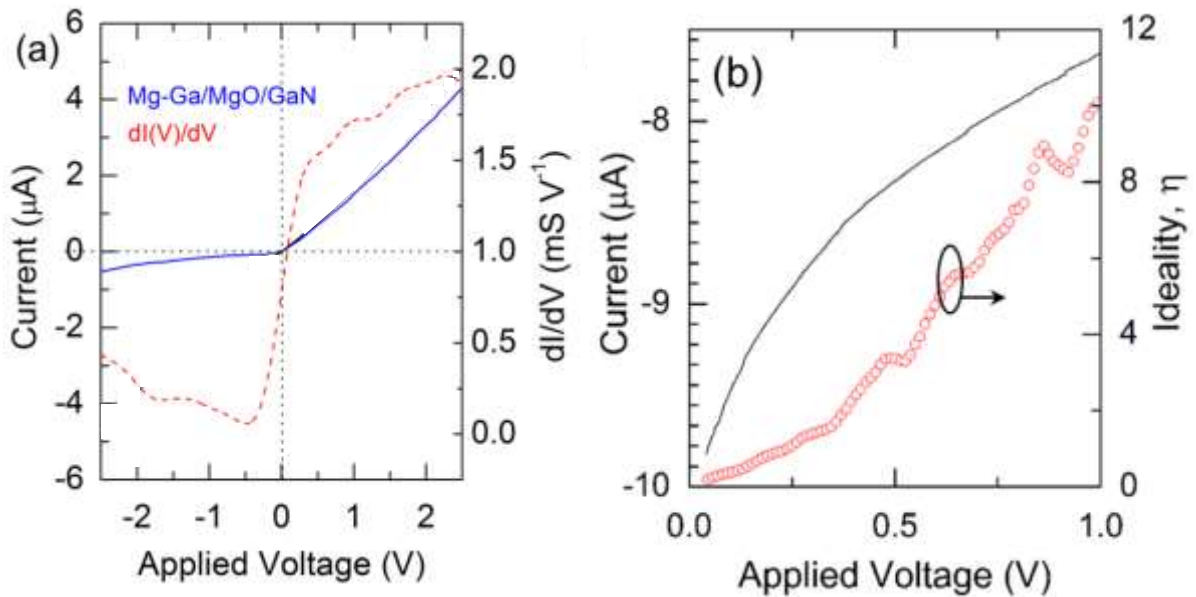


Figure 11. (a) I-V curves for porous *n*-type GaN with a MgO dielectric layer underneath. (b) $\ln(I)$ -V curve and the voltage dependence of the ideality factor for the diode.

An approximation towards the fabrication of porous GaN LEDs produced by CVD

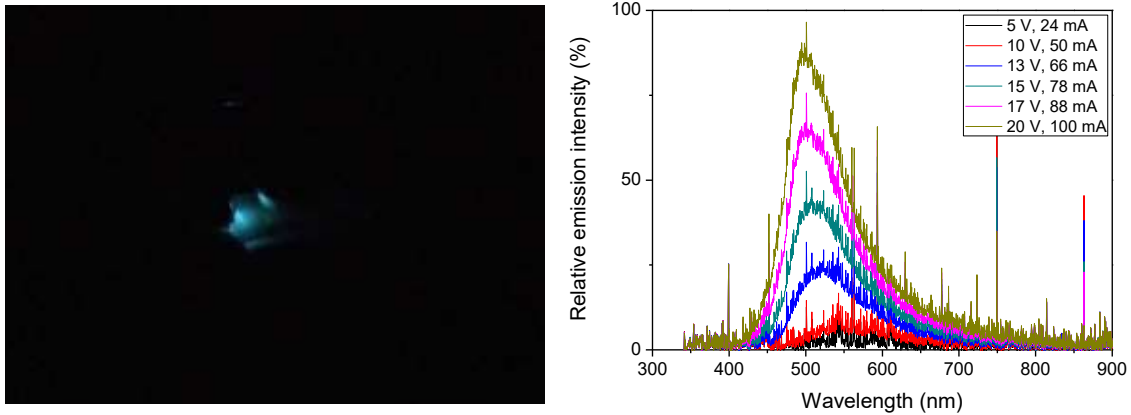
To explore the possibility of fabricating LEDs based on porous GaN produced by CVD we used the diodes formed by an *n*-type porous GaN layer deposited on a *p*-type non-porous GaN substrate, described above (28).

These structures were characterized as LEDs by injecting current by a two probes measurement system that allowed establishing contacts on the top of the substrate and on the top of the porous GaN layer, using a Keithley 2400 sourcemeter. To ensure a good electrical contact on the sample, especially on the rough surface of the porous substrate, In/Ga liquid drops were deposited on the top of the substrate and the porous GaN layer to obtain a good wetting, in which the needles of the two probes measurement systems were introduced. At the same time, the use of this liquid alloy allowed to generate an Ohmic contact on both sides of the diode.

Figure 12 (a) shows the optical image taken showing the electroluminescence (EL) generated by these devices at 100 mA. It can be seen that light blue light is generated by these kind of structures. Since no electrodes were deposited covering the whole surface of the sample, the light arises only from the point where the contact was established, thus it is emitted from a narrow area of the device.

Figure 12 (b) shows the EL spectra of these light blue LEDs at the injection currents from 24 to 100 mA. The first important thing to note here are the high voltages that we needed to apply to obtain these injection currents. This is due to the high resistivity of the substrates used. The emission spectra consists of only one peak. At low injection currents (24-50 mA), this peak is very broad, with very low intensity, centered at around 542 nm. It is not until we applied 66 mA that the emission peak is clearly defined, centered at ~521 nm. This corresponds to a voltage of 13 V that seems to be the turn on voltage for these structures. As the injection current increases, the emission peak shifts towards shorter wavelengths, and it becomes centered at 500 nm for an injection current of 100 mA. The full width at half maximum (FWHM) of this emission peak also becomes

347 narrower as the injection current increases, passing from 103 nm at 66 mA to 77 nm at
348 100 mA.
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352 Figure 12. (a) Optical image of the emission generated, and (b) room temperature
353 electroluminescence spectra of the LEDs based on an *n*-type porous GaN layer deposited
354 on a *p*-type non-porous GaN substrate.
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357 Despite the voltages we need to apply to obtain light from these structures are still
358 very high, we are optimistic that by selecting non-porous GaN substrates with lower
359 resistivity, we would be able to reduce the turn on voltage for these LEDs. Also, we
360 observed that even if we increase the injection current of the LED to the point in which
361 we cause the rupture of the diode and the emission of the device is stopped, by moving
362 the top contact to another point of the surface of the porous layer, we can obtain again the
363 emission. This would indicate that the epitaxial layer consists on a grain structure. Thus,
364 here, the resistance generated at the grain boundaries might also play a role in the high
365 turn on voltages obtained. Nevertheless, the grain structure of the LED might be seen as
366 an advantage since it would be formed by a multitude of tiny diode structures connected
367 among them in parallel. Thus, the failure or the rupture of the Schottky diode would not
368 cause the failure of the whole system.
369

370 Conclusions

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372 In this paper, we reviewed the potentiality of porous GaN produced by CVD to
373 fabricate *p-n* junction rectifiers, MOS diodes and LEDs deposited by a simple synthesis
374 method on large substrate areas. The results reviewed here, taken as a whole, demonstrate
375 that high quality *p-n* junctions of porous *n*-type and porous *p*-type GaN can be obtained
376 by chemical vapor deposition. The electrical characteristics demonstrate the high
377 electronic quality of the produced porous GaN layers.

378 We believe that these kind of structures can be extended to other III-N materials such
379 as InN and AlN as a route toward porous and graded index III-N materials that constitute
380 a basis for the development of white light emitting LEDs with reduced reflection losses
381 and narrowed output light cones that might improve their external quantum efficiencies,
382 among other applications.
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Acknowledgments

This work was supported by the Spanish Government under projects TEC2014-55948-R and Mineco/AEI/FEDER MAT2016-75716-C2-1-R and the Catalan Authority under project 2014SGR1358. FD acknowledges additional support through the ICREA Academia awards 2010ICREA-02 for excellence in research.

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